User's Guide

DS160PR412-421EVM Evaluation Module

ABSTRACT

The DS160PR412-421EVM evaluation module provides a complete high-bandwidth platform for evaluating the signal conditioning features of the DS160PR412 and DS160PR421 Quad-Channel PCI Express 4.0 Linear Redrivers. This evaluation board can be used for standard compliance testing, performance evaluation, and initial system prototyping.

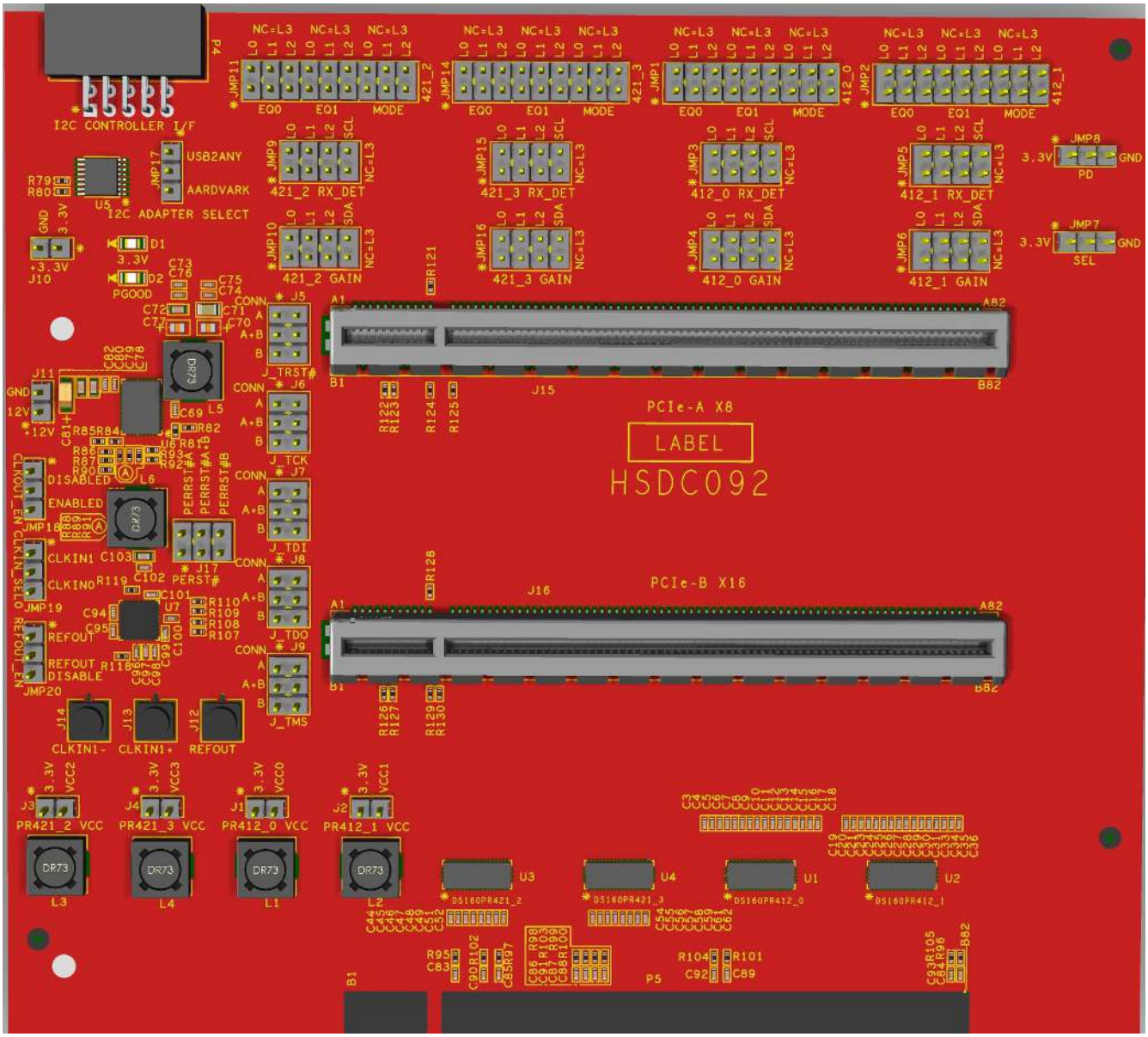

Figure 1-1. DS160PR412-421EVM

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Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The DS160PR412-421EVM features two DS160PR412 and two DS160PR421 linear redrivers that can extend the transmission distance of a PCIe Gen-4 x8 bus. The EVM can be directly plugged into a PCIe slot on a server or PC motherboard using the PCIe Edge connector on the board and paired with a PCIe add-in card using one of the two PCIe connectors on the EVM.

1.1 Features

This EVM has the following features:

- PCIe x16 and PCIe x8 Riser Card with two DS160PR412 and two DS160PR421 4-channel unidirectional linear redrivers operating at rates up to 25Gbps.
- DS160PR412: linear redriver with 1:2 MUX
- DS160PR421: linear redriver with 2:1 DEMUX
- Linear equalization for seamless support of link training and PCIe channel extension
- CTLE boosts up to 18 dB at 8 GHz
- Device configuration and MUX selection by pin control, SMBus, or I2C.
- Flow-thru layout with no heat sink required
- Industrial temperature range: –40°C to 85°C

1.2 Applications

- PCI Express Gen 1, 2, 3, and 4
- High-speed interfaces up to 25Gbps
- Enterprise server motherboard, workstation
- Enterprise storage
- Enterprise add-in card, end-point

2 Description

2.1 DS160PR412 and DS160PR421 4-Level I/O Control Inputs

Each DS160PR412 and DS160PR421 features 4-level input pins (MODE, GAIN/SDA, EQ0/ADDR, EQ1, and RX_DET/SCL) that are used to control the configuration of the device. These 4-level inputs use a resistor divider to help set the four valid levels to provide a wider range of control settings.

Table 2-1. Four-Level Control Pin Settings

PIN LEVEL	PIN SETTING
L0	1 kΩ to GND
L1	13 kΩ to GND
L2	59 kΩ to GND
L3	Float

2.2 DS160PR412 and DS160PR421 Modes of Operation

Each DS160PR412 and DS160PR421 can be configured to operate in either Pin Mode, SMBus Mode, or I2C Slave Mode. The mode of operation of the DS160PR412 and DS160PR421 is determined by the pin strap setting on the MODE pin as shown in Table 2-2.

Table 2-2. Modes of Operation

MODE PIN LEVEL	MODE OF OPERATION
L0	Pin Mode
L1	SMBus Mode or I2C Slave Mode
L2	SMBus Mode or I2C Slave Mode
L3	RESERVED

2.3 DS160PR412 and DS160PR421 SMBus or I2C Register Control Interface

The DS160PR412 and DS160PR421 internal registers can be accessed through standard SMBus protocol. The DS160PR412 and DS160PR421 features two banks of channels, Bank 0 (Channels 0-1) and Bank 1 (Channels 2-3), each featuring a separate register set and requiring a unique SMBus slave address. The SMBus slave address pairs (one for each channel bank) are determined at power up based on the configuration of the MODE and EQ0/ADDR pins. The pin state is read on power up, after the internal power-on reset signal is deasserted.

There are 8 unique SMBus slave address pairs (one address for each channel bank) that can be assigned to the device by placing external resistor straps on the MODE and EQ0/ADDR pins as shown in Table 2-3. When multiple DS160PR412 and DS160PR421 devices are on the same SMBus interface bus, each channel bank of each device must be configured with a unique SMBus slave address pair.

Table 2-3. DS160PR412 and DS160PR421 SMBus Address Map

MODE	EQ0/ADDR Pin Level	Channels 0-1: 7-Bit Address [HEX]	Channels 2-3: 7-Bit Address [HEX]
L1	L0	0x18	0x19
L1	L1	0x1A	0x1B
L1	L2	0x1C	0x1D
L1	L3	0x1E	0x1F
L2	L0	0x20	0x21
L2	L1	0x22	0x23
L2	L2	0x24	0x25
L2	L3	0x26	0x27

2.4 DS160PR412 and DS160PR421 Equalization Control

Each channel of the DS160PR412 and DS160PR421 features a continuous-time linear equalizer (CTLE) that applies high-frequency boost and low-frequency attenuation to help equalize the frequency-dependent insertion loss effects of the passive channel. Table 2-4 shows available equalization boost through EQ control pins (EQ1 and EQ0) for all channels when in Pin Control mode (MODE = L0).

Table 2-4. Equalization Control Settings

EQ INDEX	EQ1 PIN LEVEL	EQ0 PIN LEVEL	CTLE BOOST AT 4 GHz (dB)	CTLE BOOST AT 8 GHz (dB)
0	L0	L0	–0.25	–0.5
1	L0	L1	2.0	4.0
2	L0	L2	2.5	5.0
3	L0	L3	3.0	6.0
4	L1	L0	4.0	7.0
5	L1	L1	4.5	7.5
6	L1	L2	5.0	8.0
7	L1	L3	6.0	9.5
8	L2	L0	7.0	10
9	L2	L1	8.0	11
10	L2	L2	8.5	12.5
11	L2	L3	9.0	13
12	L3	L0	9.5	14.5
13	L3	L1	10.0	15
14	L3	L2	10.5	16.0
15	L3	L3	12	18

The equalization gain of each channel of each device can also be set by writing to SMBus / I2C registers in I2C Mode. See the *DS160PR412, DS160PR421 Programming Guide* for details.

2.5 DS160PR412 and DS160PR421 RX Detect State Machine

Each DS160PR412 and DS160PR421 deploys an RX Detect state machine that governs the RX detection cycle as defined in the PCI Express specification. At power up or after a manually triggered event, the redriver determines whether or not a valid PCI Express termination is present at the far end of the link. The RX_DET/SCL pin of DS160PR412 and DS160PR421 provides additional flexibility to system designers to appropriately set the device in their desired mode, according to Table 2-5.

Table 2-5. 4-Level Control Pin Settings

PD PIN LEVEL	RX_DET/SCL PIN LEVEL	DESCRIPTION
L	L0	PCI Express RX detection state machine is disabled. Recommended for non-PCI Express use cases. Inputs are always 50 Ω.
L	L1	PCI Express RX detection state machine is enabled. Recommended for PCI Express use cases. Pre Detect: Hi-Z, Post Detect: 50 Ω. Outputs poll every approximately 150 µs until three consecutive valid RX termination detections.
L	L2	PCI Express RX detection state machine is enabled. Recommended for PCI Express use cases. Pre Detect: Hi-Z, Post Detect: 50 Ω. Outputs poll every approximately 150 µs until two consecutive valid RX termination detections.
L	L3 (Float)	PCI Express RX detection state machine is enabled. Recommended for PCI Express use cases. Pre Detect: Hi-Z, Post Detect: 50 Ω. Outputs poll every approximately 150 µs until a valid RX termination detection.
H	X	Manual reset, inputs are Hi-Z

2.6 DS160PR412 and DS160PR421 DC Gain Control

When operating in Pin Mode, the GAIN/SDA pin can be used to set the overall datapath DC (low frequency) gain of the DS160PR412 and DS160PR421 as shown in Table 2-6.

Table 2-6. GAIN Control

GAIN/SDA PIN LEVEL	GAIN SETTING
L0	–6 dB
L1	–3 dB
L2	3 dB
L3	0 dB (Recommended for most use cases)

The DC gain of each channel of each device can also be set by writing to SMBus / I2C registers in Slave or Master Modes. See the *DS160PR412, DS160PR421 Programming Guide* for details.

2.7 DS160PR412-421EVM Global Controls

Table 2-7 shows the DS160PR412 and DS160PR421 EVM global controls that affect all devices on the board.

Table 2-7. EVM Global Controls

COMPONENT	NAME	FUNCTION OR DESCRIPTION
J1	DS160PR412-0 VCC	Pin 1 : Board VCC Pin 2: PR412_0 VCC
J2	DS160PR412-1 VCC	Pin 1 : Board VCC Pin 2: PR412_1 VCC
J3	DS160PR421-2 VCC	Pin 1 : Board VCC Pin 2: PR421_2 VCC
J4	DS160PR421-3 VCC	Pin 1 : Board VCC Pin 2: PR421_3 VCC
J5	PCIe JTAG TRST	1-2: Edge Finger to PCIe-A 3-4 Edge Finger to PCIe A + B 5-6 Edge Finger to PCIe-B
J6	PCIe JTAG TCK	1-2: Edge Finger to PCIe-A 3-4 Edge Finger to PCIe A + B 5-6 Edge Finger to PCIe-B
J7	PCIe TDI	1-2: Edge Finger to PCIe-A 3-4 Edge Finger to PCIe A + B 5-6 Edge Finger to PCIe-B
J8	PCIe TDO	1-2: Edge Finger to PCIe-A 3-4 Edge Finger to PCIe A + B 5-6 Edge Finger to PCIe-B
J9	PCIe TMS	Access point to the GND reference.
J10	Board Regulator 3.3-V Output	Pin 1 : Board 3.3V Pin 2: GND
J11	Board 12-V Supply	Pin 1 : Board 12V Pin 2: GND
JMP7	MUX SEL	1-2 : PCIe Edge Finger to PCIe-B 2-3: PCIe Edge Finger to PCIe-A
JMP8	Redriver PD	1-2 : Power Down 2-3: Normal Operation
JMP17	I2C Interface Sel	1-2 : USB2ANY 2-3: Aardvark
JMP18	CLK Buffer Enable	1-2 : Disabled 2-3: Enabled
JMP19	CLK Buffer Input Sel	1-2 : CLKIN1 2-3: CLKIN0
JMP20	CLK Buffer Ref. Out	1-2 : Enabled 2-3: Disabled

2.8 DS160PR412-421EVM Downstream Devices Control

Table 2-8 shows DS160PR412-421EVM downstream devices controls that affect DS1 and DS2 devices on the board.

Table 2-8. EVM Downstream Devices Controls

COMPONENT	NAME	FUNCTION OR DESCRIPTION
JMP1	DS160PR412_0 EQ/MODE	1-2: EQ0 L0 3-4: EQ0 L1 5-6: EQ0 L2 NC: EQ0 L3 7-8: EQ1 L0 9-10: EQ1 L1 11-12: EQ1 L2 NC: EQ1 L3 13-14: MODE = L0 15-16: MODE= L1 17-18: MODE= L2 NC: MODE = L3
JMP2	DS160PR412_1 EQ/MODE	1-2: EQ0 L0 3-4: EQ0 L1 5-6: EQ0 L2 NC: EQ0 L3 7-8: EQ1 L0 9-10: EQ1 L1 11-12: EQ1 L2 NC: EQ1 L3 13-14: MODE = L0 15-16: MODE= L1 17-18: MODE= L2 NC: MODE = L3
JMP3	DS160PR412_0 RX_DET/SCL	1-2:RX_DET L0 3-4: RX_DET L1 5-6: RX_DET L2 7-8: SCL NC: RX_DET L3
JMP4	DS160PR412_0 GAIN/SDA	1-2:GAIN L0 3-4: GAIN L1 5-6: GAIN L2 7-8: SCL NC: GAIN L3
JMP5	DS160PR412_1 RX_DET/SCL	1-2:RX_DET L0 3-4: RX_DET L1 5-6: RX_DET L2 7-8: SCL NC: RX_DET L3
JMP6	DS160PR412_1 GAIN/SDA	1-2:GAIN L0 3-4: GAIN L1 5-6: GAIN L2 7-8: SCL NC: GAIN L3

2.9 DS160PR412-421EVM Upstream Devices Control

Table 2-9 shows DS160PR412-421EVM upstream devices controls that affect US1-US2 devices on the board.

Table 2-9. EVM Upstream Devices Controls

COMPONENT	NAME	FUNCTION OR DESCRIPTION
JMP11	DS160PR421_2 EQ/MODE	1-2: EQ0 L0 3-4: EQ0 L1 5-6: EQ0 L2 NC: EQ0 L3 7-8: EQ1 L0 9-10: EQ1 L1 11-12: EQ1 L2 NC: EQ1 L3 13-14: MODE = L0 15-16: MODE= L1 17-18: MODE= L2 NC: MODE = L3
JMP14	DS160PR421_3 EQ/MODE	1-2: EQ0 L0 3-4: EQ0 L1 5-6: EQ0 L2 NC: EQ0 L3 7-8: EQ1 L0 9-10: EQ1 L1 11-12: EQ1 L2 NC: EQ1 L3 13-14: MODE = L0 15-16: MODE= L1 17-18: MODE= L2 NC: MODE = L3
JMP9	DS160PR421_2 RX_DET/SCL	1-2:RX_DET L0 3-4: RX_DET L1 5-6: RX_DET L2 7-8: SCL NC: RX_DET L3
JMP10	DS160PR421_2 GAIN/SDA	1-2:GAIN L0 3-4: GAIN L1 5-6: GAIN L2 7-8: SCL NC: GAIN L3
JMP15	DS160PR421_3 RX_DET/SCL	1-2:RX_DET L0 3-4: RX_DET L1 5-6: RX_DET L2 7-8: SCL NC: RX_DET L3
JMP16	DS160PR421_3 GAIN/SDA	1-2:GAIN L0 3-4: GAIN L1 5-6: GAIN L2 7-8: SCL NC: GAIN L3

2.10 Quick-Start Guide (Pin Mode)

Check that the shunts are at the following positions as Table 2-10 shows.

Table 2-10. Pin Mode Shunt Configuration

SHNT#	HEADER	SHUNT ACROSS PINS
1	JMP1	1-2
2	JMP1	7-8
3	JMP1	13-14
4	JMP2	1-2
5	JMP2	7-8
6	JMP2	13-14
7	JMP11	1-2
8	JMP11	7-8
9	JMP11	13-14
10	JMP14	1-2
11	JMP14	7-8
12	JMP14	13-14
13	JMP7	1-2
14	JMP8	2-3
15	JMP17	1-2
16	J17	1-2
17	J17	3-4
18	J17	5-6
19	JMP18	2-3
20	JMP19	2-3
21	JMP20	2-3

The redrivers are configured to operate in Pin Mode (MODE pins tied to L0).

1. RX_Detect state machine of all redrivers is enabled by leaving RX_DET pin open.
2. The redrivers are enabled (PWDN pins tied to GND).
3. The board is configured for any PCIe bus width.
4. DC Gain of all redrivers is set to 0 dB by leaving the GAIN config pin open for the redrivers.
5. EQ level of the RX CTLEs of all redrivers is set to 7 dB at 8 GHz by default.
6. If necessary, adjust EQ levels of the downstream and upstream redrivers, or both, by arranging shunts on JMP1, JMP2 for downstream redrivers and JMP11 and JMP14 for the upstream redrivers.
7. Plug the EVM into a PCIe x16 server motherboard slot. Ensure the motherboard is powered down before installing the EVM or configured for hot-plug operation.
8. Install a compatible PCIe endpoint card into one of the PCIe connectors on the EVM based on configuration of the SEL pin. Note: PCIe-A requires enabling bifurcation on the motherboard.
9. Power-up the motherboard.

2.11 Quick-Start Guide (SMBus Slave Mode)

1. Configure all devices to operate in the SMBus Slave Mode by setting their MODE pins to the L1 level. This is accomplished by placing a shunt across pins 15–16 on JMP1, JMP2, JMP11, and JMP14 .
2. Set a unique SMBus Slave address for each device by placing shunts in the following arrangement:
   - On JMP1 connector, place shunt across pins 1-2 L0, downstream device PR412_0.
   - On JMP2 connector, place a shunt across pins 3-4 L1 for downstream device PR412_1.
   - On JMP11 connector, place a shunt across pins 5-6 L2 for upstream device PR421_2.
   - On JMP14 connector, remove shunts across 1-2, 3-4, 5-6 so EQ0_ADD# pin is floating L3 for upstream device PR421_3.

3. On JMP3-6, JMP9, JMP10, JMP15, and JMP16 move shuts from current position and install across pins 7-8.
4. Enable all devices by pulling their PD pins to GND. This is accomplished by placing a shunt on JMP8 across pins 2-3.
5. Connect USB2ANY Adapter to P4 (Note that the USB2ANY Adapter is not supplied with the DS160PR412-421EVM). Install shunt on JMP17 across pins 1-2.
6. Install SigCon Architect Version 3.0.0.15 application and the DS160PR412-421 profile.
7. Plug the EVM into a PCIe x16 server motherboard slot. Ensure the motherboard is powered down before installing the EVM or configured for hot-plug operation.
8. Install a compatible PCIe endpoint card into the straddle connector of the EVM.
9. Power-up the motherboard.
10. Start the SigCon Architect application.
11. Select the DS160PR412-421 Configuration Page and select the *Apply* box to enable the device profile. If necessary, edit device addresses in the Edit Device Addresses box.
12. In the DS160PR412-421 High Level Page, select Block Diagram as shown in Figure 2-1.
13. Select desired EQ Settings and Driver VOD.
14. Select the devices to which you want to apply the selected settings and click the *Apply to All Channels* button.

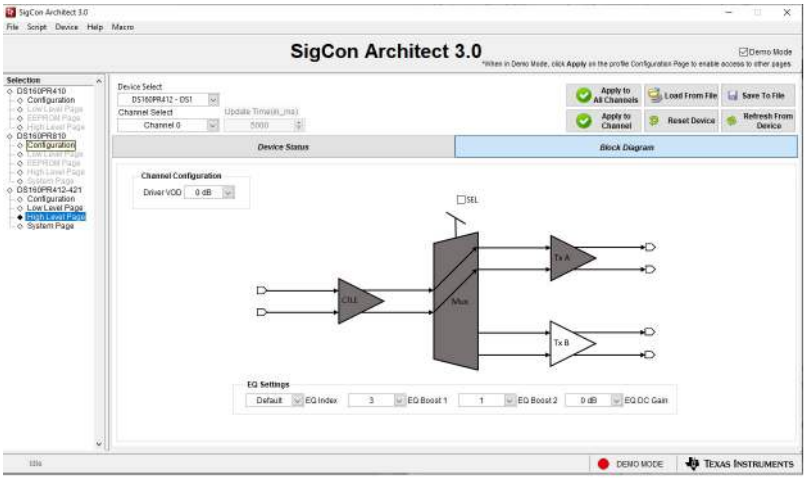

Figure 2-1. SigCon Architect DS160PR412-421 High Level Page

3 Schematics

Figure 3-1 through Figure 3-9 show the EVM schematics.

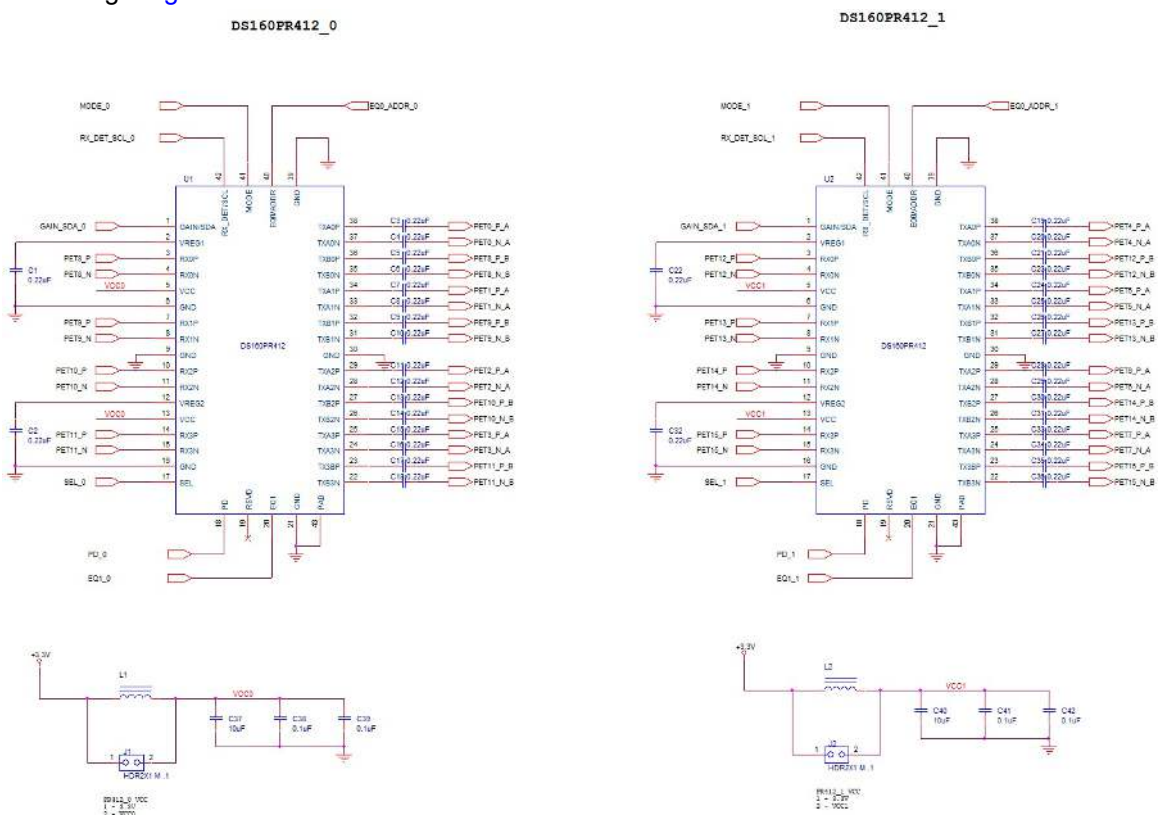

Figure 3-1. DS160PR412

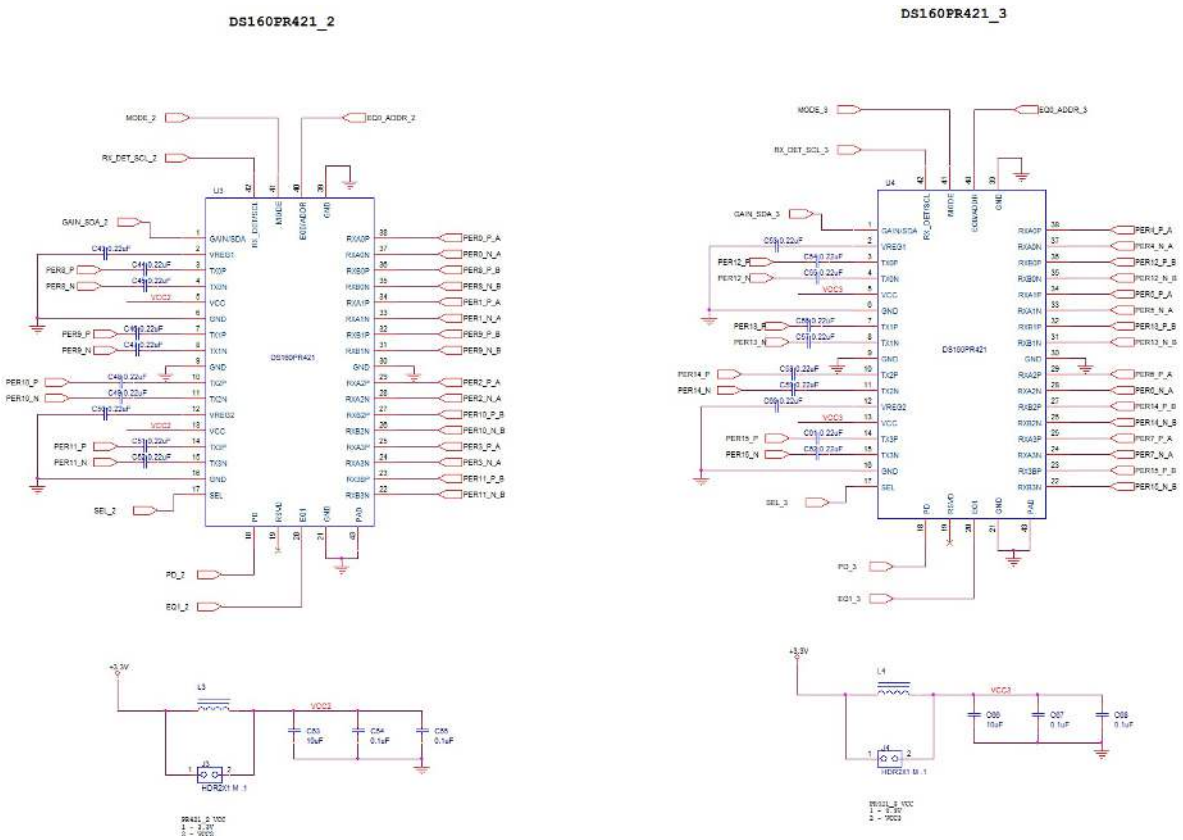

Figure 3-2. DS160PR421

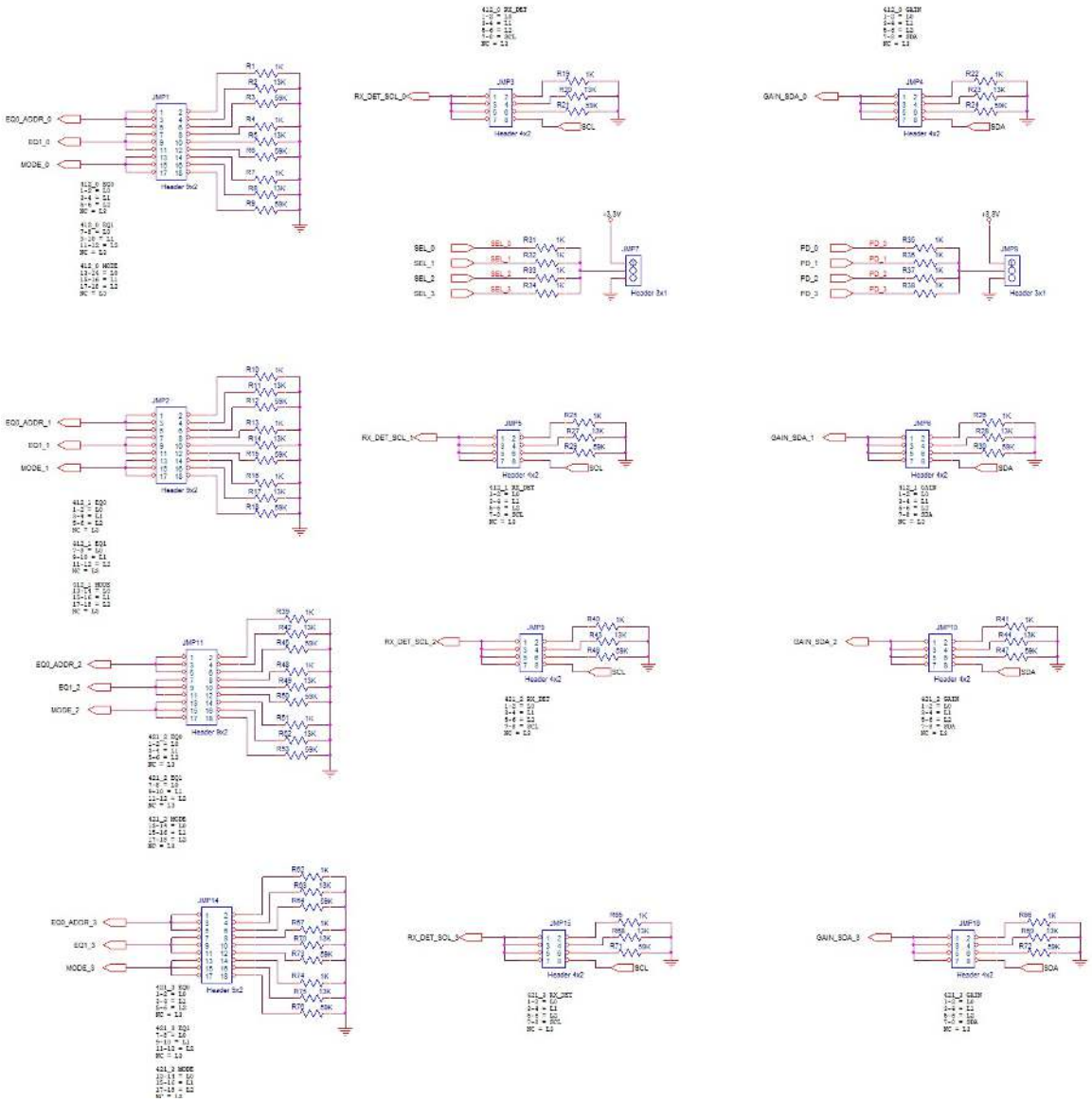

Figure 3-3. Configuration Headers

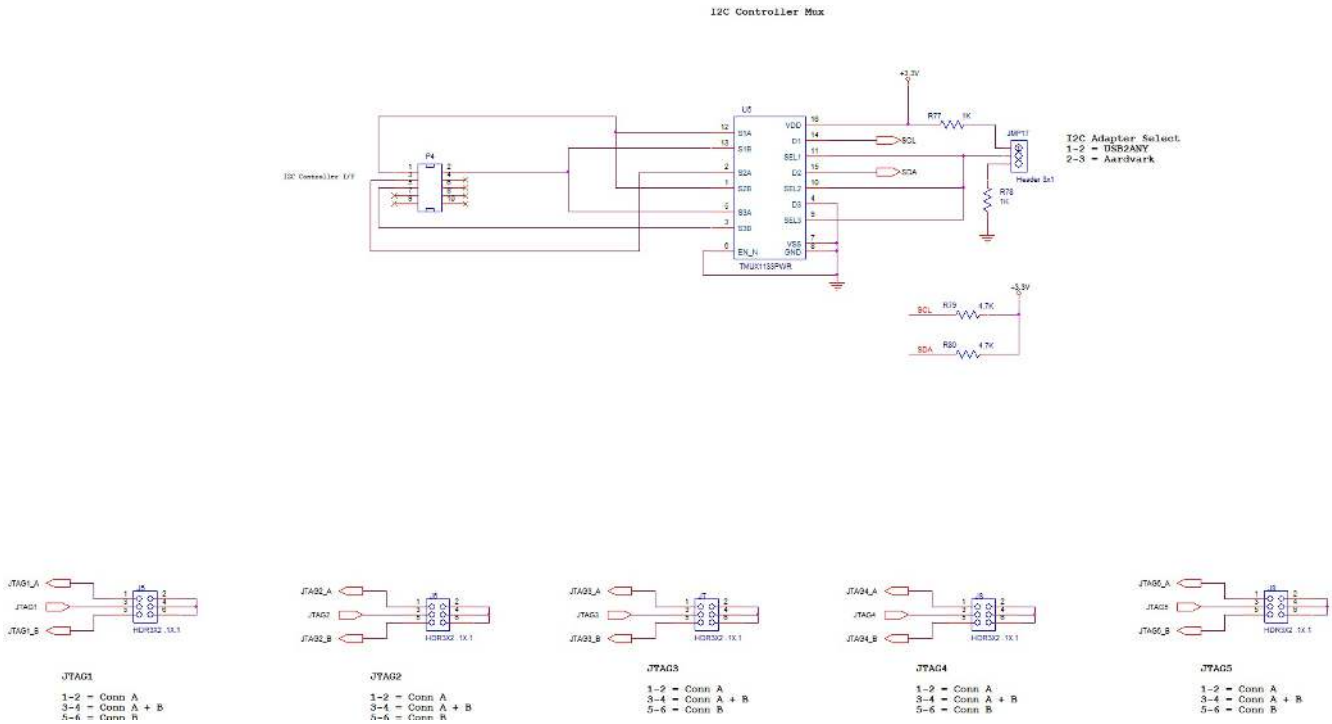

Figure 3-4. I2C Adapter Selection

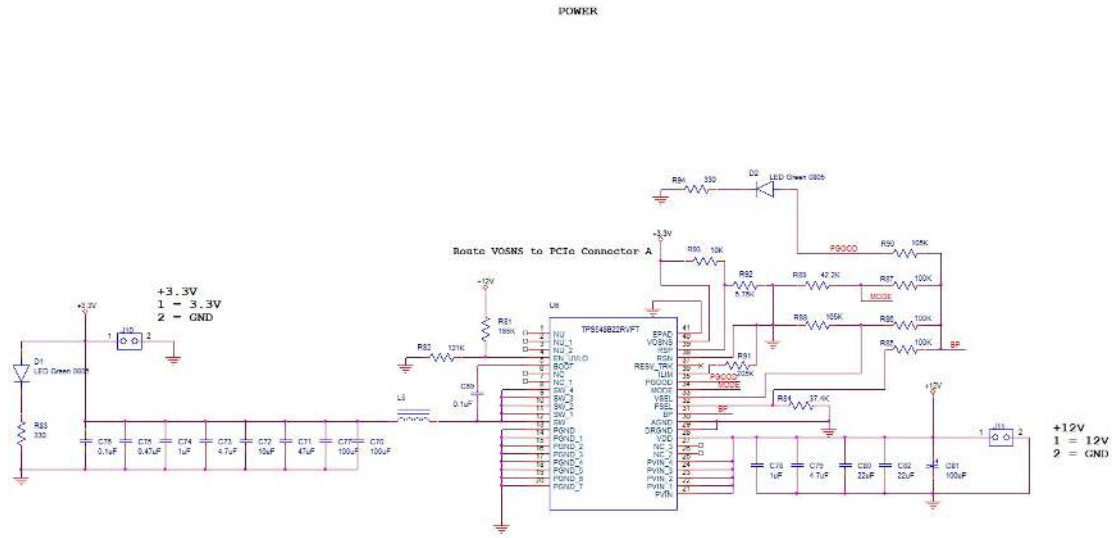

Figure 3-5. Power

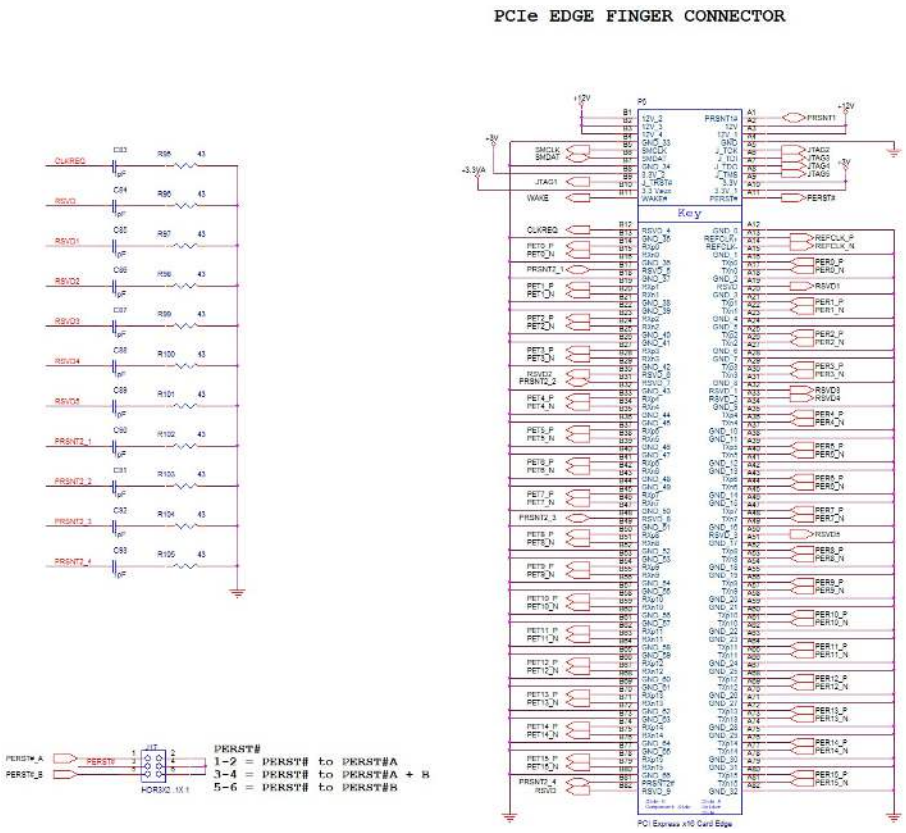

Figure 3-6. EDGE Finger

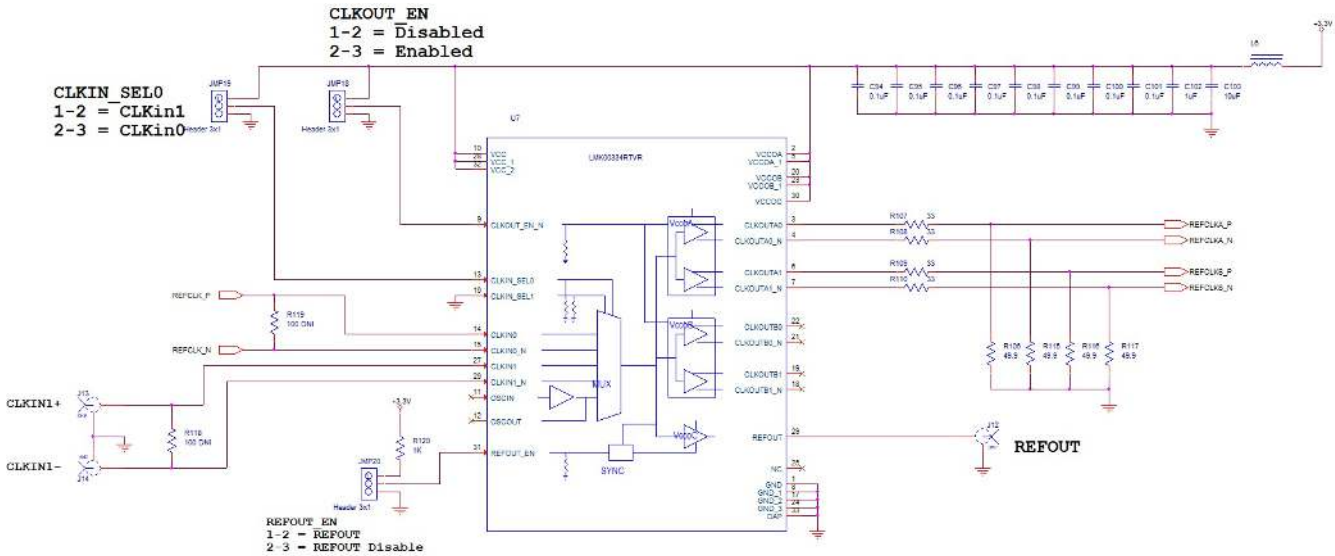

Figure 3-7. PCIe Clock

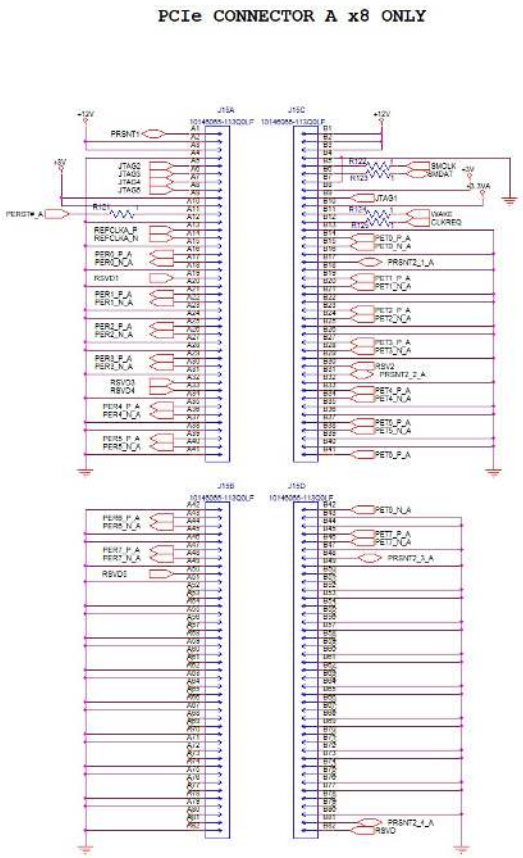

Figure 3-8. PCIe x8 Connector A

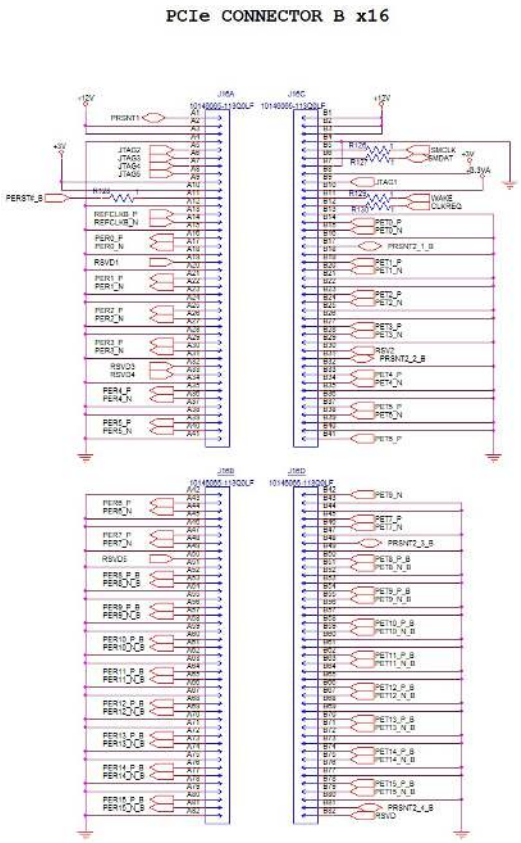

Figure 3-9. PCIe x16 Connector B

4 PCB Layouts

Figure 4-1 through Figure 4-6 illustrate the EVM PCB layout images.

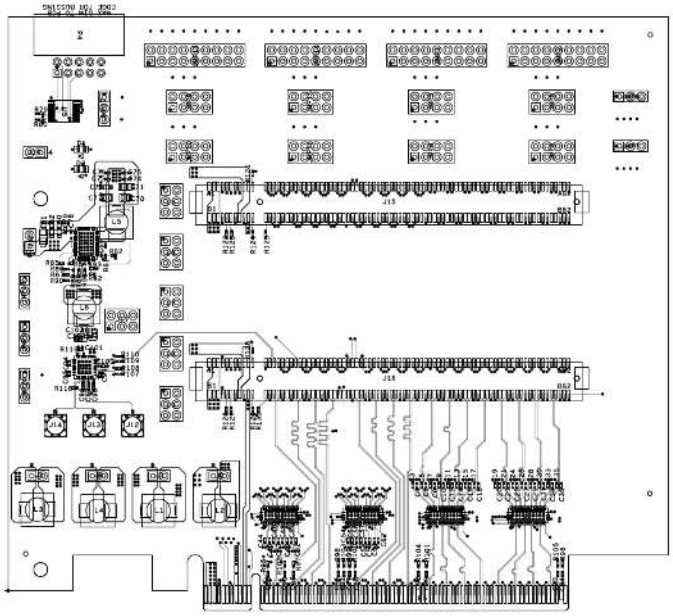

Figure 4-1. Top Layer

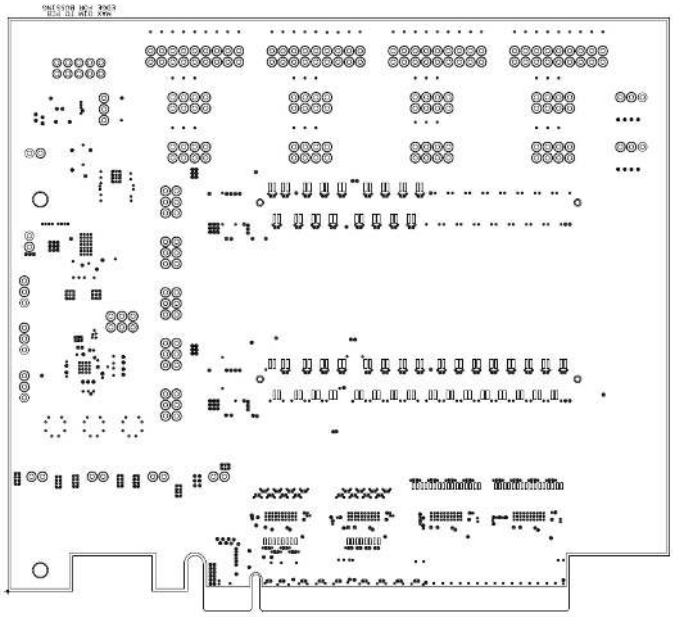

Figure 4-2. Layer 2

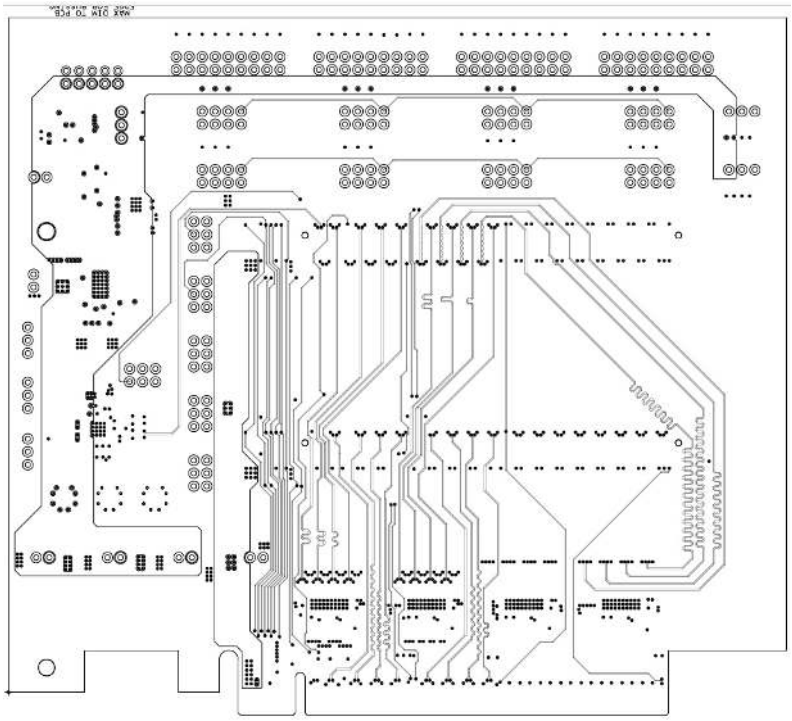

Figure 4-3. Layer 3

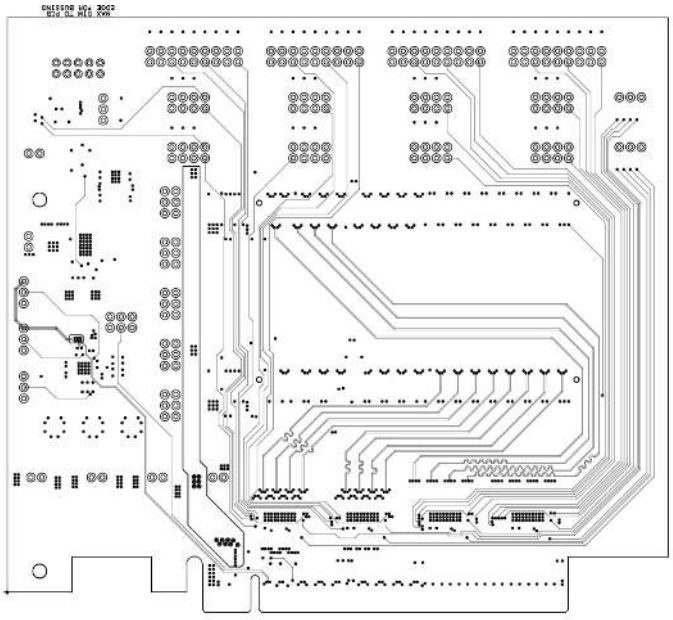

Figure 4-4. Layer 4

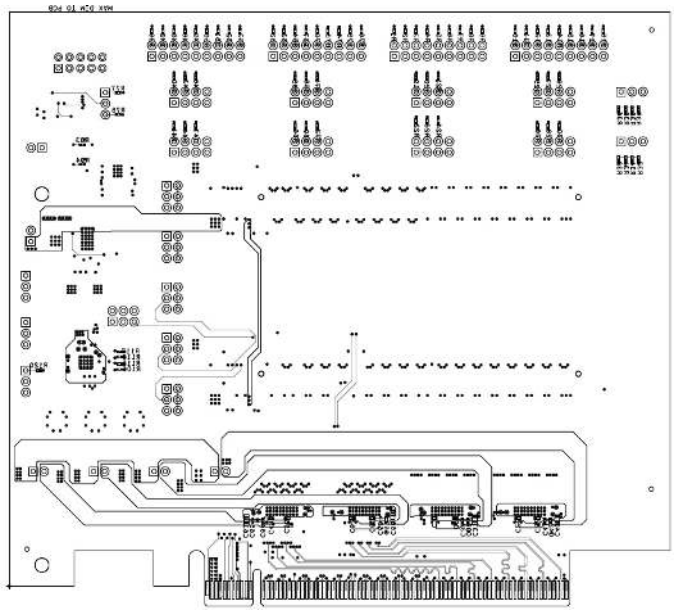

Figure 4-5. Layer 5

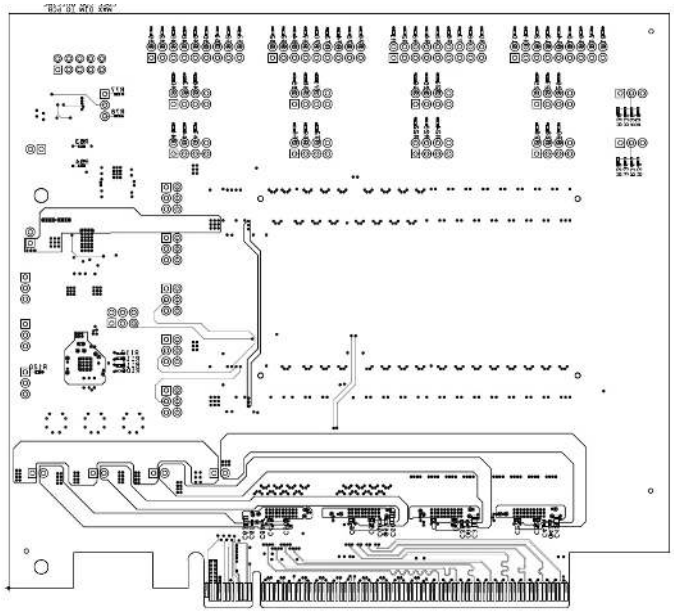

Figure 4-6. Bottom Layer

5 Bill of Materials

Table 5-1 displays the EVM bill of materials.

Table 5-1. DS160PR412-421 Bill of Materials

ITEM	QTY	Reference	Part	Manufacturer	Part Number
1	56	C1,C2,C3,C4,C5,C6,C7,C8,C9,C10,C11,C12,C13,C14,C15,C16,C17,C18,C19,C20,C21,C22,C23,C24,C25,C26,C27,C28,C29,C30,C31,C32,C33,C34,C35,C36,C43,C44,C45,C46,C47,C48,C49,C50,C51,C52,C53,C54,C55,C56,C57,C58,C59,C60,C61,C62	0.22uF	Murata Electronics	GRM155R61A224KE19J
2	5	C37,C40,C63,C66,C103	10uF	Murata Electronics	GRM188R60J106ME47D
3	18	C38,C39,C41,C42,C64,C65,C67,C68,C69,C76,C94,C95,C96,C97,C98,C99,C100,C101	0.1uF	Murata Electronics	GRM155R71A104KA01J
4	2	C70,C77	100uF	AVX Corporation	F950J107MPAAQ2
5	1	C71	47uF	Taiyo Yuden	JMK212BJ476MG-T
6	1	C72	10uF	Murata Electronics	GRM188R61A106KE69D
7	2	C73, C79	4.7uF	Murata Electronics	GRM155R60J475ME47D
8	3	C74,C78,C102	1uF	Yageo	CC0402KRX5R6BB105
9	1	C75	0.47uF	Murata Electronics	GRM155R60J474KE19D
10	2	C80,C82	22uF	Murata Electronics	GRM188C80G226MEA0D
11	1	C81	100uF	KEMET	T520A107M006ATE070
12	11	C83,C84,C85,C86,C87,C88,C89,C90,C91,C92,C93	1pF	Murata Electronics	GRM1555C1H1R0CA01D
13	2	D1,D2	LED Green 0805	Arrow (Lumex)	670-1006 (SML_LX0805GC)
14	4	JMP1,JMP2,JMP11,JMP14	Header 9x2	AMP	103322-9
15	8	JMP3,JMP4,JMP5,JMP6,JMP9,JMP10,JMP15,JMP16	Header 4x2	AMP	103322-4
16	6	JMP7,JMP8,JMP17,JMP18,JMP19,JMP20	Header 3x1	AMP	103321-3
17	6	J1,J2,J3,J4,J10,J11	HDR2X1 M .1	AMP	103321-2
18	6	J5,J6,J7,J8,J9,J17	Header 4x2	AMP	103322-4
19	3	J12,J13,J14	SMP	Rosenberger	19S101-40ML5
20	2	J15,J16	Header	Amphenol ICC (FCI)	10146065-113Q0LF
21	1	LB1	Label	Brady	THT-14-423-10THT-14-423-10
22	6	L1,L2,L3,L4,L5,L6	6.8uH	Eaton	DRA73-6R8-R
23	1	PCB1	HSDC092A	Any	HSDC092
24	1	P4	Header 5x2 0.1" Shroud RA thru-hole	3M	30310-5002HB30310-5002HB
25	1	P5	PCI Express x16 Card Edge		
26	1	P6	PCI Bracket	Keystone	9203
27	31	R1,R4,R7,R10,R13,R16,R19,R22,R25,R26,R31,R32,R33,R34,R35,R36,R37,R38,R39,R40,R41,R48,R51,R62,R65,R66,R6	1K	Panasonic Electronic Components	ERJ-2GEJ102X
28	20	R2,R5,R8,R11,R14,R17,R20,R23,R27,R28,R42,R43,R44,R49,R52,R63,R68,R69,R70,R75	13K	Panasonic Electronic Components	ERJ-2GEJ133X
29	20	R3,R6,R9,R12,R15,R18,R21,R24,R29,R30,R45,R46,R47,R50,R53,R64,R71,R72,R73,R76	59K	Panasonic Electronic Components	ERJ-2RKF5902X
30	2	R79,R80	4.7K	Panasonic Electronic Components	ERJ-2GEJ472X

Table 5-1. DS160PR412-421 Bill of Materials (continued)

ITEM	QTY	Reference	Part	Manufacturer	Part Number
31	2	R81,R88	165K	Panasonic Electronic Components	ERJ-2RKF1653X
32	1	R82	121K	Yageo	RC0402FR-07121KL
33	2	R83,R94	330	Panasonic Electronic Components	ERA-2AEB331X
34	1	R84	37.4K	Panasonic Electronic Components	ERJ-2RKF3742X
35	3	R85,R86,R87	100K	Panasonic Electronic Components	ERJ-2GEJ104X
36	1	R89	42.2K	Panasonic Electronic Components	ERJ-2RKF4222X
37	1	R90	105K	Panasonic Electronic Components	ERJ-2RKF1053X
38	1	R91	205K	Panasonic Electronic Components	ERJ-2RKF2053X
39	1	R92	5.76K	Panasonic Electronic Components	ERJ-2RKF5761X
40	1	R93	10K	Panasonic Electronic Components	ERA-2AED103X
41	11	R95,R96,R97,R98,R99,R100,R101,R102,R103,R104,R105	43	Panasonic Electronic Components	ERA-2AKD430X
42	4	R106,R115,R116,R117	49.9	Panasonic Electronic Components	ERJ-2RKF49R9X
43	4	R107,R108,R109,R110	33	Panasonic Electronic Components	ERA-2AKD330X
44	0	R118,R119	100	Panasonic Electronic Components	ERA-2AED101X
45	10	R121,R122,R123,R124,R125,R126,R127,R128,R129,R130	1	Yageo	RC0402FR-071RL
46	2	SCRW1,SCRW2	screw	Keystone Electronics	9900
47	2	U1,U2	DS160PR412	Texas Instruments	DS160PR412
48	2	U3,U4	DS160PR421	Texas Instruments	DS160PR421
49	1	U5	TMUX1133PWR	Texas Instruments	TMUX1133PWR
50	1	U6	TPS548B22RVFT	Texas Instruments	TPS548B22RVFT
51	1	U7	LMK00334RTVR	Texas Instruments	LMK00334RTVR

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