HARRIS

HA-5180

Low Bias Current, Low Power JFET Input Operational Amplifier

May 1990

Features

- Ultra Low Bias Current 250fA
- Low Power Supply Current 0.8mA
- Low Offset Voltage ..... 0.5mV Max.
- Unity Gain Bandwidth 2MHz
- Slew Rate 7V/μs

Applications

- Electrometer Amplifier Designs
- Photo Current Detectors
- Precision, Long-Term Integrators
- Low Drift Sample & Hold Circuits
- Very High Impedance Buffers
- High Impedance Biological Micro Probes
- Refer to Application Note 555

Description

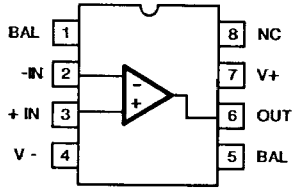
The Harris HA-5180 is an ultra low input bias current, JFET input, monolithic operational amplifier which also features low power, low offset voltage and excellent AC characteristics. Employing FET/Bipolar construction coupled with dielectric isolation this operational amplifier offers the lowest input bias currents (250fA typical) available in any monolithic operational amplifier. The HA-5180 has another unique feature in which the offset bias current may be nulled by externally adjusting the offset voltage.

The HA-5180 also offers excellent AC performance not previously available in similar hybrid or monolithic op amp designs. The 2MHz bandwidth and 7V/μs slew rate of the HA-5180 extends the bandwidth and speed for applications such as very low drift sample and hold amplifiers and photo-current detectors. Other applications include use in electrometer designs, pH/Ion sensitive electrodes, low current oxygen sensors, long term precision integrators and very high impedance buffer measurement designs.

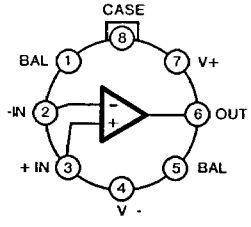
The HA-5180 is packaged in an 8 pin (TO-99) Metal Can and an 8 lead Mini-DIP and is pin compatible with most existing op amp configurations. The case of the TO-99 package is internally connected to pin 8 so that it may be connected to the same potential as the input. This feature helps minimize stray leakage to the case, helps shield the amplifier from external noise and reduces common mode input capacitance. For military grade product, refer to the HA-5180/883 data sheet.

Pinouts

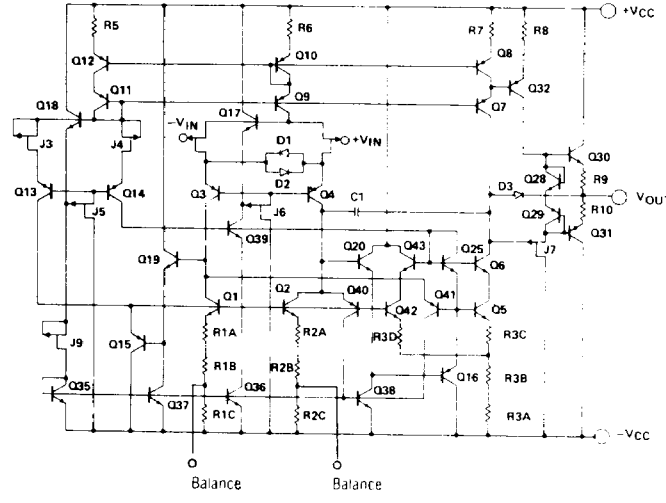
HA7-5180 (CERAMIC MINI-DIP)
TOP VIEW



HA2-5180 (TO-99 METAL CAN)
TOP VIEW



Schematic



CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

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Absolute Maximum Ratings (Note 1)

T_A = +25°C Unless Otherwise Specified
Voltage Between V+ and V- Terminals 40V
Differential Input Voltage..... ±40V
Output Short Circuit Duration ..... Indefinite
Power Dissipation (Note 2)..... 300mW

Operating Temperature Ranges

HA-5180-2.....-55°C ≤ T_A ≤ +125°C
HA-5180-5..... 0°C ≤ T_A ≤ +75°C
Storage Temperature Range .....-65°C ≤ T_A ≤ +150°C

Electrical Specifications V+ = +15V, V- = -15V, Unless Otherwise Specified.

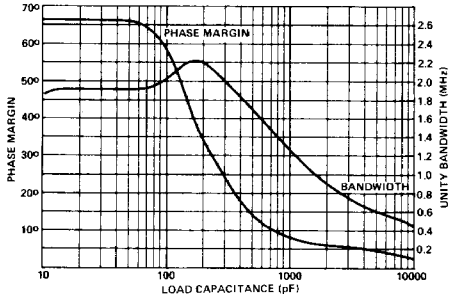
PARAMETER	TEMP	HA-5180-2 -55°C to +125°C			HA-5180-5 0°C to + 75°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
INPUT CHARACTERISTICS								
Offset Voltage	+25°C	-	1	3	-	1	3	mV
	Full	-	-	4	-	-	4	mV
Average Offset Voltage Drift	Full	-	5	-	-	5	-	µV/°C
Bias Current (Note 3)	+25°C	-	250	1000	-	250	1000	fA
	Full	-	100	500	-	6	30	pA
Offset Current (Note 3)	+25°C	-	30	200	-	30	200	fA
	Full	-	6	30	-	1	5	pA
Common Mode Range	Full	±10	±12	-	±10	±12	-	V
Differential Input Resistance	+25°C	-	10^{12}	-	-	10^{12}	-	Ω
Input Capacitance	+25°C	-	5	-	-	5	-	pF
Input Noise Voltage, 0.1Hz to 10Hz	+25°C	-	5	-	-	5	-	μV_{p-p}
Input Noise Voltage Density								
f_O = 10Hz	+25°C	-	200	-	-	200	-	$nV/\sqrt{Hz}$
f_O = 100Hz	+25°C	-	120	-	-	120	-	$nV/\sqrt{Hz}$
f_O = 1000Hz	+25°C	-	70	-	-	70	-	$nV/\sqrt{Hz}$
Input Noise Current (f = 1kHz)	+25°C	-	0.01	-	-	0.01	-	$pA/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 4)	+25°C	200K	1M	-	200K	1M	-	V/V
	Full	150K	-	-	150K	-	-	V/V
Common Mode Rejection Ratio (Note 5)	Full	90	110	-	90	110	-	dB
Closed Loop Bandwidth (A_{VCL} = +1)	+25°C	-	2	-	-	2	-	MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 6)	+25°C	±10	±12	-	±10	±12	-	V
	Full	±10	-	-	±10	-	-	V
Full Power Bandwidth (Note 7)	+25°C	-	110	-	-	110	-	kHz
Output Current (Note 8)	+25°C	±10	±15	-	±10	±15	-	mA
Output Resistance (Note 9)	+25°C	-	25	-	-	25	-	Ω
TRANSIENT RESPONSE								
Overshoot	+25°C	-	30	50	-	30	50	%
Rise Time	+25°C	-	75	-	-	75	-	ns
Slew Rate	+25°C	4	7	-	4	7	-	V/µs
Settling Time (Note 10)	+25°C	-	2	-	-	2	-	µs
POWER SUPPLY CHARACTERISTICS								
Supply Current	Full	-	0.7	1	-	0.8	1	mA
Power Supply Rejection Ratio (Note 11)	Full	85	105	-	85	105	-	dB

NOTES:

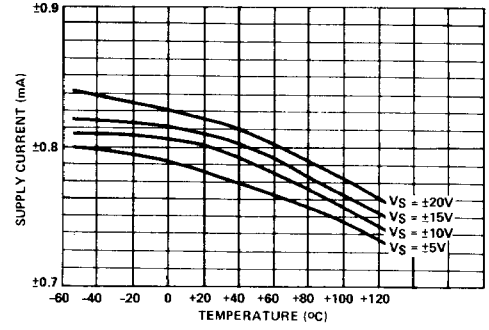
1. Absolute Maximum Ratings are limiting values applied individually beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. Derate at 6.9 mW/°C for operation at ambient temperatures above +75°C.
3. This parameter is guaranteed by design and is not 100% tested.
4. V_{OUT} = ±10V; R_L = 2K. Gain dB = $20 \log_{10} A_V$.
5. ΔV_{CM} = ±10V D.C.
6. R_L = 2K.
7. R_L = 2K, V_{PEAK} = 10V; Full power bandwidth guaranteed based on slew rate measurement using $FPBW = \frac{\text{Slew Rate}}{2\pi V_{Peak}}$
8. V_{OUT} = ±10V.
9. Output resistance specified under open loop conditions (f = 100Hz).
10. Settling time is speified to 0.1% of final value for a 10V output step and A_V = -1.
11. ΔV_{SUPPLY} = ±10V D.C. to ±20V D.C.

Typical Performance Curves

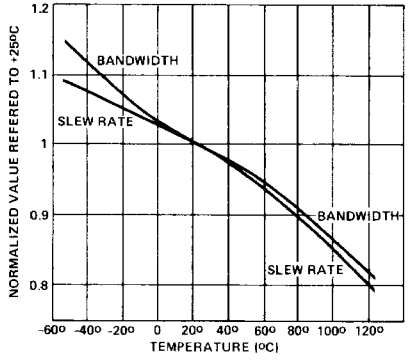
SMALL SIGNAL BANDWIDTH AND PHASE MARGIN vs. LOAD CAPACITANCE



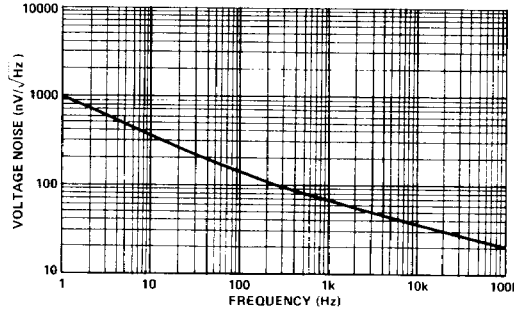
SUPPLY CURRENT vs. TEMPERATURE



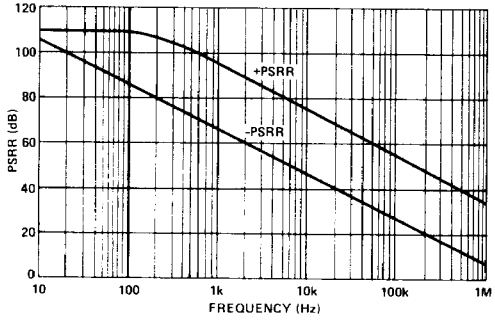
NORMALIZED AC PARAMETERS vs. TEMPERATURE



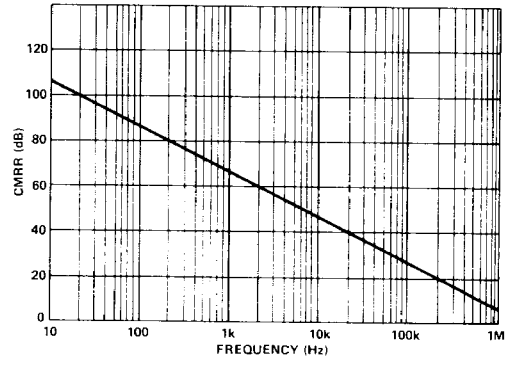
INPUT VOLTAGE NOISE vs. FREQUENCY



PSRR vs. FREQUENCY

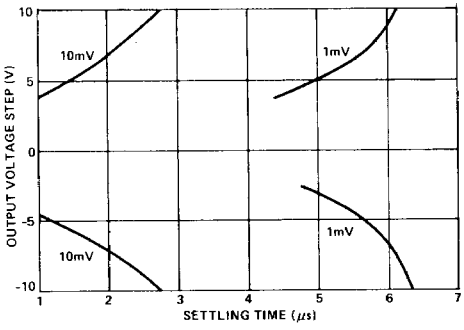


CMRR vs. FREQUENCY

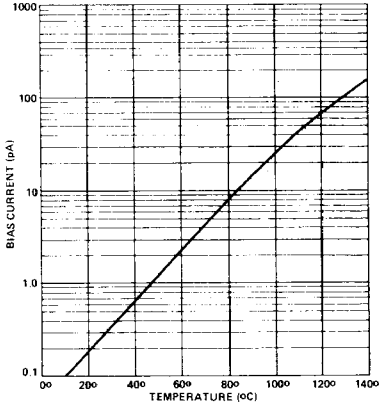


Typical Performance Curves (Continued)

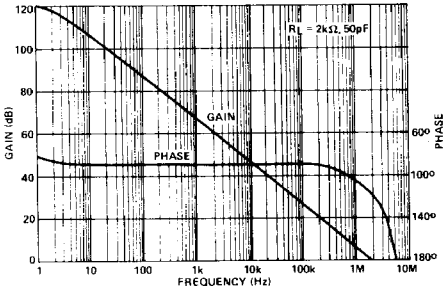
SETTLING TIME FOR VARIOUS OUTPUT STEP VOLTAGES



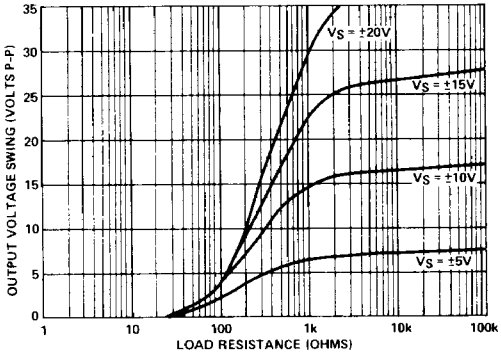
BIAS CURRENT vs. TEMPERATURE



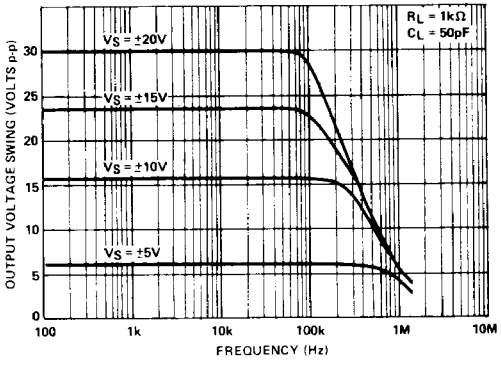
OPEN LOOP FREQUENCY RESPONSE



OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



OUTPUT VOLTAGE SWING vs. FREQUENCY



Typical Applications

The HA-5180 offers one of the lowest input bias currents of any monolithic operational amplifier and is ideal for use in applications for measuring signals from very high impedance or very low current sources. To fully utilize the capabilities of the HA-5180, care should be taken to minimize noise pickup and current leakage paths with the use of shielding and guarding techniques and by placing the device as close as possible to the signal source. The small size and low quiesent current (possible battery operation) of the HA-5180 allows easy installation at the signal source or inside a probe. The HA-5180 is internally compensated and is capable of driving long signal cables which have several hundred pF capacitive loading.

If it is not possible to place the HA-5180 very close to the signal source, then the use of shielded coaxial cable will offer the best isolation of the high impedance signal line from external noise sources. However, the effects of leakage, capacitance and vibrational noise should be taken into account when using coaxial cables. Leakage can be minimized by using cables with very high insulation resistance (such as polyethylene or Virgin Teflon). For example, the current to voltage converter circuit (as shown in Figure 1) will eliminate leakage across the insulation of the cable by forcing the signal line to the same potential as the shield. This circuit also provides fast response to input signals because the cable capacitance is never forced to be charged or discharged. However, the cable capacitance directly increases the input capacitance of the circuit and could cause the circuit to become unstable; if so, adding capacitance across Rf will stabilize the circuit again. Leakage can also be reduced in the high-impedance non-inverting configuration (see Figure 2) by bootstrapping the shield to the same potential as the signal source instead of ground. If low closed-loop gains are used, the non-inverting configuration could also become unstable due to the positive feedback to the input through the cable capacitance. One method of compensating this circuit is to place a small (low leakage) capacitor from the input to ground. This technique will also reduce the effective capacitance presented to the signal source. When large closed-loop gains and/or long cable lengths are used, a buffer should be added to the circuit to drive the shield.

When using coaxial cable with the HA-5180 the cable should be kept as rigid and vibration free as possible. Frictional movement of the shield over the insulation can generate electrical charge which is picked up by the high impedance signal line as noise. Movement and bending of the cable can also cause charge movement due to small changes in cable capacitance and capacitance to surrounding objects. Another source of noise currents is that which is generated by the movement of a conductor in a magnetic field.

For lowest leakage at the device inputs either use a teflon IC socket or connect the signal line to the HA-5180 inputs using teflon standoffs. A guard ring, as shown in Figure 3, applied to both sides of the pc board and bootstrapped to the same potential as the input signal will minimize leakage paths across the pc board. Pin 8 of the TO-99 can, which is internally tied to the case, should also be tied to the bootstrap potential to help minimize noise pickup and leakage currents across the package insulation. This technique will also reduce common mode input capacitance.

Cleanliness of circuit boards and components is also important for achieving low leakage currents. Printed circuit boards and components should be thoroughly cleaned by using a low residue solvent such as TMC Freon , rinsed by deionized water and dried with nitrogen. The circuit board should be protected from high contamination and high humidity environments. A good quality conformal coating with low dielectric absorption provides the best protection from humidity and contamination.

Input protection is generally not necessary when designing with the HA-5180. Many electrometer type devices, especially CMOS, require elaborate zener protection schemes which may compromise overall performance. The Harris dielectric isolation process and JFET input design enables the HA-5180 to withstand input signals several volts beyond either supply and large differential signals equal to the rail-to-rail supply voltage without damage or degradation of performance.

For more information see Application Note 555.

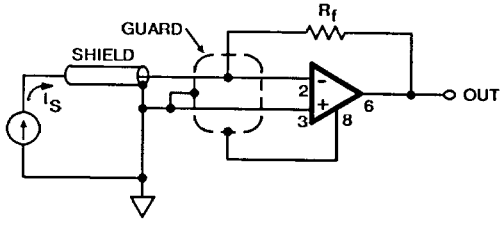


FIGURE 1. CURRENT TO VOLTAGE CONVERTER

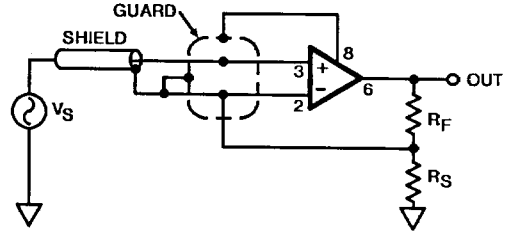


FIGURE 2. VERY HIGH IMPEDANCE NON-INVERTING AMPLIFIER

Typical Applications (Continued)

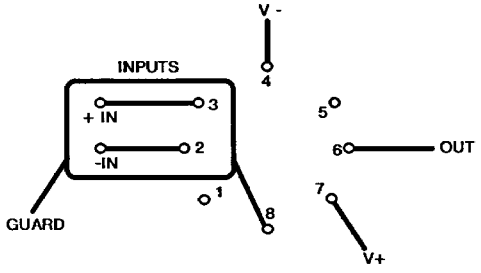


FIGURE 3. GUARD RING EXAMPLE

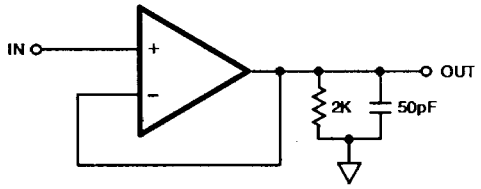


FIGURE 4. SLEW RATE AND TRANSIENT RESPONSE TEST CIRCUIT

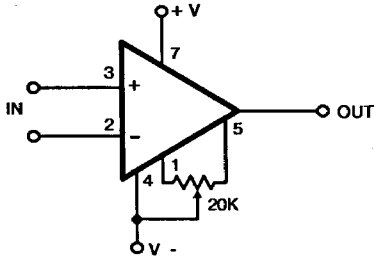
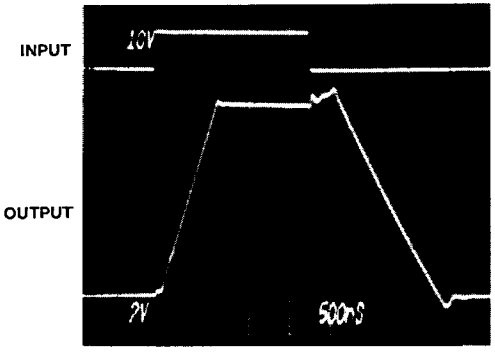
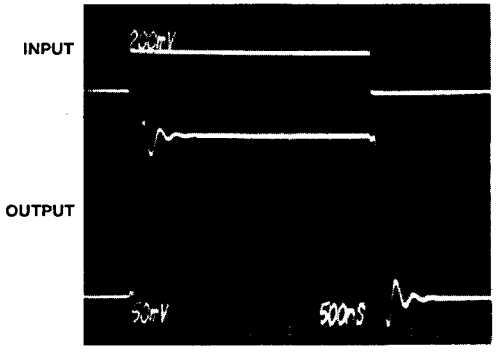


FIGURE 5. SUGGESTED OFFSET ADJUSTMENT CIRCUIT

LARGE SIGNAL RESPONSE
Vertical Scale (Volts: 5V/Div. Input)
(Volts: 2V/Div. Output)
Horizontal Scale (Time: 500ns/Div.)



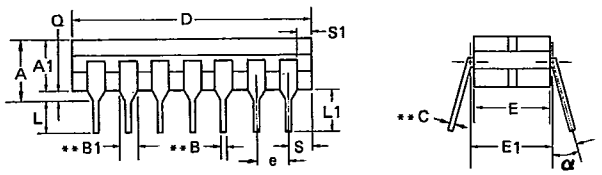
SMALL SIGNAL RESPONSE
Vertical Scale (Volts: 100mV/Div. Input)
(Volts: 50mV/Div. Output)
Horizontal Scale (Time: 500ns/Div.)



Package Configuration

T-90-20

A B C D E .300 CERAMIC DUAL-IN-LINE



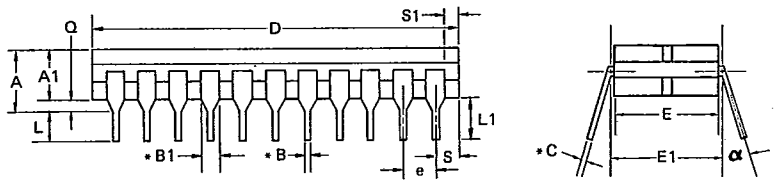
PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
A	8 SSI	— .200	.140 .160	.016 .023	.050 .065	.008 .015	.375 .395	.245 .265	.290 .310	.100 BSC	.125 .150	.150 —	— .055	.005 —	.015 .060	0° 15°
B1	14 MSI	— .200	.140 .170	.016 .023	.050 .065	.008 .015	.753 .785	.265 .285	.290 .310	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
B2	14 LSI	— .200	.140 .170	.016 .023	.050 .065	.008 .015	.753 .785	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
C1	16* MSI	— .200	.140 .170	.016 .023	.050* .065*	.008 .015	.753 .785	.265 .285	.290 .310	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°
C2	16* LSI	— .200	.140 .170	.016 .023	.050* .065*	.008 .015	.753 .785	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°
D	18 LSI	— .200	.140 .170	.016 .023	.050* .065*	.008 .015	.882 .915	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
E	20 LSI	— .200	.140 .170	.016 .023	.050* .065*	.008 .015	.940 .970	.285 .305	.300 .320	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°

* End leads are half leads where B remains the same and B1 is $\frac{0.035}{0.045}$

** Solder dip finish add +0.003 inches

F .400 CERAMIC DUAL-IN-LINE

G H .600 CERAMIC DUAL-IN-LINE



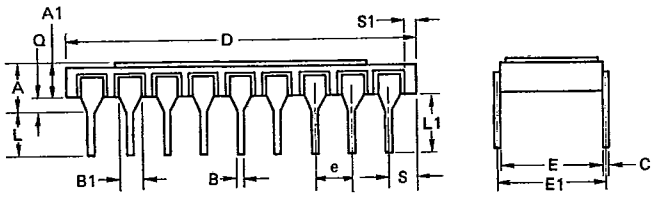
PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q	DIM. α
F .400	22 LSI	— .225	.150 .180	.016 .023	.050 .065	.008 .015	1.055 1.085	.375 .395	.395 .415	.100 BSC	.125 .180	.150 —	— .080	.005 —	.015 .060	0° 15°
G .600	24 LSI	— .225	.150 .180	.016 .023	.050 .065	.008 .015	1.24 1.27	.515 .535	.595 .615	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°
H .600	28 LSI	— .225	.160 .190	.016 .023	.050 .065	.008 .015	1.44 1.47	.515 .535	.595 .615	.100 BSC	.125 .180	.150 —	— .098	.005 —	.015 .060	0° 15°

* Solder dip finish add +0.003 inches.

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches. BSC means basic spacing between centerlines.

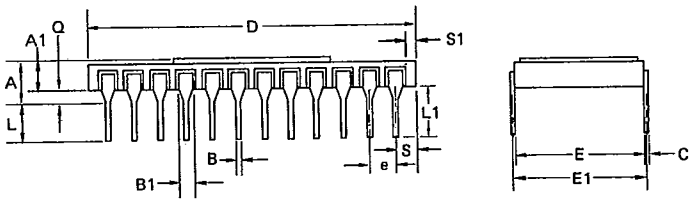
Package Configuration

I .300 SIDEBRAZE DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
I	18	— .200	.080 .110	.016 .023	.045 .060	.008 .015	.890 .910	.280 .300	.290 .310	.100 BSC	.125 .180	.150 —	— .098	.005 —	.025 .045

J K L .600 SIDEBRAZE DUAL-IN-LINE



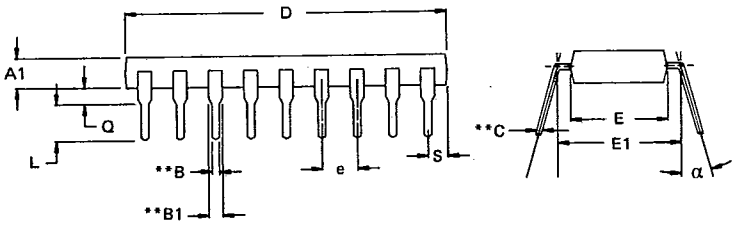
PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. L1	DIM. S	DIM. S1	DIM. Q
J	24	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.185 1.215	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.040 .060
K	28	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.385 1.415	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.030 .060
L	40	— .225	.080 .110	.016 .023	.040 .054	.008 .015	1.980 2.020	.587 .603	.598 .612	.100 BSC	.125 .180	.150 —	— .080	.005 —	.040 .060

NOTE: Dimensions are $\frac{\text{Min}}{\text{Max}}$. Dimensions are in inches.

BSC means basic spacing between centerlines.

Package Configuration

M N O P Q .300 PLASTIC DUAL-IN-LINE

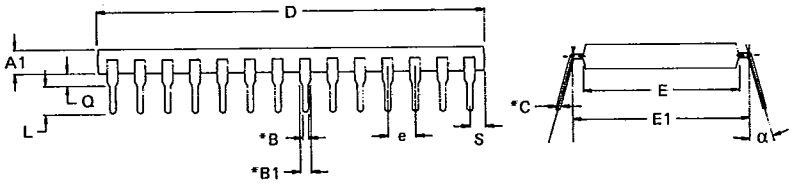


PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
M	8	.125/.140	.016/.023	.050/.070	.008/.015	.370/.390	.245/.265	.290/.310	.090/.110	.110/.150	.030/.050	.020/.040	0°/15°
N	14	.125/.140	.016/.023	.050/.070	.008/.015	.750/.770	.245/.265	.290/.310	.090/.110	.110/.150	.030/.050	.020/.040	0°/15°
O	16*	.125/.140	.016/.023	.050/.070	.008/.015	.750/.770	.245/.265	.290/.310	.090/.110	.110/.150	.025/.035	.020/.040	0°/15°
P	18	.125/.140	.016/.023	.050/.070	.008/.015	.900/.920	.245/.265	.290/.310	.090/.110	.110/.150	.040/.060	.020/.040	0°/15°
Q	20	.130/.145	.016/.023	.050/.070	.008/.015	1.030/1.050	.250/.270	.290/.310	.090/.110	.110/.150	.060/.080	.020/.040	0°/15°

* End leads are half leads where B remains the same and B1 is 0.035/0.045

** Solder dip finish add 0.003 inches.

R S .600 PLASTIC DUAL-IN-LINE



PKG. CODE	LEAD COUNT	DIM. A1	DIM. B	DIM. B1	DIM. C	DIM. D	DIM. E	DIM. E1	DIM. e	DIM. L	DIM. S	DIM. Q	DIM. α
R	24	.145/.155	.016/.023	.050/.070	.008/.015	1.24/1.26	.540/.560	.590/.610	.090/.110	.110/.150	.045/.095	.020/.040	0°/15°
S	28	.145/.155	.016/.023	.050/.070	.008/.015	1.54/1.57	.540/.560	.590/.610	.090/.110	.110/.150	.110/.160	.020/.040	0°/15°

* Solder dip finish add 0.003 inches.

NOTE: Dimensions are Min/Max. Dimensions are in inches.

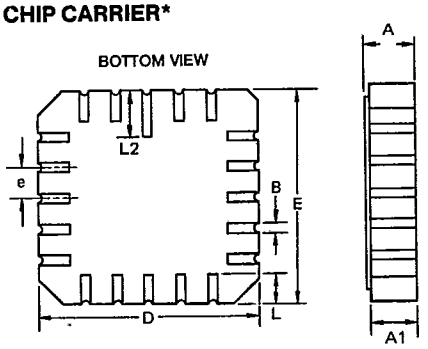
BSC means basic spacing between centerlines.

Package Configuration

T .350 CERAMIC LEADLESS CHIP CARRIER*

U .450 CERAMIC LEADLESS CHIP CARRIER*

V .650 CERAMIC LEADLESS CHIP CARRIER*

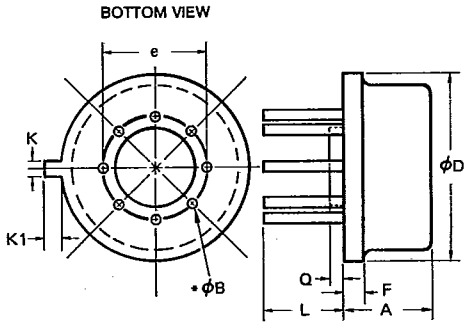


PKG. CODE	LEAD COUNT	DIM. A	DIM. A1	DIM. B	DIM. D	DIM. E	DIM. e	DIM. L	DIM. L2
T	20 .350 SQ	.073 .089	.063 .077	.022 .028	.342 .358	.342 .358	.050 BSC	.045 .055	.075 .095
U	28 .450 SQ	.074 .088	.064 .076	.022 .028	.442 .458	.442 .458	.050 BSC	.045 .055	.075 .095
V	44 .650 SQ	.073 .089	.063 .077	.022 .028	.643 .662	.643 .662	.050 BSC	.045 .055	.075 .095

* Solder dip finish for military parts conform to MIL-M-38510, Type A.

W TO-99 METAL CAN

X TO-100 METAL CAN



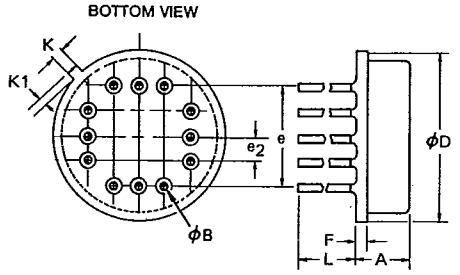
PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. F	DIM. K	DIM. K1	DIM. L	DIM. Q
W	8 TO-99	.165 .185	.016 .018	.345 .365	.190 .210	.020 .040	.028 .034	.028 .040	.505 .550	.015 .040
X	10 TO-100	.165 .185	.016 .018	.345 .365	.220 .240	.020 .040	.028 .034	.028 .040	.505 .550	.015 .040

* Solder dip finish add +0.003 inches.

NOTE: Dimensions are Min/Max. Dimensions are in inches.

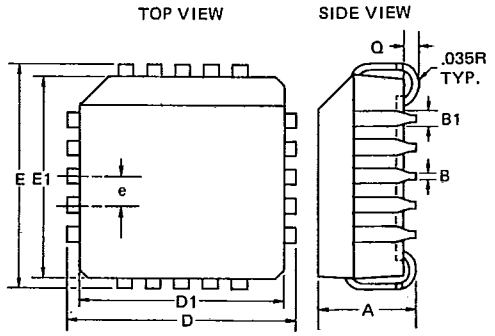
BSC means basic spacing between centerlines.

Y TO-8 METAL CAN



PKG. CODE	LEAD COUNT	DIM. A	DIM. ϕB	DIM. ϕD	DIM. e	DIM. e2	DIM. F	DIM. K	DIM. K1	DIM. L
Y	12 TO-8	.130 / .150	.016 / .021	.585 / .615	.400 / BSC	.100 / BSC	.020 / .040	.027 / .034	.027 / .045	.500 / .550

AA AB AC PLASTIC LEADED CHIP CARRIER



PKG. CODE	LEAD COUNT	DIM. A	DIM. B	DIM. B1	DIM. D/E	DIM. D1/E1	DIM. e	DIM. Q
AA	20	.165 / .180	.013 / .021	.026 / .032	.385 / .395	.350 / .356	.050 / BSC	.020 / —
AB	28	.165 / .180	.013 / .021	.026 / .032	.485 / .495	.450 / .456	.050 / BSC	.020 / —
AC	44	.165 / .180	.013 / .021	.026 / .032	.685 / .695	.650 / .656	.050 / BSC	.020 / —

NOTE: Dimensions are Min / Max. Dimensions are in inches. BSC means basic spacing between centerlines.