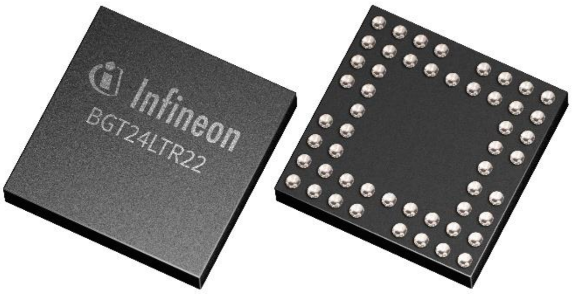
BGT24LTR22

Low Power Multichannel 24GHz Radar MMIC for Smart Sensing Applications



Features

- 24 GHz transceiver MMIC (2 TX, 2 RX)
- Fully integrated low phase noise VCO
- Medium power amplifier with variable output power
- Integrated power detectors
- Homodyne low noise quadrature receivers
- Configurable analog baseband amplification stages
- Frequency divider
- Low power consumption
- Multimode operation (Master/Slave)
- Fully ESD protected device
- Single ended RF terminals
- Single supply voltage 1.5V
- WFWLB-52-3 pin plastic package sized 3.63mmx3.63mm
- Pb-free (RoHS compliant) package

Potential Applications

- Smart home appliances
- Drone collision avoidance
- Traffic monitoring
- Security applications

Description

BGT24LTR22 is a low power, low noise multi-channel Silicon Germanium transceiver MMIC for 24 GHz radar applications. It provides building blocks for analog signal generation and reception, operating in the frequency range from 24.0 GHz up to 24.25 GHz. Integrated digital blocks controlling the chip are implemented in order to support radar system design.

The device is manufactured in Infineon's B11HFC BiCMOS technology offering a cutoff frequency higher than 300GHz. It is housed in Infineons plastic embedded Wafer Level Ball Grid Array (eWLB) package which can be processed in standard SMT flow.

Table of Content

1 Electrical Characteristics

Attention: ***Test ■ means that the parameter is not subject to production test. It was verified by design or characterization respectively.***

1.1 Absolute Maximum Ratings

Table 1 **Absolute Maximum Ratings: T_A = -40 °C .. 85°C;** all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	-0.3	-	$V_{DD,max}$ +0.3	V	
DC voltage at RF pins	$V_{DC,RF}$	0	-	0	V	DC-short at RF pins (RX1, RX2, TX1, TX2) to GND
DC voltage at VCO tuning pin VTUNE	V_{TUNE}	0	-	5	V	
Voltage applied to all other user I/O pins	$V_{DC,I/O}$	-0.3	-	V_{DD} +0.3	V	
RF input power RX inputs	P_{RF}	-	-	0	dBm	Pins RX1, RX2
Total power dissipation	P_{DISS}	-	-	500	mW	
Storage temperature range	T_{STG}	-40	-	150	°C	
Operational temperature range	T_C	-40	-	+85	°C	Temperature at package soldering point
Thermal resistance of package	$R_{th,P}$	-	18	-	K/W	Represents bulk silicon to package solder balls

Attention: ***Stresses exceeding the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.***

1.2 ESD Integrity

Table 2 ESD integrity

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
ESD robustness HBM[1]	$V_{ESD\text{-}HBM}$	-1	-	1	kV	All pins
ESD robustness CDM[2]	$V_{ESD\text{-}CDM}$	-500	-	500	V	All pins

1) According to ANSI/ESDA/JEDEC JS-001 (R = 1.5kOhm, C = 100pF) for Electrostatic Discharge Sensitivity Testing, Human Body Model (HBM)-Component Level

2) According to ESDA/JEDEC JS-002 Field-Induced Charged Device Model (CDM), Test Method for Electrostatic-Discharge-Withstand Thresholds of Microelectronic Components

Please note that this result is subject to:
- lot variations within the manufacturing process as specified by Infineon
- changes in the specific test setup

1.3 Power Supply

Table 3 Power Supply Electrical Characteristics: T_A = -40 °C .. 85 °C

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Supply voltage	V_{DD}	1.45	1.5	1.6	V	
Supply current nominal operation mode	I_{DD_ON}	-	170	230	mA	SPI Settings – Refer to AN607
Supply current in reduced power consumption mode	I_{DD_RED}	-	135	-	mA	SPI Settings – Refer to AN607
Supply current standby-mode	I_{DD_STDBY}	-	-	1	mA	SPI Settings – Refer to AN607

1.4 TX Section

Table 4 TX Section Electrical Characteristics: T_A = -40 °C .. 85 °C, V_{DD} = 1.45 V .. 1.6 V; all parameters are for master mode operation (unless otherwise specified)

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
VCO frequency range	f_{VCO}	24.0	-	24.25	GHz	
VCO phase noise	P_N	-	-65 -85	-50 -70	dBc/Hz	@10kHz offset @100kHz offset
VCO AM noise	P_{AM}	-	-148	-	dBc/Hz	@100kHz offset
Tuning voltage to cover VCO frequency range	V_{TUNE}	0	0.7	3	V	ISM band covered from 0 V to 1.5 V

Table 4 **TX Section Electrical Characteristics:** T_A = -40 °C .. 85 °C, V_{DD} = 1.45 V .. 1.6 V; all parameters are for master mode operation (unless otherwise specified)

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
VCO tuning sensitivity within VCO frequency range	$\Delta f / \Delta V_{TUNE}$	500	1600	3000	MHz/V	
VCO temperature drift within VCO frequency range	$\Delta f / \Delta T$	-	-5	-	MHz/K	
2nd Harmonic suppression	$\Delta P_{fund,H2}$	15	27	-	dBc	
VCO nonharmonic suppression	P_{SPUR}	-	-55	-40	dBm	
TX output power[1]	P_{TX1}	1	5	9.5	dBm	
TX output power dynamic range	ΔP_{OUT}	17	24	-	dB	
TX load impedance	Z_{TX1}	-	50	-	Ω	Single-ended at outer edge of compensation structure on PCB as indicated in AN607

1.5 RX Section

Table 5 **RX Section Electrical Characteristics:** T_A = -40 °C .. 85 °C, V_{DD} = 1.45 V .. 1.6 V; all parameters are within master mode operation (unless otherwise specified)

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
RX frequency range	f_{RX}	24.0	-	24.25	GHz	
Single-sideband noise figure[1]	NF_{SSB}	-	8	16.5	dB	@ f_{IF} = 200 kHz – Bypass Mode SPI configurable – Refer to AN607
		-	8.5	15.5		@ f_{IF} = 200 kHz – ABB Mode SPI configurable – Refer to AN607
RF downconverter conversion gain[1]	G_{DC}	16	25	33	dB	@ f_{IF} = 200 kHz – Bypass Mode SPI configurable – Refer to AN607
Analog baseband Gain	G_{ABB}	-	0/30/35/40/ 45/50/55/60	-	dB	Configurable via SPI
Input 1 dB compression point	IP_{1dB}	-	-19	-	dBm	RX in Bypass Mode
LO input power	P_{LOIN}	-	-10	-	dBm	For slave mode operation

[1] Refer to AN607 for more details about parameter variation over temperature

Table 5 **RX Section Electrical Characteristics:** T_A = -40 °C .. 85 °C, V_{DD} = 1.45 V .. 1.6 V; all parameters are within master mode operation (unless otherwise specified)

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Baseband high pass filters cut off frequency	$F_{c\text{-}hpf}$	-	20/50/80/100	-	kHz	Configurable via SPI 1st order, -3 dB definition
Baseband low pass filters cut off frequency	$F_{c\text{-}lpf}$	-	600	-	kHz	4th order, -3 dB definition
Quadrature phase imbalance	ε_P	-10	-	10	deg	
Quadrature amplitude imbalance	ε_A	-1.5	-	1.5	dB	
IF output impedance	Z_{IF}	-	400	-	Ω	Differential
IF output impedance – Bypass Mode	Z_{IFBY}	-	1	-	kΩ	Differential
IF output common mode voltage	V_{IFCMD}	-	0.75	-	V	
IF output power supply rejection ratio	*PSRR*	-	60	-	dB	@ DC
RX input impedance	*ZRXIN*	-	50	-	Ω	Single-ended at outer edge of compensation structure on PCB as indicated in AN607

1.6 Frequency Divider

Table 6 **Frequency Divider Electrical Characteristics:** T_A = -40 °C .. 85 °C, V_{DD} = 1.45 V .. 1.6 V, Freq = 24GHz

Parameter	Symbol	Value			Unit	Note/ Test Condition
		Min.	Typ.	Max.		
Dividing factor 1	D_{DIV1}	-	2^20	-	-	selectable via SPI
Dividing factor 2	D_{DIV2}	-	2^16	-	-	selectable via SPI
Dividing factor 3	D_{DIV3}	-	2^14	-	-	selectable via SPI
Dividing factor 4	D_{DIV4}	-	2^13	-	-	selectable via SPI
Dividing factor 5	D_{DIV5}	-	16	-	-	selectable via SPI
Divider output power	P_{DIV5}	-13	-5	0	dBm	For dividing factor 5 - @50 Ohms load
Divider output voltage range	V_{DIV}	0	-	V_{DD}	V	For dividing factors 1 to 4
External capacitive load	$C_{extLoad}$	-	-	15	pF	For dividing factors 1 to 4

2 SPI Interface

2.1 SPI Timing Requirements

The BGT24LTR22 is configured using a 4-wire SPI interface. It is used to configure the internal modules of the BGT24LTR22 chip via registers. The main tasks are to set the mode of operation of the TX and/or RX chain and the baseband section. Communication with an external micro controller is done via the four dedicated pins SPIDI, SPIDO, SPICS and SPICLK. Figure 1 demonstrates how the timing of the SPI behaves. The "working edge" is the rising edge of the clock `SPICLK`. The master application processor presents data for BGT24LTR22 at the falling edge on `SPIDI`, BGT24LTR22 samples data at the rising edge. Read data is presented for the master on the rising edge on `SPIDO`. Refer to the application note AN607 for all details related to the SPI registers to control the MMIC.

Note: Asynchronous reset (`SPIRST`) must be de-asserted at least 10 ns before the falling edge of `SPICLK`.

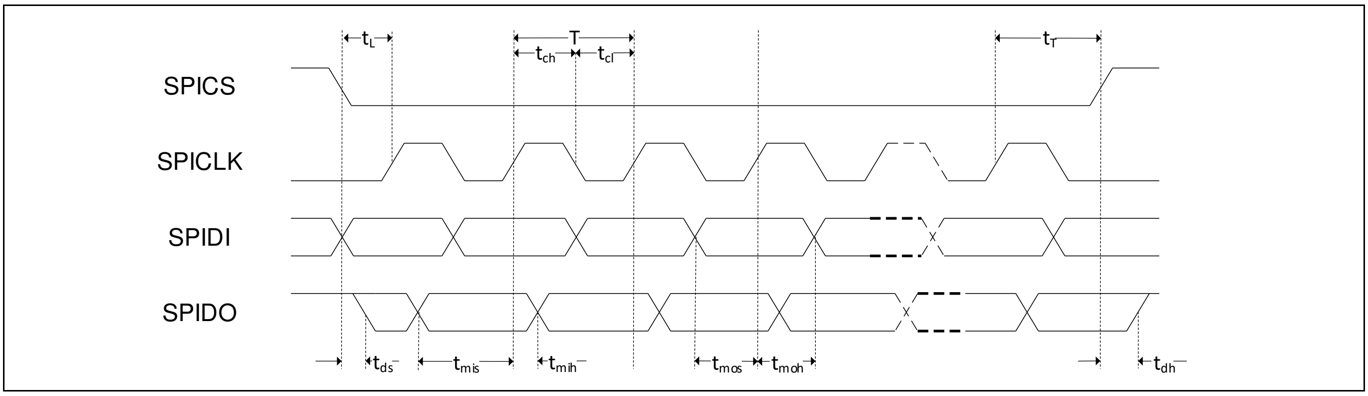


Figure 1 SPI timing diagram

Table 7 SPI Interface timing requirements

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
SPI clock period	T	20			ns	50MHz, with <1% clock jitter
Clock high time	t_{ch}	9			ns	
Clock low time	t_{cl}	9			ns	
Setup time SPIDI	t_{mos}	5			ns	
Hold time SPIDI	t_{moh}	5			ns	
Setup time SPIDO	t_{mis}	5			ns	
Hold time SPIDO	t_{mih}	1			ns	
Delay time from the output pad logic	$t_{pad\_out\_dly}$			5	ns	

3 Block Diagram and Pin Description

3.1 Block Diagram

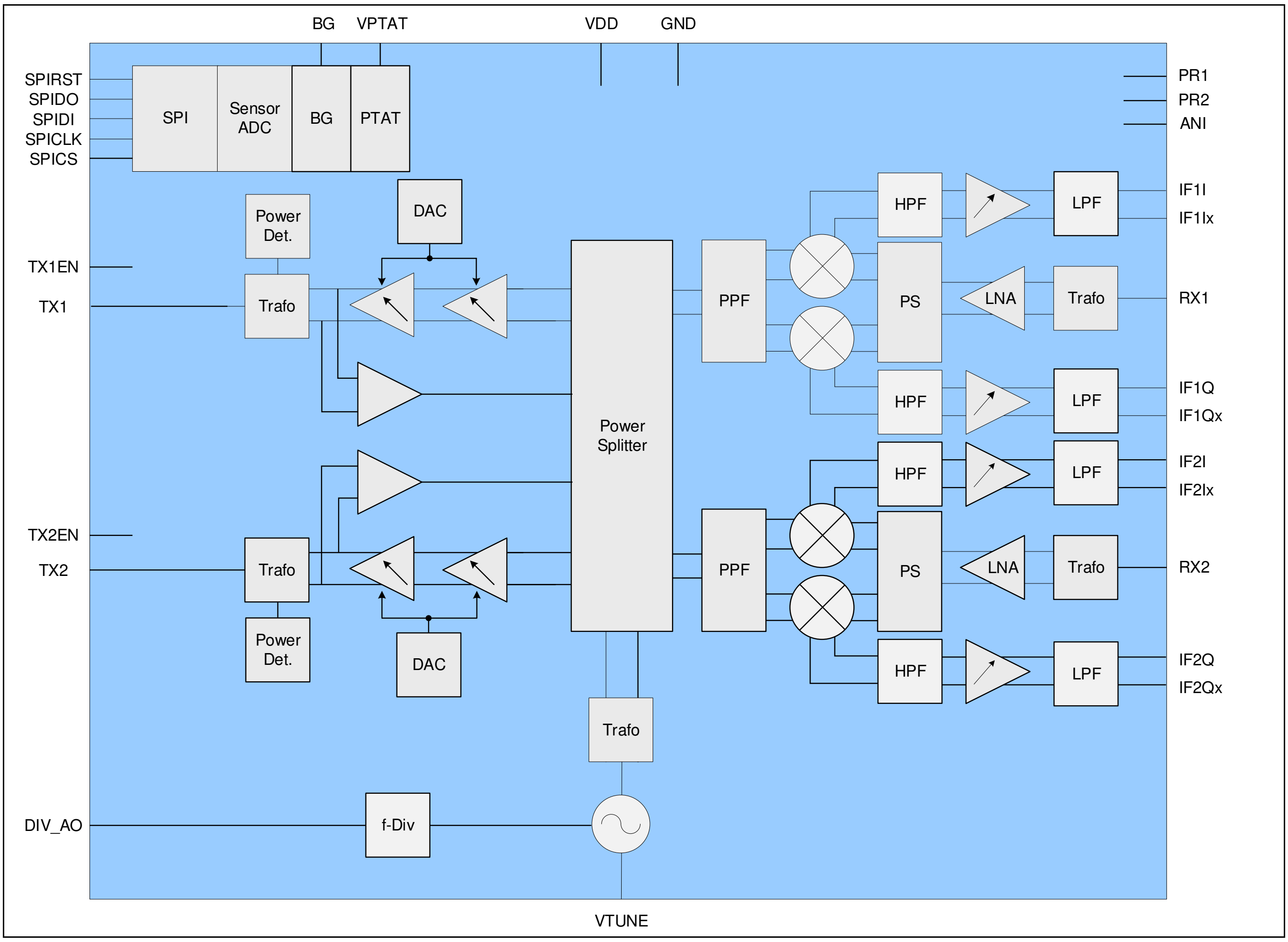


Figure 2 BGT24LTR22 block diagram

3.2 Pin Out

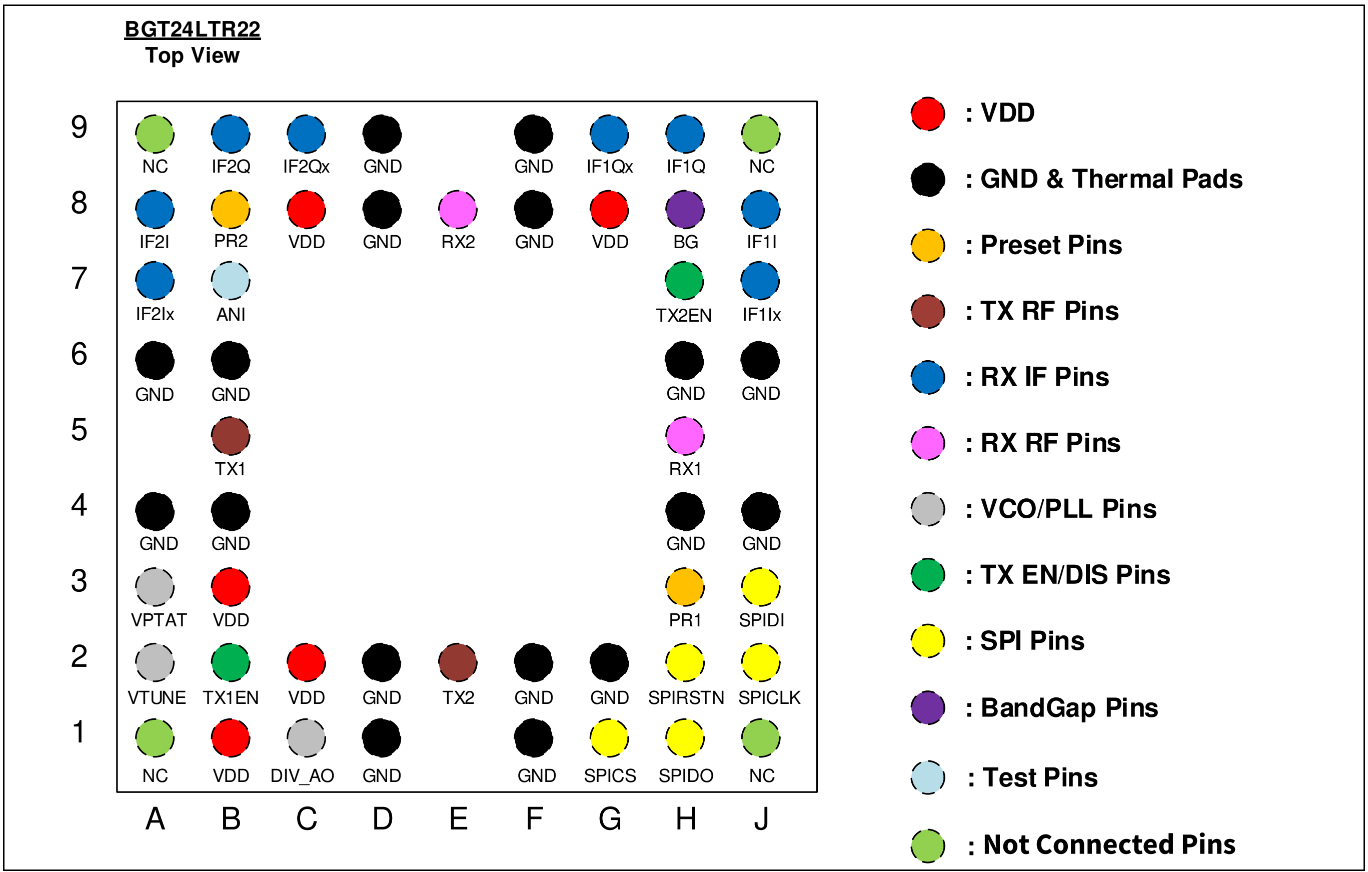


Figure 3 Pin out (top view)

3.3 Pin Definition and Function

Table 8 Pin definition and function

Pin Number	Name	Function
A1, A9, J1, J9	NC	No connection
B1, B3, C2, C8, G8	VDD	DC supply voltage
H5	RX1	RF input - receiver 1
E8	RX2	RF input - receiver 2
E2	TX2	Bidirectional RF I/O RF output – transmitter 2/LO input 2
B5	TX1	Bidirectional RF I/O RF output – transmitter 1/LO input 1
J8, J7	IF1I, IF1Ix	Complementary in phase downconverter IF output – receiver 1
H9, G9	IF1Q, IF1Qx	Complementary quadrature phase downconverter IF output - receiver 1
A8, A7	IF2I, IF2Ix	Complementary in-phase downconverter IF output – receiver 2

Table 8 Pin definition and function

Pin Number	Name	Function
B9, C9	IF2Q, IF2Qx	Complementary quadrature phase downconverter IF output - receiver 2
A4, A6, B4, B6, D1, D2, D8, D9, F1, F2, F8, F9, G2*, H4, H6, J4, J6	GND	Ground
H3	PR1	Mode select – pin 1
B8	PR2	Mode select - pin 2
C1	DIV_AO	Frequency divider output
B2	TX1EN	Enable transmitter 1
H7	TX2EN	Enable transmitter 2
H8	BG	Bandgap voltage output
A2	VTUNE	VCO frequency tuning input
A3	VPTAT	PTAT voltage source output
G1	SPICS	SPI chip select (spi_cs_i)
H1	SPIDO	SPI data out (spi_do_o)
H2	SPIRST	SPI reset
J2	SPICLK	SPI clock (spi_clk_i)
J3	SPIDI	SPI data in (spi_di_i)
B7	ANI	Analog input for testing

Note: It is mandatory to connect Pin G2 to ground for SPI programming

4 Package Dimensions and Footprint

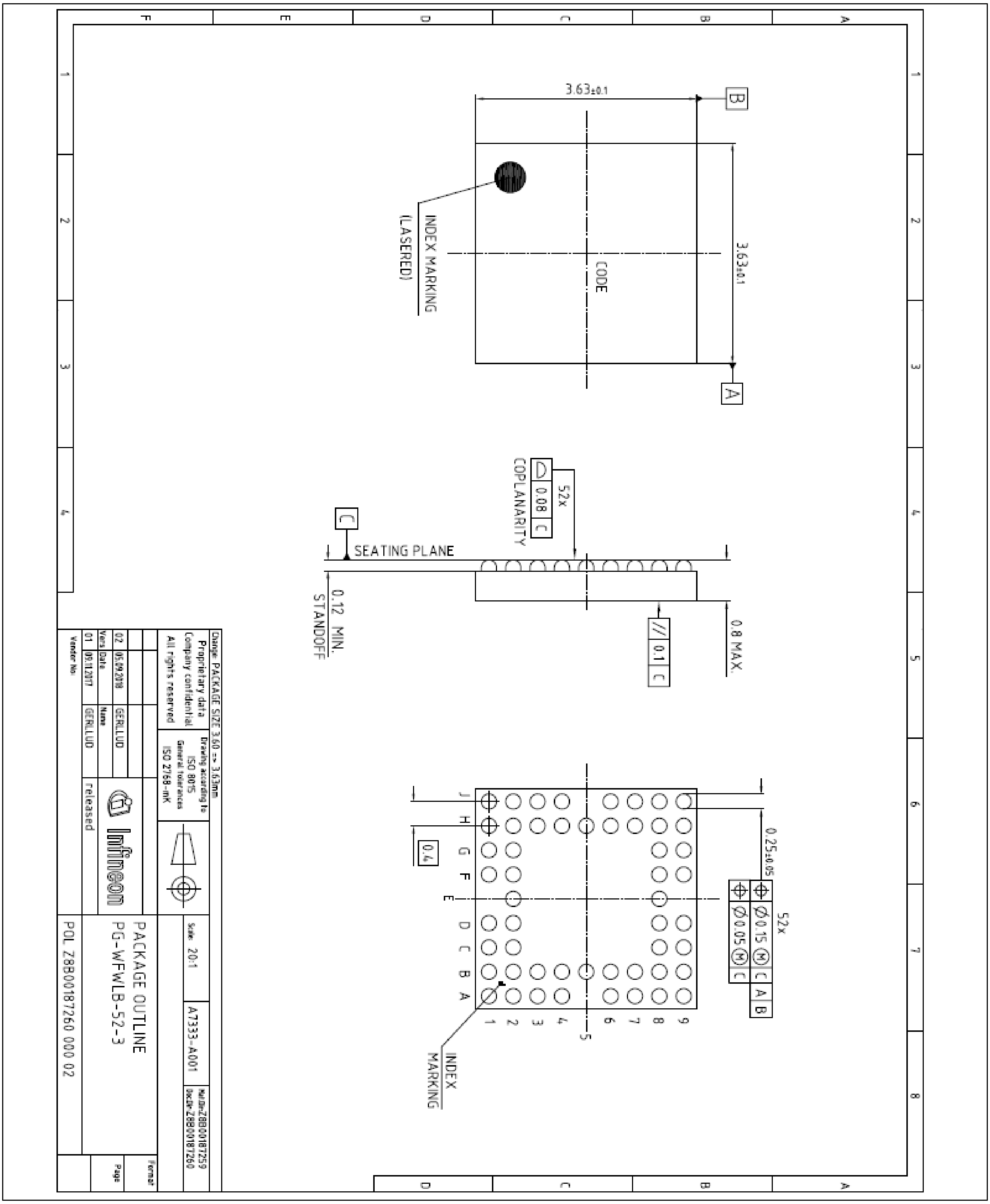


Figure 4 **Package outline. Top, side and bottom view of WFWLB-52-3**

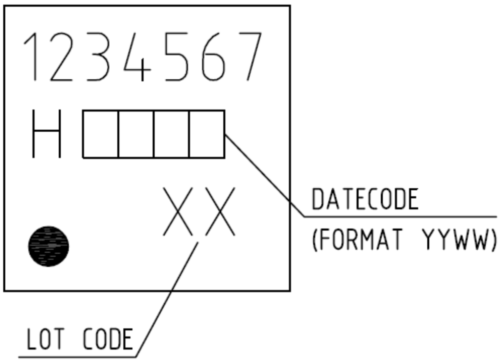


Figure 5 Marking layout of WFWLB-52-3

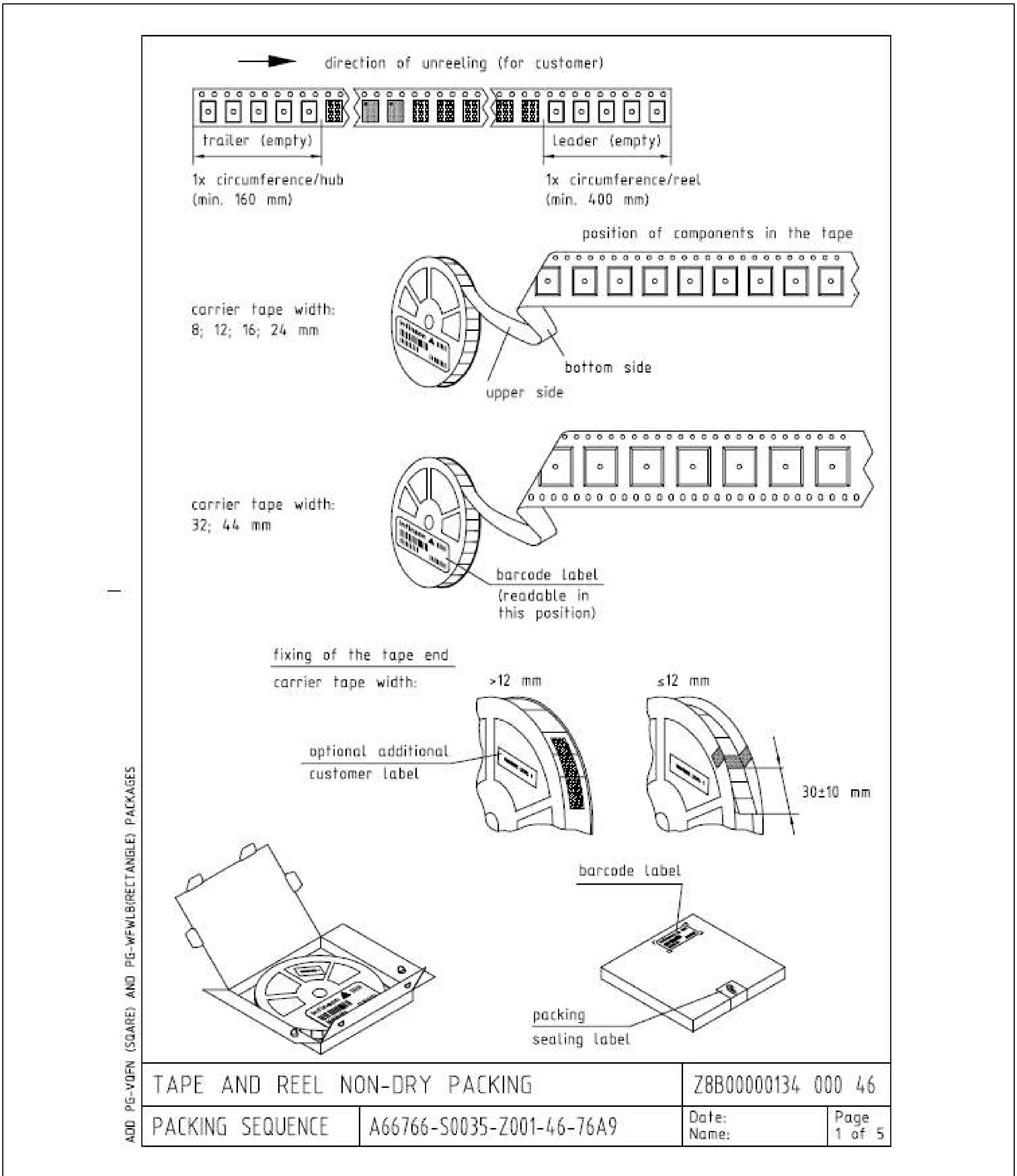


Figure 6 **Tape and reel of WFWLB-52-3**

Revision history

Document version	Date of release	Description of changes
V1.0	dd/mm/2020	First release

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