DEVELOPMENTAL HALT REPORT
R-00000274

Product Tested: 600W power supply

Service Proposal #: S-0000274

Job #: 3348-3976

Test Dates: 24/09/2007 to 26/09/2007

Report Date: 03/10/2007

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1.0 Objective

Poor reliability, low MTBF, frequent field returns, high in-warranty costs, and customer dissatisfaction are often the result of design and/or process weaknesses, even if a product has successfully passed qualification tests and burn-in.

The product was subjected to the HALT process to uncover design and/or process weaknesses. During the HALT process, the product was subjected to progressively higher stress levels brought on by thermal dwells, vibration, rapid temperature transitions and combined environments.

Throughout the HALT process, the intent was to subject the product to stimuli well beyond the expected field environments to determine the operating and destruct limits of the product. Failures, which typically show up in the field over a period of time at much lower stress levels, are quickly discovered while applying high stress conditions over a short period of time.

HALT is primarily a margin discovery process. In order to ruggedise the product, the root cause of each of failure needs to be determined and the problems corrected until the fundamental limit of the technology for the product can be reached. This process will yield the widest possible margin between product capabilities and the environment in which it will operate, thus increasing the product's reliability, reducing the number of field returns and realizing long-term savings.

The operating and destruct limits discovered during HALT on these units could be used to develop an effective Highly Accelerated Stress Screen (HASS) for manufacturing which will quickly detect any process flaws or new weak links without taking significant life out of the product. The HASS process will ensure that the reliability gains achieved through HALT will be maintained in future production.

2.0 Executive Summary

HALT was performed using one sample. During the HALT process, our goal was to find the operating and destruct limits for the units tested using thermal step stress, vibration step stress, and combined environment of temperature and multi-axis, 6 degree-of-freedom vibration. Once these limits were determined, our goal was to fix the weak links and stress even further to expand the limits as much as possible. The operating and destruct limits are summarized in Table 1. See Section 5.0 for a detailed discussion of failures. The HALT exposed specific weaknesses, which need to be addressed:

2.1 Cold step stress

The unit failed to restart after a power cycle at -80°C and recovered after returning to ambient temperature. Testing stopped at -80°C.

2.2 Hot step stress

The 5V output module 1 in slot D went into current limit after power cycling at +45°C due to known tolerance issue in the current limiting circuitry.
At +100°C the 5V output module 1 in slot D shut down due to the failure of an op-amp on the output control circuit.

2.3 Rapid thermal transitions

There were no issues found during the temperature cycling profile.

2.4 Vibration Step Stress

At the end of the dwell at 25G the 20V output module 3 in slot A shut down due to arcing in the connector. At 35G all outputs turned off when the power transformer core was damaged.

2.5 Combined Environment Stress

The unit began to fail intermittently during the hot temperature dwell on the 4th cycle at 14G and +70° due to arcing in the output module connectors. Another unit was inserted and on the next cycle the power transformer core was damaged.

Table 1 - Summary of PSU Operating and Destruct Limits

Stress Limit	***Chamber Setpoint Level***
Temp LOL	< -60ºC > -80°C
Temp LDL	<-80ºC
Temp UOL	+95ºC
Temp UDL	+95ºC
Thermal Transitions	-50ºC to +70ºC
Vibration OL	20G
Vibration DL	30G
Combined OL	< -50ºC to +70ºC and 20G
Combined DL	< -50ºC to +70ºC and 20G

Notes:

1. All temperature and vibration values are chamber setpoints. See Section 5 and the Appendix for product levels.
2. LOL / LDL = Lower Operating / Destruct Limit. UOL / UDL = Upper Operating / Destruct Limit. For vibration there is an upper limit only.
3. Operating Limit is defined as the point at which the product is still fully functional but when the applied stress is increased, the product is no longer functional.
4. Destruct Limit is defined as the point at which the product still returns to full operation when the applied stress is decreased to within the operating limit but when the applied stress is increased the unit fails to return to operation when the applied stress is returned to within the operating limit.
5. When the limit is preceded by a “>” or “<” sign it indicates that we stopped prior to a failure, either because of a limitation of the chamber, the test setup, or per customer request.
6. The limits shown are the worst case limits. In other words, the limits for the product that had the lowest limits of all units tested under that stress. These limits reflect the product limits before any modifications.

3.0 HALT Process

The test procedure followed is outlined in the ARTC Service Proposal noted on the front page of this report. Any deviations from this procedure are noted below:

- During each dwell the system was functionally tested.

4.0 HALT Setup

4.1 Fixturing and Airflow

The product was tested one unit at a time. The product under test was secured using two bars of aluminium U-channel and all-thread to clamp the metal chassis to the vibration table. Air from the chamber plenum was directed onto the units. The fixture was designed to maximize both transmission of energy from the vibration table to the product and thermal transition rates, as well as to help maintain consistent temperatures on all the components inside the test units. Pictures illustrating the fixturing and arrangement of test units in the test chamber are presented in Appendix A.

4.2 Description of Test Equipment

Table 2 - Anecto Test Equipment

Description	*Manufacturer*	*Model*	*S/N*	*Cal Due*
Thermal & Vibration Test Chamber	QualMark	OVS 2.5 HP	2604980254	23/11/07
Data logger	Hewlett Packard	34970A	U537037399	14/08/08
Data logger Thermocouples	Omega	TT-T-30	N/A	N/A
Chamber Thermocouples	Omega	C03-T-60	N/A	N/A
Spectrum Analyzer	Data Physics	Dp430	3869	N/A
Accelerometer	Dytran	3035B1G	3355	14/03/08
Accelerometer	Dytran	3035B1G	3514	11/09/08
Accelerometer	Dytran	3035B1G	3455	15/03/08

4.4 Data Collection

Thermocouples were attached to various points on the devices under test using kapton tape. These thermocouples remained in place throughout thermal step stress and rapid thermal transitions. The product thermal response at each thermocouple location was recorded at each level of thermal stress. See appendix B for thermal graphs.

Table 3 - Data logger Channel Assignment Temperature

Channel	*Location or Description*
101	Primary HS
102	Wiring Board
103	Output 3A
104	Output 2B
105	Output 2C
106	Output 1D

Table 4 - Data logger Channel Assignment Output Voltage

Channel	*Location or Description*
114	OP 2C
115	OP 1D
116	OP 2B
117	OP 3A

Table 5 - OVS Control System Thermocouple Placement

Channel	***Placement***
Product (control)	PSU chassis
Air	Above chassis
Honeywell	Wall of chamber

4.5 Test Routine

The device under test was connected to external equipment and was functionally tested throughout the HALT.

Correct operation of the PSU was verified by monitoring the current and voltage output, also an oscilloscope was used to monitor the output voltages for transients.

5.0 HALT Results

5.1 Thermal Step Stress

The test unit was subjected to cold thermal step stress beginning at +20°C, with the temperature decreasing in 10°C increments as far as -40°C and 20°C steps thereafter. Once the thermocouples located on the units stabilized, the unit dwelled at that setpoint for 10 minutes. Once cold thermal step stress was completed, the unit was returned to +20°C and remained there until the thermocouples located on the unit stabilized. Once the unit reached +20°C, it was tested to ensure they were still fully functional. Hot thermal step stress began at a setpoint temperature of +30°C with the temperature increasing in 10°C increments as far as +40°C and 5°C steps thereafter. Once the thermocouples located on the unit reached the setpoint temperature, the unit dwelled at that setpoint for 10 minutes. The results of thermal testing are summarized in Tables 6 and 7.

Table 6 – Cold Thermal Step Stress Results (°C)

Setpoint	*Functional Test Results*	*Notes*
+20	OK	1
+10	OK	1
0	OK	1
-10	OK	1
-20	OK	1
-30	OK	1
-40	OK	1
-50	Skipped	1
-60	OK	1
-70	Skipped	1
-80	See notes below	1,2
+20	OK	1

Notes:

1. The system was functionally tested during every dwell.
2. The unit failed to recover after power cycle at -80°C, the unit recovered fully when returned to ambient temperature.

Table 7 – Hot Thermal Step Stress Results (°C)

Setpoint	*Functional Test Results*	*Notes*
+30	OK	1
+40	OK	1
+45	See note below	1,2
+50	OK	1
+55	OK	1
+60	OK	1
+65	OK	1
+70	OK	1
+75	OK	1
+80	OK	1
+85	OK	1
+90	OK	1
+95	OK	1
+100	See Note below	1,3
+30	OK	1

Notes:

1. The system was functionally tested during every dwell.
2. The 5V output module 1 in slot D went into current limit after power cycling at +45°C due to known tolerance issue in the current limiting circuitry, the unit recovered fully after 2nd cycle no further power cycling performed to eliminate this issue.
3. At +100°C the 5V output module 1 in slot D shut down due to the failure of an op-amp on the output control circuit, the component had a temperature rating of +85°C and failed during the dwell at +100°C.

5.2 Rapid Thermal Transitions

The device under test was subjected to seven and a half temperature cycles from +70°C to –50°C at an average thermal transition rate of 60°C per minute. The average thermal transition rate is computed from the average transition of all the product temperature response thermocouples. The rate is computed through the centre region of the entire transition, which discounts 20% at each end of the transition. Air temperature limits were set to +100°C and –70°C to prevent excessive overshoot. The results of rapid thermal transitions testing is summarised in Table 8.

Table 8 - Rapid Thermal Transition Results (°C)

Cycle	*Setpoint*	*Functional Test Results*	*Notes*
1	+70	OK	1
1	-50	OK	1
2	+70	OK	1
2	-50	OK	1
3	+70	OK	1
3	-50	OK	1
4	+70	OK	1
4	-50	OK	1
5	+70	OK	1
5	-50	OK	1
6	+70	OK	1
6	-50	OK	1
7	+70	OK	1
7	-50	OK	1
8	+70	OK	1
8	+25	OK	1

Notes:

1. The system was functionally tested during every dwell. No issues were found.

5.3 Vibration Step Stress

The device under test was clamped firmly to the vibration table to maximise energy transmission and subjected to vibration step stress beginning at a setpoint of 5 Grms with the vibration increasing in 5 Grms increments at 15 minute intervals. The results are summarized in Tables 9a and 9b.

Table 9a - Vibration Step Stress Results

Setpoint	*Functional Test Results*	*Notes*
5	OK	1
10	OK	1
15	OK	1
20	OK	1
25	See note below	1,2
30	OK	1
35	See note below	1,3

Table 9b - Vibration Step Stress Results

Setpoint	*Functional Test Results*	*Notes*
20	See note below	1,4
25	See note below	1,4
30	See note below	1,4

Notes:

1. The system was functionally tested and during every dwell.
2. At the end of the dwell at 25G the 20V output module 3 in slot A shut down.
3. At 35G all outputs turned off and testing was stopped, two of these modules recovered when the vibration stopped but two remained inoperable. The problem was due to intermittent contact in the module connectors which caused excessive arcing and burned the connector.
4. Additional vibration testing and analysis with another unit showed that there was also an issue with the output modules contacting the power transformer core on the wiring board causing mechanical damage to the transformers. This occurred at vibration levels of 20G and above.

Table 8 - Vibration Levels Measured During Vibration Step Stress (Grms)

Chamber	*x-axis Channel 1*		*y-axis Channel 2*		*z-axis Channel 3*	
Setpoint	2Hz-3kHz	2Hz-10kHz	2Hz-3kHz	2Hz-10kHz	2Hz-3kHz	2Hz-10kHz
5	4.294	7.440	2.998	6.912	13.688	15.116
10	5.048	9.599	3.494	8.978	15.492	17.240
15	9.312	17.517	6.131	12.148	21.876	24.447
20	13.014	22.857	7.958	17.228	27.602	30.787
25	15.992	24.933	8.975	20.338	31.925	40.937
30	17.448	27.475	9.022	25.305	43.272	50.202
35	17.085	28.232	9.980	27.533	56.651	64.165

5.4 Combined Environment

The device under test was subjected combined environment testing incorporating a temperature profile of seven and a half cycles from +70°C to –50°C at an average thermal transition rate of 60°C per minute and the introduction of increasing levels of vibration starting at 8G and increasing in 2G steps at the end of each hot/cold cycle. The results are summarized in Table 10.

Table 10 - Combined Environment Results

Cycle	*Temp (°C)*	*Vibe (Grms)*	*Functional Test Results*	*Notes*
1	+70	8	OK	1
1	-50	8	OK	1
2	+70	10	OK	1
2	-50	10	OK	1
3	+70	12	OK	1
3	-50	12	OK	1
4	+70	14	see note below	1,2
4	-50	14	OK	1,2
5	+70	16	see note below	1,3
5	-50	16	not completed	na
6	+70	18	not completed	na
6	-50	18	not completed	na
7	+70	20	not completed	na
7	-50	20	not completed	na
8	+20	22	not completed	na

Notes:

1. The system was functionally tested during every dwell.
2. The unit began to fail intermittently during the hot temperature dwell on the 4th cycle at 14G and +70°C the testing was paused to try and alleviate the problem by securing the wiring board more effectively to the chassis with glue to prevent any further arcing in the connectors.
3. Testing continued with another unit, this unit also failed after completing one more cycle and when it was analysed it was found that the power transformer core was damaged by contact with the output module above it. Testing stopped during the 5th cycle.

6.0 Synopsis

Each of the failures found during the HALT process (see section 2.0) needs to be examined and the root cause of the failure determined. Once the root cause of each failure is determined, engineering judgment is used to determine whether corrective action should be taken to fix the problem. The product should then undergo a verification HALT to ensure that the design margins have been increased to the fundamental limit of technology and that the fixes made did not induce new failure modes. The ruggedisation of the product will not be increased unless each of the failures found during the HALT process are taken to root cause and corrective action implemented.

Appendix A – Photographs

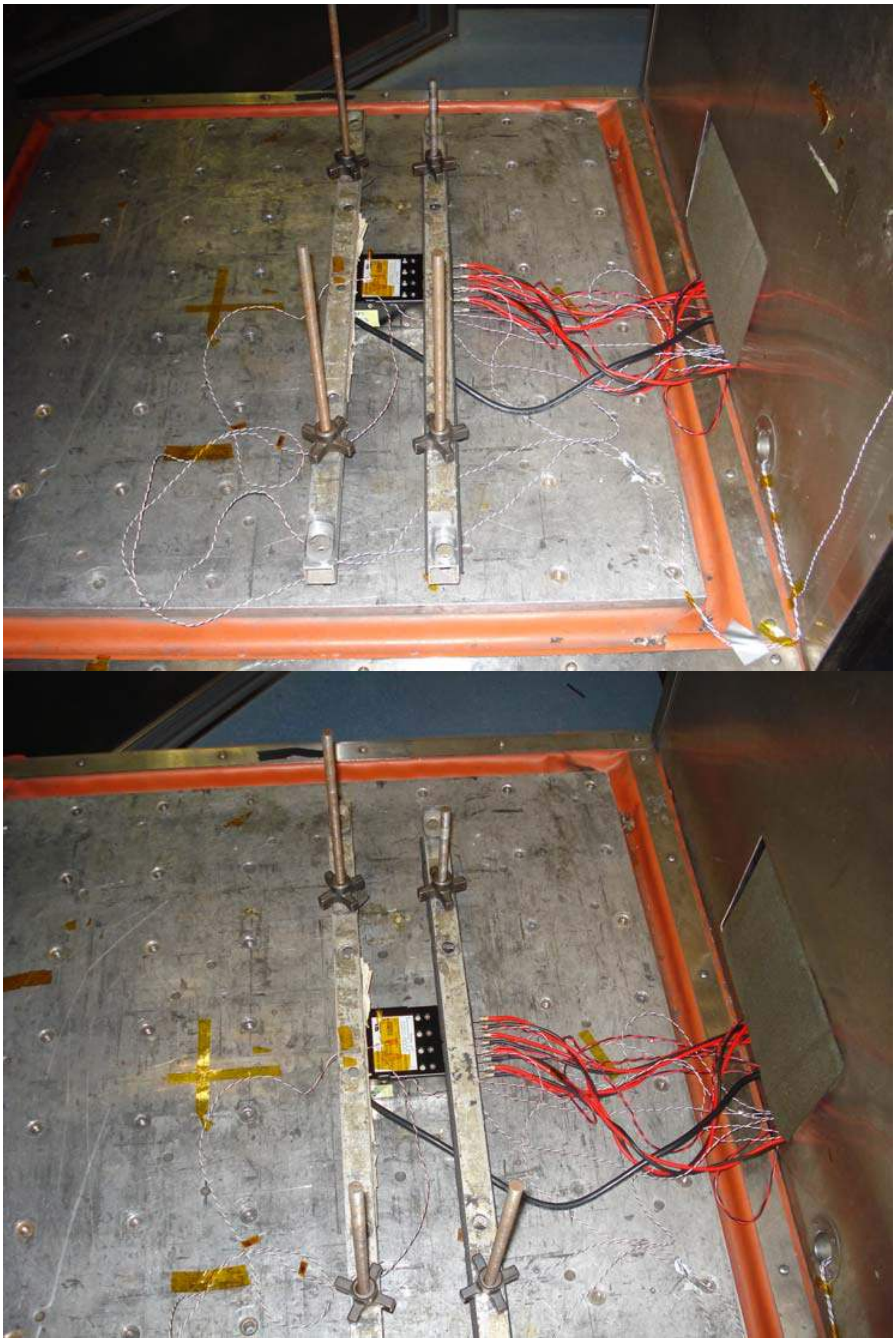
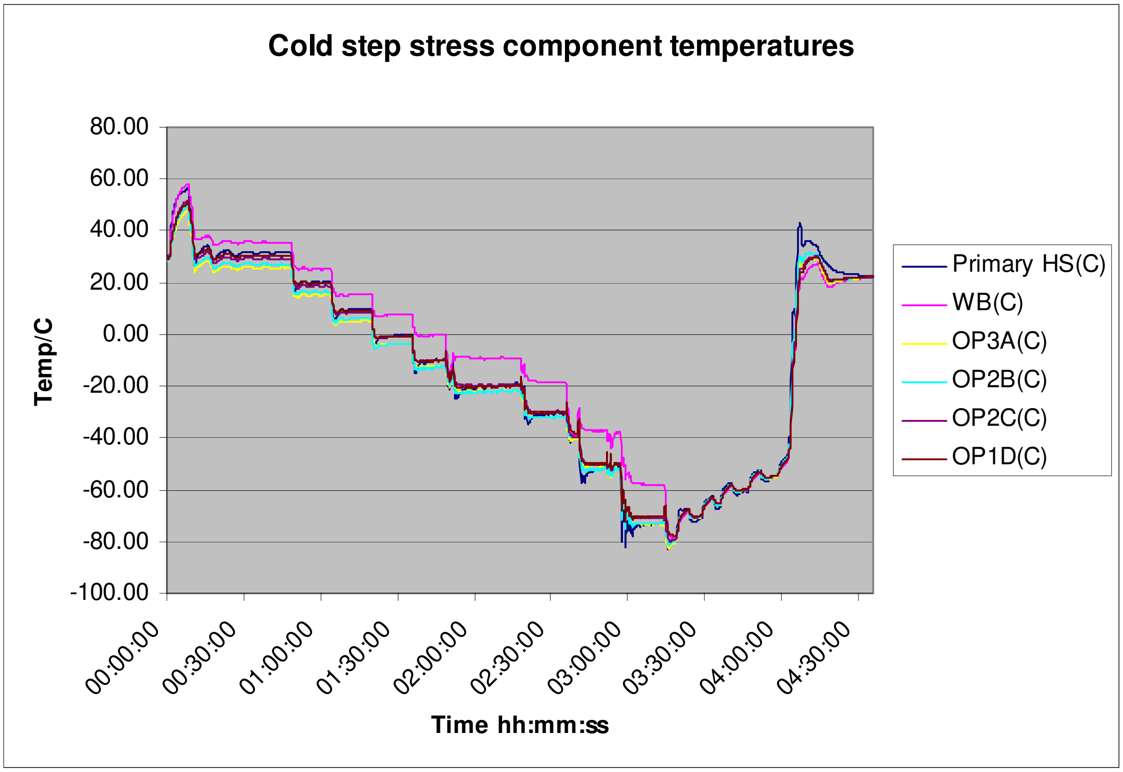
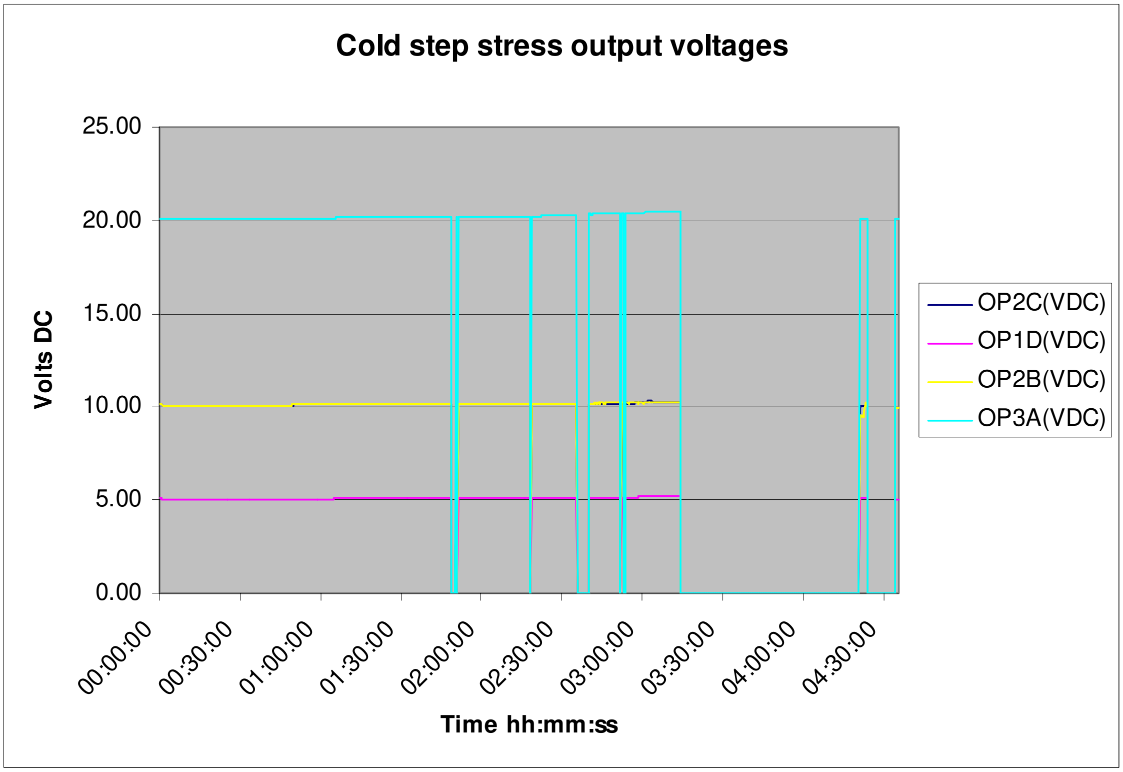
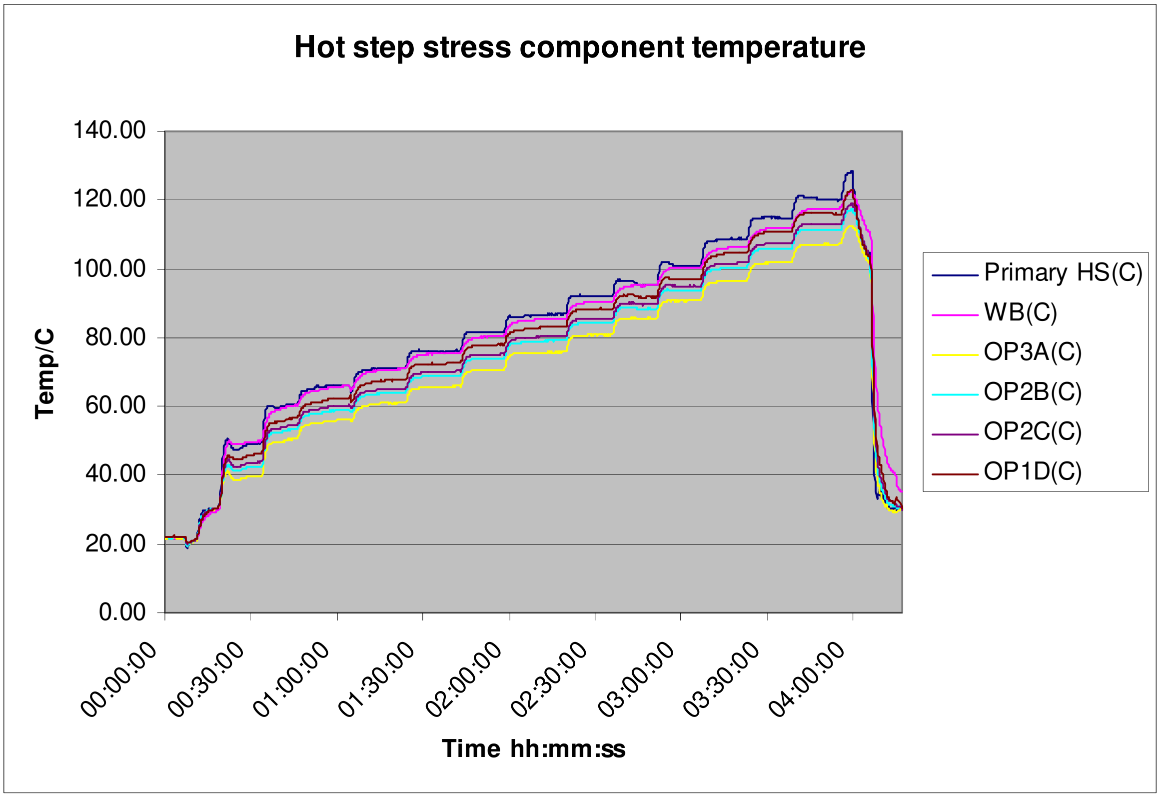


Figure 1 – Thermal and vibration Set-up

Appendix B – Thermal and Vibration Graphs



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100.00
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20.00
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Temp/C
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00:30:00
01:00:00
01:30:00
02:00:00
02:30:00
03:00:00
03:30:00
04:00:00
Time hh:mm:ss
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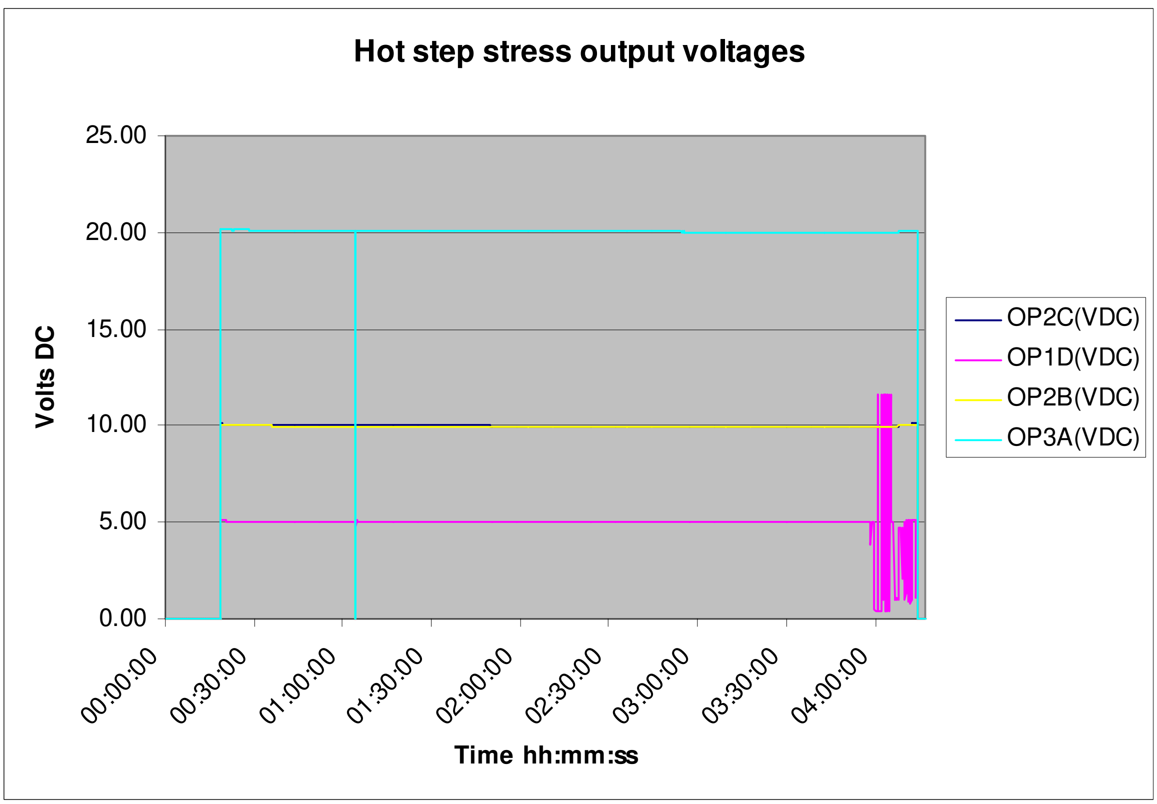
WB(C)
OP3A(C)
OP2B(C)
OP2C(C)
OP1D(C)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10.00
5.00
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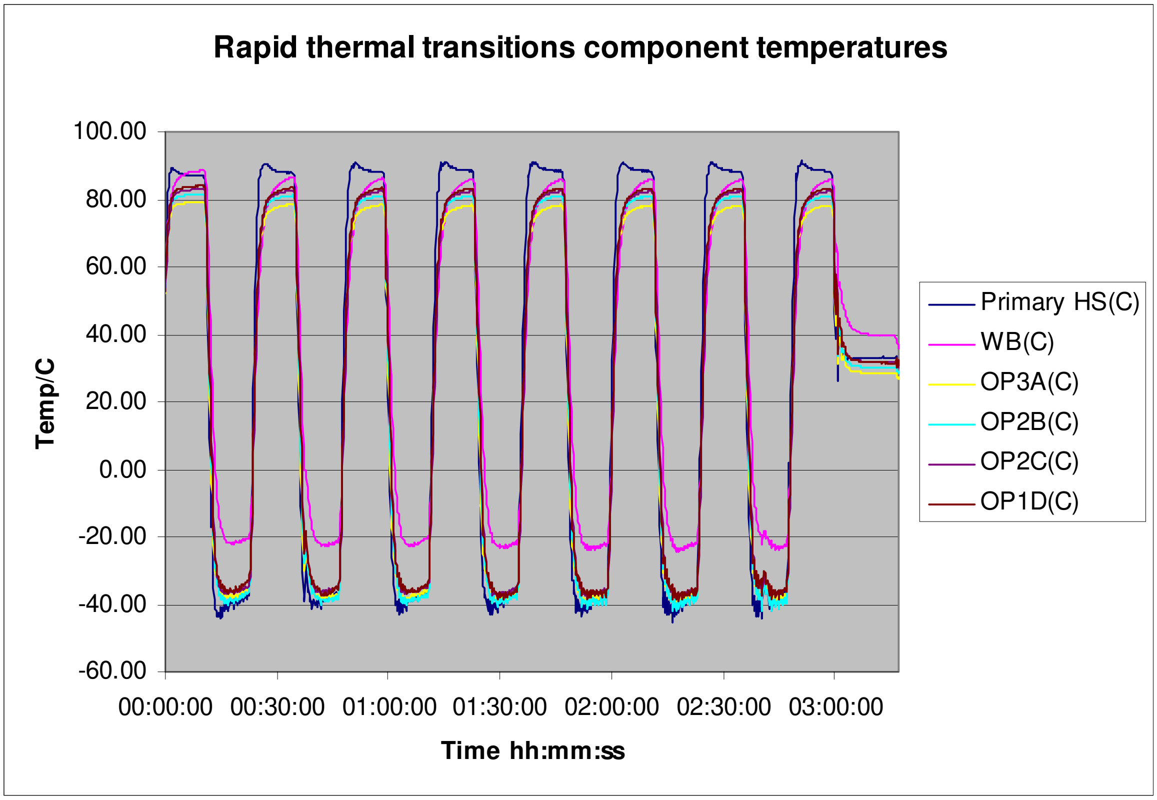
01:00:00
01:30:00
02:00:00
02:30:00
03:00:00
03:30:00
04:00:00
Time hh:mm:ss
OP2C(VDC)
OP1D(VDC)
OP2B(VDC)
OP3A(VDC)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00:30:00
01:00:00
01:30:00
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02:30:00
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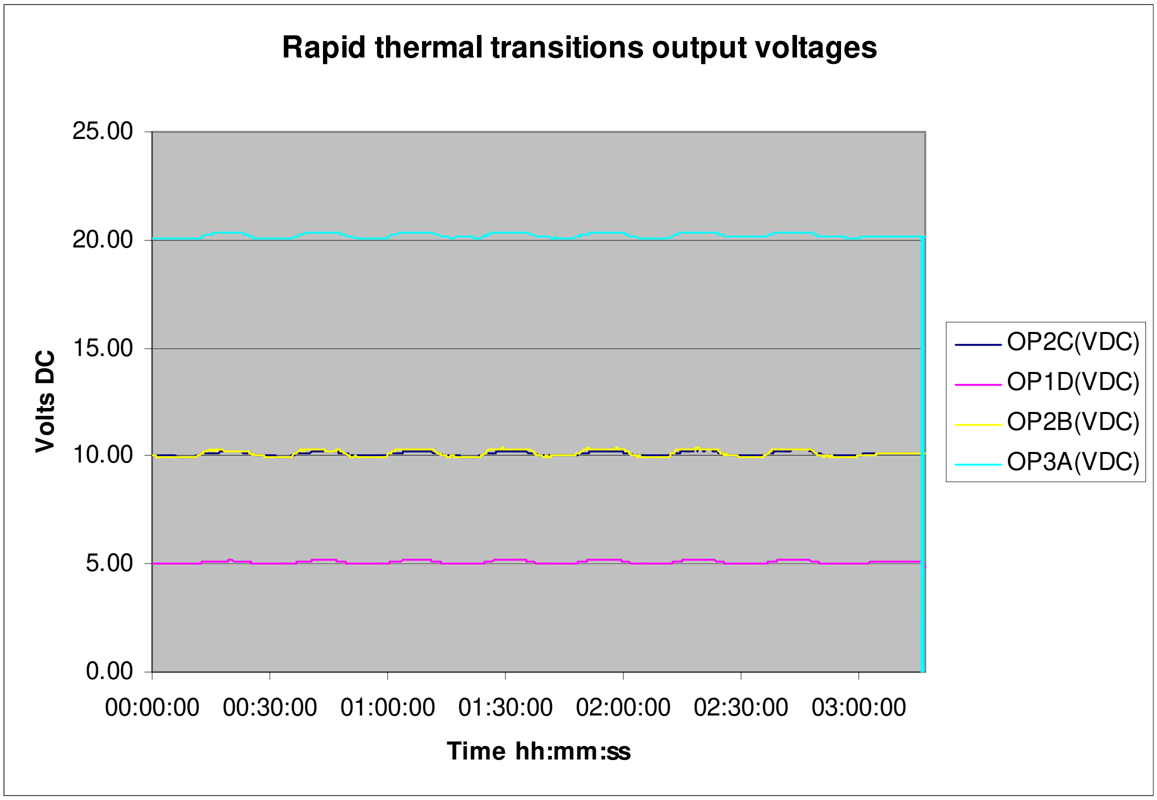
OP3A(C)
OP2B(C)
OP2C(C)
OP1D(C)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01:30:00
02:00:00
02:30:00
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Time hh:mm:ss
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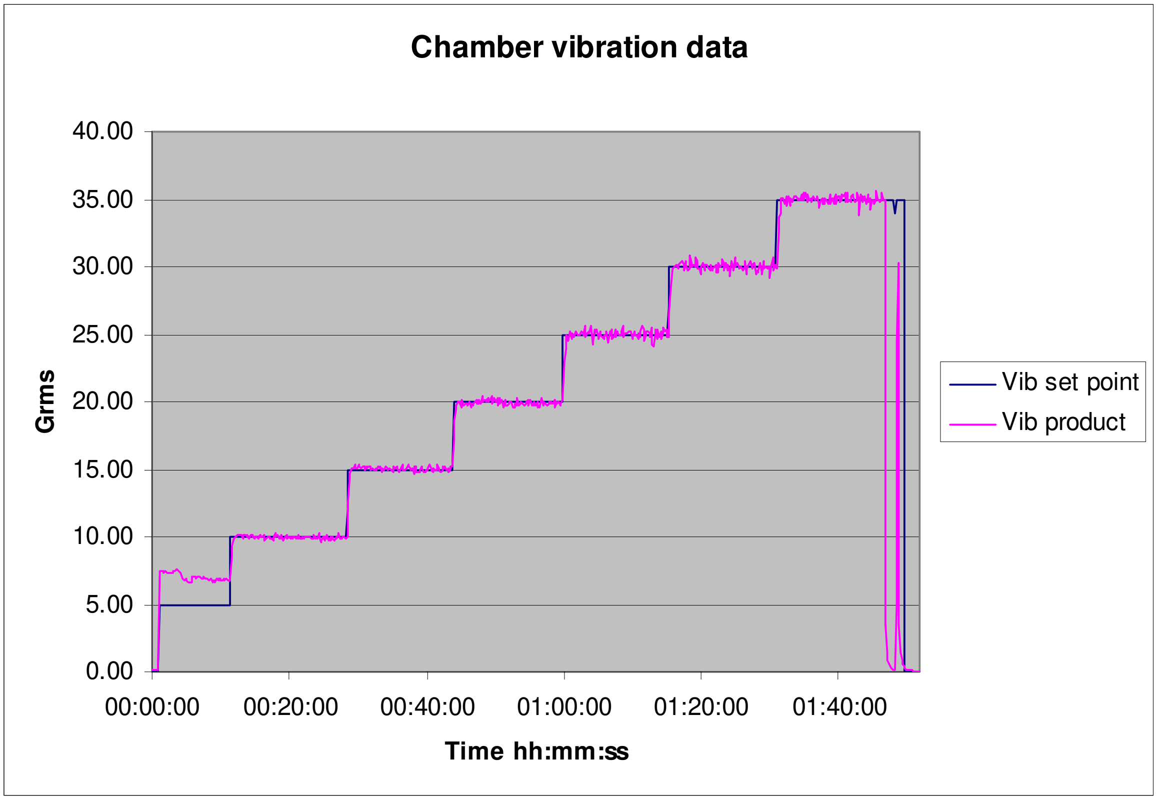
OP1D(VDC)
OP2B(VDC)
OP3A(VDC)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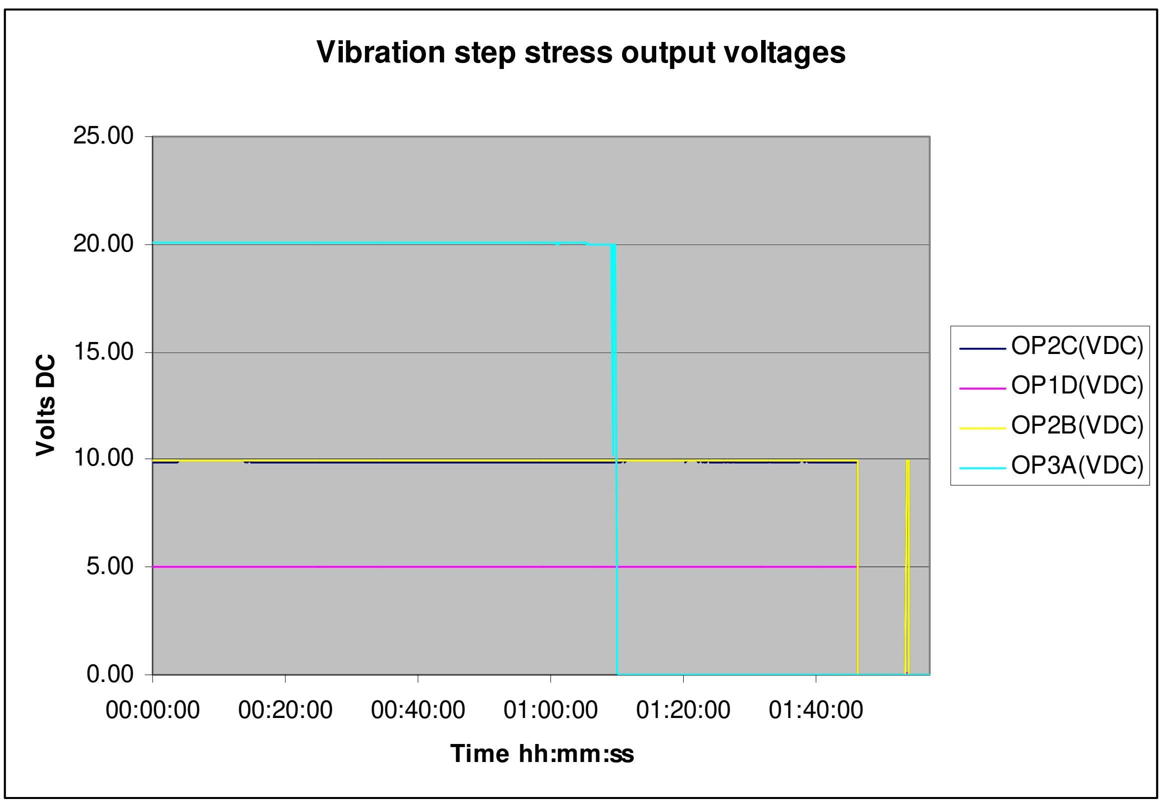
01:40:00
Time hh:mm:ss
Vib set point
Vib product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0.00
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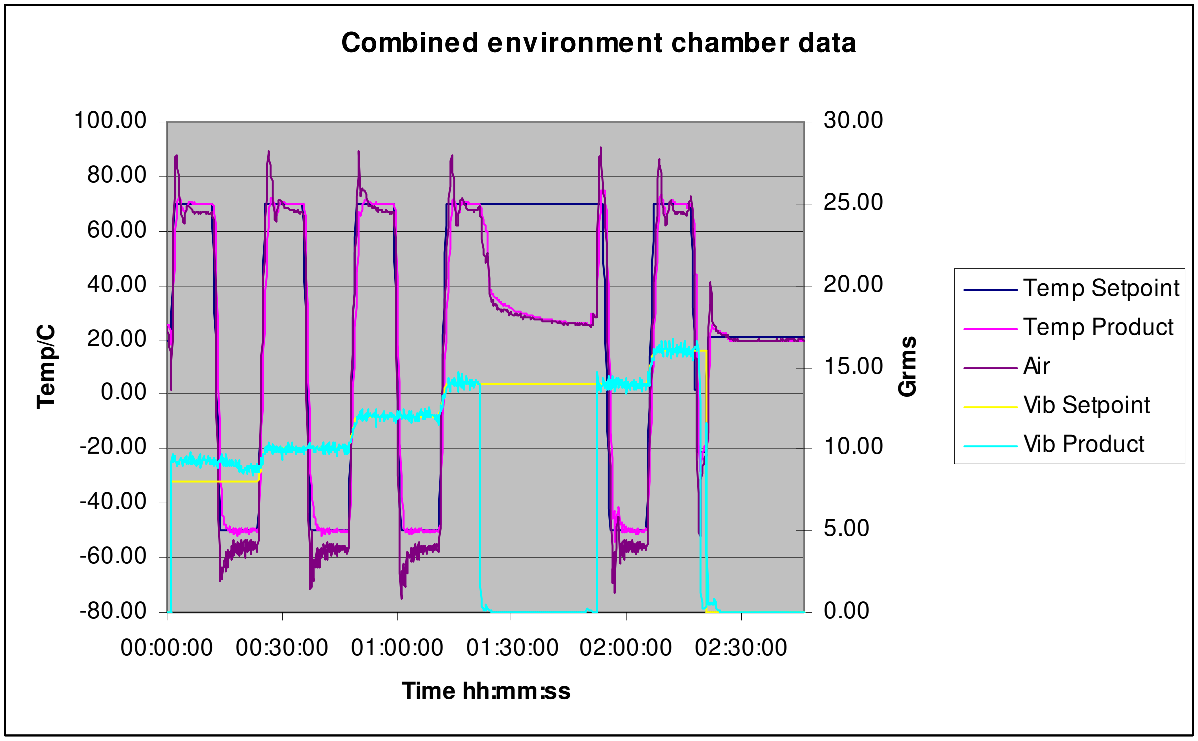
00:40:00
01:00:00
01:20:00
01:40:00
Time hh:mm:ss
OP2C(VDC)
OP1D(VDC)
OP2B(VDC)
OP3A(VDC)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20.00
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10.00
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00:00:00
00:30:00
01:00:00
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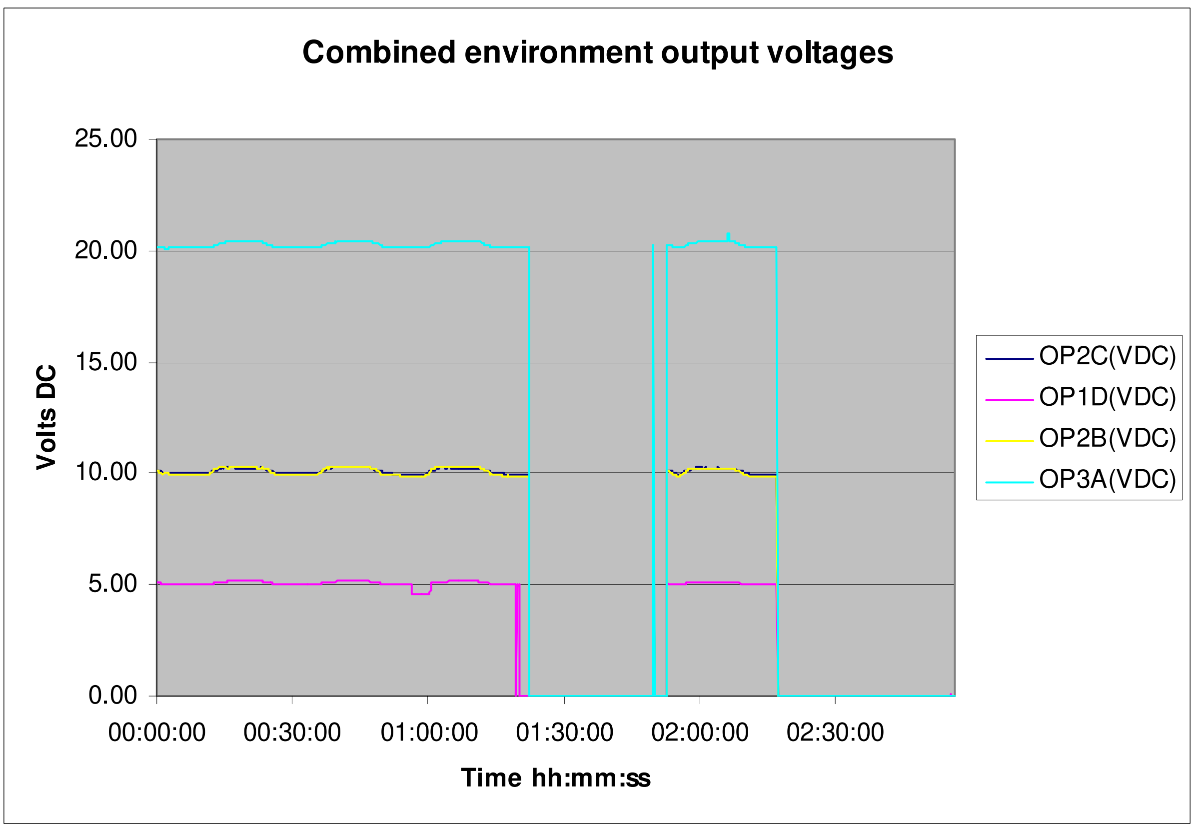
02:00:00
02:30:00
Time hh:mm:ss
Temp Setpoint
Temp Product
Air
Vib Setpoint
Vib Product


Combined environment output voltages
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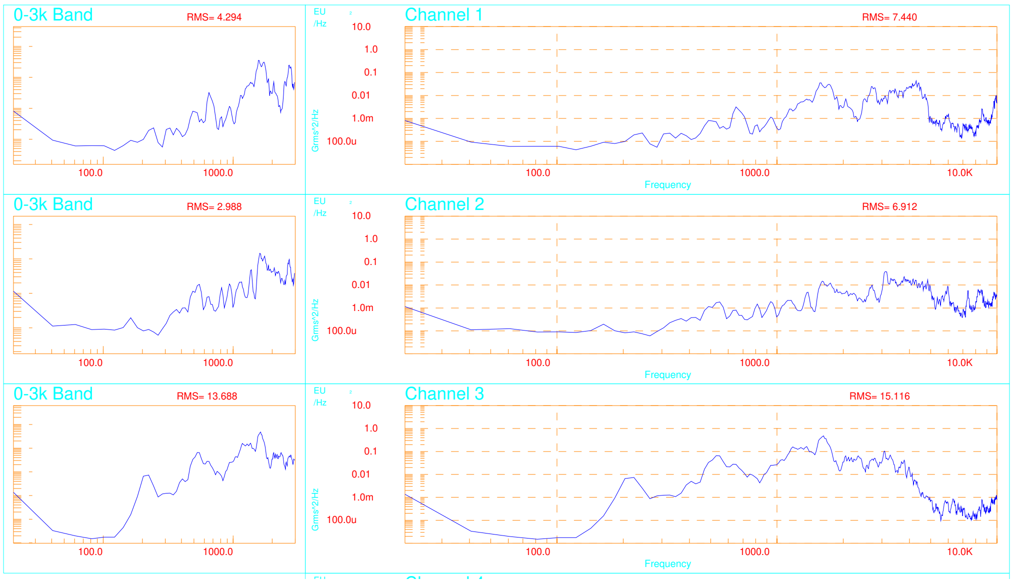
15.00
10.00
5.00
0.00
Volts DC
00:00:00
00:30:00
01:00:00
01:30:00
02:00:00
02:30:00
Time hh:mm:ss
OP2C(VDC)
OP1D(VDC)
OP2B(VDC)
OP3A(VDC)

Appendix C – Vibration Plots

5 Grms



35 Grms