



# EV1412-0600-A EVALUATION BOARD USER GUIDE



## Introduction

This user guide describes the evaluation board provided for the FS1412 µPOL™ product.

The board generates an output voltage (V<sub>OUT</sub>) of 1V for loads of 0–12A from an input voltage (PV<sub>IN</sub>) of 12V.

## **Specifications**

- Input voltage (PV<sub>IN</sub>) = +12V
- Output voltage (V<sub>OUT</sub>) = +1V
- Output load (I<sub>O</sub>) = 0–12A
- Switching frequency (F<sub>SW</sub>) = 1.0MHz
- Output capacitance (C<sub>O</sub>) = 4x47μF (MLCC)
- Input capacitance (C<sub>IN</sub>) = 3x22μF (MLCC)
- Dimensions (width x length x thickness) = 61mm x 89mm x 1.6mm

## **Connections**

Name	Identifier	Description	
PV <sub>IN</sub>	J1	Input voltage (+12V)	
PGnd	J4	Ground for input voltage	
Vout	J3	Output voltage (+1V)	
PGnd	J2	Ground for output voltage	
Vin	V <sub>IN</sub>	LDO input voltage	
Vcc	Vcc	Internal supply (Vcc) – output of an LDO regulator	
PGnd	PGnd	Power ground	
En	TP11	Enable	
PGood	PGood	Power Good	
SCL	J5	I2C/PMBUS clock line	
SDA	J5	I2C/PMBUS data line	
SALERT	SALERT	SMBALERT#	
SYNC	J6	External sync signal	
Load	J7	Used to connect load: 20-pin Intel Mini Slammer connector	
Output voltage selector	18	Used to select output voltage before power up	
Output transient ripple voltage	J9	Used for measurement: 50Ω ultra-miniature coaxial connector	

The board is configured for a single input supply. An internal low drop-out regulator generates the internal supply  $(V_{CC})$  from  $V_{IN}$ . The Enable (En) input is connected to  $PV_{IN}$  through a resistor divider, so that no external Enable signal is needed.

# Operation

To use the evaluation board:

- 1. Connect a well-regulated +12V input supply to  $PV_{IN}$  (J1) and Gnd (J4).
- 2. Connect a load of 0-12A to V<sub>OUT</sub> (J3) and Gnd (J2).



## **Description**

The evaluation board consists of a 4-layer PCB made from FR4 glass-reinforced epoxy laminate material. All layers use 2oz copper (equating to a thickness of 0.0694mm). The major power components, including the FS1412, are mounted on the top side of the board.

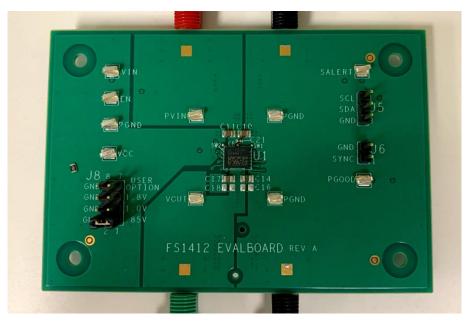


Figure 1 View of board (top)

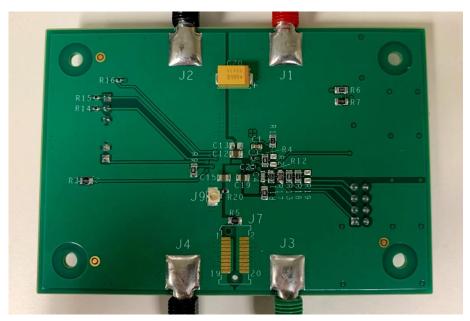


Figure 2 View of board (bottom)



Figure 3 to Figure 6 show the layout of the board layers and Figure 7 shows a schematic of the electrical circuit.

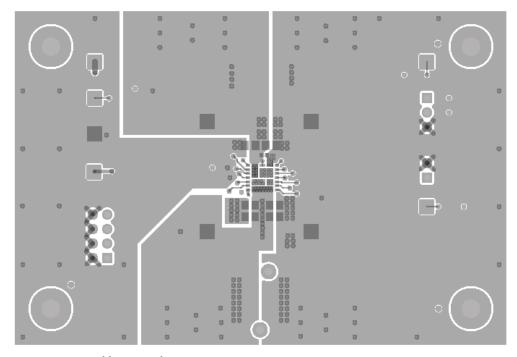


Figure 3 Board layout - layer 1

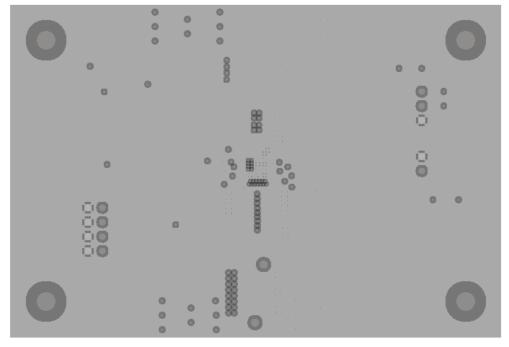


Figure 4 Board layout - layer 2



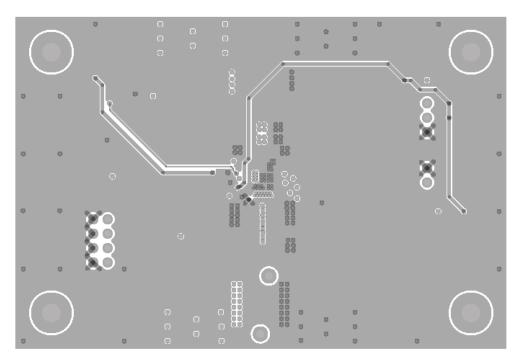


Figure 5 Board layout - layer 3

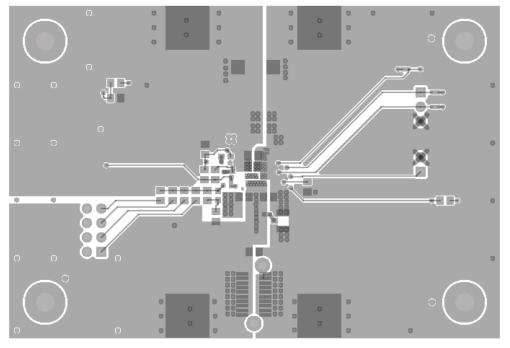


Figure 6 Board layout - layer 4



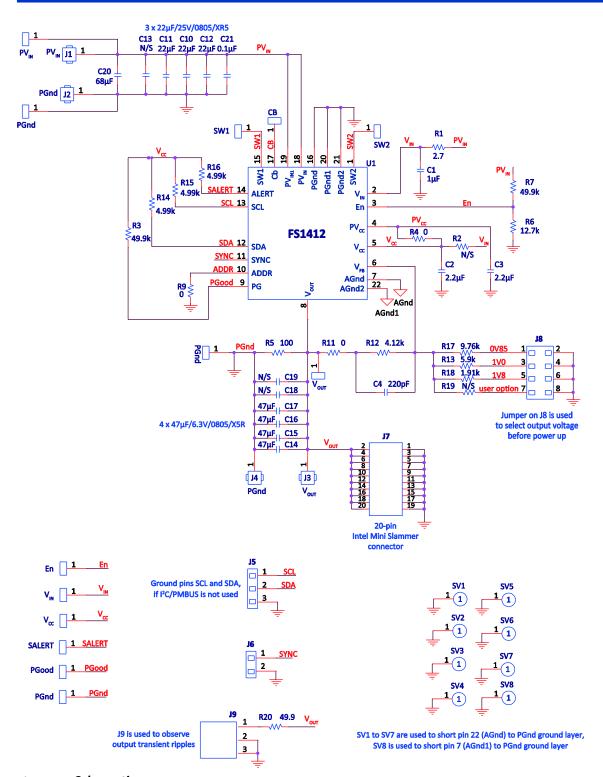


Figure 7 Schematic

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Part reference	Quantity	Value	Description	Manufacturer	Part number
C1	1	1μF	0603, 25V, X5R		
C10,C11,C12	3	22μF	0805, 25V, X5R		
C14,C15,C17,C19	4	47μF	0805, 6.3V, X5R		
C2,C3	2	2.2μF	0402, 10V, X7S		
C20	1	68μF	25V, tantalum		
C21	1	0.1μF	0402, 25V, X7R		
C4	1	220pF	0603, COG, 50V		
J1	1	108-0902-001	PV <sub>IN</sub> banana connector, red	Johnson (Cinch Connectivity Solutions)	108-0902-001
J2,J4	2	108-0903-001	Gnd banana connector, black		108-0903-001
J3	1	108-0904-001	V <sub>OUT</sub> banana connector, green		108-0904-001
J5	1	68000-103HLF	3 pin header, 0.1" pitch	Amphenol	68000-103HLF
J6	1	68000-102HLF	2 pin header, 0.1" pitch		68000-102HLF
J7	1	Not inserted	Mini Slammer connector, 20-pin	Intel	Q6UJ9A00MS25
18	1	M20-9760442	Through-board connector, 8-pin, two-row, 0.1" pitch	Harwin	M20-9760442
19	1	U.FL-R-SMT(10)	50Ω ultra-miniature coaxial connector	Hirose Electric	U.FL-R-SMT(10)
R1	1	2.7Ω	0805		
R12	1	4.12kΩ	0805, 1%		
R13	1	5.90kΩ	0805, 1%		
R14,R15,R16	3	4.99kΩ	0402		
R17	1	10kΩ	0805, 1%		
R18	1	1.91kΩ	0805, 1%		
R20	1	49.9Ω	0402, 1%		
R3,R7	2	49.9kΩ	0805		
R4,R9,R11	3	0	0805		
R5	1	100Ω	0805		
R6	1	12.7kΩ	0805		
U1	1	FS1412	Main IC	TDK	
VIN, EN, PGND, VCC, PVIN, PGND, VOUT, PGND, SALERT, PGOOD	10	5018	Test points	Keystone	5018



# **Typical performance**

Figure 8 to Figure 18 show typical operating waveforms for the evaluation board, while Figure 19 shows a thermal image of the board in operation. In all cases, the board is operating at room temperature with no airflow;  $PV_{IN}$  is 12V,  $V_{OUT}$  is 1V and  $I_O$  is 0–12A.

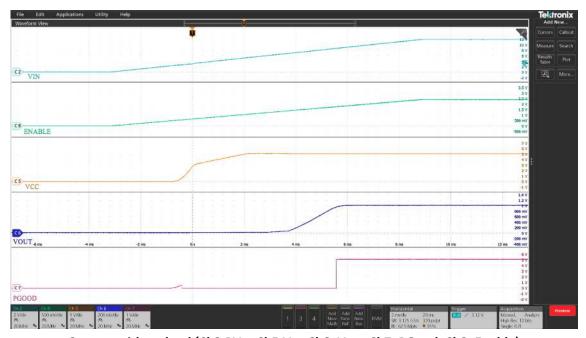


Figure 8 Startup with no load (Ch2:PV<sub>IN</sub>, Ch5:V<sub>CC</sub>, Ch6: V<sub>OUT</sub>, Ch7: PGood, Ch8: Enable)

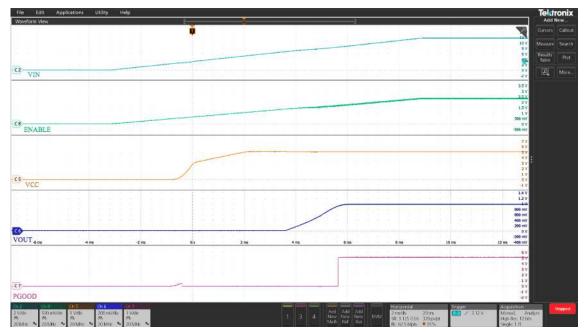


Figure 9 Startup with 12A load (Ch2:PV<sub>IN</sub>, Ch5:V<sub>CC</sub>, Ch6: V<sub>OUT</sub>, Ch7: PGood, Ch8: Enable)



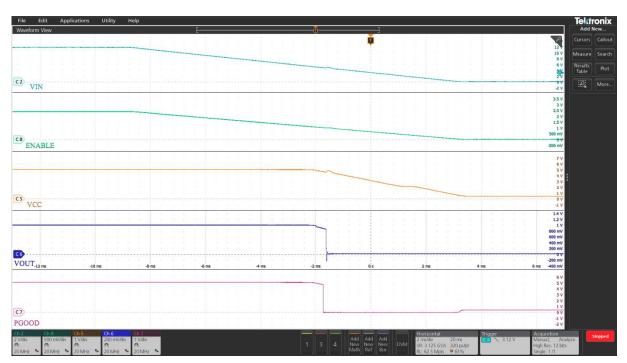


Figure 10 Shutdown with Enable de-assertion at 12A load (Ch2:PV<sub>IN</sub>, Ch5:V<sub>CC</sub>, Ch6: V<sub>OUT</sub>, Ch7: PGood, Ch8: Enable)

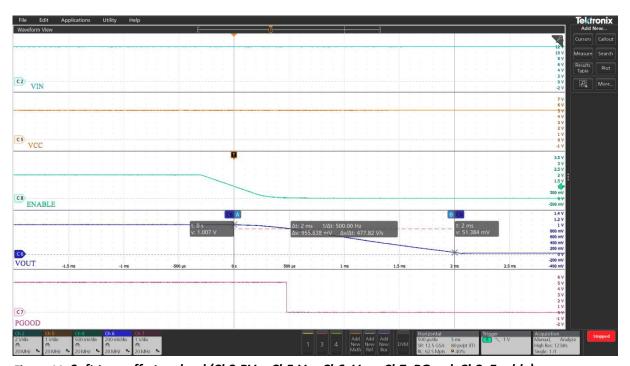


Figure 11 Soft turn off at no load (Ch2:PV<sub>IN</sub>, Ch5:V<sub>CC</sub>, Ch6: V<sub>OUT</sub>, Ch7: PGood, Ch8: Enable)



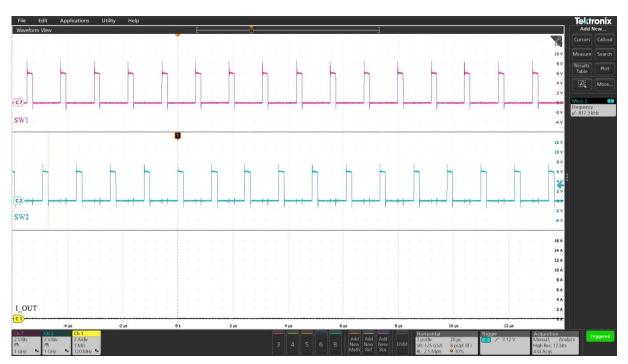


Figure 12 Switch node waveforms at no load

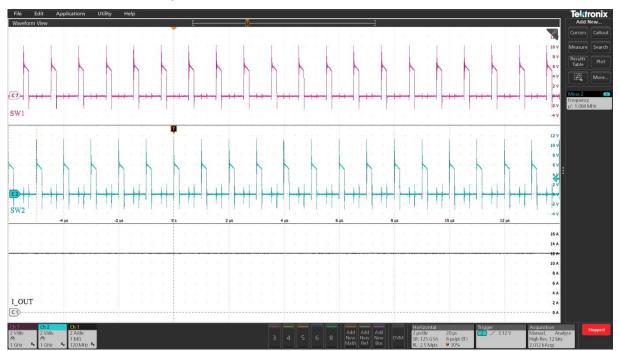


Figure 13 Switch node waveforms at 12A



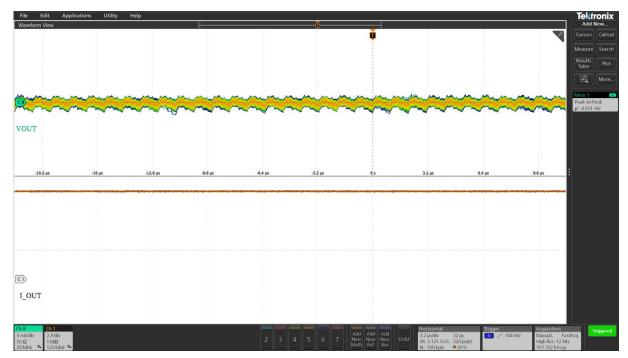


Figure 14  $V_0$  ripple at 12A (Ch1: $I_0$ , Ch8:  $V_{0UT}$ ), peak-peak  $V_0$  ripple = 4.6mV

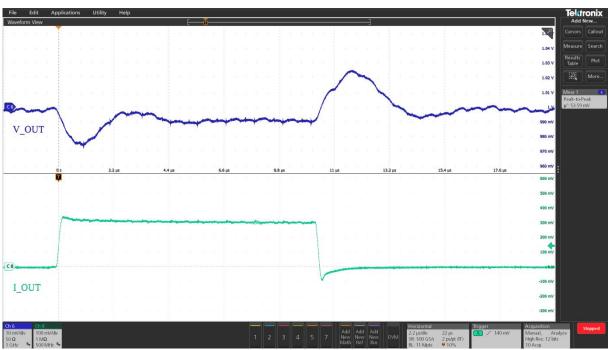


Figure 15 Transient response 0A to 6A (Ch6:  $V_{OUT}$ , Ch8: $I_O$ ), peak-peak deviation = 53mV, load slew rate = 40A/ $\mu$ s



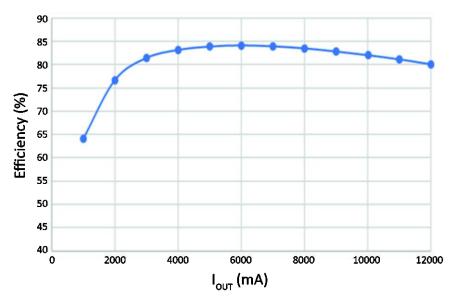


Figure 16 Efficiency

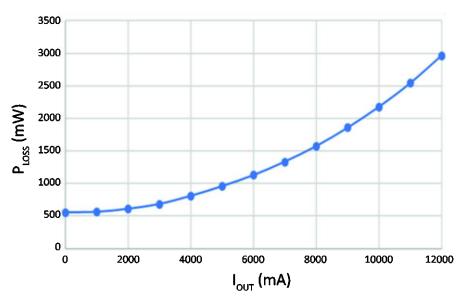


Figure 17 Power loss



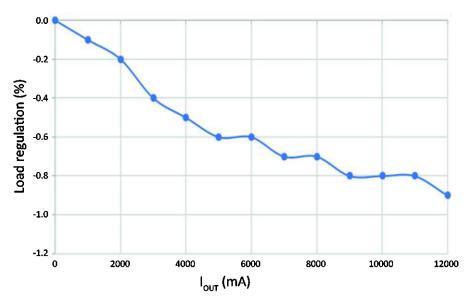


Figure 18 Load regulation ( $I_{0} = 0-12A$ )



Figure 19 Thermal image at  $PV_{IN} = 12V$ ,  $V_{OUT} = 1.0V$ ,  $I_O = 12A$ , room temperature, no airflow, FS1412 maximum temperature rise = 55.5°C



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- EP 1561156A1 1561268A2 1576710A1 1576711A1 1604254A4 1604264A4 1714369A2 1745536A4 1769382A4 1899789A2 1984801A2
- US 20040246754 2004090219A1 2004093533A1 2004123164A1 2004123167A1 2004178780A1 2004179382A1 200502203344 20050223252 2005209373A1 20060061214 2006015619A1 20060174145 20070226526 20070234095 20070240000 20080052551 20080072080 20080186006 6741099 6788036 6936999 6949916 7000125 7049798 7069021 7080265 7249267 7266709 7315156 7372682 7373527 7394445 7456617 7459892 7493504 7526660
- WO 04044718A1 04045042A3 04045042C1 04062061A1 04062062A1 04070780A3 04084390A3 04084391A3 05079227A3 05081771A3 06019569A3 2007001584A3 2007094935A3