HPA-MCU Interface Board

The HPA-MCU Interface Board was designed to provide a complete system development platform using evaluation modules from the Data Acquisition Products Group. This board passes control and data signals from a variety of Micro Controller and Digital Signal Processors (DSP) to and from A-to-D and D-to-A converter evaluation modules (EVM's) from Texas Instruments. DSP boards compatible with this interface card include the TMS320F2407, TMS320F2808 and the TMS320F2812 eZdsp™ platforms from Spectrum Digital (www.SpectrumDigital.com). Micro Controller boards compatible with this interface card include the TMS470R1A1024. When combined with sensor or amplifier boards, the HPA-MCU Interface Board can provide a complete data acquisition system for a variety of applications.

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1 Introduction

The HPA-MCU Interface Board is intended to provide Data Converter customers with the greatest amount of flexibility for the evaluation of Data Acquisition Products from Texas Instruments. The HPA-MCU Interface Board follows the guidelines set forth in the *Designing Modular EVM's for Data Acquisition Products* (SLAA185) document and provides access to the SCI, SPI, CAN and I2C ports found on the 2000 series DSP as well as the MSP430 and TMS470 micro controllers. The Multi Channel Buffered Serial Port (McBSP) of the TMS320F2812 is also supported, as is the parallel data bus found on both the TMS320F2407 and TMS320F2812.

eZdsp is a trademark of Spectrum Digital.

The interface board consists of two signal conditioning sites, two serial EVM sites and a parallel EVM site. Regardless of the interface type, all EVM's compatible with the HPA-MCU Interface Board have a standard analog interface and standard power connector. Three position screw terminals J1 and J4 and two position screw terminals J7, J8, J9, and J10 provide access to a common power bus routed to all sites.

1.1 DSP and Micro Controller Board Options

The HPA-MCU board is supplied with male pin headers in connector locations J15, J16 and J17. These male pin headers are intended to plug into female mating connectors installed on the bottom side of the user supplied micro controller or DSP board. J15 serves the parallel address and data bus found on the TMS320F2407 and TMS320F2812 DSP. J16 serves the McBSP port found on the TMS320F2812. J17 serves General Purpose Input/Output (GPIO), SCI, SPI, CAN and I2C ports. Recomended mating connectors to J15, J16 and J17 are Samtec part numbers SSW-130-21-G-D, SSW-120-21-G-S and SSW-120-21-G-D respectivly. Information regarding the mating connectors can be obtained from the Samtec website at www.Samtec.com.

The TMS320F2407, TMS320F2808 and TMS320F2812 eZdsp™ Development Systems from Spectrum Digital (sold as stand alone products) do not ship with the appropriate mating connectors installed. Spectrum Digital's warranty expressly states that any user modification made to their Devleopment Systems are done so at the customers risk. Customer installed mating connectors may void the eZdsp™ product warranty. Bundled Development Systems which include appropriate mating connectors as well as the HPA-MCU Interface Board may be available for purchase through Spectrum Digital. Please contact Spectrum Digital for additional information.

1.2 Communication Options

The HPA-MCU board provides three 9-Pin sub D connectors for CAN and RS232 communication options. J18 and J19 are DB9 Female and DB9 Male (respectivly) connectors. These two connectors are associated with the SCI ports found on the TMS320 and TMS470 processors platforms. DPDT switch SW2 is provided as a means to implement a "Null-Modem" connection between the serial ports in order to achieve loop back testing. When SW2 is in the "normal" position, the TX and RX lines associated with SCI port 1 are connected to J18 pins 2 and 3 (respectively). When SW2 is switched to the "null modem" position, the TX and RX connections of SCI port 1 are swapped. TX is connected to J18 pin 3 and RX is connected to J18 pin 2. The combination of male and female DB9 connectors, as well as U7 - a dual port MAX3232, allow the use of readily available standard 9-Pin serial cables to be used to test serial communication between J18 and J19 and ports 1/2 of the installed processor.

J20 is associated with U10 - an SN65HV235 3.3V CAN transciever. Loop back communication options between two CAN ports may be available depending on the installed micro controller or DSP board. The SN65HV235 can also provide an internal loopback function by closing jumper W2 (default condition).

1.3 Power Connections to the Interface Card

The screw terminals along the bottom edge of the HPA-MCU Interface Board give access to the common power bus. Three port terminals J1 and J4 provide analog power. Two port terminals J7, J8, J9, and J10 provide the digital voltages. Two resistor locations, R7 and R8, located on the interface board give the user the option of powering the installed Micro Controller or DSP board through the Interface Board common power bus.

CAUTION

Installing R7 will provide +3.3VDC to the MCU board connectors J15(pins 1 and 2), J16(pin 1) and J17(pins 1 and 2). Installing R8 will provide +5VDC to connectors J15(pins 1 and 2), J16(pin 1) and J17(pins 1 and 2) as well. Under no circumstance should both R7 and R8 be populated at the same time as this may cause serious damage to analog EVM's as well as microcontroller boards. By default, R7 and R8 are not factory installed. Current limiting resistors or surface mount fuses may be used in these locations if desired.

Analog and digital power to compatible data converter EVM's must always be supplied from a clean, well regulated external source via J1, J4, and J7–J10. For best analog performance, linear power supplies are recommended. Table 1 shows the typical external power connections.

Table 1. External Power Connections

Screw Terminal	Applied Voltage	Typical Function
J1	±VA (±15 VMax)	Analog Voltage – Provide analog power for signal conditioning, sensor boards, amplifiers, etc.
J4	±5V (±5.5 VMax)	Analog Voltage – Provide analog power for signal conditioning, sensor boards, amplifiers, etc.
J7	+5 (5.5 Max)	Digital Voltage – Power to digital logic – ADC's, DAC's, etc.
J8	+VD (undefined)	Digital Voltage – Reserved for future use
J9	+1.8 V (2.3 VMax)	Digital Voltage – Core logic voltage for CODEC's, etc.
J10	+3.3 V (3.7 VMax)	Digital Voltage – Power to digital logic – ADC's, DAC's, etc.

2 Signal Conditioning Sites

The signal conditioning sites provide a 20 pin analog I/O header, as well as a 6-pin header for the analog power supply connections. A second 20-pin header is provided for added stability of signal conditioning boards.

2.1 Signal Conditioning I/O Connector

The Analog I/O connectors, J2 and J3, are designed to provide up to eight single ended or four differential channels to/from the data converter EVM's. External reference voltages may also be applied to the data converter through the analog I/O connector. Since the reference requirements vary by converter type, no restrictions are placed on the input voltage levels. Be sure to check the documentation for the EVM before applying any input signals. Single and dual channel converters will leave the unused pins open.Table 2 shows the standard analog connector pin out.

Table 2. Signal Conditioning I/O Connections

Signal	Pin Number		Signal
A0(–)	1	2	A0(+)
A1(–)	3	4	A1(+)
A2(–)	5	6	A2(+)
A3(–)	7	8	A3(+)
AGND	9	10	A4
AGND	11	12	A5
AGND	13	14	A6
VCOM	15	16	A7
AGND	17	18	REF–
AGND	19	20	REF+

The 20-pin headers located beside JP1 and JP2 provide stability for the signal conditioning boards – no signals are routed to or from these connectors. These connectors are labeled *Analog 1* and *Analog 2* on the interface board silk screen and in the assembly drawing found in Section 6 of this manual.

2.2 Signal Conditioning Power Connector

The Interface Board provides a common power bus to both signal conditioning sites. The power connector used on the Interface Board is a 6 pin male header. Four power connectors JP1, JP2, JP3 and JP4 are provided—each with the same pin out. The purpose of this is to allow an A-to-D converter to use the same signal conditioning board as a D-to-A converter, simply by rotating the signal conditioning board 180 degrees. For additional details, please refer to the *DAP Signal Conditioning Board Users Guide* (SLAU105).

Table 3 shows the power connector voltages supplied to the signal conditioning module.

Table 3. Signal Conditioning Power Connections—JP1, JP2, JP3 and JP4

Signal	Pin Number		Signal
+VA	1	2	–VA
+5VA	3	4	–5VA
AGND	5	6	AGND

3 Serial Interface EVM Sites

The serial interface consists of two serial digital I/O connectors (J11 and J12), two power connectors (JP5 and JP6) and two analog I/O connectors (J5 and J6). The analog I/O connectors are configured as *pass through* connections from/to the signal conditioning site connectors J2 and J3.

3.1 Serial Site Digital I/O Connections

The digital I/O connectors are 20 pin male headers providing access to the various signals defined in the F2407, F2808 and F2812 eZdsp™. Reference Manuals, as well as the TMS470R1A1024 Reference Manual. SPST switch SW1.1 controls the signals available to Serial Site 2 through a pair of SN74CBTLV3257 FET Muxes located at U6 and U8. When SW1.1 is open (silkscreen marked "0"), J11 is normally connected to an Serial Peripheral Interface (SPI) port. When SW1.1 is closed (silkscreen marked "1"), Serial Site 2 may be used with the Multi channel Buffered Serial Port (McBSP) found on TMS320F2812 DSP's. Table 4 shows the serial connector pin out for the F2812eZdsp™.

Table 4. Typical F2812 Serial Site Digital I/O Connections—J11 and J12

Signal			Pin Number		Signal		
Site 1 (J12)	Site 2 (J11) SW1.1 Open	Site 2 (J11) SW1.1 Closed			Site 1 (J12)	Site 2 (J11) SW1.1 Open	Site 2 (J11) SW1.1 Closed
NC	CLKOUT	IOPB9	1	2	IOPA11	IOPA7	IOPA7
SPICLKa	PWM12	MCLKXa	3	4	DGND	DGND	DGND
IOPA12	CAP1/QEP1	MCLKRa	5	6	CANTXa	CANTXa	CANTXa
SPISTEa	T1PWM/T1CMP	MFSXa	7	8	CANRXa	CANRXa	CANRXa
IOPB1	CAP2/QEP2	MFSRa	9	10	DGND	DGND	DGND
SPISIMOa	PWM10	MDXa	11	12	IOPA4	IOPA5	IOPA5
SPISOMIa	PWM11	MDRa	13	14	IOPA3	IOPA3	IOPA3
XINT1	CAP3/QEPI1	XINT2	15	16	IOPD5	IOPD5	IOPD5
PWM1	PWM2	PWM2	17	18	DGND	DGND	DGND
T1CTRIP	XINT1	IOPE0	19	20	IOPB8	IOPB8	IOPB8

Most of the signals shown above can be configured as simple GPIO. In general, the TMS320F2812 will support an SPI (clock stop) type interface as well as a McBSP (continuous clock) type interface. The McBSP port can also work in SPI mode, providing two identicle operating modes on J11 and J12. With the exception of the McBSP signals, the F2407eZdsp™ provides the same connections shown in Table 4.

Note:

Several serial interface EVM's require the use of a GPIO signal applied to pin 1 of their digital I/O connector. When serial site 1 of the HPA-MCU Interface is used with the F2812 in SPI mode, a two pin shunt jumper placed between pins 1 and 2 may be able to facilitate the GPIO requirements. Please consult the schematic in the EVM users guide to see if this is possible.

The muxing of the peripherals on the TMS320F2808 provide a slightly different interconnection scheme. The F2808 device does not support McBSP protocol, so J11 and J12 are configured as two independent SPI ports. Table 5 shows the serial connector pin out for the F2808eZdsp™.

Table 5. Typical F2808 Serial Site Digital I/O Connections—J11 and J12

Signal			Pin Number		Signal		
Site 1 (J12)	**Site 2 (J11) SW1.1 Open**	**Site 2 (J11) SW1.1 Closed**			**Site 1 (J12)**	**Site 2 (J11) SW1.1 Open**	**Site 2 (J11) SW1.1 Closed**
GPIO7	GPIO11	NC	1	2	GPIO13	GPIO6	GPIO6
SPICLKa	SPICLKb	NC	3	4	DGND	DGND	DGND
GPIO34	GPIO6	NC	5	6	CANTXa	CANTXa	CANTXa
SPISTEa	SPISTEb	NC	7	8	CANRXa	CANRXa	CANRXa
GPIO9	GPIO21	NC	9	10	DGND	DGND	DGND
SPISIMOa	SPISIMOb	NC	11	12	GPIO5	GPIO5	GPIO5
SPISOMIa	SPISOMIb	NC	13	14	GPIO3	GPIO3	GPIO3
GPIO14	GPIO34	GPIO23	15	16	SCLa	SCLa	SCLa
EPWM1A	GPIO1	GPIO1	17	18	DGND	DGND	DGND
GPIO12	GPIO15	GPIO15	19	20	SDAa	SDAa	SDAa

3.2 Serial Power Connector

The Interface Board provides a common power bus to both serial sites. The power connector used on the Interface Board is a 10 pin male header. Two power connectors JP5 and JP6 are provided—each with the same pin out. JP5 sevices serial Site 2, while JP6 services serial Site 1. Table 6 shows the power connector voltages supplied to the signal conditioning module.

Table 6. Serial Power Connections—JP5 and JP6

Signal(1)	Pin Number		Signal
+VA	1	2	–VA
+5VA	3	4	–5VA
DGND	5	6	AGND
+1.8VD	7	8	VD1
+3.3VD	9	10	+5VD

(1) P5 is also used for the parallel EVM site.

3.3 Analog I/O Connectors

As mentioned previously, the analog I/O connectors act as pass through connectors to the signal conditioning sites. Table 7 shows the analog signals passed to/from signal conditioning module to the input/output of compatible modular EVM's.

Table 7. Analog I/O Connections—J6 and J5

Signal	Pin Number		Signal
A0(–)	1	2	A0(+)
A1(–)	3	4	A1(+)
A2(–)	5	6	A2(+)
A3(–)	7	8	A3(+)
AGND	9	10	A4
AGND	11	12	A5
VCOM	13	14	A6
AGND	15	16	A7
AGND	17	18	REF–
REFIN	19	20	REF+

4 Parallel Interface EVM Sites

The parallel interface consists of a 32-pin header (J14) which provides access up to 16 parallel data bits, and a 20-pin parallel control header (J13). The parallel control header provides 4-muxed address lines, read and write strobes, interrupt capabilities, chip select and clock signals. Analog I/O and power is also provided.

4.1 Parallel Analog I/O and Power Connections

The parallel site uses the same analog I/O and power connections described in the serial interface section of this manual. Typically, a parallel ADC EVM will use the analog interface connector located at J6, and the power connector located at JP5. A parallel DAC EVM will typically use the analog connector located at J5. If pass through power connections are made on either the DAC or ADC EVM, the ADC and DAC boards could be *stacked* allowing a complete signal chain to be realized. Read the specific EVM Users Guide to determine if a stacking arrangement is possible. See the previous sections for pin out details of the analog I/O and power connectors.

4.2 Parallel Control Connector

The parallel control connector feeds chip select, read, write and address lines to the parallel EVM's. The address decoding for most parallel EVM's will be done on the EVM card itself, lending way to the possibility of *stacking* several cards together. Table 8 shows the typical signals found on parallel interface EVM's, designed to be used with the HPA-MCU Interface Board.

Table 8. Parallel Control Connections—J13

Signal	Pin Number		Signal
DC_CSa ($\overline{DS}$, $\overline{PS}$ or $\overline{IS}$ via W3)	1	2	DGND
$\overline{WE}$	3	4	DGND
$\overline{RE}$	5	6	DGND
EVM_A0 (A2 or A12)	7	8	DGND
EVM_A1 (A3 or A13)	9	10	DGND
EVM_A2 (A4 or A14)	11	12	DGND

Table 8. Parallel Control Connections—J13 (continued)

Signal	Pin Number		Signal
EVM_A3 (A5 or A15)	13	14	DGND
GPIO (SPARE – NC)	15	16	DGND
T2PWM	17	18	DGND
XINT2	19	20	DGND

DC_CSa is intended to act as a chip select to the EVM, not necessarily the actual data converter being evaluated. Carefully read the documentation that came with your EVM for details on how this signal is used. W3 allows the user to connect the card to I/O, Data or Program space.

The EVM address lines EVM_A0 through EVM_A3 are fed from a four bit 2:1 bus switch, U5. Typically, this provides access to DSP address lines A2..A5, or A12..A15. SPST switch SW1.2 controls which address lines are sent to the parallel control connector. When SW1.2 is closed, address lines A12 through A15 are sent to the data converter EVM. When SW1.2 is open, the EVM uses address lines A2 through A5.

4.3 Parallel Data Bus Connector

The Parallel data connector used on the Interface Card is a 32 pin male header. Typical parallel EVM's will have a data bus that is a minimum of 16 bits wide and a maximum of 24 bits. The C2000 Interface Board is limited to a 16 bit data bus, but accepts cards designed to the 24-bit wide maximum. Data is aligned LSB to LSB. Table 9 shows the parallel data bus connections.

Table 9. Parallel Data Bus Connections—J14

Signal	Pin Number		Signal
D0	1	2	DGND
D1	3	4	DGND
D2	5	6	DGND
D3	7	8	DGND
D4	9	10	DGND
D5	11	12	DGND
D6	13	14	DGND
D7	15	16	DGND
D8	17	18	DGND
D9	19	20	DGND
D10	21	22	DGND
D11	23	24	DGND
D12	25	26	DGND
D13	27	28	DGND
D14	29	30	DGND
D15	31	32	DGND

5 Related Documentation From Texas Instruments

1. *Designing Modular EVM's for Data Acquisition Products* (SLAA185)
2. *DAP Signal Conditioning Board Users Guide* (SLAU105)
3. *MAX3232, Multichannel RS-232 Line Driver/Receiver* (SLLS410)
4. *SN74CBTD3861, 10-Bit Bus Switch* (SCDS017)
5. *SN65HVD235, CAN Tranceiver* (SLLS557)
6. *SN74LVTH16245, 16-Bit Bus Tranceiver* (SCBS143)
7. *SN74CBT3257, 4-Bit 1-of-2 FET Multiplexer/Demultplexer* (SCDS040)

5.1 Related Third Party Documentation

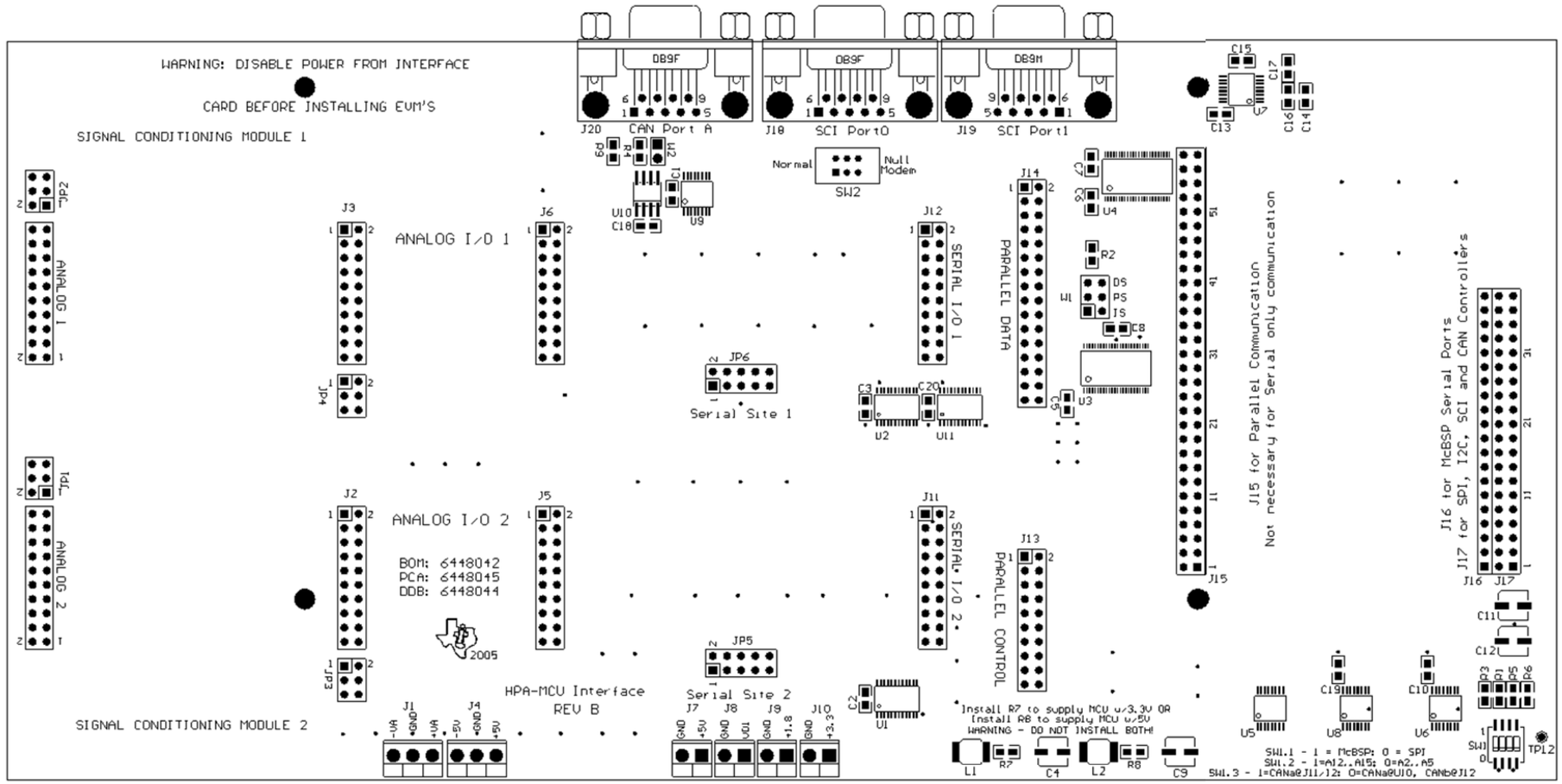
1. *LF2407A eZdsp Technical Reference*–www.spectrumdigital.com
2. *LF2808 eZdsp Technical Reference*–www.spectrumdigital.com
3. *LF2812 eZdsp Technical Reference*–www.spectrumdigital.com

6 HPA-MCU Interface Board Assembly and Board Schematics

Table 10 shows the Bill of Materials (BOM) for the HPA-MCU Interface Board.

Table 10. Bill of Materials

Designators	Description	Manufacturer	Mfg. Part Number
C1 C2 C3 C5 C6 C7 C8 C10 C13 C14 C15 C16 C17 C18 C19 C20	0.1 µF, 0805, Ceramic, X7R, 50V, 10%	TDK	C2012X7R1E104K
C4 C9 C11 C12	33 µF, 16V, Aluminum	Panasonic	ECEV1AA330SR
ANALOG 1& 2 J2 J3 J5 J6 J11 J12 J13	10 Pin, Dual Row, SMT Header (20 Pos.)	Samtec	TSW-110-07-L-D
J14	16 Pin, Dual Row, SMT Header (32 Pos.)	Samtec	TSW-116-07-L-D
JP1 JP2 JP3 JP4 W1	3 Pin, Dual Row, SMT Header (6 Pos.)	Samtec	TSW-103-07-L-D
JP5 JP6	5 Pin, Dual Row, SMT Header (10 Pos.)	Samtec	TSW-105-07-L-D
J7 J8 J9 J10	2 Terminal Screw Commector	OST	ED1514
J1 J4	3 Terminal Screw Commector	OST	ED1515
J15	30 Pin, Dual Row, SMT Header (60 Pos.)	Samtec	TSW-130-07-L-D
J16	20 Pin, Single Row, SMT Header (20 Pos.)	Samtec	TSW-120-07-L-S
J17	20 Pin, Dual Row, SMT Header (40 Pos.)	Samtec	TSW-120-07-L-D
J18 J20	DB9 Female, Right Angle	AMP/Tyco	747844-4
J19	DB9 Male, Right Angle	AMP/Tyco	747840-4
L1 L2	15 µH Inductor, SMT, 1608 Series	Inductors, Inc.	CTDS1608C-153
R1 R2 R3 R5 R6	10K Ω, 0805, 5%, 0.1 W resistor	Yageo America	9C08052A1002JLHFT
R4 R9	120 Ω, 0805, 5%, 0.1 W resistor	Yageo America	9C08052A1200JLHFT
R7 R8	Not Installed		
SW1	4 Position SPST Switch	CTS Corp	218-10LPST
SW2	DPDT Slide Switch	E-Switch	EG2209
U1 U2 U11	10-Bit FET Bus Switch With Level Shifting	Texas Instruments	SN74CBTD3861PW
U3 U4	16-Bit Bus Transciever	Texas Instruments	SN74LVTH16245ADGGR
U5 U6 U8 U9	4-Bit 1of 2 FET Multiplexer/Demultiplexer	Texas Instruments	SN74CBTLV3257PWR
U7	Multichannel RS-232 Line Driver/Reciever	Texas Instruments	MAX3232CPWR
U10	3.3V Can Tranceiver with Auto Loop-back	Texas Instruments	SN65HVD235D
W2	2 Pin, TH Header	Samtec	TSW-102-07-L-S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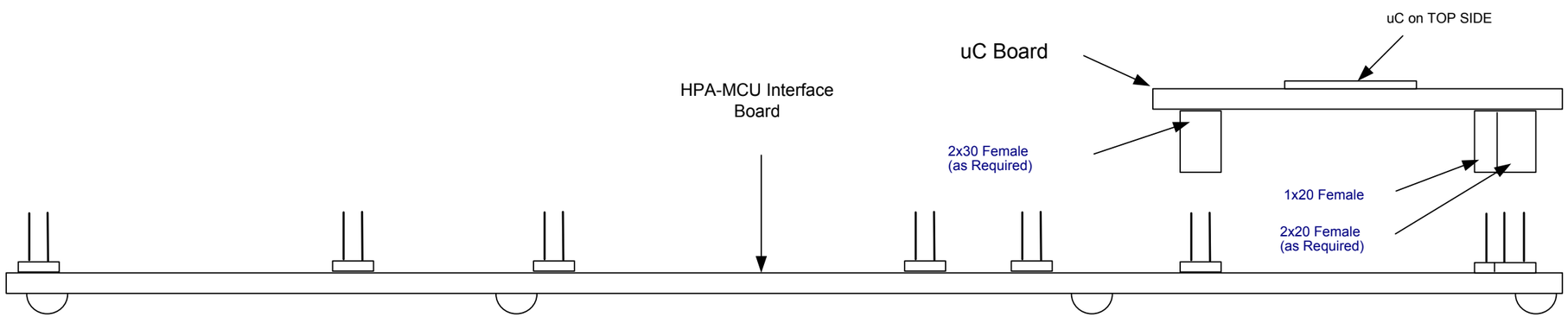
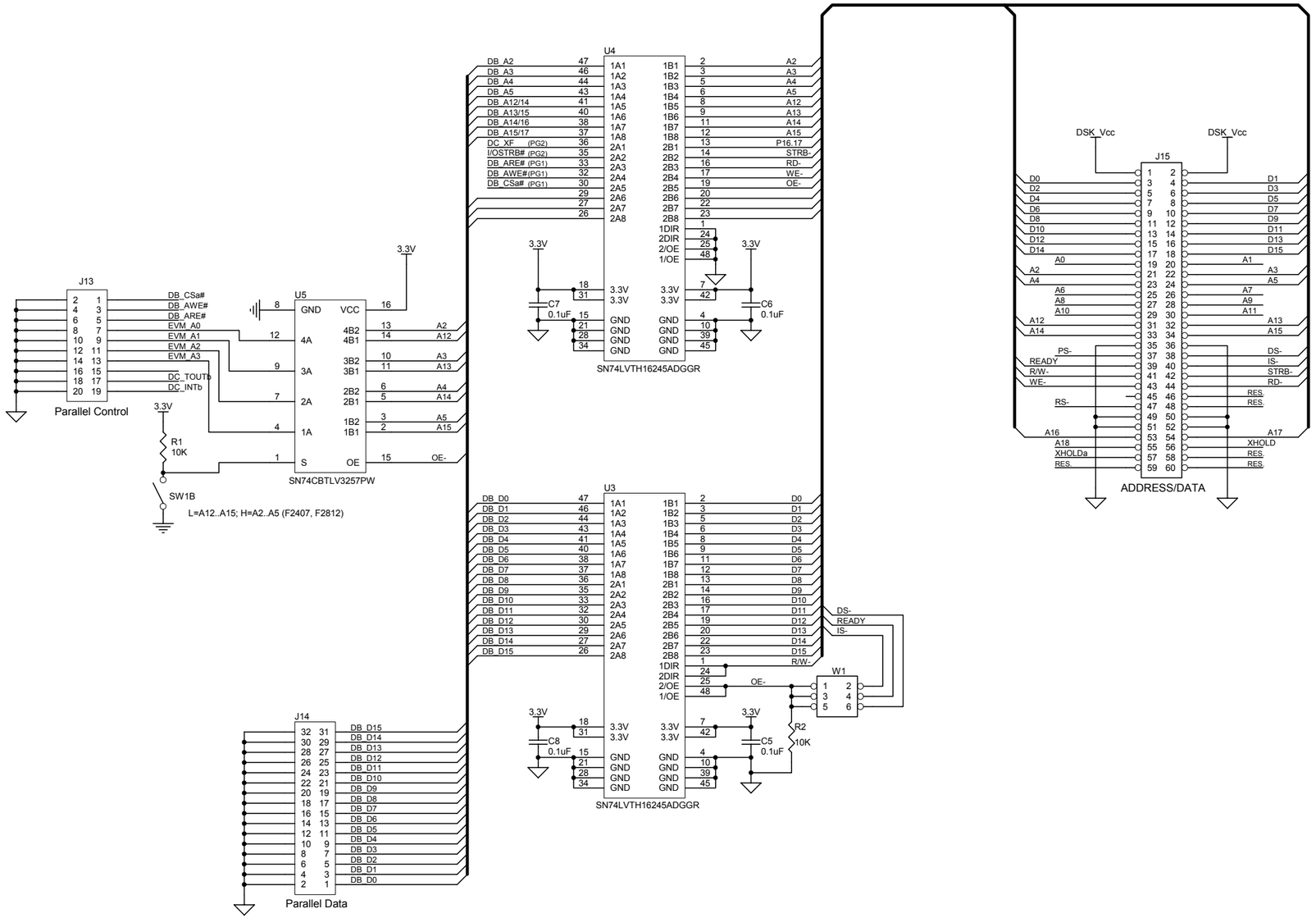
CARD BEFORE INSTALLING EVM'S
SIGNAL CONDITIONING MODULE 1
SIGNAL CONDITIONING MODULE 2
ANALOG I/O 1
ANALOG I/O 2
BOM: 6448042
PCA: 6448045
DDB: 6448044
2005
HPA-MCU Interface
REV B
J20 CAN Port A
J18 SCI Port0
J19 SCI Port1
DB9F
DB9M
Normal
Null Modem
SW2
Serial Site 1
Serial Site 2
PARALLEL DATA
PARALLEL CONTROL
SERIAL I/O 1
SERIAL I/O 2
J15 for Parallel Communication
Not necessary for Serial only communication
J16 for McBSP Serial Ports
J17 for SPI, I2C, SCI and CAN Controllers
Install R7 to supply MCU w/3.3V OR
Install R8 to supply MCU w/5V
WARNING - DO NOT INSTALL BOTH!
SW1.1 - 1 = McBSP; 0 = SPI
SW1.2 - 1=A12..A15; 0=A2..A5
SW1.3 - 1=CANa@U11/12; 0=CANa@U10, CANb@U12


uC Board
uC on TOP SIDE
HPA-MCU Interface
Board
2x30 Female
(as Required)
1x20 Female
2x20 Female
(as Required)

Revision History		
REV	ECN Number	Approved
A	Initial Release	TH



Engineer:	Tom Hendrick
Drawn By:	Tom Hendrick
FILE:	HPA_AEC_sh1.sch

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

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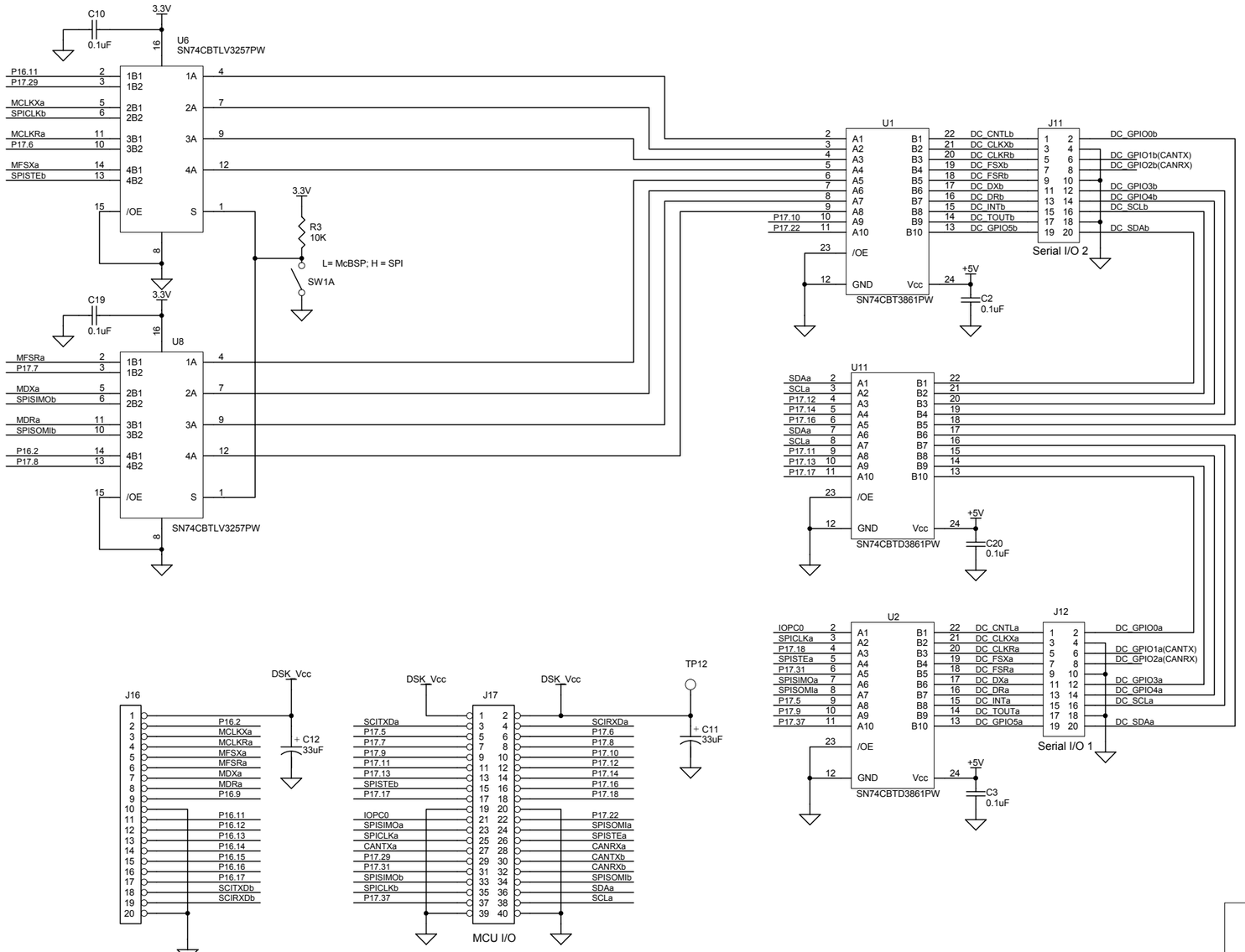

Engineer:	Tom Hendrick
Drawn By:	Tom Hendrick
FILE:	

TEXAS INSTRUMENTS

12500 TI Boulevard. Dallas, Texas 75243

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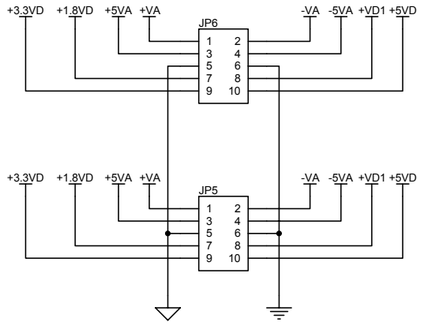
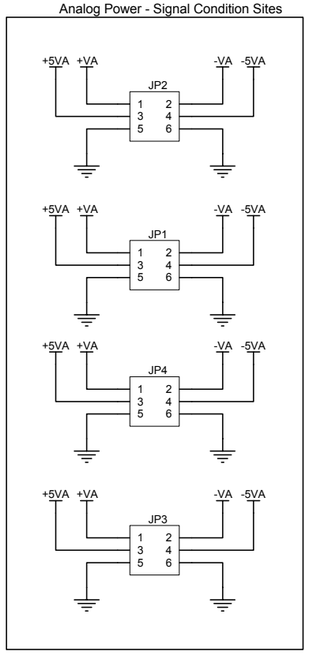
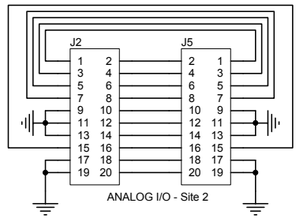
DATE: 13-Jun-2005 SIZE: SHEET: 2 OF: 3

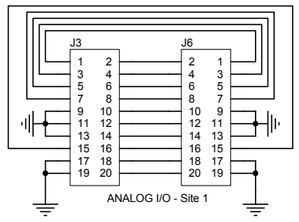
EVM Analog/Digital Power Connectors



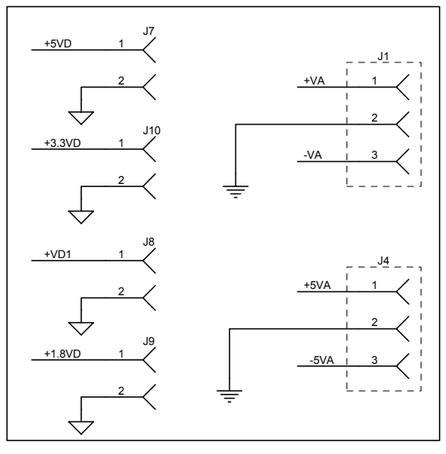
Analog Power - Signal Condition Sites



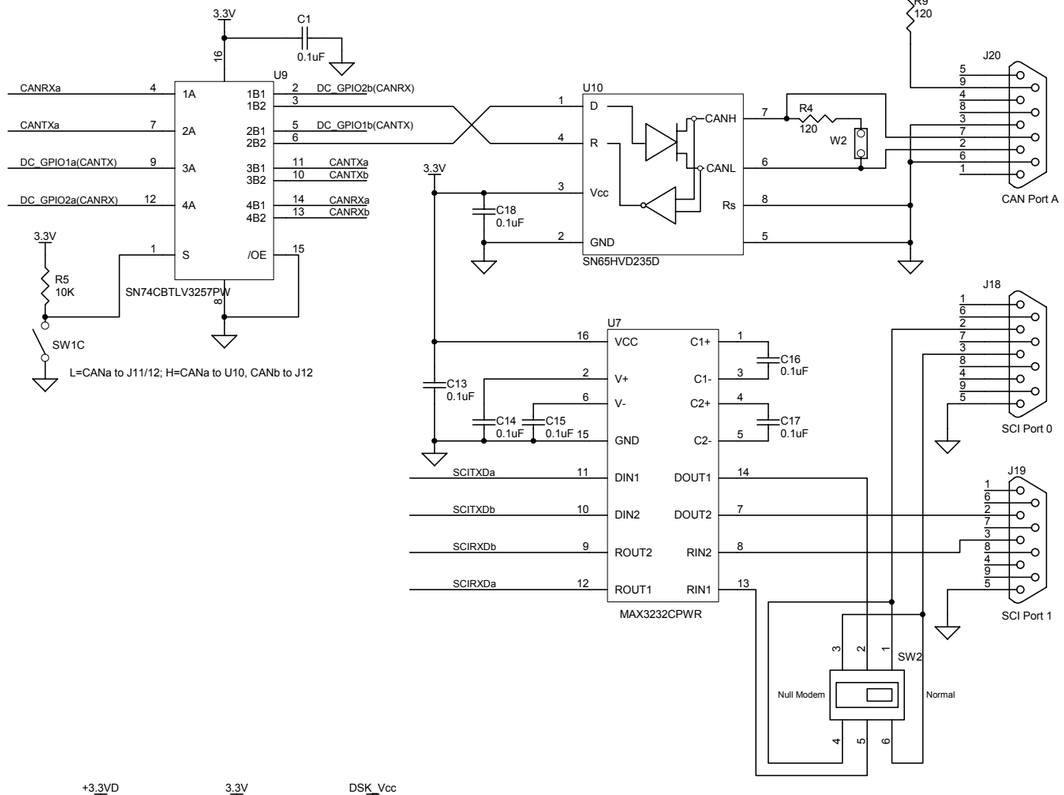


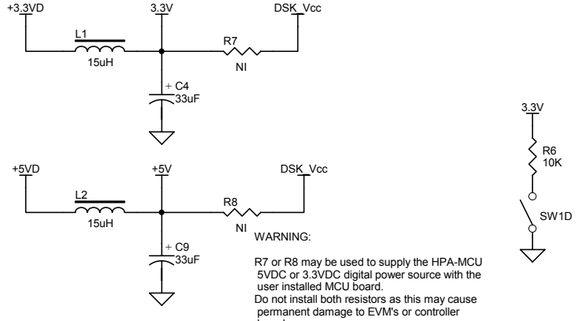


MAIN POWER INPUT TERMINALS



SCI and CAN Communication Options





WARNING:

R7 or R8 may be used to supply the HPA-MCU 5VDC or 3.3VDC digital power source with the user installed MCU board.
Do not install both resistors as this may cause permanent damage to EVM's or controller boards.
Please refer to the Users Guide and MCU

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Title:	HPA-MCU Interface Card
Engineer: Tom Hendrick	DOCUMENTCONTROL #: 6440845 REV: A
Drawn By: Tom Hendrick	DATE: 13-Jun-2005 SIZE: SHEET: 3 OF: 3
FILE:	

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