STANDARD MICROSYSTEMS CORPORATION

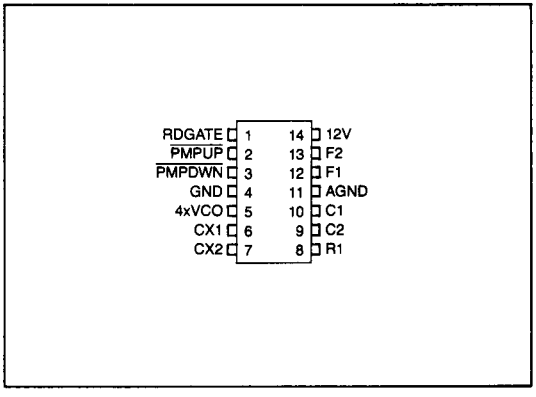
HDC 9223
PRELIMINARY

High Performance Analog Data Separator Support Circuit (ADSSC) For Hard Disk

FEATURES

- ☐ Significantly reduces component count in hard disk systems
- ☐ Completely compatible with the HDC 9226 Hard Disk Data Separator and the HDC 9224 Universal Disk Controller
- ☐ Simplifies design and improves performance of ST506 Hard Disk Controller sub-system
- ☐ Eliminates costly critical "tune up" adjustments
- ☐ Space saving 14 pin package
- ☐ Monolithic analog solution reduces critical pc board layout
- ☐ Single + 12V power supply
- ☐ Printed Circuit Board Artwork available to facilitate prototyping and evaluation

PIN CONFIGURATION



SECTION VII

GENERAL DESCRIPTION

The HDC 9223 Analog Data Separator Support Circuit (ADSSC) is a 14 pin device, which when used with the HDC 9224 Universal Disk Controller and the HDC 9226 Hard Disk Data Separator significantly simplifies the design of a high performance hard disk data separator.

The HDC 9223, combined with the HDC 9226 and a few resistors and capacitors, forms a phase locked loop which performs phase and frequency locking onto either the MFM or FM data stream output by ST506 or ST412 type drives.

By reducing the number of critical discrete components to a minimum and eliminating all critical adjustments, the HDC 9223 and HDC 9226 simplify the task of the designer.

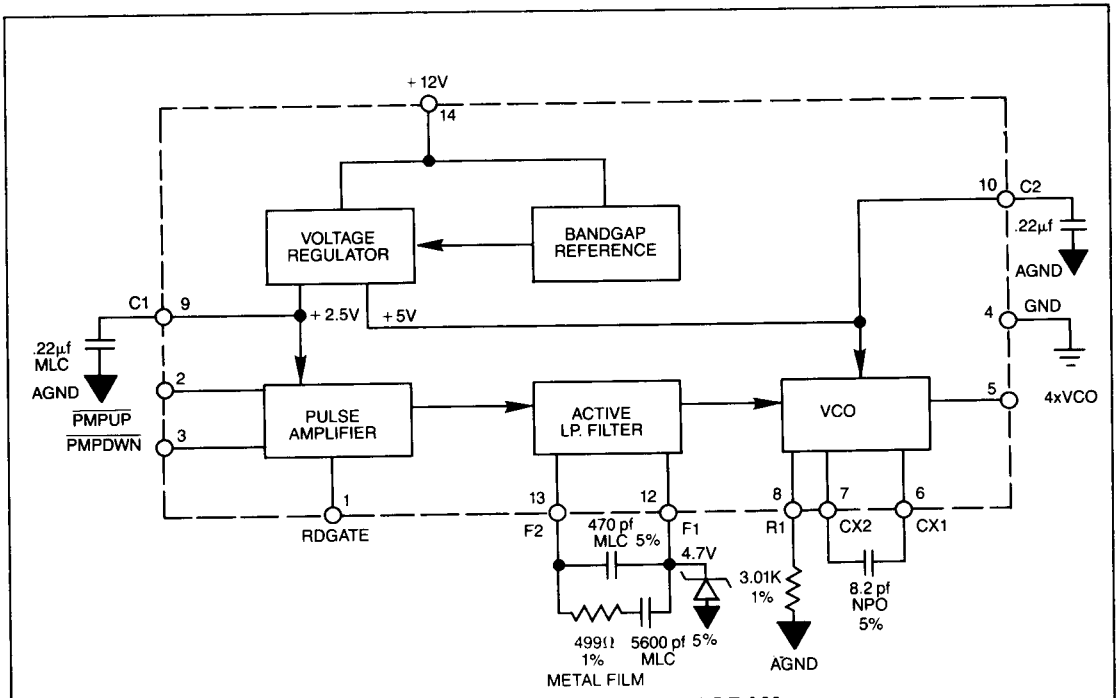


FIGURE 1: HDC 9223 BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	DESCRIPTION
1	Read Gate	RDGATE	This active high input controls the gain of the loop. A high level decreases the gain and a low level increases the gain.
2	$\overline{\text{Pump Up}}$	$\overline{\text{PMPUP}}$	This active low input causes the VCO to increase its frequency.
3	$\overline{\text{Pump Down}}$	$\overline{\text{PMPDWN}}$	This active low input causes the VCO to decrease its frequency.
4	Digital Ground	GND	This is the ground connection for the digital circuitry within the HDC 9223.
5	Four Times VCO	4xVCO	This is the VCO output. It will vary from 18 to 22 MHz as a function of the $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDWN}}$ input signals.
6	External Capacitor Connection 1	CX1	An 8.2 pf external NPO capacitor is connected across pins 6 and 7.
7	External Capacitor Connection 2	CX2	
8	External Resistor Connect	R1	A 3.01K 1% resistor is connected from this pin to Analog Ground.
9	External Filter Cap Connection 1	C1	A .22µf MLC capacitor is connected from this pin to Analog Ground.
10	External Filter Cap Connection 2	C2	A .22µf MLC capacitor is connected from this pin to Analog Ground.
11	Analog Ground	AGND	This is the ground connection for the analog circuitry within the HDC 9223.
12	External Filter Connection 1	F1	A filter network should be connected to this pin as shown in Figure 4.
13 •	External Filter Connection 2	F2	A filter network should be connected to this pin as shown in Figure 4.
14	+ 12 Volts	12V	Connect the power supply to this pin. A .22µf bypass capacitor should also be connected from this pin to Analog Ground.

DESCRIPTION OF OPERATION

The functional block diagram of the HDC 9223 is shown in Figure 1. The major functional blocks within the HDC 9223 are a voltage controlled oscillator (VCO), an active loop filter, and a pulse amplifier. The gain of the pulse amplifier is controlled by the RDGATE logic input.

The voltage controlled ocsillator generates the 4xVCO output (nominally 20 MHz). The frequency of this output is determined by the signals on the $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDWN}}$ inputs to the HDC 9223. Since the half bit time for data from the disk is 100ns, the HDC 9226 divides the frequency of the 4xVCO signal in half, and compares the phase and frequency of the resulting 10 MHz signal to that of the incoming data. The HDC 9226 then varies the pulse width on the $\overline{\text{PMPUP}}$ and $\overline{\text{PMPDWN}}$ lines to adjust the output frequency of the VCO on the HDC 9223, closing the loop.

A voltage regulator and bandgap voltage reference ensure power supply rejection and stable VCO operation.

MAXIMUM GUARANTEED RATINGS

Operating Temperature Range ..... 0 to 70 C
Storage Temperature Range ..... −55 to +150 C
Lead Temperature (soldering, 10 sec) ..... +300 C
Positive Voltage on any Pin, with respect to Ground ..... V_{CC} +0.5V
Negative Voltage on any Pin, with respect to Ground ..... −0.5V

Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the "Maximum Guaranteed Ratings" not be exceeded, or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when AC power is switched off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibly exists it is suggested that a clamp circuit be used.

DC ELECTRICAL SPECIFICATIONS

(TA = 0C to 70C, V_{CC} = 12.0V ± 5%)

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Notice: This is not a final specification.
Some parametric limits are subject to change.

Parameter	Min.	Max.	Units	Comments
SUPPLY CURRENT I_{CC}		60	mA	
SUPPLY VOLTAGE V_{CC}	11.4	12.6	V	12V ± 5%
INPUT VOLTAGE V_{IL} V_{IH}	 3.6	2.4	V V	 I_{OL} = 2.0mA I_{OH} = −400μA
OUTPUT VOLTAGE V_{OL} V_{OH}	 4.1	1.2	V V	 I_{OL} = 2.0mA I_{OH} = −400μA
INPUT CURRENT I_{IL} I_{IH}		−10 40	μA μA	 V_{IL} = 0.8V V_{IH} = 3.0V

AC ELECTRICAL CHARACTERISTICS

(TA = 0C to 70C, V_{CC} = 12.0V ± 5%)

PRELIMINARY
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Parameter	Symbol	Min.	Max.	Units	Comments
$\overline{\text{PMPUP}}$, $\overline{\text{PMPDWN}}$ pulse width	t_{PW}	15	125	ns	Measured at 50% amplitude (Fig. 2)
$\overline{\text{PMPUP}}$, $\overline{\text{PMPDWN}}$ rise time	t_{IR}		10	ns	Measured between 0.6 and 1.8V (Fig. 2)
$\overline{\text{PMPUP}}$, $\overline{\text{PMPDWN}}$ fall time	t_{IF}		10	ns	Measured between 0.6 and 1.8V (Fig. 2)
Output Frequency (when locked)		18	22	MHz	
4xVCO rise time	t_{OR}		15	ns	Measured between 1.5 and 3.0V; Cload = 10pf (Fig. 3)
4xVCO fall time	t_{OF}		15	ns	Measured between 1.5 and 3.0V; Cload = 10pf (Fig. 3)
4xVCO pulse width high	t_{OH}	16		ns	Fig. 3 Measured at 2.5V
4xVCO pulse width low	t_{OL}	16		ns	Fig. 3 Measured at 2.5V

SECTION VII

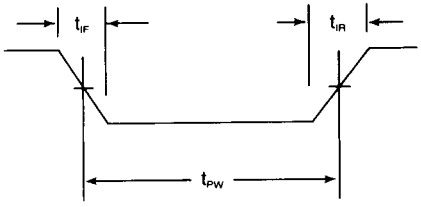

FIGURE 2:
$\overline{\text{PMPUP}}$/$\overline{\text{PMPDWN}}$ TIMING

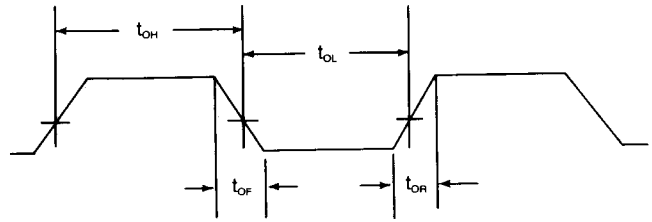

FIGURE 3: 4xVCO TIMING

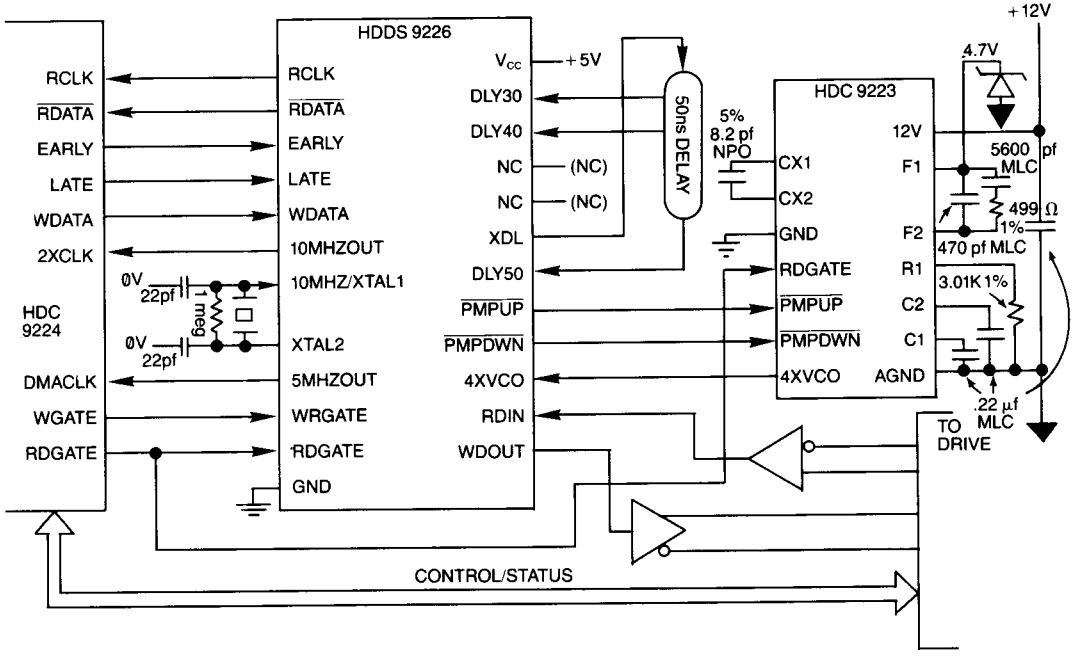

FIGURE 4: TYPICAL CIRCUIT CONFIGURATION

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