

# n-Channel Power MOSFET

OptiMOS™  
BSF077N06NT3 G

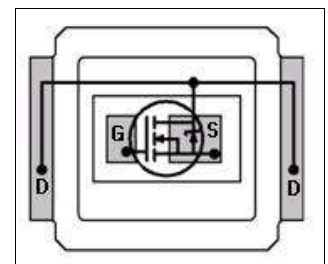
## Data Sheet

1.4, 2011-03-01  
Preliminary

Industrial & Multimarket

## 1 Description

OptiMOS™60V products are class leading power MOSFETs for highest power density and energy efficient solutions. Ultra low gate- and output charges together with lowest on state resistance in small footprint packages make OptiMOS™ 60V the best choice for the demanding requirements of switched mode power supplies in Servers, Datacom and Telecom applications but also for motor drives. With almost no parasitic package inductances, the CanPAK allows best controllability of the gate in highly dynamic switching environments. This package in addition features best cooling capability through top-side cooling of the metal can. Hence, this packaging technology combined with the OptiMOS silicon enables highest efficiency levels while having minimal space requirements at the same time



### Features

- Optimized technology for DC/DC converters
- 100% avalanche tested
- Excellent gate charge x  $R_{DS(on)}$  product (FOM)
- Qualified according to JEDEC<sup>1)</sup> for target applications
- Superior thermal resistance
- Pb-free plating; RoHS compliant
- Halogen-free according to IEC61249-2-21
- Double.sided cooling
- Compatible with DirectFET® package ST footprint and outline
- Low profile (<0.7mm)
- Low parasitic inductance

### Applications

- DC/DC converters
- Synchronous rectification
- Power distribution
- Motor drive applications



**Table 1 Key Performance Parameters**

Parameter	Value	Unit	Related Links
$V_{DS}$	60	V	<a href="#">IFX OptiMOS webpage</a> <a href="#">IFX OptiMOS product brief</a> <a href="#">IFX OptiMOS spice models</a> <a href="#">IFX Design tools</a>
$R_{DS(on),max}$	7.7	mΩ	
$I_D$	56	A	
$Q_{OSS}$	28	nC	
$Q_{g,typ}$	34		

Type	Package	Marking
BSF077N06NT3 G	MG-WDSO-N-2	0206

1) J-STD20 and JESD22

## 2 Maximum ratings

at  $T_j = 25\text{ °C}$ , unless otherwise specified.

**Table 2 Maximum ratings**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Continuous drain current	$I_D$	-	-	56	A	$V_{GS}=10\text{ V}, T_C=25\text{ °C}$
				36		$V_{GS}=10\text{ V}, T_C=100\text{ °C}$
				13		$V_{GS}=10\text{ V}, T_A=25\text{ °C}, R_{thJA}=58\text{ K/W}^1)$
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	-	-	224		$T_C=25\text{ °C}$
Avalanche energy, single pulse	$E_{AS}$	-	-	150	mJ	$I_D=30\text{ A}, R_{GS}=25\text{ }\Omega$
Gate source voltage	$V_{GS}$	-20	-	20	V	
Power dissipation	$P_{tot}$	-	-	38	W	$T_C=25\text{ °C}$
				2.2		$T_A=25\text{ °C}, R_{thJA}=58\text{ K/W}^3)$
Operating and storage temperature	$T_j, T_{stg}$	-40	-	150	°C	
IEC climatic category; DIN IEC 68-1		55	150	56	Ncm	

- 1) DirectFET ® is a trademark of International Rectifier Corporation. BSF077N06NT3 G uses DirectFET ® technology licensed from International Rectifier Corporation.
- 2) See figure 3 for more detailed information
- 3) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70µm thick) copper area for drain connection. PCB is vertical in still air.

## 3 Thermal characteristics

**Table 3 Thermal characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Thermal resistance, junction - case	$R_{thJC}$	-	1.0	-	°K/W	bottom
			3.3	-		top
Device on PCB	$R_{thJA}$	-	-	58		6 cm <sup>2</sup> cooling area <sup>1)</sup>

- 1) Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70µm thick) copper area for drain connection. PCB is vertical in still air

## 4 Electrical characteristics

Electrical characteristics, at  $T_j=25\text{ °C}$ , unless otherwise specified.

**Table 4 Static characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Drain-source breakdown voltage	$V_{(BR)DSS}$	60	15	-	V	$V_{GS}=0\text{ V}$ , $I_D=1\text{ mA}$
Gate threshold voltage	$V_{GS(th)}$	2	3	4		$V_{DS}=V_{GS}$ , $I_D=33\text{ }\mu\text{A}$
Zero gate voltage drain current	$I_{DSS}$	-	0.1	10	$\mu\text{A}$	$V_{DS}=30\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=25\text{ °C}$
		-	10	100		$V_{DS}=60\text{ V}$ , $V_{GS}=0\text{ V}$ , $T_j=125\text{ °C}$
Gate-source leakage current	$I_{GSS}$	-	10	100	nA	$V_{GS}=20\text{ V}$ , $V_{DS}=0\text{ V}$
Drain-source on-state resistance	$R_{DS(on)}$	-	6.6	7.7	$\text{m}\Omega$	$V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$
Gate resistance	$R_G$	-	0.5	-	$\Omega$	
Transconductance	$g_{fs}$	23	46		S	$ V_{DS} >2 I_{D RDS(on)max} $ , $I_D=30\text{ A}$

**Table 5 Dynamic characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Input capacitance	$C_{iss}$	-	2800	3700	$\text{pF}$	$V_{GS}=0\text{ V}$ , $V_{DS}=30\text{ V}$ , $f=1\text{ MHz}$
Output capacitance	$C_{oss}$	-	800	1060		
Reverse transfer capacitance	$C_{rss}$	-	22	-		
Turn-on delay time	$t_{d(on)}$	-	12	-	ns	$V_{DD}=30\text{ V}$ , $V_{GS}=10\text{ V}$ , $I_D=30\text{ A}$ , $R_G=1.6\text{ }\Omega$
Rise time	$t_r$	-	4	-		
Turn-off delay time	$t_{d(off)}$	-	18	-		
Fall time	$t_f$	-	3	-		

**Table 6 Gate charge characteristics<sup>1)</sup>**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Gate to source charge	$Q_{gs}$	-	15	-	nC	$V_{DD}=30\text{ V}$ , $I_D=30\text{ A}$ , $V_{GS}=0\text{ to }10\text{ V}$
Gate to drain charge	$Q_{gd}$	-	3	-		
Switching charge	$Q_{sw}$	-	15	-		
Gate charge total	$Q_g$	-	34	46		
Gate plateau voltage	$V_{plateau}$	-	5.2	-	V	
Output charge	$Q_{oss}$		28	37		$V_{DD}=30\text{ V}$ , $V_{GS}=0\text{ V}$

1) See figure 16 for gate charge parameter definition

**Table 7 Reverse diode characteristics**

Parameter	Symbol	Values			Unit	Note / Test Condition
		Min.	Typ.	Max.		
Diode continuous forward current	$I_s$			30	A	$T_C=25\text{ °C}$
Diode pulse current	$I_{S,pulse}$			120		
Diode forward voltage	$V_{SD}$	-	0.9	1.2	V	$V_{GS}=0\text{ V}$ , $I_F=30\text{ A}$ , $T_j=25\text{ °C}$
Reverse recovery charge	$Q_{rr}$	-	56	-	nC	$V_R=30\text{ V}$ , $I_F=I_s$ ,
Reverse recovery time	$t_{rr}$	-	41	-	ns	$di_F/dt=400\text{ A}/\mu\text{s}$

## 5 Electrical characteristics diagrams

Table 8

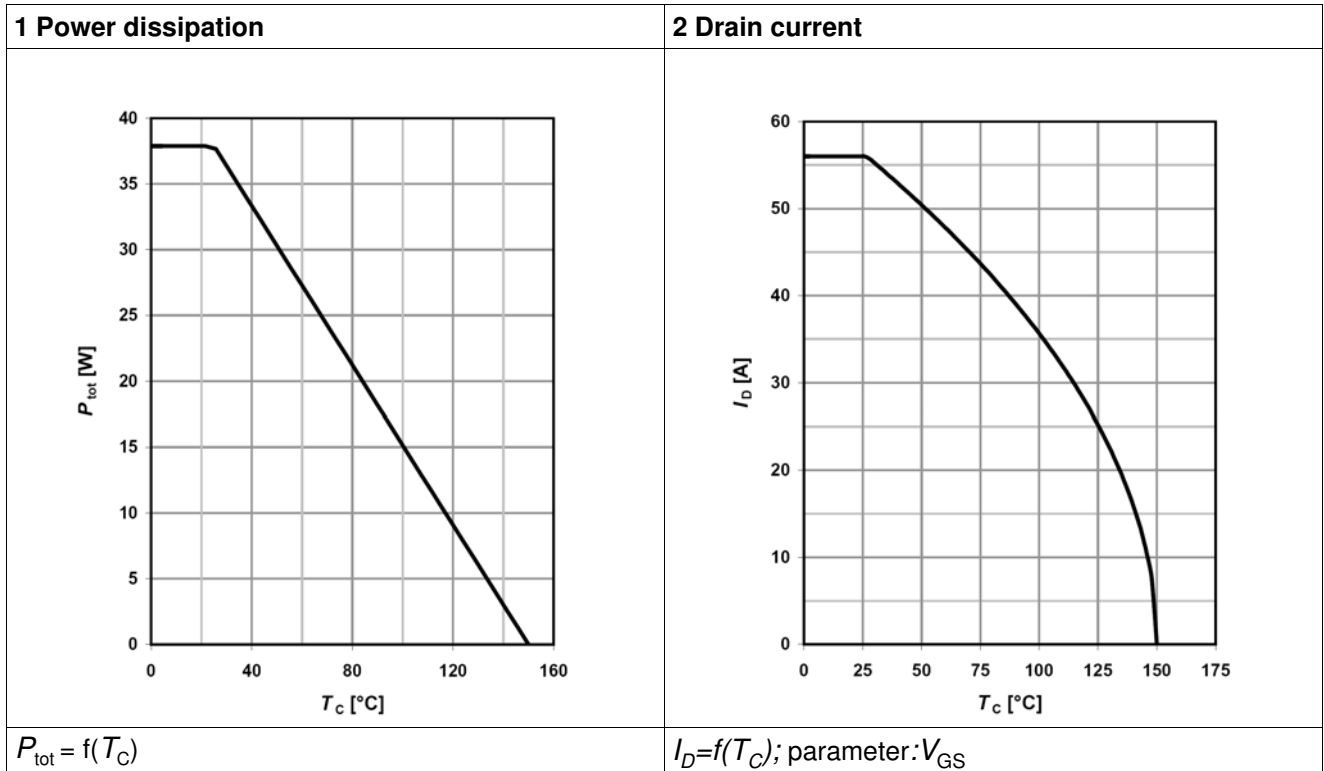


Table 9

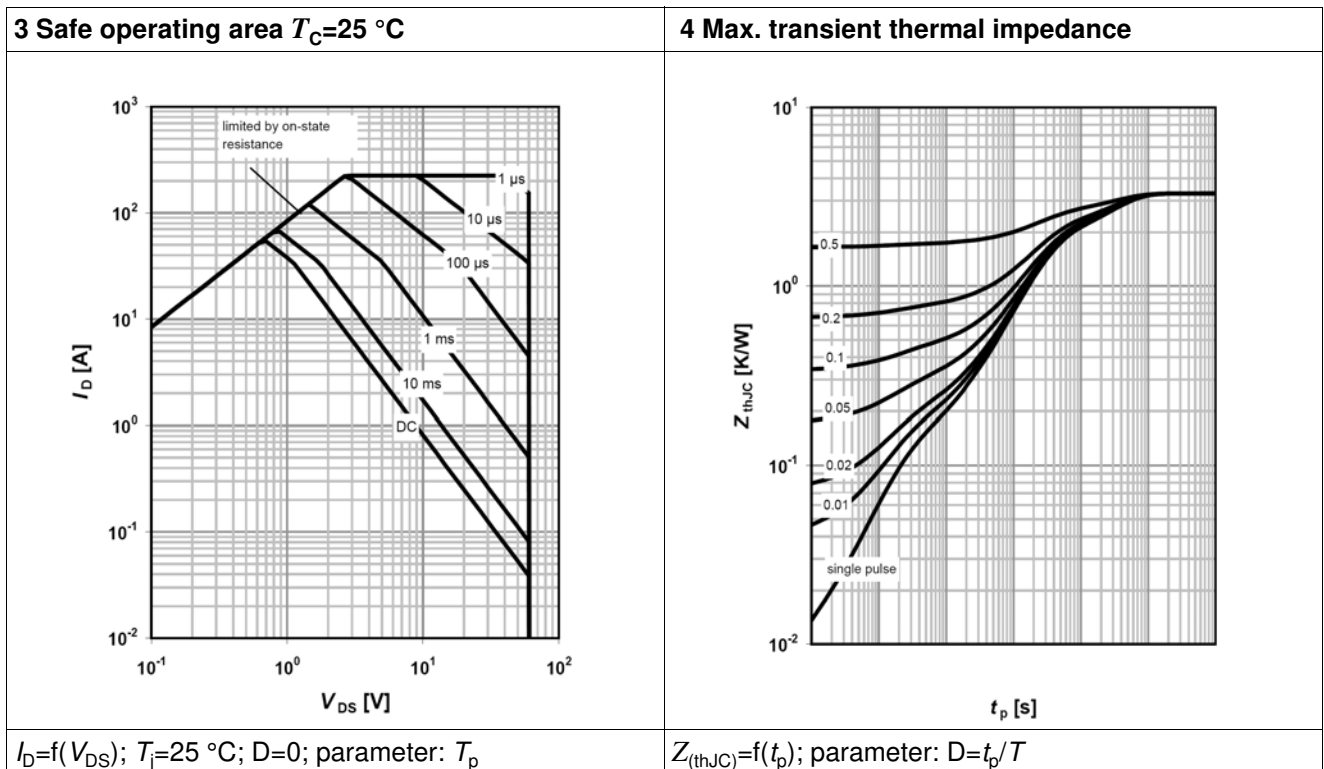




Table 10

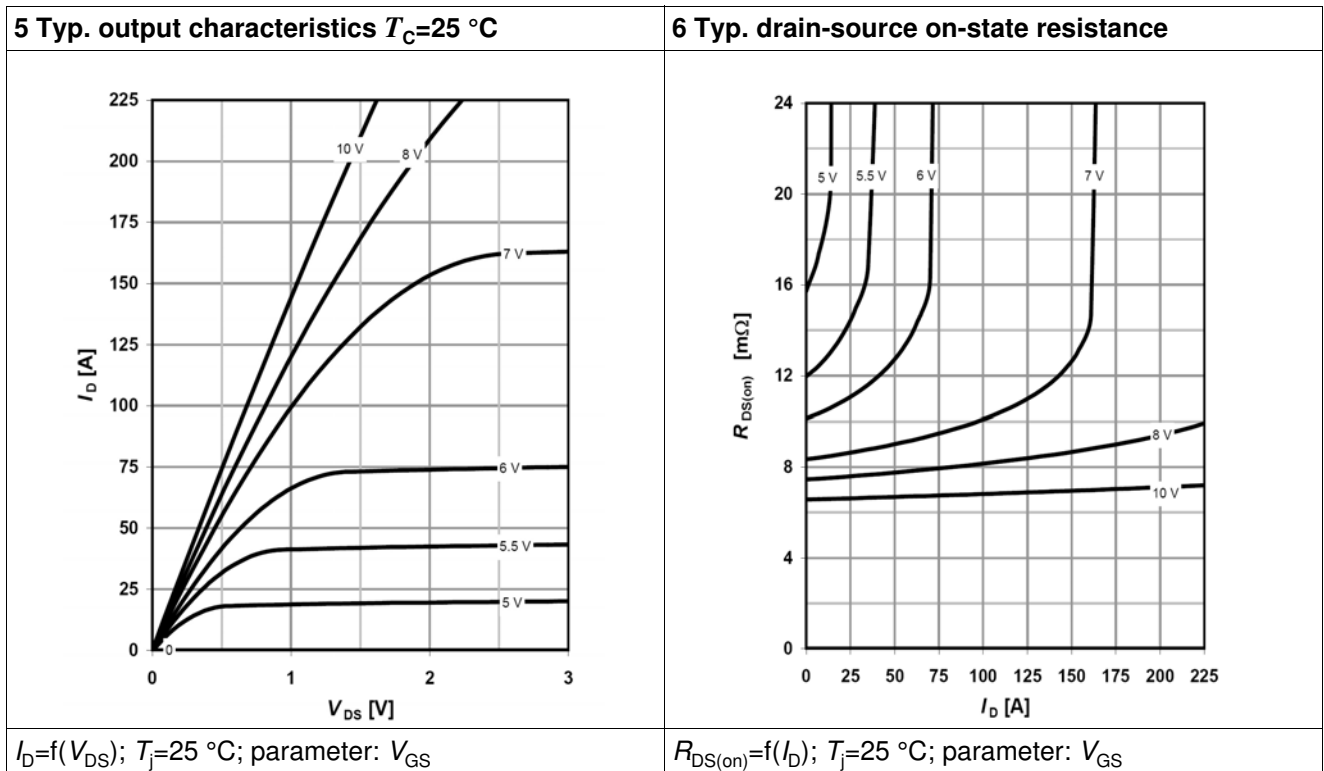


Table 11

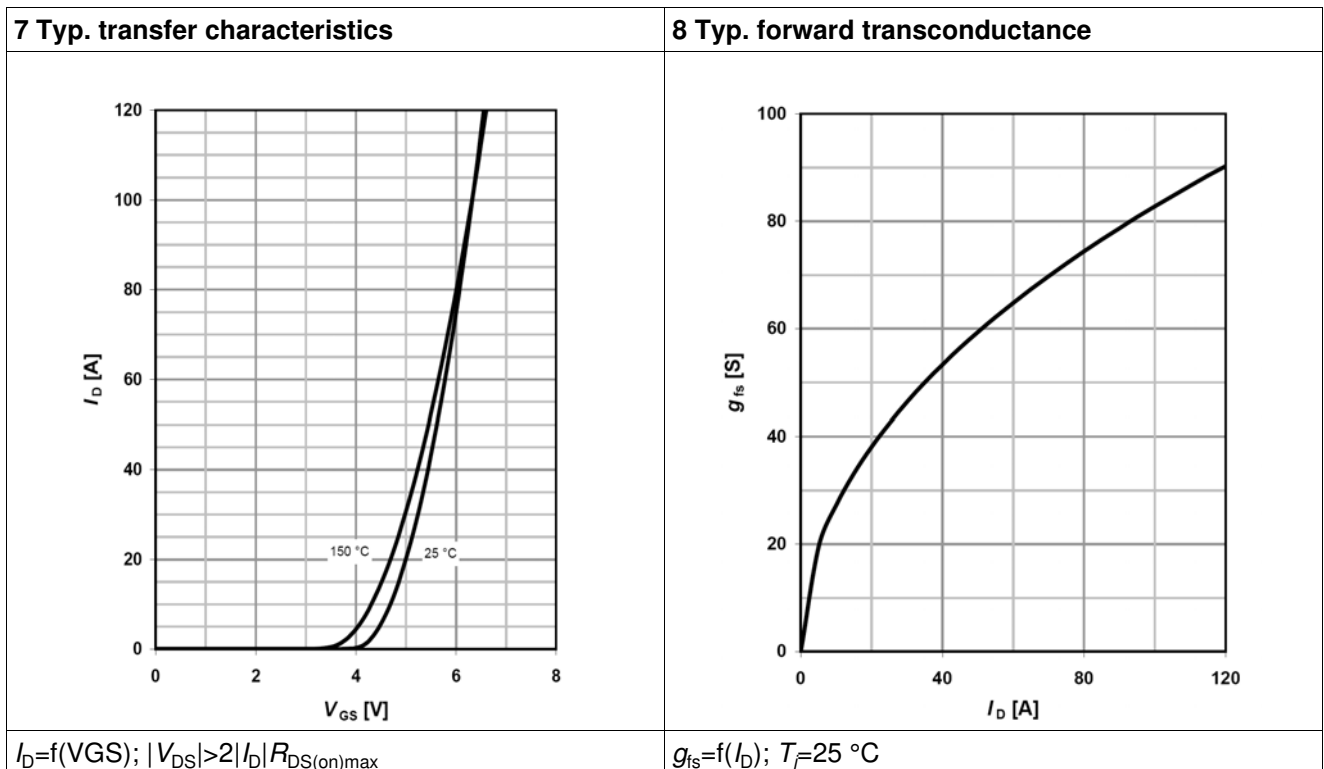


Table 12

<p><b>9 Drain-source on-state resistance</b></p> <p><math>R_{DS(on)} = f(T_j)</math>; <math>I_D = 30 \text{ A}</math>; <math>V_{GS} = 10 \text{ V}</math></p>	<p><b>10 Typ. gate threshold voltage</b></p> <p><math>V_{GS(th)} = f(T_j)</math>; <math>V_{GS} = V_{DS}</math></p>
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Table 13

<p><b>11 Typ. capacitances</b></p> <p><math>C = f(V_{DS})</math>; <math>V_{GS} = 0 \text{ V}</math>; <math>f = 1 \text{ MHz}</math></p>	<p><b>12 Forward characteristics of reverse diode</b></p> <p><math>I_F = f(V_{SD})</math>; parameter: <math>T_j</math></p>
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Table 14

13 Avalanche characteristics	14 Typ. gate charge
$I_{AS}=f(t_{AV}); R_{GS}=25 \Omega; \text{parameter: } T_{j(\text{start})}$	$V_{GS}=f(Q_{\text{gate}}); I_D=30 \text{ A pulsed}; \text{parameter: } V_{DD}$

Table 15

15 Drain-source breakdown voltage	16 Gate charge waveforms
$V_{BR(DSS)}=f(T_j); I_D=1 \text{ mA}$	

## 6 Package outlines

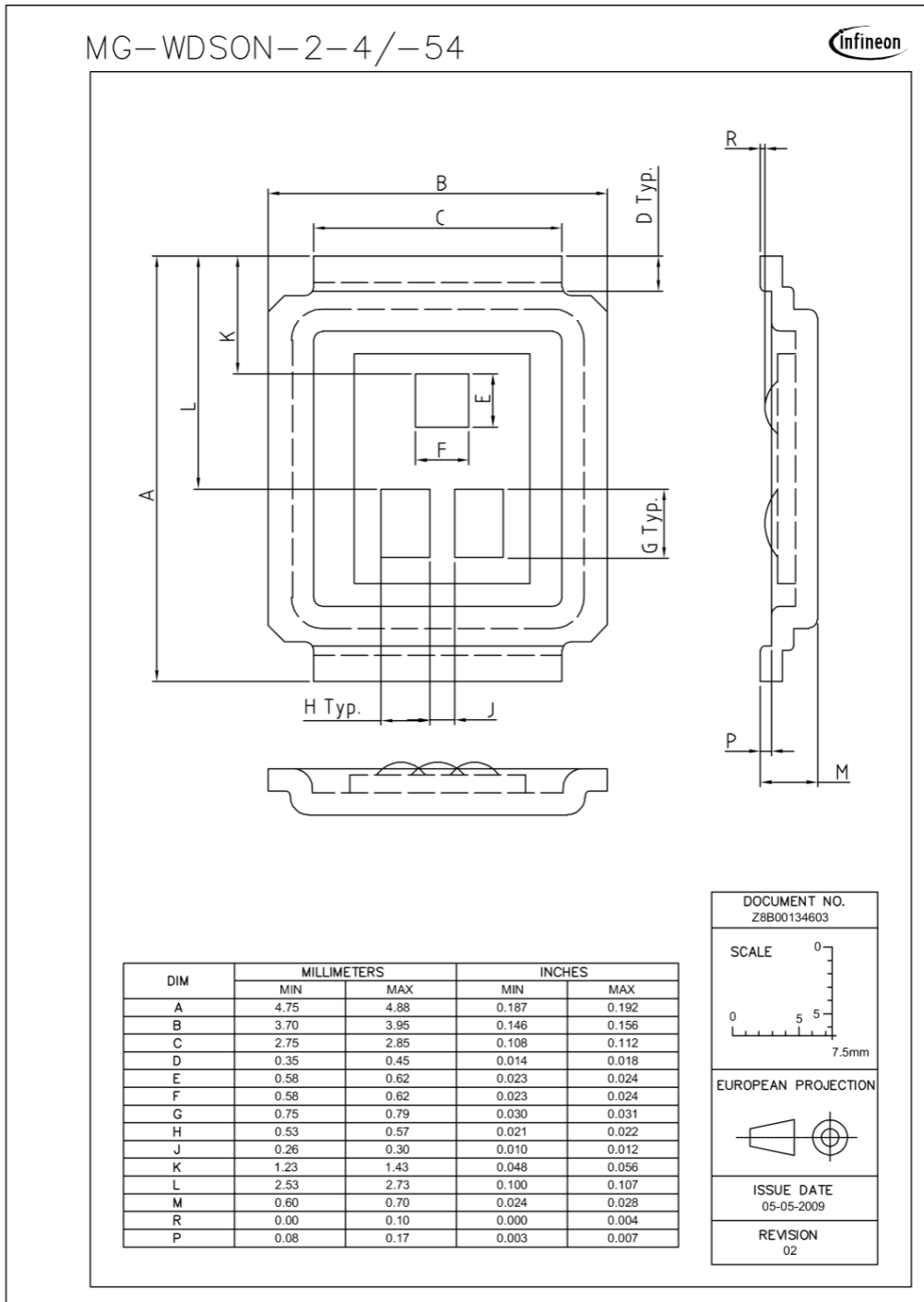


Figure 1 Outlines MG-WDSO-2, dimensions in mm/inches

7 Package outlines

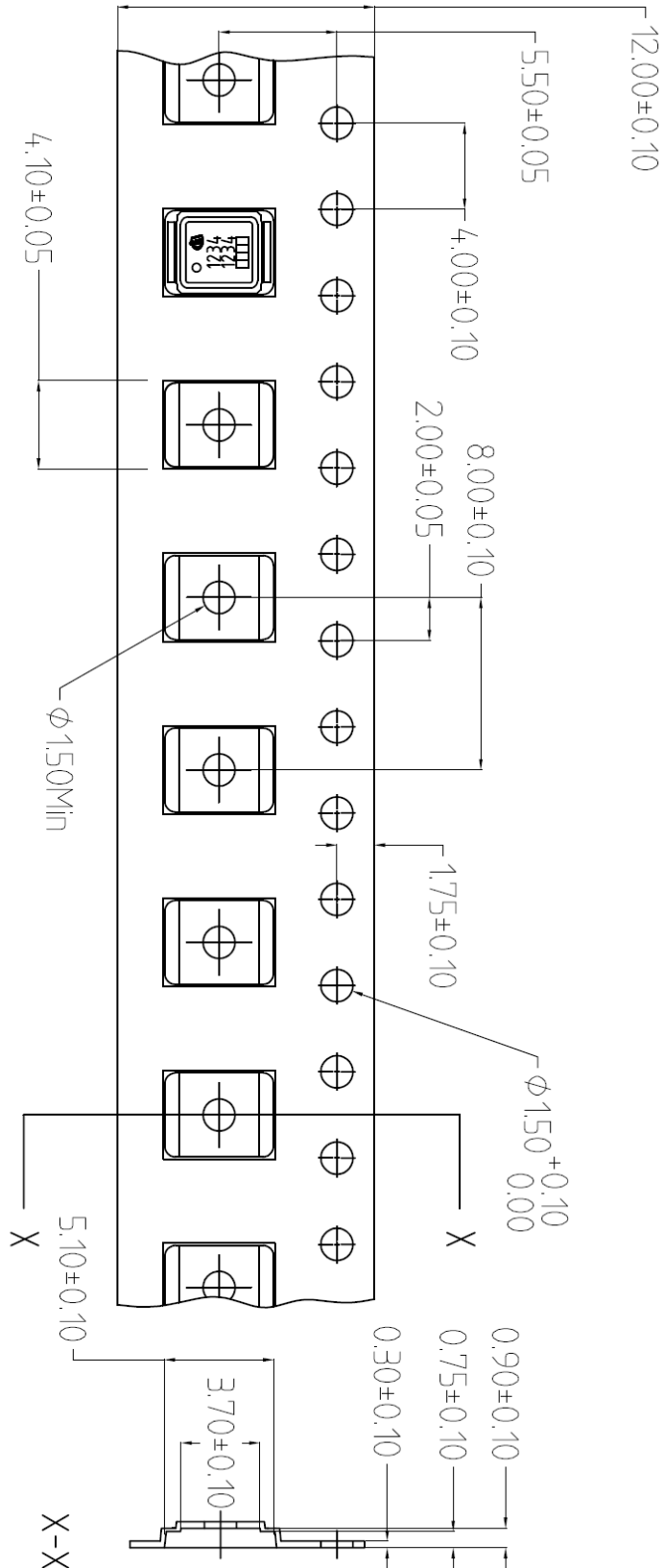
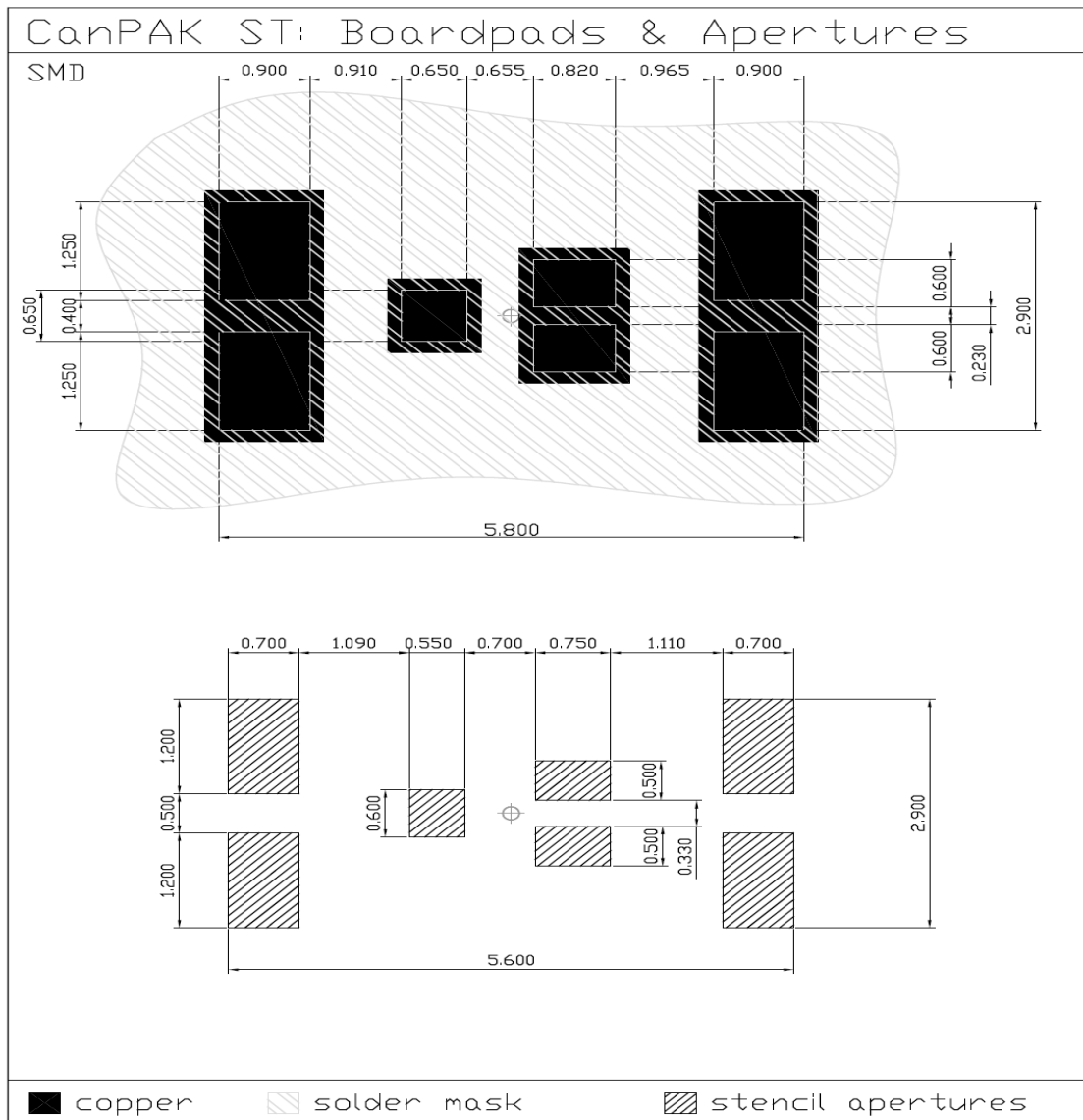
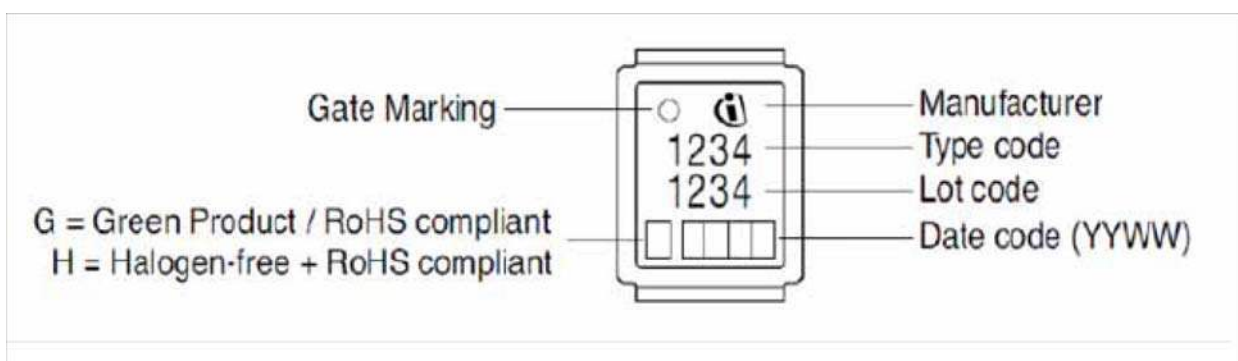


Figure 2 Outlines MG-WDSO-2, dimensions in mm/inches

## 8 Package outlines



## 9 Marking layout



## 9 Revision History

**Revision History: 2011-03-01, 1.4**

**Previous Revision:**

Revision	Subjects (major changes since last revision)
0.1	Release of target data sheet
1.0	Release Preliminary data sheet
1.3	DirectFET Disclaimer expired
1.4	Insert Marking layout

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