

**SI PMOS® Power-Transistor**
**Features**

- N-channel - Normal Level -Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Avalanche test
- Repetive Avalanche up to  $T_{jmax} = 175\text{ °C}$
- $dv/dt$  rated

**Product Summary**

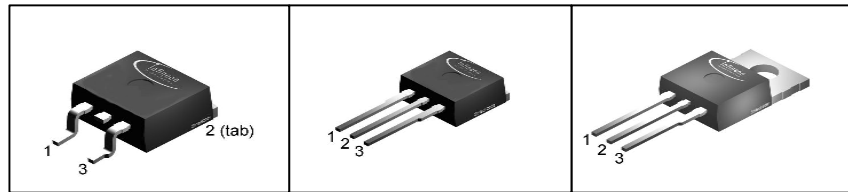
$V_{DS}$	55	V
$R_{DS(on),max}$ (SMD version)	7.7	mΩ
$I_D$	80	A

**Green Package**

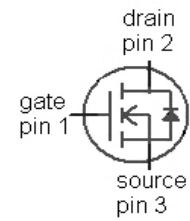
PG-TO263-3-2

PG-TO262-3-1

PG-TO220-3-1



Type	Package	Ordering Code	Marking
SPB80N06S-08	PG-TO263-3-2	SP0000-84808	1N0608
SPI80N06S-08	PG-TO262-3-1	SP0000-82518	1N0608
SPP80N06S-08	PG-TO220-3-1	SP0000-84809	1N0608


**Maximum ratings, at  $T_j=25\text{ °C}$ , unless otherwise specified**

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current <sup>1)</sup>	$I_D$	$T_C=25\text{ °C}$ , $V_{GS}=10\text{ V}$	80	A
		$T_C=100\text{ °C}$ , $V_{GS}=10\text{ V}$	80	
Pulsed drain current <sup>2)</sup>	$I_{D,pulse}$	$T_C=25\text{ °C}$	320	
Avalanche energy, single pulse	$E_{AS}$	$I_D=80\text{ A}$ , $R_{GS}=25\text{ Ω}$ , $V_{DD}=25\text{ V}$	700	mJ
Avalanche energy, periodic <sup>2)</sup>	$E_{AR}$	$T_j=175\text{ °C}$	30	
Reverse diode $dv/dt$ <sup>2)</sup>	$dv/dt$	$I_D=80\text{ A}$ , $V_{DS}=40\text{ V}$ , $di/dt=200\text{ A/μs}$ , $T_{j,max}=175\text{ °C}$	6	kV/μs
Gate source voltage	$V_{GS}$		±20	V
Power dissipation	$P_{tot}$	$T_C=25\text{ °C}$	300	W
Operating and storage temperature	$T_j$ , $T_{stg}$		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Thermal characteristics<sup>2)</sup>**

Thermal resistance, junction - case	$R_{thJC}$		-	0.38	0.5	K/W
Thermal resistance, junction - ambient, leaded	$R_{thJA}$		-	-	62	
SMD version, device on PCB	$R_{thJA}$	minimal footprint	-	-	62	
		6 cm <sup>2</sup> cooling area <sup>3)</sup>	-	-	40	

**Electrical characteristics, at  $T_j=25\text{ }^\circ\text{C}$ , unless otherwise specified**

**Static characteristics**

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	55	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=240\text{ }\mu\text{A}$	2.1	3.0	4	
Zero gate voltage drain current	$I_{DSS}$	$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ }^\circ\text{C}$	-	0.1	1	$\mu\text{A}$
		$V_{DS}=25\text{ V}, V_{GS}=0\text{ V}, T_j=150\text{ }^\circ\text{C}^{2)}$	-	10	100	
Gate-source leakage current	$I_{GSS}$	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	10	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=80\text{ A}$	-	6.5	8	m $\Omega$
		$V_{GS}=10\text{ V}, I_D=80\text{ A}$ SMD version	-	6.2	7.7	
Transconductance <sup>2)</sup>	$g_{fs}$	$ V_{DS} >2 I_D R_{DS(on)max}, I_D=80\text{ A}$	-	73	-	S

footnote on page 3

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

**Dynamic characteristics<sup>2)</sup>**

Input capacitance	$C_{iss}$	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	3660	-	pF
Output capacitance	$C_{oss}$		-	1075	-	
Reverse transfer capacitance	$C_{rss}$		-	540	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=30\text{ V}, I_D=80\text{ A},$ $V_{GS}=10\text{ V}, R_G=2.4\ \Omega$	-	22	-	ns
Rise time	$t_r$		-	53	-	
Turn-off delay time	$t_{d(off)}$		-	54	-	
Fall time	$t_f$		-	32	-	

**Gate Charge Characteristics<sup>2)</sup>**

Gate to source charge	$Q_{gs}$	$V_{DD}=44\text{ V}, I_D=80\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	19	-	nC
Gate to drain charge	$Q_{gd}$		-	62	-	
Gate charge total	$Q_g$		-	125	187	
Gate plateau voltage	$V_{plateau}$		-	5.4	-	V

**Reverse Diode<sup>2)</sup>**

Diode continuous forward current	$I_S$	$T_C=25\text{ }^\circ\text{C}$	-	-	80	A
Diode pulse current	$I_{S,pulse}$		-	-	320	
Diode forward voltage	$V_{SD}$	$V_{GS}=0\text{ V}, I_F=80\text{ A},$ $T_j=25\text{ }^\circ\text{C}$	-	0.9	1.3	V
Reverse recovery time	$t_{rr}$	$V_R=27.5\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	105	-	ns
Reverse recovery charge	$Q_{rr}$		-	30	-	

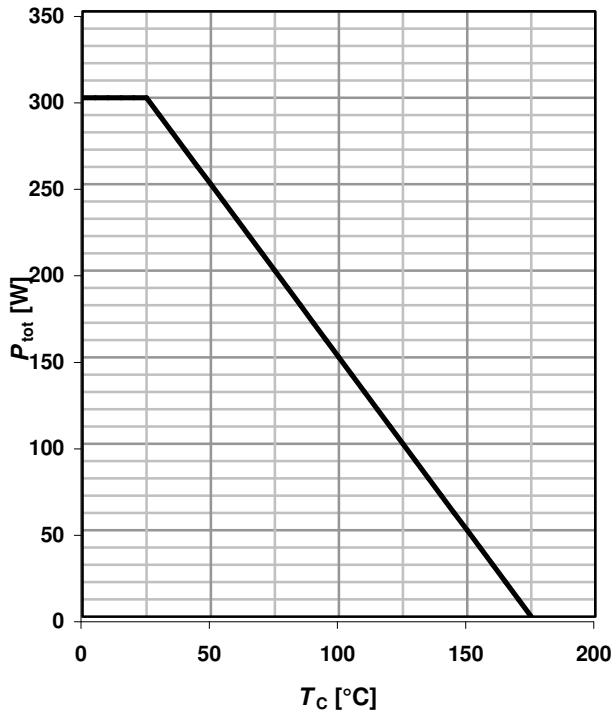
<sup>1)</sup> Current is limited by bondwire; with an  $R_{thJC}=0.5\text{ K/W}$  the chip is able to carry 132A at 25°C. For detailed information see Application Note APPS071E at [www.infineon.com/optimos](http://www.infineon.com/optimos)

<sup>2)</sup> Defined by design not subjected to production test.

<sup>3)</sup> Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm<sup>2</sup> (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

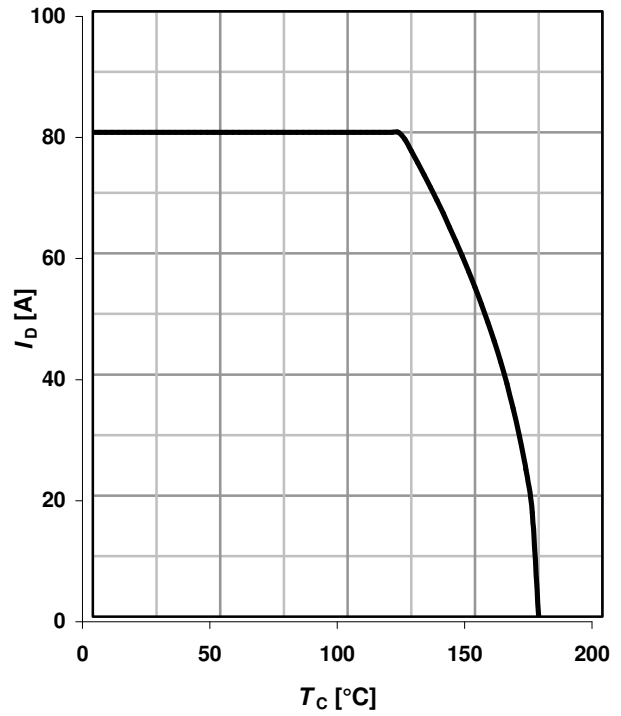
### 1 Power dissipation

$$P_{tot}=f(T_C)$$



### 2 Drain current

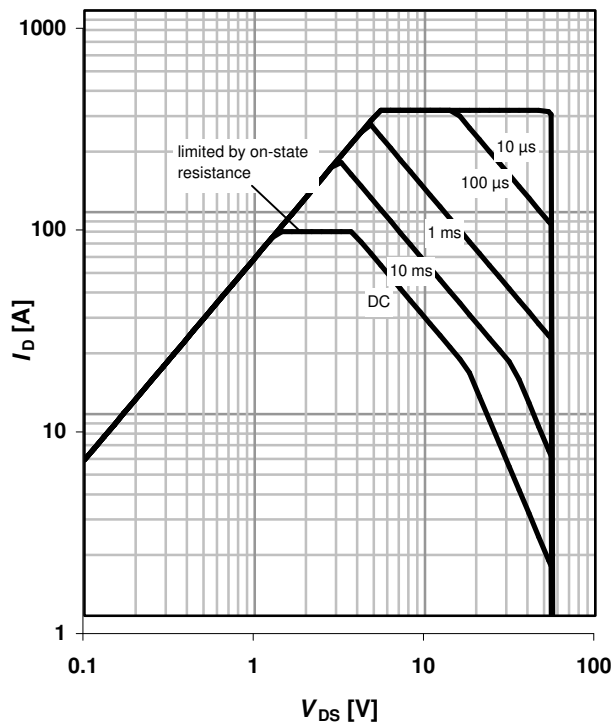
$$I_D=f(T_C); V_{GS}=10\text{ V}$$



### 3 Safe operating area

$$I_D=f(V_{DS}); T_C=25\text{ °C}; D=0$$

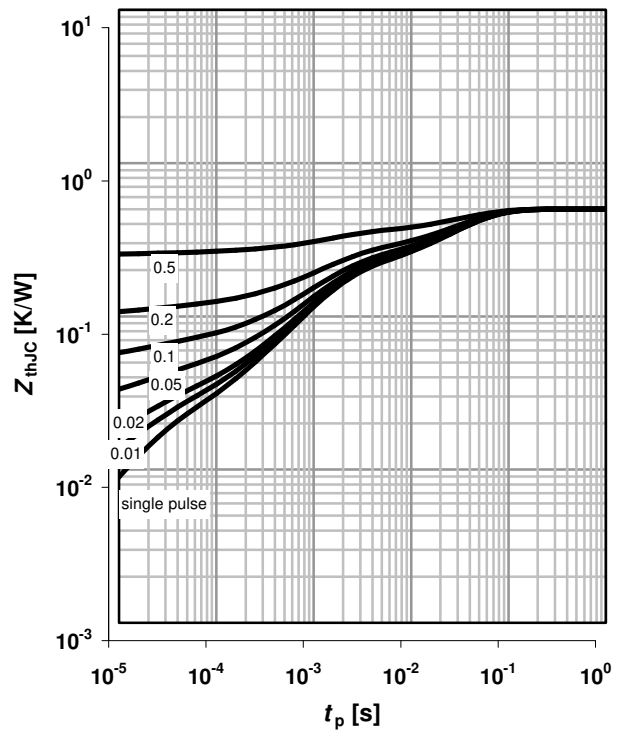
parameter:  $t_p$



### 4 Max. transient thermal impedance

$$Z_{thJC}=f(t_p)$$

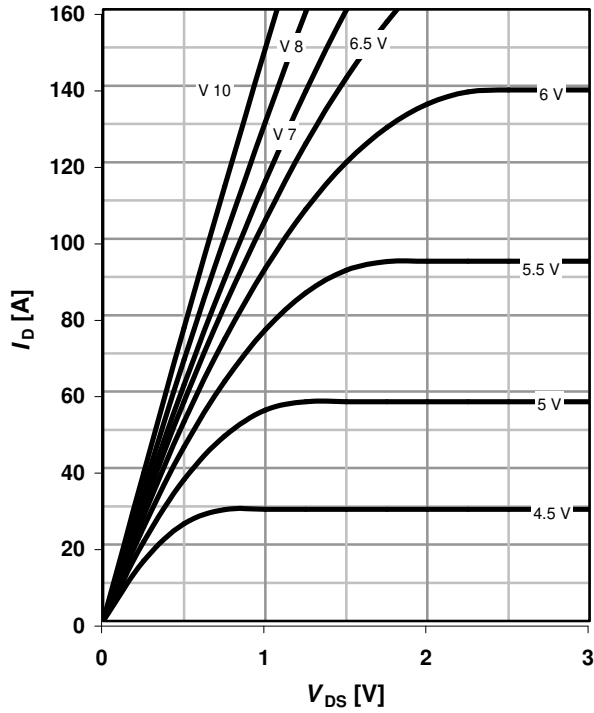
parameter:  $D=t_p/T$



**5 Typ. output characteristics**

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

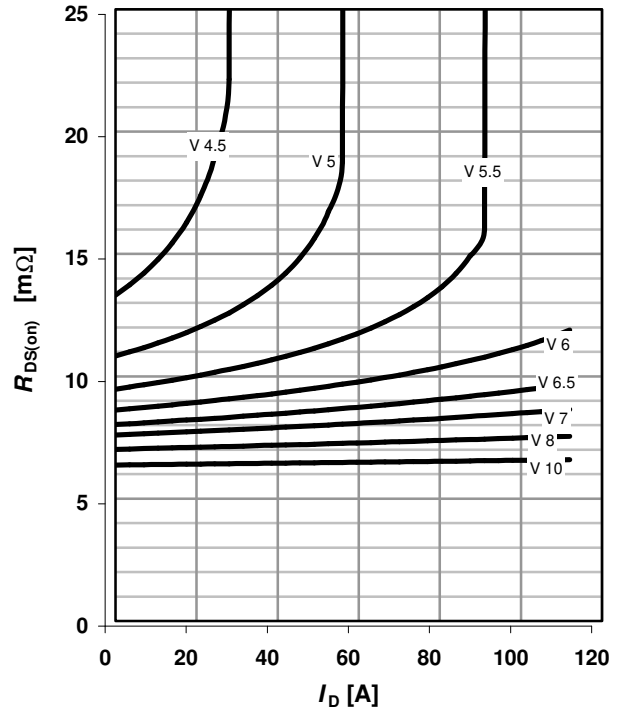
parameter:  $V_{GS}$



**6 Typ. drain-source on resistance**

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

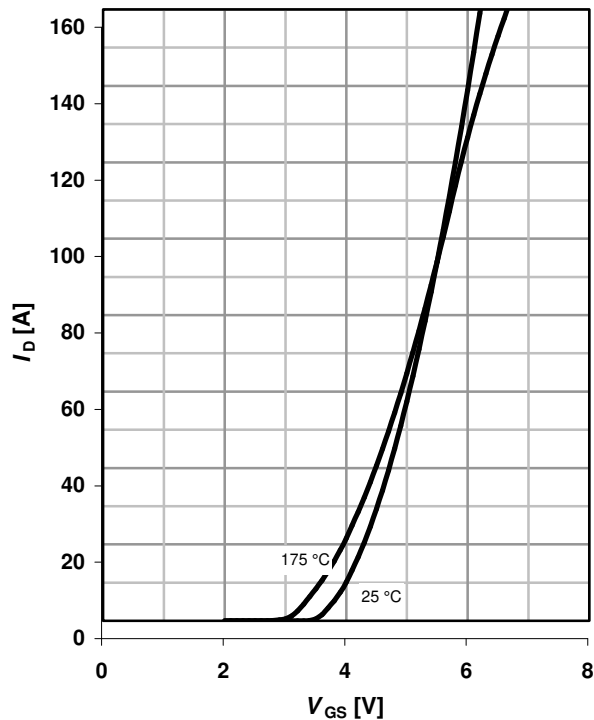
parameter:  $V_{GS}$



**7 Typ. transfer characteristics**

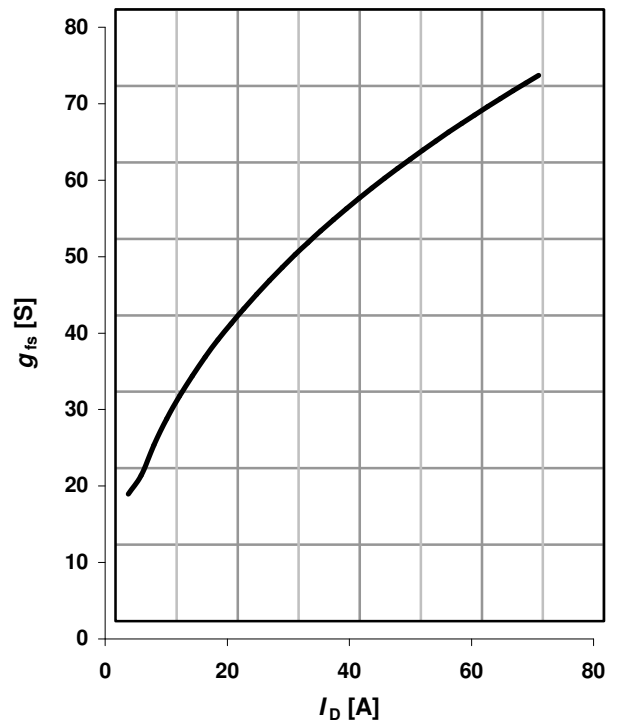
$I_D = f(V_{GS}); |V_{DS}| > 2|I_D|R_{DS(on)max}$

parameter:  $T_j$



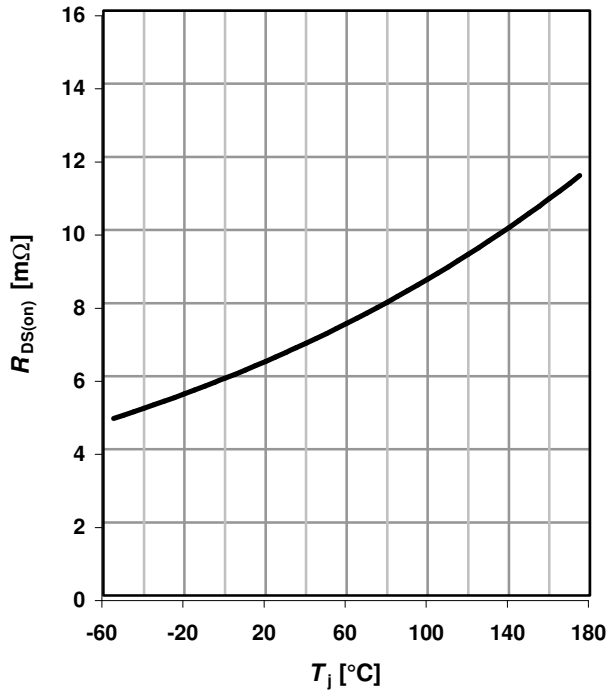
**8 Typ. forward transconductance**

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$



**9 Typical Drain-source on-state resistance**

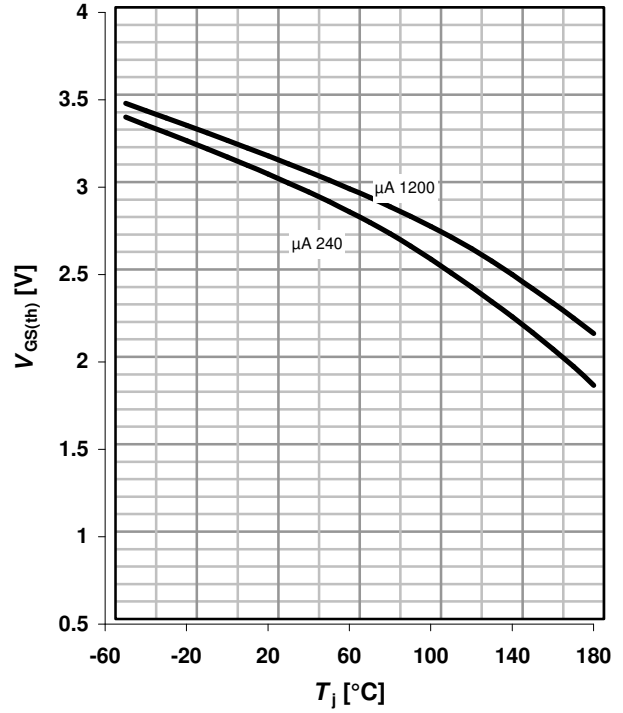
$R_{DS(on)}=f(T_j)$ ;  $I_D=80\text{ A}$ ;  $V_{GS}=10\text{ V}$



**10 Typ. gate threshold voltage**

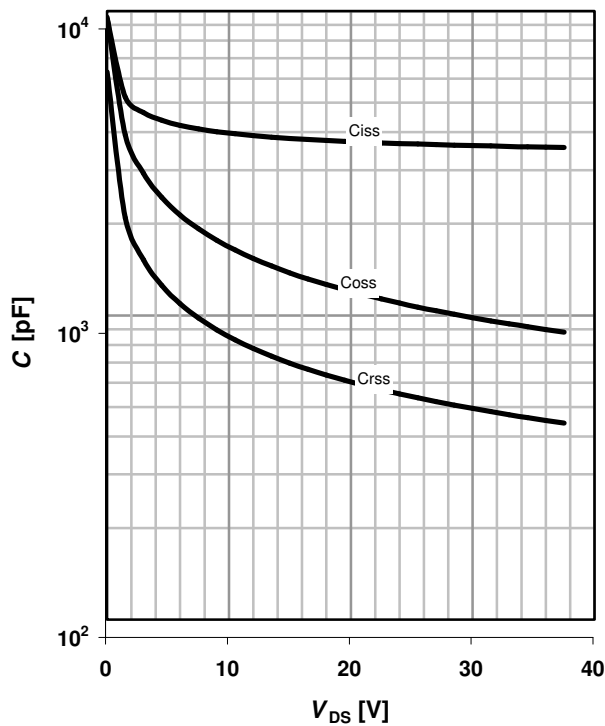
$V_{GS(th)}=f(T_j)$ ;  $V_{GS}=V_{DS}$

parameter:  $I_D$



**11 Typ. capacitances**

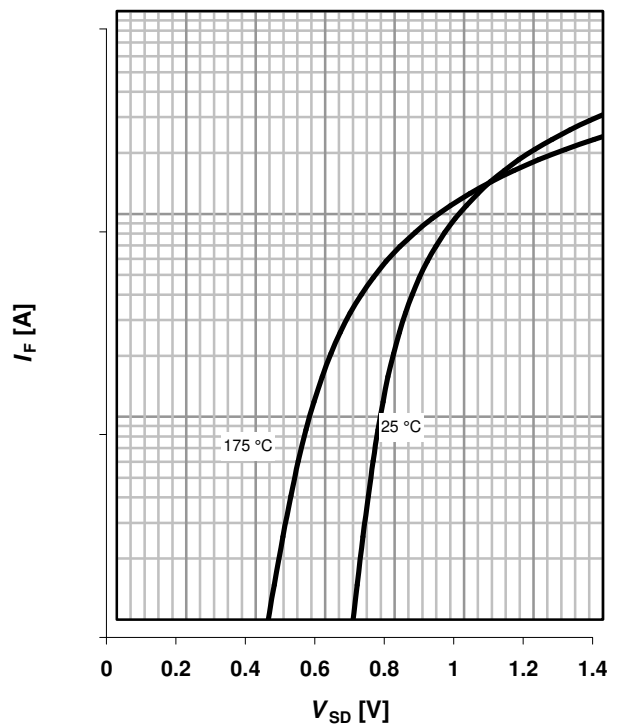
$C=f(V_{DS})$ ;  $V_{GS}=0\text{ V}$ ;  $f=1\text{ MHz}$



**12 Forward characteristics of reverse diode**

$I_F=f(V_{SD})$

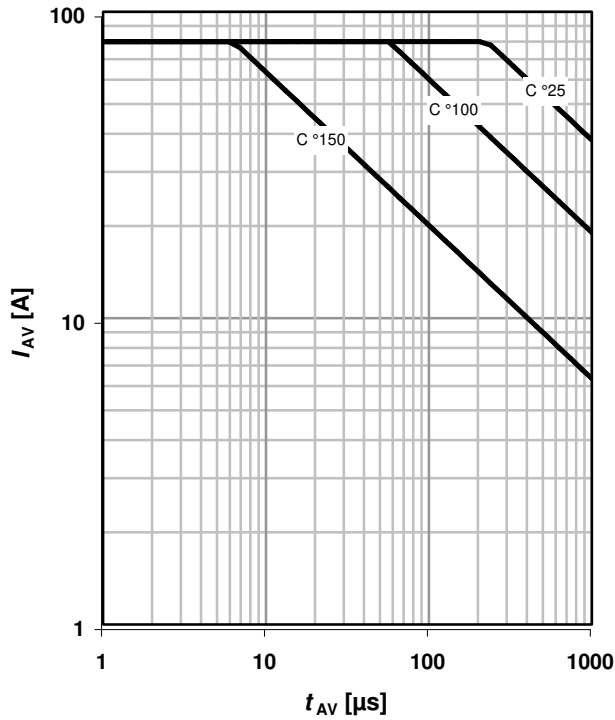
parameter:  $T_j$



**13 Typ. Avalanche characteristics**

$I_{AS}=f(t_{AV}); R_{GS}=25\ \Omega$

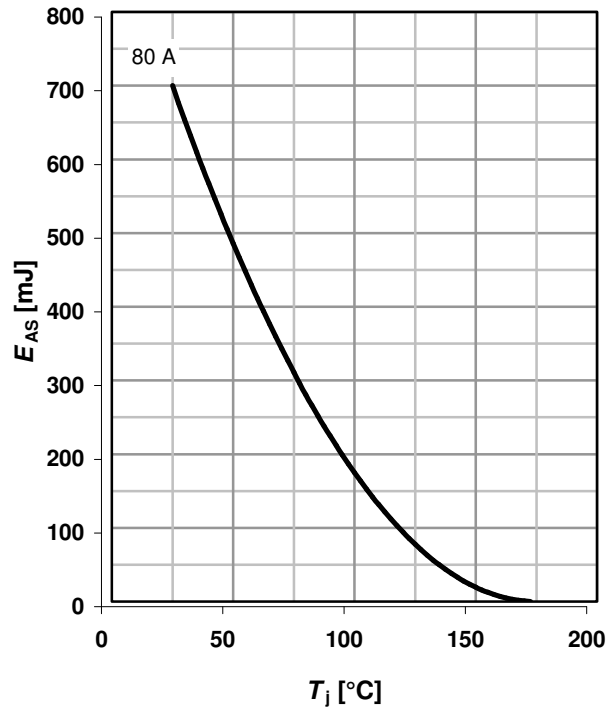
parameter:  $T_{j(\text{start})}$



**14 Typ. Avalanche Energy**

$E_{AS}=f(T_j); V_{DD} = 25\ \text{V}; R_{GS}=25\ \Omega$

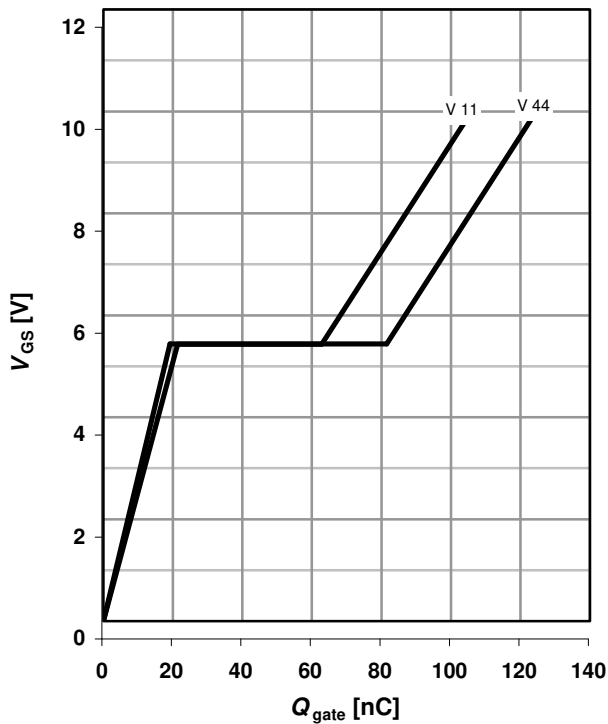
parameter:  $I_D$



**15 Typ. gate charge**

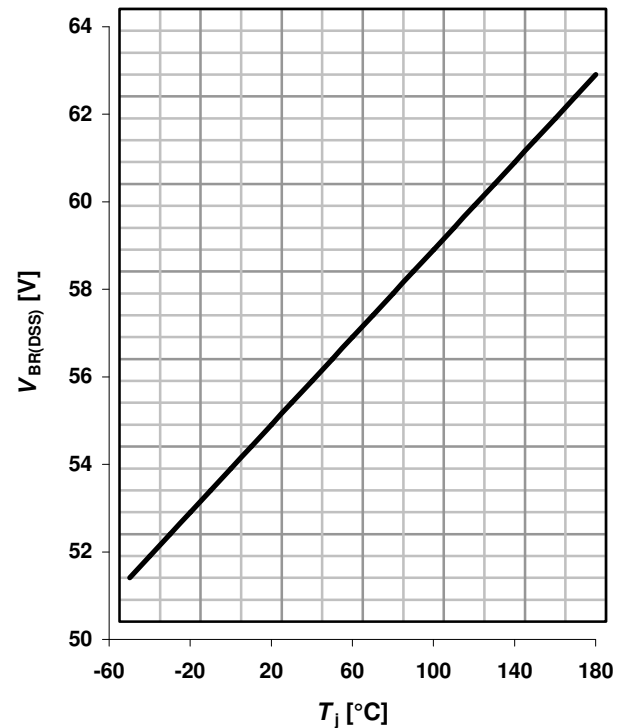
$V_{GS}=f(Q_{\text{gate}}); I_D=80\ \text{A}$  pulsed

parameter:  $V_{DD}$



**16 Drain-source breakdown voltage**

$V_{BR(DSS)}=f(T_j); I_D=250\ \mu\text{A}$





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