To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

MOS FIELD EFFECT TRANSISTOR

μPA2650T1E

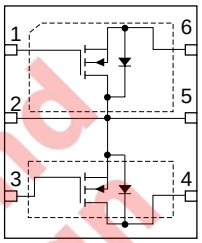
DUAL N-CHANNEL MOSFET FOR SWITCHING

DESCRIPTION

The μPA2650T1E is a switching device, which can be driven directly by a 4.5 V power source.

The μPA2650T1E contains dual MOSFET which features a low on-state resistance and excellent switching characteristics, and is suitable for applications such as DC/DC converter of portable machine and so on.

PIN CONNECTION (Top View)



1: Gate1
2: Drain1/Source2 (Heat sink2)
3: Gate2
4: Drain2 (Heat sink1)
5: Drain1/Source2 (Heat sink2)
6: Source1

FEATURES

- 4.5 V drive available MOSFET
- Low on-state resistance MOSFET

MOSFET1 $R_{DS(on)1}$ = 48 mΩ TYP. (V_{GS} = 10 V, I_D = 3.0 A)
$R_{DS(on)2}$ = 55 mΩ TYP. (V_{GS} = 4.5 V, I_D = 3.0 A)

MOSFET2 $R_{DS(on)1}$ = 50 mΩ TYP. (V_{GS} = 10 V, I_D = 3.0 A)
$R_{DS(on)2}$ = 57 mΩ TYP. (V_{GS} = 4.5 V, I_D = 3.0 A)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA2650T1E	6LD3x3MLP

Marking: A2650

Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Caution This product is electrostatic-sensitive device due to low ESD capability and should be handled with caution for electrostatic discharge.

V_{ESD} = ±150 V TYP. (C = 200 pF, R = 0 Ω, Single Pulse)

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Printed in Japan

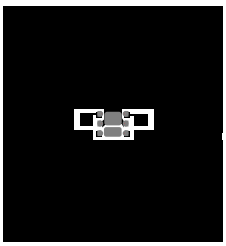
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

MOSFET1, MOSFET2

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	20	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±12	V
Drain Current (DC) Note1	$I_{D(DC)}$	±3.8	A
Drain Current (pulse) Note2	$I_{D(pulse)}$	±15.2	A
Total Power Dissipation Note1	P_T	1.1	W
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	–55 to +150	°C

Notes 1. Mounted on a 1 in^2 pad of 2 oz copper, 1.5" x 1.5" x 0.062" thick FR-4 board
(Cu pad: 322 mm^2 x 70 μm, FR-4: 1452 mm^2 x 1.6 mmt)

2. PW ≤ 10 μs, Duty Cycle ≤ 1%



FET side: 97°C/W when mounted on a 1 in^2 pad of 2 oz copper

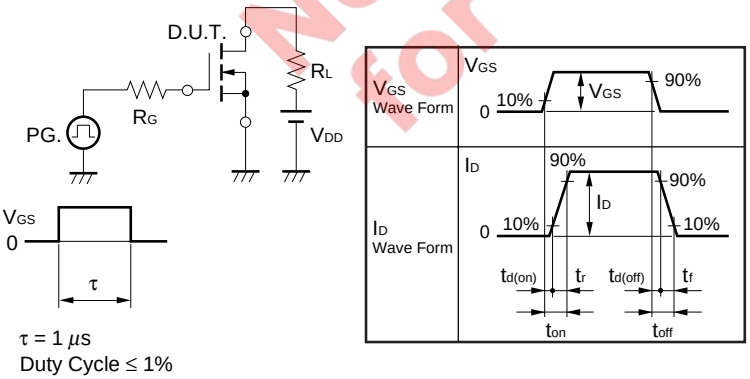
ELECTRICAL CHARACTERISTICS (T_A = 25°C)

MOSFET1, MOSFET2

CHARACTERISTICS	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 20 V, V_{GS} = 0 V				1	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±12 V, V_{DS} = 0 V				±10	μA
Gate to Source Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 0.25 mA		0.6		2.0	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 1.5 A		1.0	3.6		S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 3.0 A	MOSFET1		48	65	mΩ
			MOSFET2		50	65	mΩ
	$R_{DS(on)2}$	V_{GS} = 4.5 V, I_D = 3.0 A	MOSFET1		55	75	mΩ
			MOSFET2		57	75	mΩ
Input Capacitance	C_{iss}	V_{DS} = 10 V,			220		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,			100		pF
Reverse Transfer Capacitance	C_{rss}	f = 1.0 MHz			40		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 10 V, I_D = 1.5 A,			8.4		ns
Rise Time	t_r	V_{GS} = 4.5 V,			7.3		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω			15		ns
Fall Time	t_f				3.4		ns
Total Gate Charge	Q_G	V_{DD} = 16 V,			2.9		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 4.5 V,			0.6		nC
Gate to Drain Charge	Q_{GD}	I_D = 3.0 A			1.0		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = 3.0 A, V_{GS} = 0 V			0.89		V

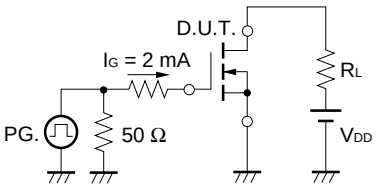
Note Pulsed: PW ≤ 350 μs, Duty Cycle ≤ 2%

TEST CIRCUIT 1 SWITCHING TIME



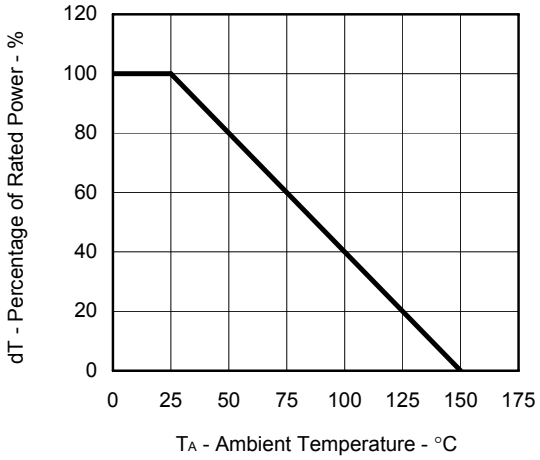
τ = 1 μs
Duty Cycle ≤ 1%

TEST CIRCUIT 2 GATE CHARGE

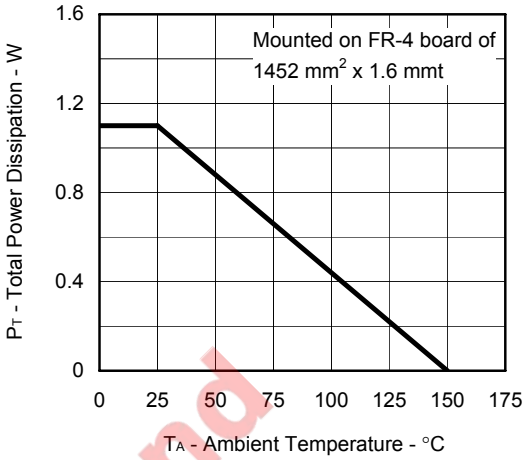


MOSFET TYPICAL CHARACTERISTICS (T_A = 25°C)

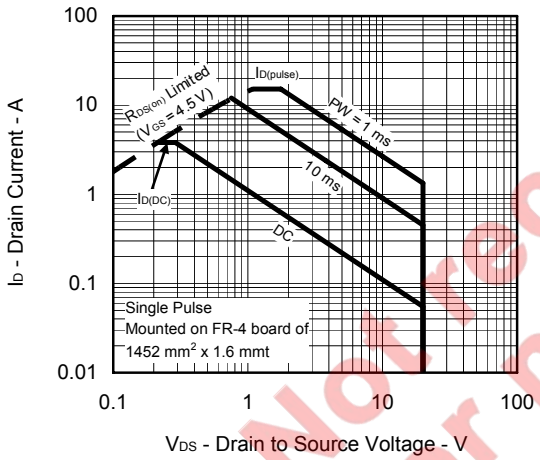
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



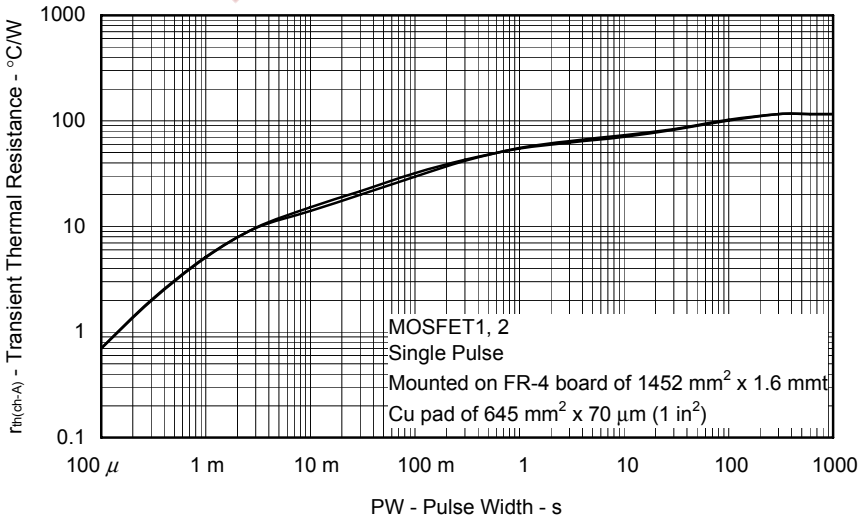
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



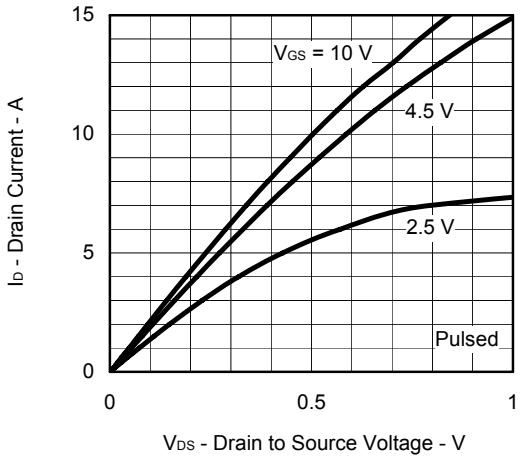
FORWARD BIAS SAFE OPERATING AREA



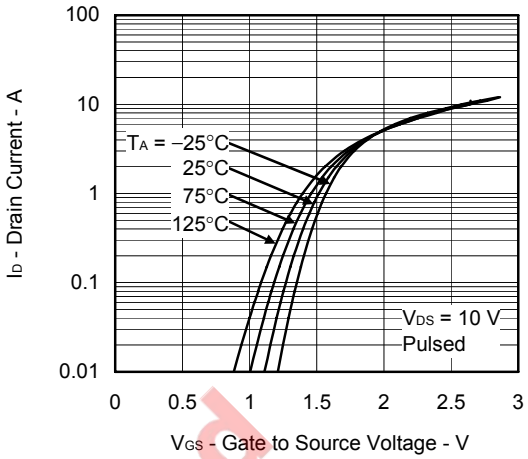
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



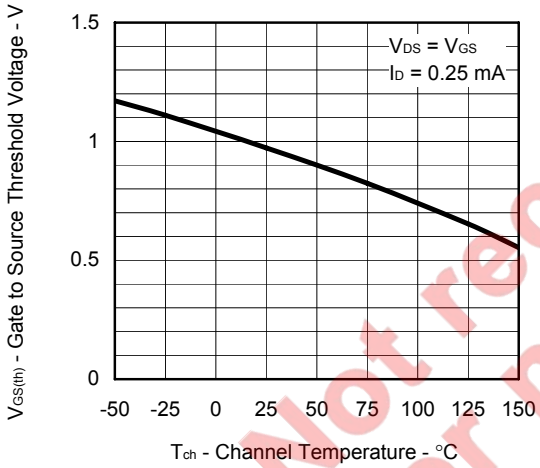
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



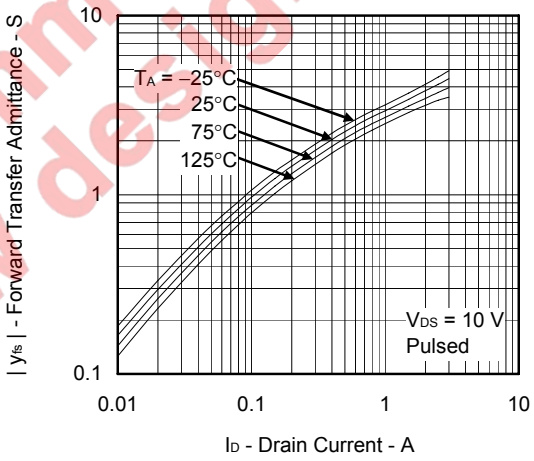
FORWARD TRANSFER CHARACTERISTICS



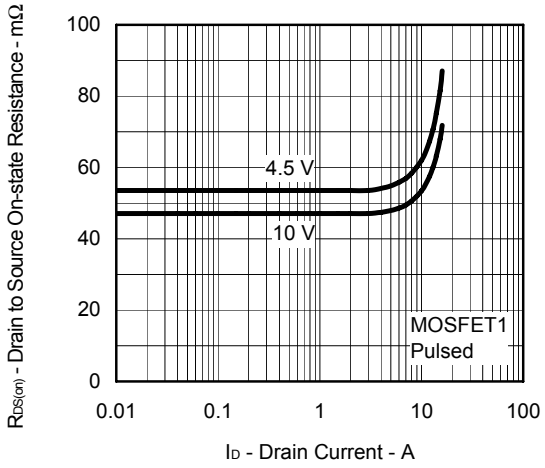
GATE TO SOURCE THRESHOLD VOLTAGE vs.
CHANNEL TEMPERATURE



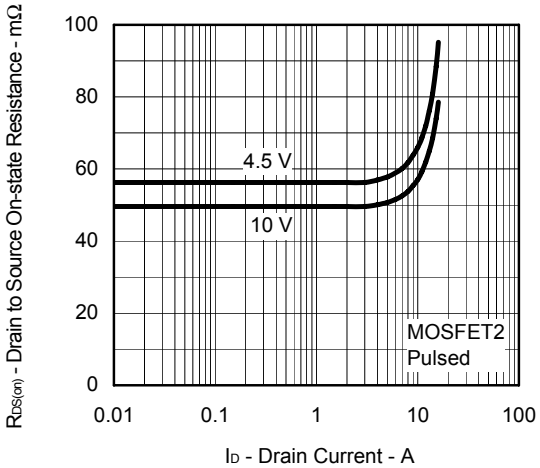
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



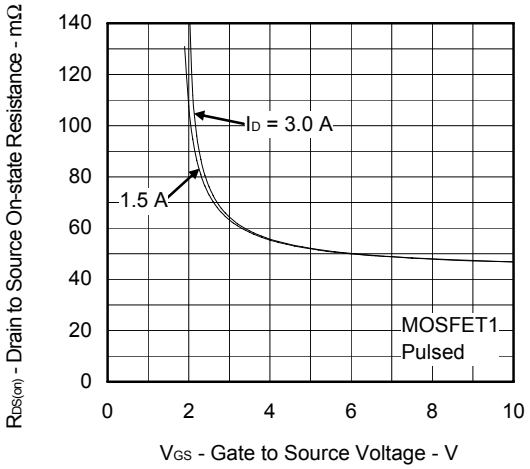
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



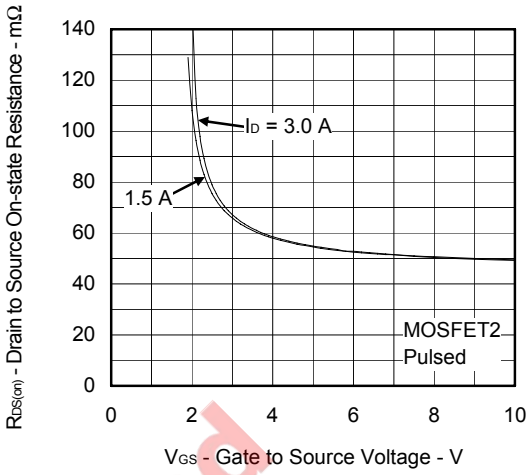
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



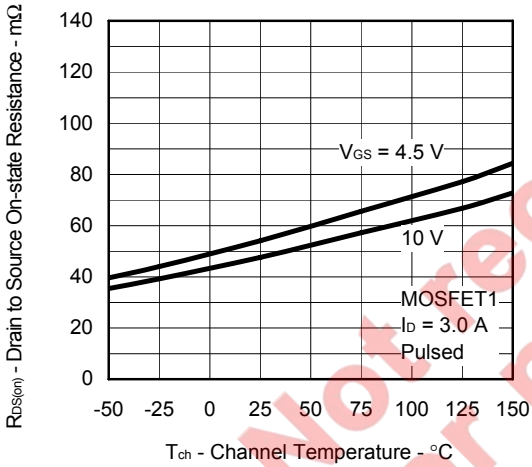
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



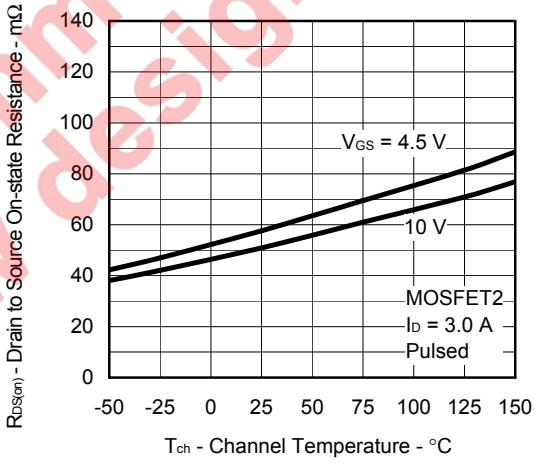
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



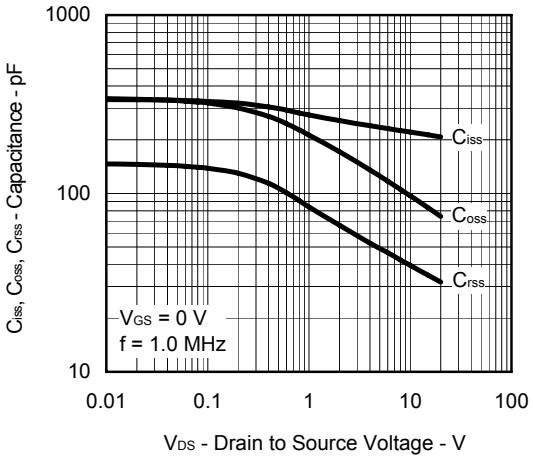
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



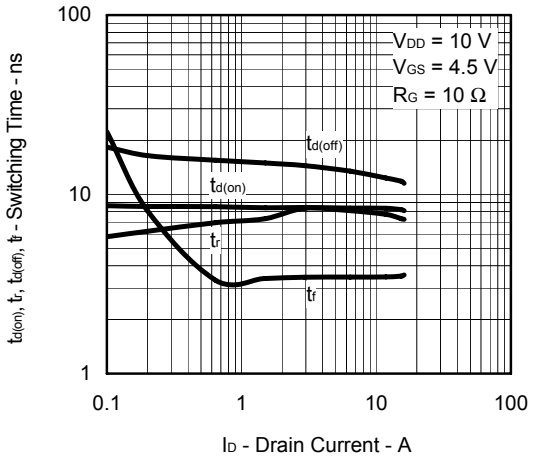
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



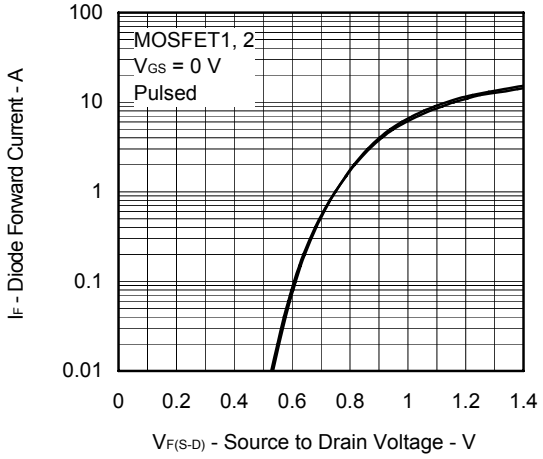
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



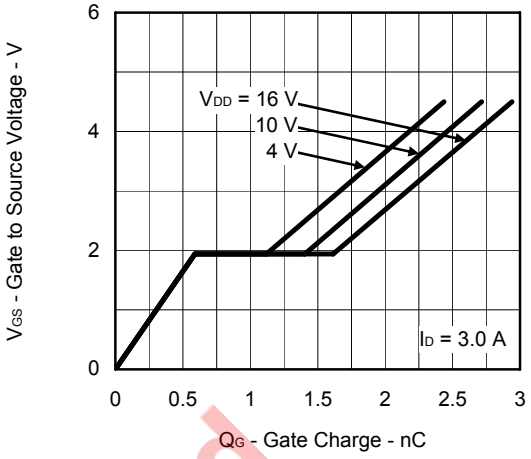
SWITCHING CHARACTERISTICS



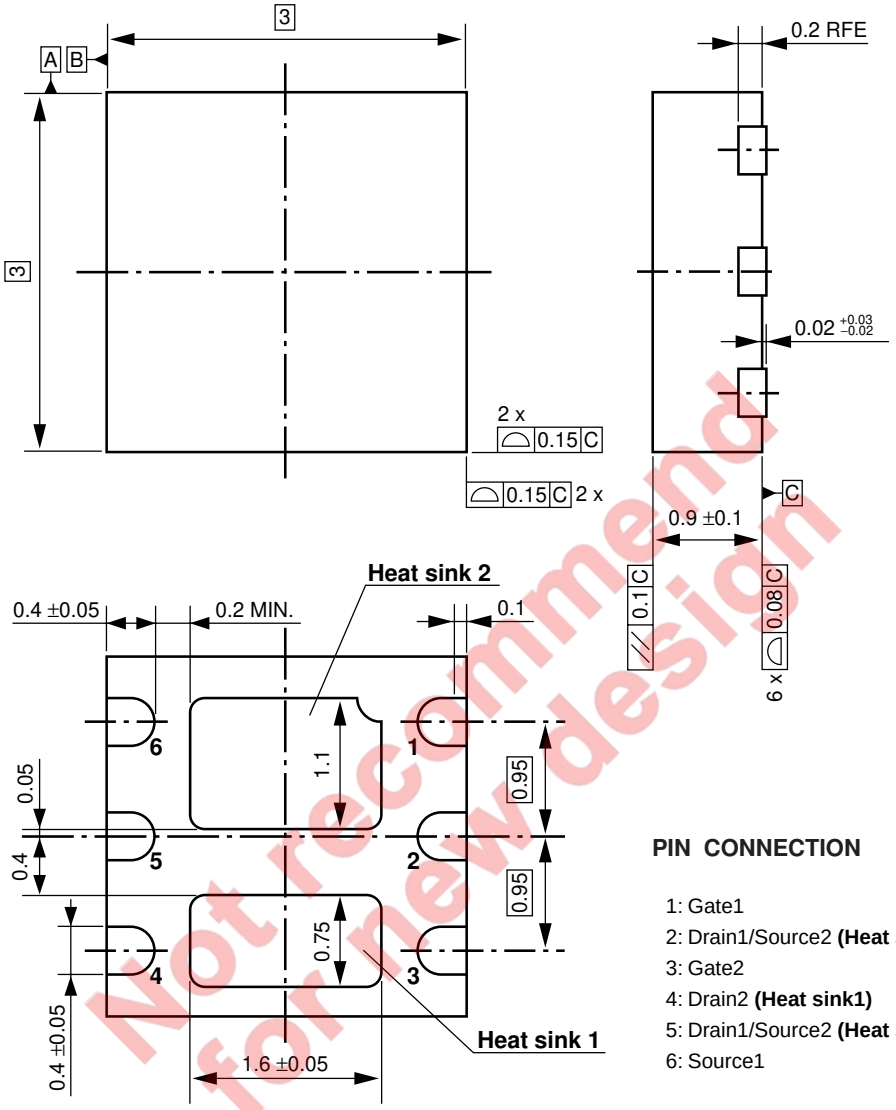
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



DYNAMIC INPUT CHARACTERISTICS



PACKAGE DRAWING (Unit: mm)



PIN CONNECTION

1: Gate1
2: Drain1/Source2 **(Heat sink2)**
3: Gate2
4: Drain2 **(Heat sink1)**
5: Drain1/Source2 **(Heat sink2)**
6: Source1

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