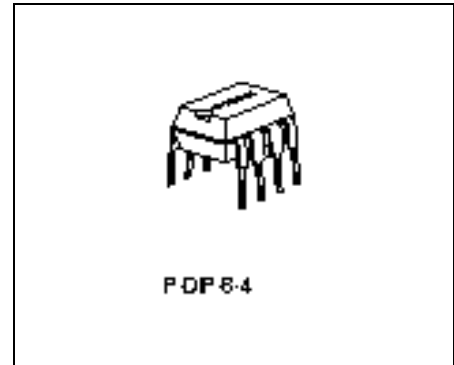


# 1 Overview

## 1.1 Features

- Optimized for headlight beam control applications
- Delivers up to 0.8 A
- Low saturation voltage;  
typ. 1.2 V total @ 25 °C; 0.4 A
- Output protected against short circuit
- Overtemperature protection with hysteresis
- Over- and undervoltage lockout
- No crossover current
- Internal clamp diodes



## 1.2 Description

The TLE 4209 is a fully protected H-Bridge Driver designed specifically for automotive headlight beam control and industrial servo control applications.

The part is built using Infineons bipolar high voltage power technology DOPL.

The device is available in a P-DIP-8-4 package.

The servo-loop-parameter pos.- and neg. Hysteresis, pos.- and neg. deadband and angle-amplification are programmable with external resistors.

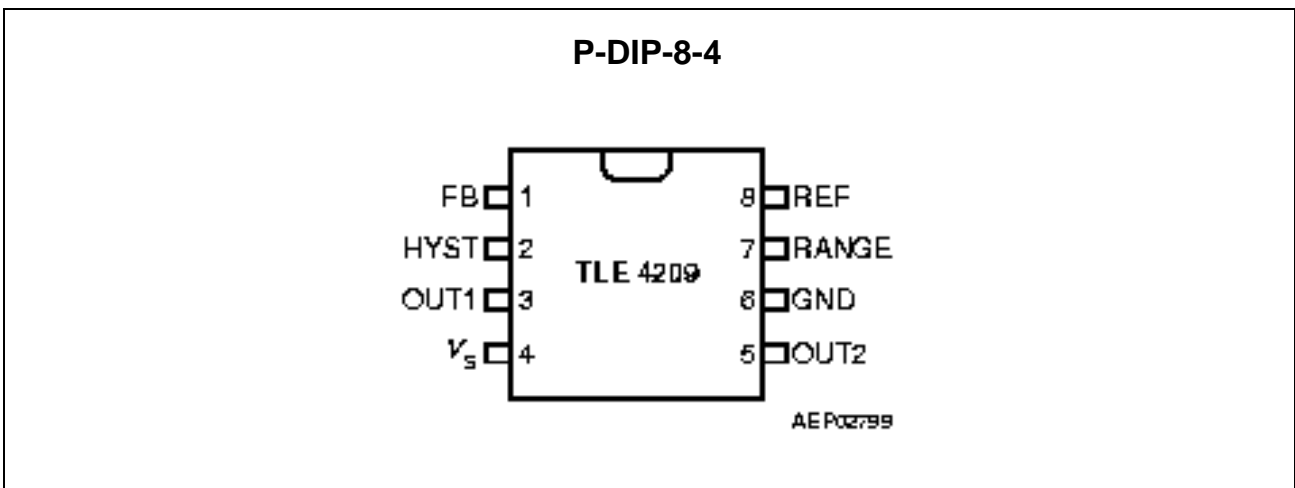
An internal window-comparator controls the input line. In the case of a fault condition, like short circuit to GND, short circuit to supply-voltage, and broken wire, the TLE 4209 stops the motor immediately (brake condition).

Furthermore the built in features like over- and undervoltage-lockout, short-circuit-protection and over-temperature-protection will open a wide range of automotive- and industrial applications.

Type	Package
TLE 4209	P-DIP-8-4

### 1.3 Pin Definitions and Functions

Pin No.	Symbol	Function
<b>P-DIP-8-4</b>		
1	FB	Feedback Input
2	HYST	Hysteresis I/O
3	OUT1	Power Output 1
4	$V_S$	Power Supply Voltage
5	OUT2	Power Output 2
6	GND	Ground
7	RANGE	Range Input
8	REF	Reference Input



**Figure 1** Pin Configuration (top view)

1.4 Functional Block Diagram

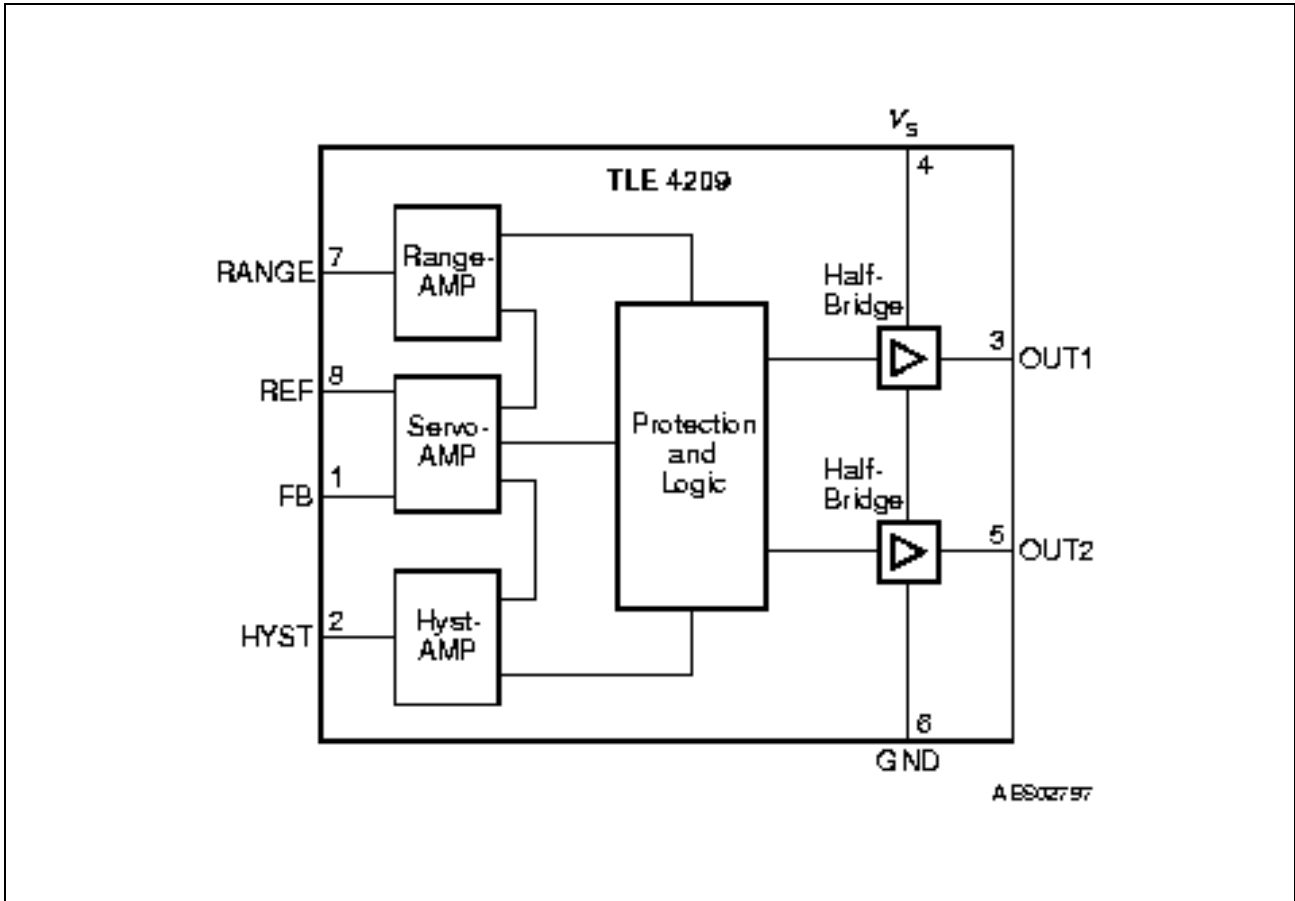


Figure 2 Block Diagram

### 1.5 Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		

#### Voltages

Supply voltage	$V_S$	- 0.3	45	V	-
Supply voltage	$V_S$	- 1	-	V	$t < 0.5 \text{ s}; I_S > - 2 \text{ A}$
Logic input voltages (FB, REF, RANGE, HYST)	$V_I$	- 0.3	20	V	-

#### Currents

Output current (OUT1, OUT2)	$I_{OUT}$	-	-	A	internally limited
Output current (Diode)	$I_{OUT}$	- 1	1	A	-
Input current (FB, REF, RANGE, HYST)	$I_{IN}$	- 2	2	mA	$t < 2 \text{ ms}; t/T < 0.1$
		- 6	6	mA	

#### Temperatures

Junction temperature	$T_j$	- 40	150	°C	-
Storage temperature	$T_{stg}$	- 50	150	°C	-

#### Thermal Resistances

Junction ambient (P-DIP-8-4)	$R_{thjA}$		100	K/W	-
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*Note: Stresses above those listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

**1.6 Operating Range**

Parameter	Symbol	Limit Values		Unit	Remarks
		min.	max.		
Supply voltage	$V_S$	8	18	V	After $V_S$ rising above $V_{UV\ ON}$
Supply voltage increasing	$V_S$	- 0.3	$V_{UV\ ON}$	V	Outputs in tristate
Supply voltage decreasing	$V_S$	- 0.3	$V_{UV\ OFF}$	V	Outputs in tristate
Output current	$I_{OUT1-2}$	- 0.8	0.8	A	-
Input current (FB, REF)	$I_{IN}$	- 50	500	$\mu A$	-
Junction temperature	$T_j$	- 40	150	$^{\circ}C$	-

Note: In the operating range, the functions given in the circuit description are fulfilled.

**1.7 Electrical Characteristics**

$8\ V < V_S < 18\ V$ ;  $I_{OUT1-2} = 0\ A$ ;  $- 40\ ^{\circ}C < T_j < 150\ ^{\circ}C$  (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Current Consumption**

Supply current	$I_S$	-	12	20	mA	-
Supply current	$I_S$	-	20	30	mA	$I_{OUT1} = 0.4\ A$ $I_{OUT2} = - 0.4\ A$
Supply current	$I_S$	-	30	50	mA	$I_{OUT1} = 0.8\ A$ $I_{OUT2} = - 0.8\ A$

**Over- and Under Voltage Lockout**

UV Switch ON voltage	$V_{UV\ ON}$	-	7.4	8	V	$V_S$ increasing
UV Switch OFF voltage	$V_{UV\ OFF}$	6.3	6.9	-	V	$V_S$ decreasing
UV ON/OFF Hysteresis	$V_{UVHY}$	-	0.5	-	V	$V_{UV\ ON} - V_{UV\ OFF}$
OV Switch OFF voltage	$V_{OV\ OFF}$	-	20.5	23	V	$V_S$ increasing
OV Switch ON voltage	$V_{OV\ ON}$	17.5	20	-	V	$V_S$ decreasing
OV ON/OFF Hysteresis	$V_{OVHY}$	-	0.5	-	V	$V_{OV\ OFF} - V_{OV\ ON}$

**1.7 Electrical Characteristics (cont'd)**
 $8\text{ V} < V_S < 18\text{ V}; I_{\text{OUT}1-2} = 0\text{ A}; -40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$  (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Outputs OUT1-2**
**Saturation Voltages**

Source (upper) $I_{\text{OUT}} = -0.2\text{ A}$	$V_{\text{SAT U}}$	–	0.85	1.15	V	$T_j = 25\text{ }^\circ\text{C}$
Source (upper) $I_{\text{OUT}} = -0.4\text{ A}$	$V_{\text{SAT U}}$	–	0.90	1.20	V	$T_j = 25\text{ }^\circ\text{C}$
Sink (upper) $I_{\text{OUT}} = -0.8\text{ A}$	$V_{\text{SAT U}}$	–	1.10	1.50	V	$T_j = 25\text{ }^\circ\text{C}$
Sink (lower) $I_{\text{OUT}} = 0.2\text{ A}$	$V_{\text{SAT L}}$	–	0.15	0.23	V	$T_j = 25\text{ }^\circ\text{C}$
Sink (lower) $I_{\text{OUT}} = 0.4\text{ A}$	$V_{\text{SAT L}}$	–	0.25	0.40	V	$T_j = 25\text{ }^\circ\text{C}$
Sink (lower) $I_{\text{OUT}} = 0.8\text{ A}$	$V_{\text{SAT L}}$	–	0.45	0.75	V	$T_j = 25\text{ }^\circ\text{C}$

Total drop $I_{\text{OUT}} = 0.2\text{ A}$	$V_{\text{SAT}}$	–	1.0	1.4	V	$V_{\text{SAT}} = V_{\text{SAT U}} + V_{\text{SAT L}}$
Total drop $I_{\text{OUT}} = 0.4\text{ A}$	$V_{\text{SAT}}$	–	1.2	1.7	V	$V_{\text{SAT}} = V_{\text{SAT U}} + V_{\text{SAT L}}$
Total drop $I_{\text{OUT}} = 0.8\text{ A}$	$V_{\text{SAT}}$	–	1.6	2.5	V	$V_{\text{SAT}} = V_{\text{SAT U}} + V_{\text{SAT L}}$

**Clamp Diodes**

Forward voltage; upper	$V_{\text{FU}}$	–	1.0	1.5	V	$I_F = 0.4\text{ A}$
Upper leakage current	$I_{\text{LKU}}$	–		5	mA	$I_F = 0.4\text{ A}$
Forward voltage; lower	$V_{\text{FL}}$	–	0.9	1.4	V	$I_F = 0.4\text{ A}$

**1.7 Electrical Characteristics (cont'd)**
 $8\text{ V} < V_S < 18\text{ V}; I_{\text{OUT}1-2} = 0\text{ A}; -40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$  (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		

**Input-Interface**
**Input REF**

Quiescent voltage	$V_{\text{REF}q}$	–	200	240	mV	$I_{\text{REF}} = 0\text{ }\mu\text{A}$
Input resistance	$R_{\text{REF}}$	4.5	6.0	7.5	k $\Omega$	$0\text{ V} < V_{\text{REF}} < 0.5\text{ V}$

**Input FB**

Quiescent voltage	$V_{\text{FB}q}$	–	200	240	mV	$I_{\text{FB}} = 0\text{ }\mu\text{A}$
Input resistance	$R_{\text{FB}}$	4.5	6.0	7.5	k $\Omega$	$0\text{ V} < V_{\text{FB}} < 0.5\text{ V}$

**Input/Output HYST**

Current Offset	$I_{\text{HYSTIO}250}$	– 2	0.35	3	$\mu\text{A}$	$I_{\text{REF}} = I_{\text{FB}} = 250\text{ }\mu\text{A}$ $V_{\text{HYST}} = V_S / 2$
	$I_{\text{HYSTIO}40}$	– 1.3	0	1.3	$\mu\text{A}$	$I_{\text{REF}} = I_{\text{FB}} = 40\text{ }\mu\text{A}$ $V_{\text{HYST}} = V_S / 2$
Current Amplification $A_{\text{HYST}} = I_{\text{HYST}} / (I_{\text{REF}} - I_{\text{FB}})$	$A_{\text{HYST}}$	0.8	0.95	1.1	–	$-20\text{ }\mu\text{A} < I_{\text{HYST}} < -10\text{ }\mu\text{A};$ $10\text{ }\mu\text{A} < I_{\text{HYST}} < 20\text{ }\mu\text{A};$ $I_{\text{REF}} = 250\text{ }\mu\text{A}$ $V_{\text{HYST}} = V_S / 2$
Current Gain $G_{\text{HYST}} = (I_{\text{HYST}} - I_{\text{HYSTIO}40}) / (I_{\text{REF}} - I_{\text{FB}})$	$G_{\text{HYST}}$	0.8	0.95	1.1	–	$I_{\text{HYST}} = \pm 2\text{ }\mu\text{A};$ $I_{\text{REF}} = 40\text{ }\mu\text{A};$ $V_{\text{HYST}} = V_S / 2$
Threshold voltage High	$V_{\text{HYH}} / V_S$	51	52	54	%	–
Deadband voltage High	$V_{\text{DBH}} / V_S$	50	50.4	51	%	–

**1.7 Electrical Characteristics (cont'd)**
 $8\text{ V} < V_S < 18\text{ V}; I_{\text{OUT}1-2} = 0\text{ A}; -40\text{ }^\circ\text{C} < T_j < 150\text{ }^\circ\text{C}$  (unless otherwise specified)

Parameter	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Deadband voltage Low	$V_{\text{DBL}} / V_S$	49	49.6	50	%	–
Threshold voltage Low	$V_{\text{HYL}} / V_S$	46	48	49	%	–
Hysteresis Window	$V_{\text{HYW}} / V_S$	3.0	4.0	5.0	%	$(V_{\text{HYH}} - V_{\text{HYL}}) / V_S$
Deadband Window	$V_{\text{DBW}} / V_S$	0.4	0.8	1.2	%	$(V_{\text{DBH}} - V_{\text{DBL}}) / V_S$

**Input RANGE**

Input current	$I_{\text{RANGE}}$	– 1	–	1	$\mu\text{A}$	$0\text{ V} < V_{\text{RANGE}} < V_S$
Switch-OFF voltage High	$V_{\text{OFFH}}$	– 25	0	100	mV	refer to $V_S$
Switch-OFF voltage Low	$V_{\text{OFFL}}$	300	400	500	mV	refer to GND

**Thermal Shutdown**

Thermal shutdown junction temperature	$T_{\text{jSD}}$	150	175	200	$^\circ\text{C}$	–
Thermal switch-on junction temperature	$T_{\text{jSO}}$	120	–	170	$^\circ\text{C}$	–
Temperature hysteresis	$\Delta T$	–	30		K	–

*Note: The listed characteristics are ensured over the operating range of the integrated circuit. Typical characteristics specify mean values expected over the production spread. If not otherwise specified, typical characteristics apply at  $T_A = 25\text{ }^\circ\text{C}$  and the given supply voltage.*



2 Diagrams

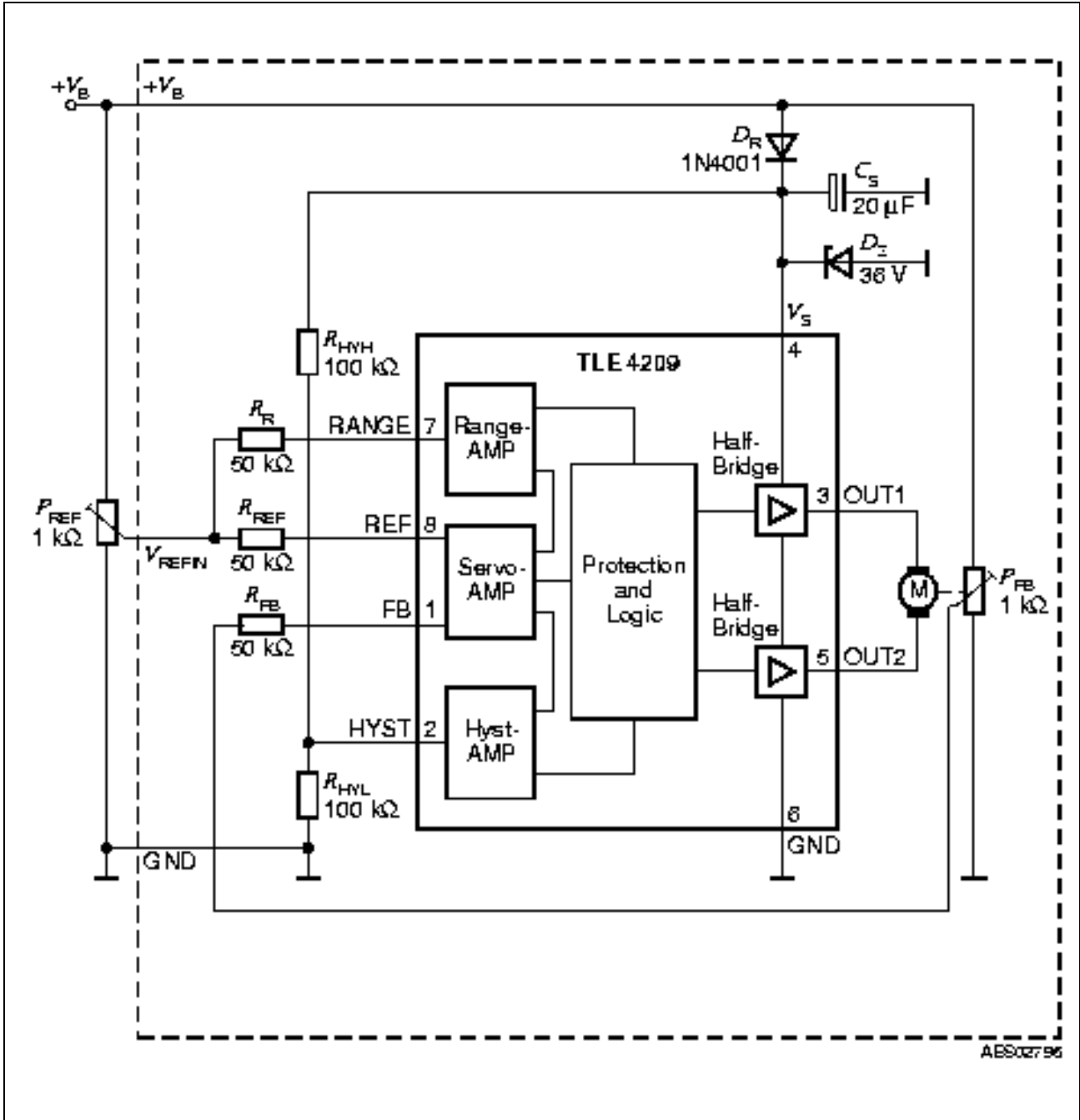


Figure 3 Application Circuit

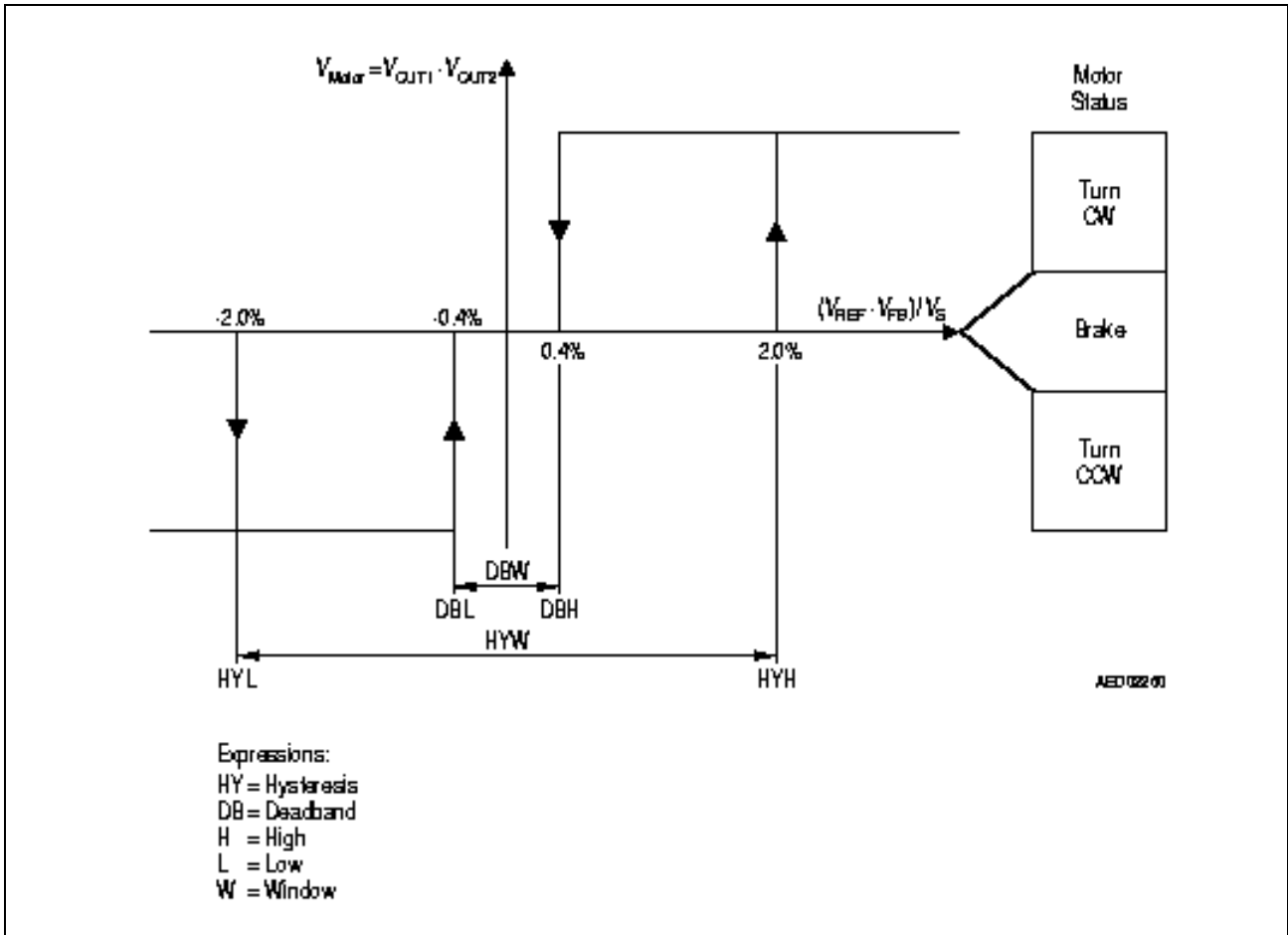


Figure 4 Hysteresis, Phaselag and Deadband-Definitions

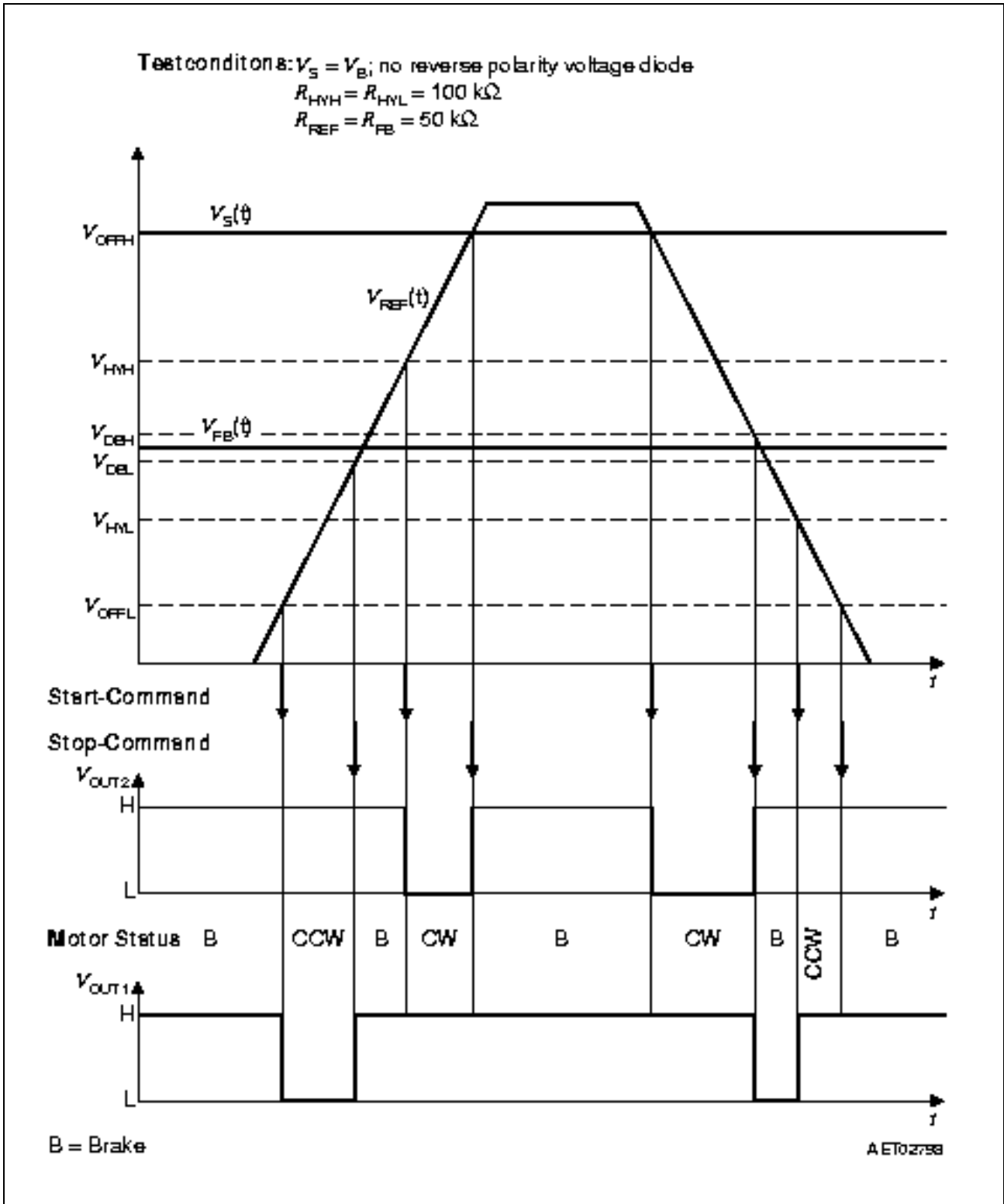
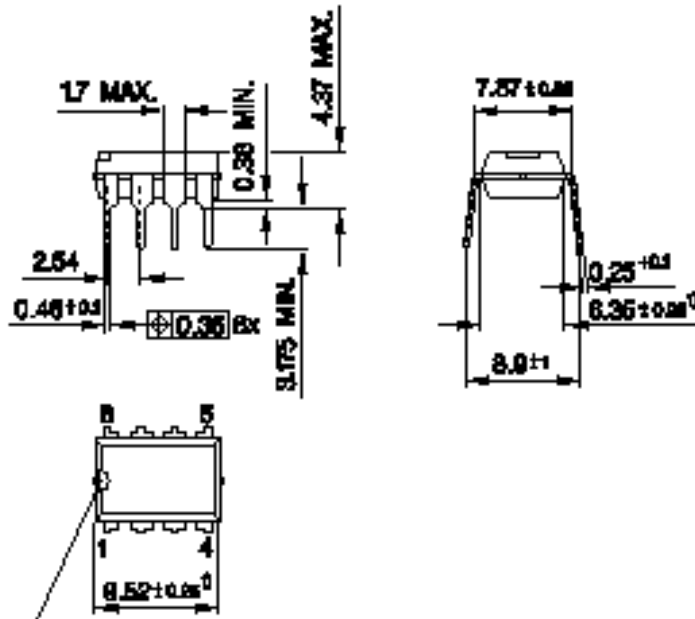


Figure 5 Timing and Phase-Lag

3 Package Outlines

**P-DIP-8-4**  
(Plastic Dual In-line Package)



Index Marking

† Does not include plastic or metal protrusion of 0.25 mm max. per side

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

SMD = Surface Mounted Device

Dimensions in mm