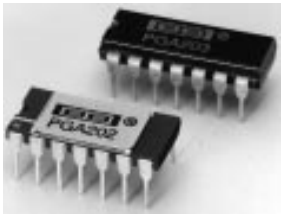
BURR - BROWN®



PGA202/203

Digitally Controlled Programmable-Gain INSTRUMENTATION AMPLIFIER

FEATURES

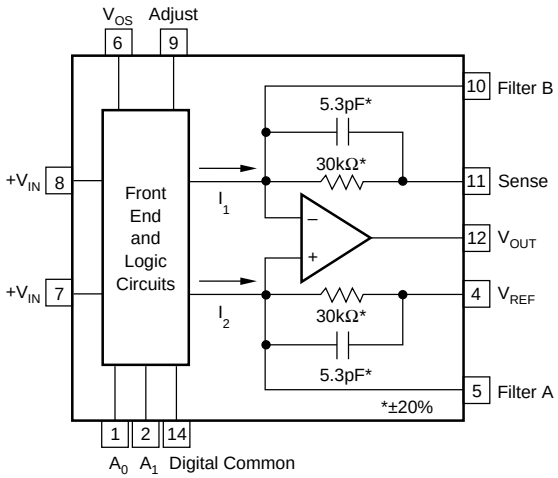
- DIGITALLY PROGRAMMABLE GAINS:
  - DECADE MODEL—PGA202
    - GAINS OF 1, 10, 100, 1000
  - BINARY MODEL—PGA203
    - GAINS OF 1, 2, 4, 8
- LOW BIAS CURRENT: 50pA max
- FAST SETTLING: 2μs to 0.01%
- LOW NON-LINEARITY: 0.012% max
- HIGH CMRR: 80dB min
- NEW TRANSCONDUCTANCE CIRCUITRY
- LOW COST

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- AUTO-RANGING CIRCUITS
- DYNAMIC RANGE EXPANSION
- REMOTE INSTRUMENTATION
- TEST EQUIPMENT

DESCRIPTION

The PGA202 is a monolithic instrumentation amplifier with digitally controlled gains of 1, 10, 100, and 1000. The PGA203 provides gains of 1, 2, 4, and 8. Both have TTL or CMOS-compatible inputs for easy microprocessor interface. Both have FET inputs and a new transconductance circuitry that keeps the bandwidth nearly constant with gain. Gain and offsets are laser trimmed to allow use without any external components. Both amplifiers are available in ceramic or plastic packages. The ceramic package is specified over the full industrial temperature range while the plastic package covers the commercial range.



Covered by U.S. PATENT #4,883,422

International Airport Industrial Park • Mailing Address: PO Box 11400 • Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd. • Tucson, AZ 85706
Tel: (520) 746-1111 • Twx: 910-952-1111 • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

PDS-1006C
Printed in U.S.A. August, 1993

SBOS002

SPECIFICATIONS

ELECTRICAL

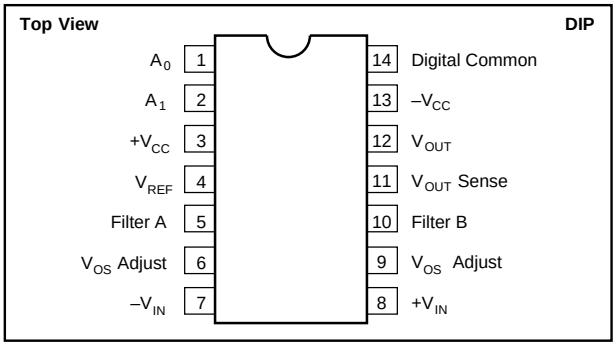
At +25°C, V_{CC} = ±15V unless otherwise noted.

PARAMETER	CONDITION	PGA202/203AG[1] MIN	PGA202/203AG[1] TYP	PGA202/203AG[1] MAX	PGA202/203BG[1] MIN	PGA202/203BG[1] TYP	PGA202/203BG[1] MAX	PGA202/203KP[1] MIN	PGA202/203KP[1] TYP	PGA202/203KP[1] MAX	UNITS
GAIN											
Error[2]	G < 1000		0.05	0.25		*	0.15		*	*	%
	G = 1000		0.1	1		0.08	0.5		*	*	%
Nonlinearity	G < 1000		0.002	0.015		*	0.012		*	*	%
	G = 1000		0.02	0.06		*	0.04		*	*	%
Gain vs Temperature	G < 100		3	25		*	15		*		ppm/°C
	G = 100		40	120		*	60		*		ppm/°C
	G = 1000		100	300		*	150		*		ppm/°C
RATED OUTPUT											
Voltage	$\|I_{OUT}\| \le 5mA$	±10	±12		*	*		*	*		V
Over Specified Temperature	See Typical Perf. Curve		±9			*			±10		V
Current	$\|V_{OUT}\| \le 10V$	±5	±10		*	*		*	*		mA
Impedance			0.5			*			*		Ω
ANALOG INPUTS											
Common-Mode Range		±10	±13		*	*		*	*		V
Absolute Max Voltage[3]	No Damage			±V_{CC}			*			*	V
Impedance, Differential			10 || 3			*			*		GΩ || pF
Common-Mode			10 || 1			*			*		GΩ || pF
OFFSET VOLTAGE (RTI)											
Initial Offset at 25°C[4]			±(0.5 + 5/G)	±(2 + 24/G)		*	±(1 + 12/G)		*	*	mV
vs Temperature			±(3 + 50/G)	±(24 + 240/G)		*	±(12 + 120/G)		*		µV/°C
Offset vs Time			50			*			*		µV/Month
Offset vs Supply	$10 \le V_{CC} \le 15$		10 + 250/G	100 + 900/G		*	50 + 450/G		*	*	µV/V
INPUT BIAS CURRENT											
Initial Bias Current: at 25°C			10	50		*	*		*	*	pA
at 85°C			640	3200		*	*		*	*	pA
Initial Offset Current: at 25°C			5	25		*	*		*	*	pA
at 85°C			320	1600		*	*		*	*	pA
COMMON-MODE REJECTION RATIO											
	G = 1	80	100		*	*		*	*		dB
	G = 10	86	110		*	*		*	*		dB
	G = 100	92	120		*	*		*	*		dB
	G = 1000	94	120		*	*		*	*		dB
INPUT NOISE											
Noise Voltage 0.1 to 10Hz			1.7			*			*		µVp-p
Noise Density at 10kHz[5]			12			*			*		nV/√Hz
OUTPUT NOISE											
Noise Voltage 0.1 to 10Hz			32			*			*		µVp-p
Density at 1kHz[5]			400			*			*		nV/√Hz
DYNAMIC RESPONSE											
Frequency Response	G < 1000		1000			*			*		kHz
	G = 1000		250			*			*		kHz
Full Power Bandwidth	G < 1000		400			*			*		kHz
	G = 1000		100			*			*		kHz
Slew Rate		10	20		15	*		*	*		V/µs
Settling Time (0.01%)[7]	G < 1000		2			*			*		µs
	G = 1000		10			*			*		µs
Overload Recovery Time[7]	G < 1000		5			*			*		µs
	G = 1000		10			*			*		µs
DIGITAL INPUTS											
Digital Common Range		$-V_{CC}$		V_{CC} – 8	*		*	*		*	V
Input Low Threshold[6]				0.8			*			*	V
Input Low Current				10			*			*	µA
Input High Voltage		2.4			*			*			V
Input High Current				10			*			*	µA
POWER SUPPLY											
Rated Voltage			±15			*			*		V
Voltage Range		±6		±18	*		*	*		*	V
Quiescent Current			6.5			*			*		mA
TEMPERATURE RANGE											
Specification		–25		85	*		*	0		70	°C
Operating		–55		125	*		*	–25		85	°C
Storage		–65		150	*		*	–40		100	°C
θ_{JA}			100			*			*		°C/W

* Same as the PGA202/203AG

NOTES: (1) All specifications apply to both the PGA202 and the PGA203. Values given for a gain of 10 are the same for a gain of 8 and other values may be interpolated. (2) Measured with a 10k load. (3) The analog inputs are internally diode clamped. (4) Adjustable to zero. (5) $V_{NOISE\ (RTI)} = \sqrt{(V_{N\ INPUT})^2 + (V_{N\ OUTPUT}/Gain)^2}$. (6) Threshold voltages are referenced to Digital Common. (7) From input change or gain change.

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	750mW
Analog and Digital Inputs	±(V_{CC} + 0.5V)
Operating Temperature Range:	
G Package	–55°C to +125°C
P Package	–40°C to +100°C
Lead Temperature (soldering, 10s)	300°C
Output Short Circuit Duration	Continuous
Junction Temperature	175°C

PACKAGE INFORMATION

MODEL	PACKAGE	PACKAGE DRAWING NUMBER(1)
PGA202KP	14-Pin Plastic DIP	010
PGA202AG	14-Pin Ceramic DIP	169
PGA202BG	14-Pin Ceramic DIP	169
PGA203KP	14-Pin Plastic DIP	010
PGA203AG	14-Pin Ceramic DIP	169
PGA203BG	14-Pin Ceramic DIP	169

NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix D of Burr-Brown IC Data Book.

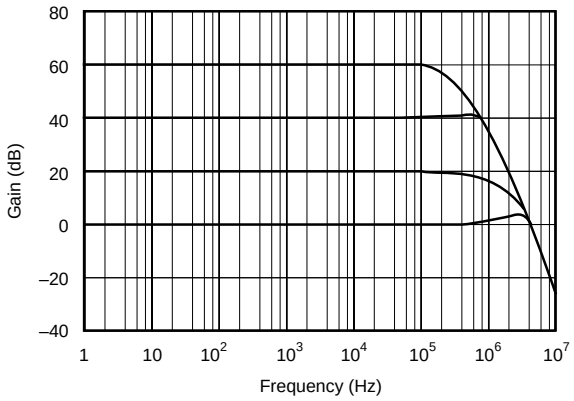
ORDERING INFORMATION

MODEL	GAINS	PACKAGE	TEMPERATURE RANGE	OFFSET VOLTAGE MAX (mV)
PGA202KP	1, 10, 100, 1000	Plastic DIP	0°C to +70°C	±(2 + 24/G)
PGA202AG	1, 10, 100, 1000	Ceramic DIP	–25°C to +85°C	±(2 + 24/G)
PGA202BG	1, 10, 100, 1000	Ceramic DIP	–25°C to +85°C	±(1 + 12/G)
PGA203KP	1, 2, 4, 8	Plastic DIP	0°C to +70°C	±(2 + 24/G)
PGA203AG	1, 2, 4, 8	Ceramic DIP	–25°C to +85°C	±(2 + 24/G)
PGA203BG	1, 2, 4, 8	Ceramic DIP	–25°C to +85°C	±(1 + 12/G)

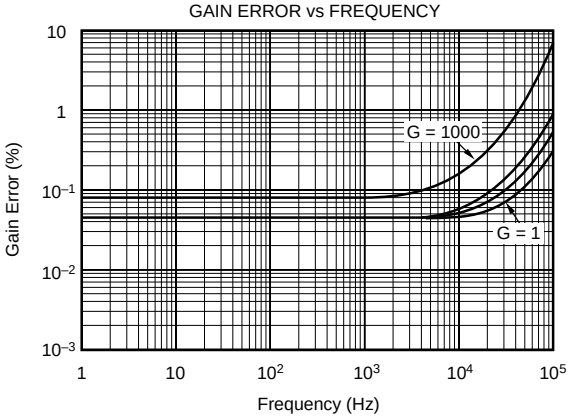
TYPICAL PERFORMANCE CURVES

T_A = +25°C, V_S = ±15V unless otherwise noted.

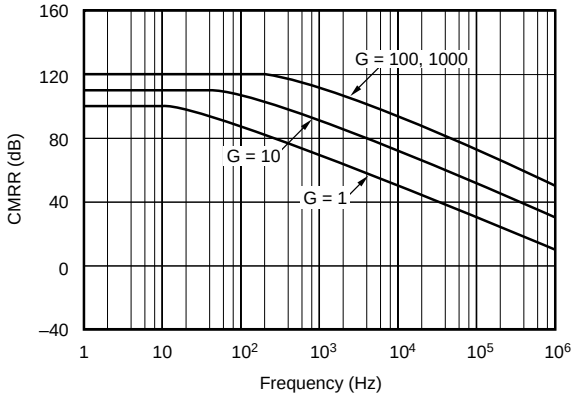
GAIN vs FREQUENCY



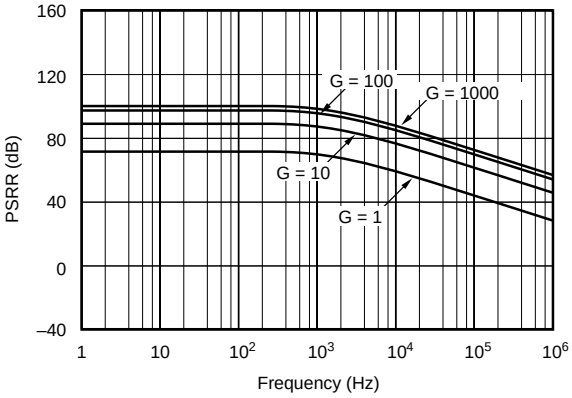
GAIN ERROR vs FREQUENCY



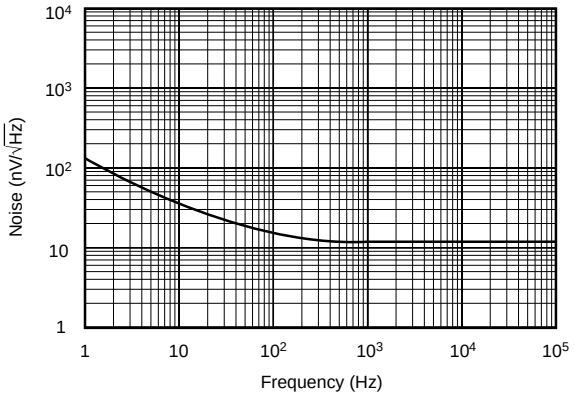
CMRR vs FREQUENCY



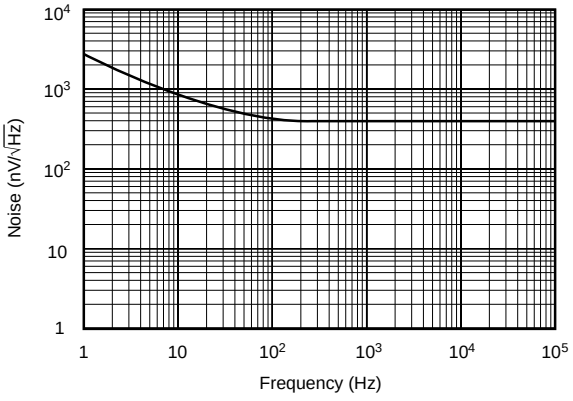
PSRR vs FREQUENCY



INPUT NOISE vs FREQUENCY



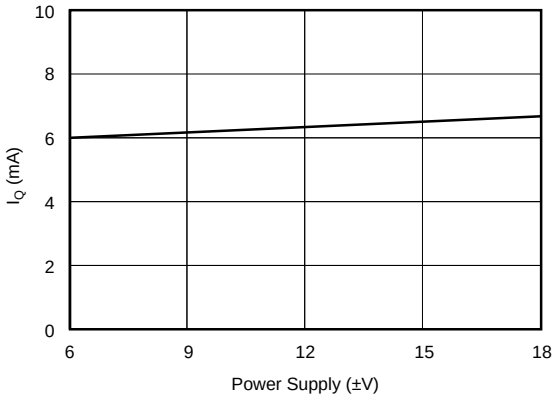
OUTPUT NOISE vs FREQUENCY



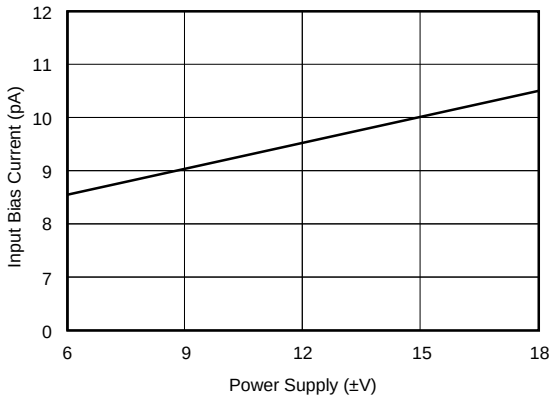
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

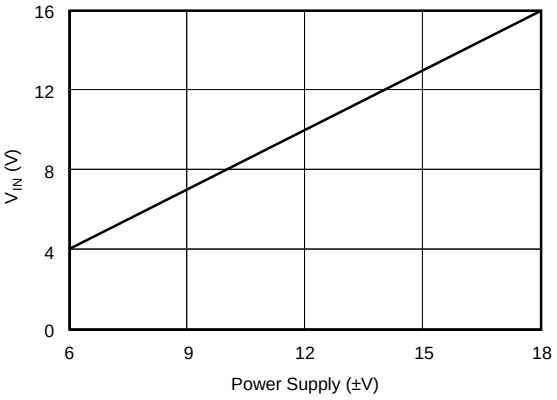
QUIESCENT CURRENT vs POWER SUPPLY



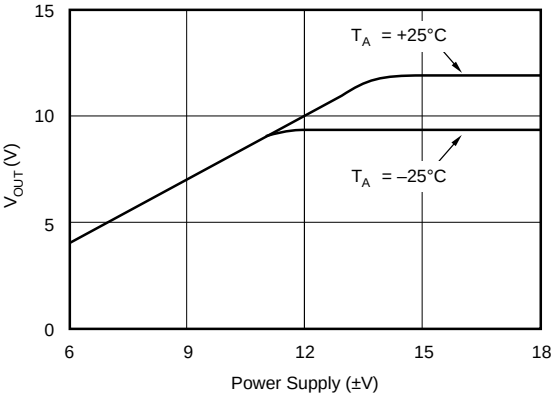
INPUT BIAS CURRENT vs POWER SUPPLY



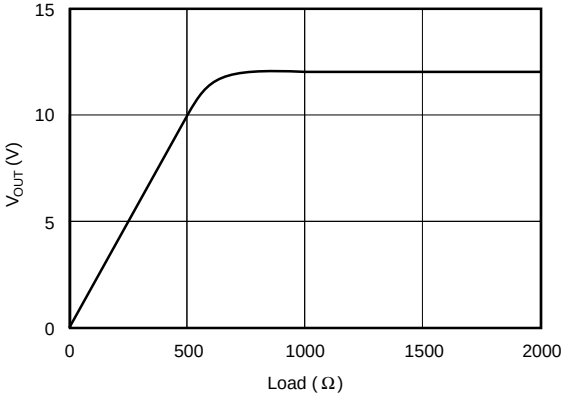
INPUT RANGE vs POWER SUPPLY



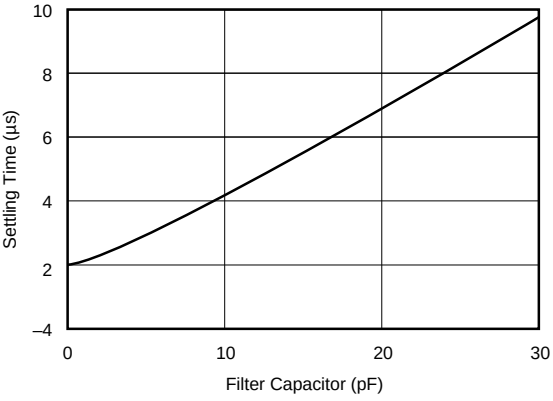
OUTPUT SWING vs POWER SUPPLY



OUTPUT SWING vs LOAD



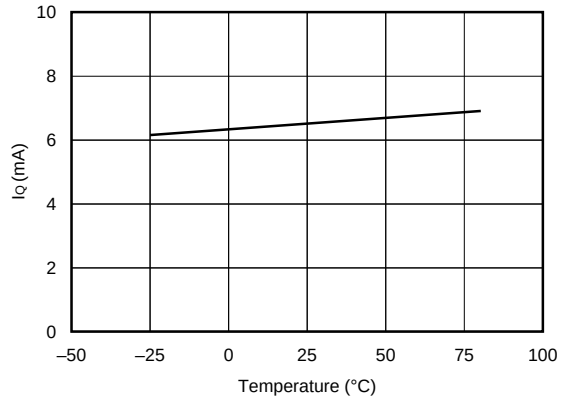
SETTLING TIME vs FILTER CAPACITOR



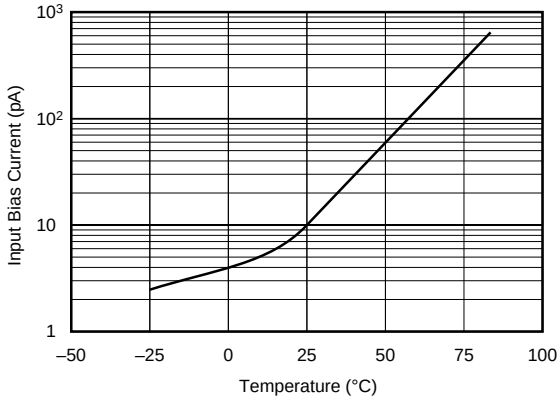
TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_S = ±15V unless otherwise noted.

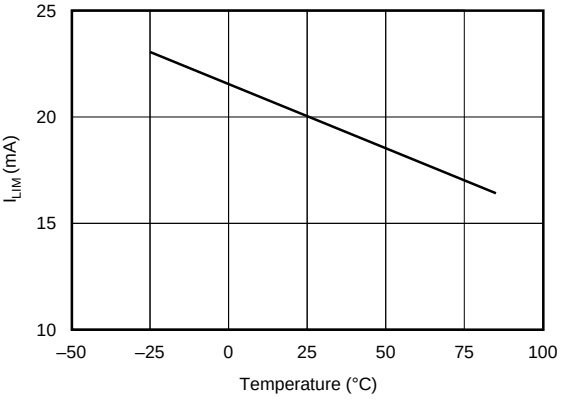
QUIESCENT CURRENT vs TEMPERATURE



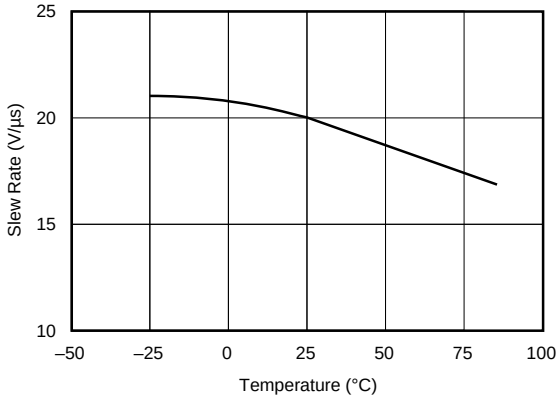
INPUT BIAS CURRENT vs TEMPERATURE



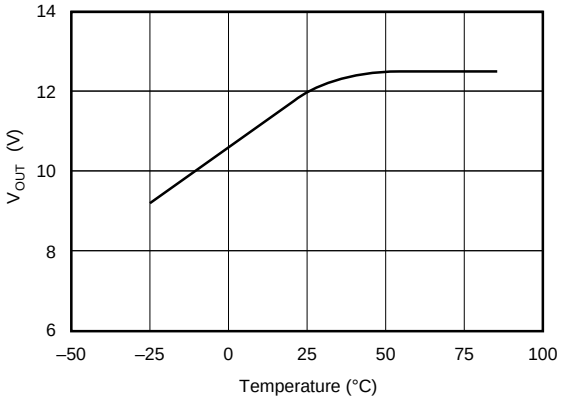
CURRENT LIMIT vs TEMPERATURE



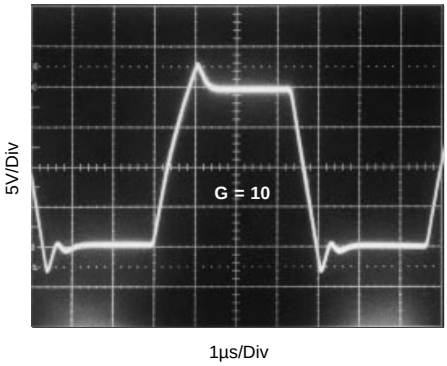
SLEW RATE vs TEMPERATURE



OUTPUT SWING vs TEMPERATURE



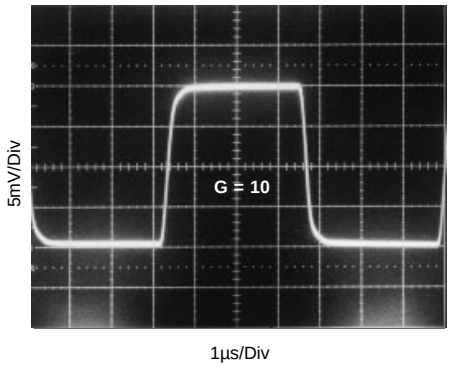
LARGE SIGNAL RESPONSE



TYPICAL PERFORMANCE CURVES (CONT)

T_A = +25°C, V_{CC} = ±15V unless otherwise noted.

SMALL SIGNAL RESPONSE



DISCUSSION OF PERFORMANCE

A simplified diagram of the PGA202/203 is shown on the first page. The design consists of a digitally controlled, differential transconductance front end stage using precision FET buffers and the classical transimpedance output stage. Gain switching is accomplished with a novel current steering technique that allows for fast settling when changing gains. The result is a high performance, programmable instrumentation amplifier with excellent speed and gain accuracy.

The input stage uses a new circuit topology that includes FET buffers to give extremely low input bias currents. The differential input voltage is converted into a differential output current with the transconductance gain selected by steering the input stage bias current between four identical input stages differing only in the value of the gain setting resistor. Each input stage is individually laser-trimmed for input offset, offset drift, and gain.

The output stage is a differential transimpedance amplifier. Unlike the classical difference amplifier output stage, the common-mode rejection is not limited by the resistor matching. However, the output resistors are laser-trimmed to help minimize the output offset and drift.

BASIC CONNECTIONS

Figure 1 shows the proper connections for power supply and signal. The power supplies should be decoupled with 1µF tantalum capacitors placed as close to the amplifier as possible for maximum performance. To avoid gain and CMR errors introduced by the external components, you should connect the grounds as indicated. Any resistance in the sense line (pin 11) or the V_{REF} line (pin 4) will lead to a gain error, so these lines should be kept as short as possible. To also maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

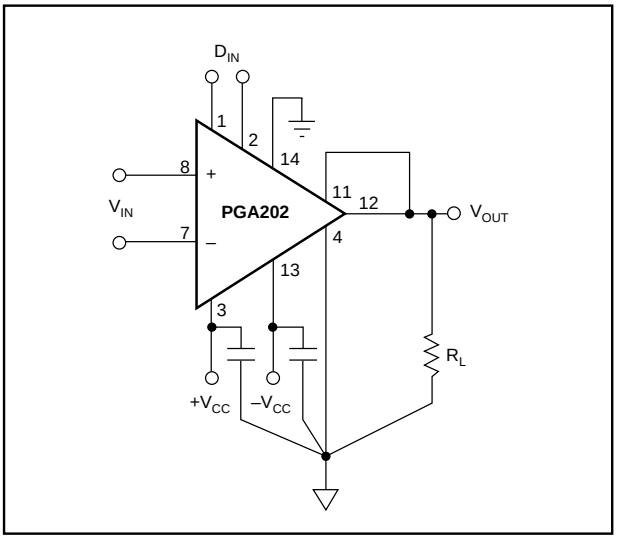


FIGURE 1. Basic Circuit Connections.

OFFSET ADJUSTMENT

Figure 2 shows the offset adjustment circuits for the PGA202/203. The input offset and the output offset are both separately adjustable. Notice that because the PGA202/203 change between four different input stages to change gain, the input offset voltage will change slightly with gain. For systems using computer autozeroing techniques, neither offset nor drift is a major concern, but it should be noted that since the input offset does change with gain, these systems should perform an autozero cycle after each gain change for optimum performance.

In the output offset adjustment circuit, the choice of the buffering op amp is very important. The op amp needs to have low output impedance and a wide bandwidth to maintain full accuracy over the entire frequency range of the PGA202/203. For these reasons we recommend the OPA602 as an excellent choice for this application.

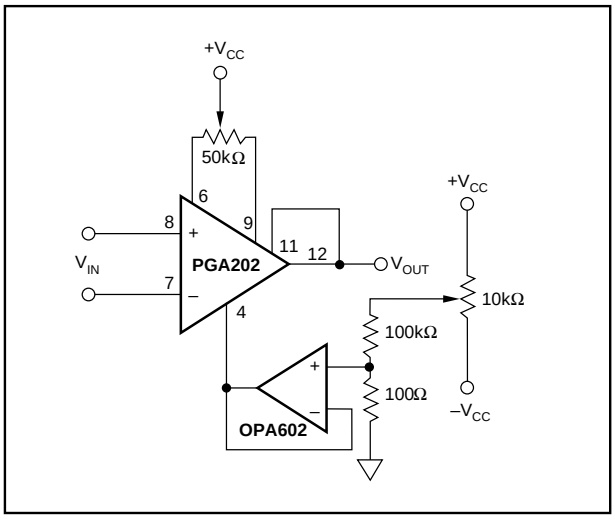


FIGURE 2. Offset Adjustment Circuits.

GAIN SELECTION

Gain selection is accomplished by the application of a 2-bit digital word to the gain select inputs. Table I shows the gains for the different possible values of the digital input word. The logic inputs are referred to their own separate digital common pin, which can be connected to any voltage between the minus supply and 8V below the positive supply. The gains are all internally trimmed to an initial accuracy of better than 0.1%, so no external gain adjustment is required. However, if necessary the gains can be increased by the use of an external attenuator around the output stage as shown in Figure 3. Recommended resistor values for certain selected output gains are given in Table II.

		PGA202		PGA203	
A_1	A_0	GAIN	ERROR	GAIN	ERROR
0	0	1	0.05%	1	0.05%
0	1	10	0.05%	2	0.05%
1	0	100	0.05%	4	0.05%
1	1	1000	0.10%	8	0.05%

TABLE I. Software Gain Selection.

OUTPUT GAIN	R_1	R_2
2	5kΩ	5kΩ
5	2kΩ	8kΩ
10	1kΩ	9kΩ

TABLE II. Output Stage Gain Control.

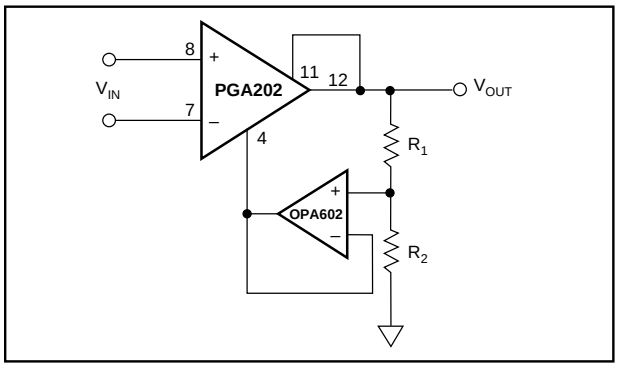


FIGURE 3. Gain Increase with Buffered Attenuator.

COMMON-MODE INPUT RANGE

Unlike the classical three op amp type of circuit, the input common-mode range of the PGA202/203 does not depend on the differential input and the gain. In the standard three op amp circuit, the input common-mode signal must be kept below the maximum output voltage of the input amplifier minus 1/2 the final output voltage. If, for example, these amplifiers can swing ±12V, then to get 12V at the output you must restrict the input common-mode voltage to only 6V. The circuitry of the PGA202/203 is such that the common-mode input range applies to either input pin regardless of the output voltage.

OUTPUT SENSE

An output sense has been provided to allow greater accuracy in connecting the load. By attaching this feedback point to the load at the load site, IR drops due to the load currents are eliminated since they are inside the feedback loop. Proper connection is shown in Figure 1. When more current is required, a power booster can be placed in the feedback loop as shown in Figure 4. Buffer errors are minimized by the loop gain of the output amplifier.

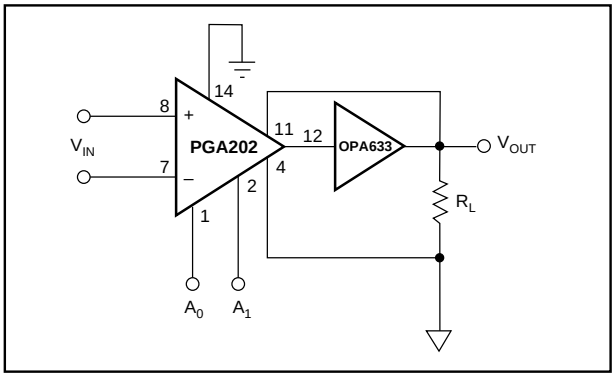


FIGURE 4. Current Boosting the Output.

OUTPUT FILTERING

The summing nodes of the output amplifier have also been made available to allow for output filtering. By placing matched capacitors in parallel with the existing internal capacitors as shown in Figure 5, you can lower the frequency response of the output amplifier. This will reduce the noise of the amplifier, at the cost of a slower response. The nominal frequency responses for some selected values of capacitor are shown in Table III.

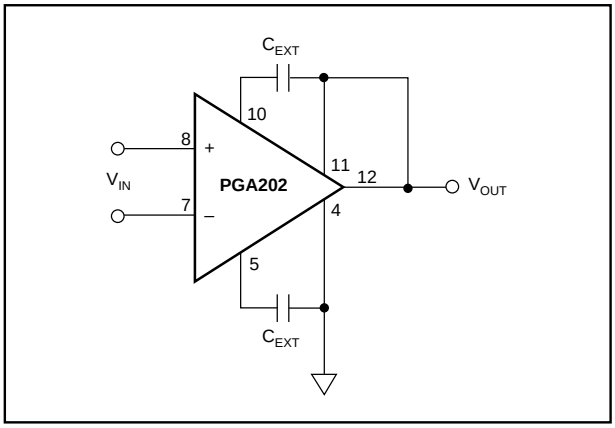


FIGURE 5. Output Filtering.

CUTOFF FREQUENCY	C_1 AND C_2
1MHz	None
100kHz	47pF
10kHz	525pF

TABLE III. Output Frequency vs Filter Capacitors.

INPUT CHARACTERISTICS

Because the PGA202/203 have FET inputs, the bias currents drawn through input source resistors have a negligible effect on DC accuracy. The picoamp currents produce no more than microvolts through megohm sources. The inputs are also internally diode clamped to the supplies. Thus, input filtering and input series protection are easily achievable.

A return path for the input bias currents must always be provided to prevent the charging of any stray capacitance. Otherwise, the amplifier could wander and saturate. A 1MΩ to 10MΩ resistor from the input to common will return floating sources such as thermocouples and AC-coupled inputs (see Applications Section, Figures 8 and 9.)

DYNAMIC PERFORMANCE

The PGA202 and the PGA203 are fast-settling FET input programmable gain instrumentation amplifiers. Careful attention to minimize stray capacitance is necessary to achieve specified performance. High source resistance will interact with the input capacitance to reduce speed and overall bandwidth. Also, to maintain stability, avoid capacitance from the output to the input or the offset adjust pins.

Applications with balanced source impedance will provide the best performance. In some applications, mismatched source impedances may be required. If the impedance in the negative input exceeds that in the positive input, stray capacitance from the output will create a net negative feedback and improve the stability of the circuit. If, however, the impedance in the positive input is greater, then the feedback due to stray capacitance will be positive and instability may result. The degree of positive feedback will, of course, depend on the source impedance imbalance as well as the board layout and the operating gain. The addition of a small bypass capacitor of about 5 to 50pF directly across the input terminals of the PGIA will generally eliminate any instability arising from these stray capacitances. CMR errors due to the source imbalance will also be reduced by the addition of this capacitor.

The PGA202 and the PGA203 are designed for fast settling in response to changes in either the input voltage or the gain. The bandwidth and the settling times are mostly determined by the output stage and are therefore independent of gain, except at the highest gain of the PGA202 where other factors in the input stage begin to dominate.

APPLICATIONS

In addition to general purpose applications, the PGA202/203 are designed to handle two important and demanding classes of applications: inputs with high source impedances, and rapid scanning data acquisition systems requiring fast settling time. Because the user has access to output sense and output common pins, current sources can also be constructed with a minimum of external components. Some basic application circuits are shown in Figures 6 through 12.

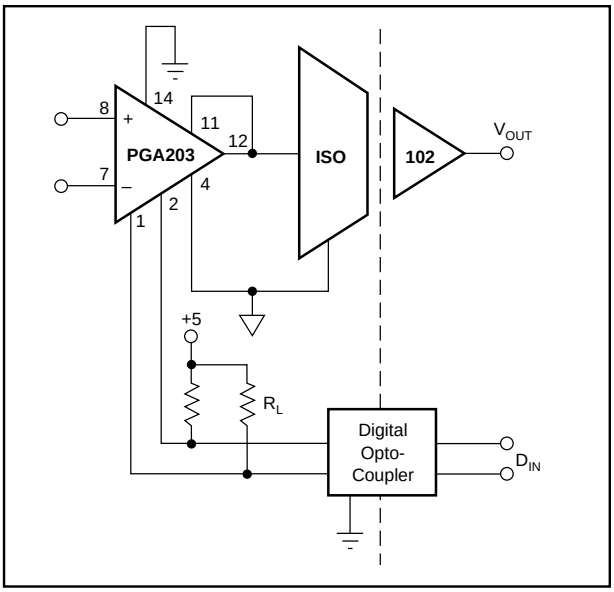


FIGURE 6. Isolated Programmable Gain Instrumentation Amplifier.

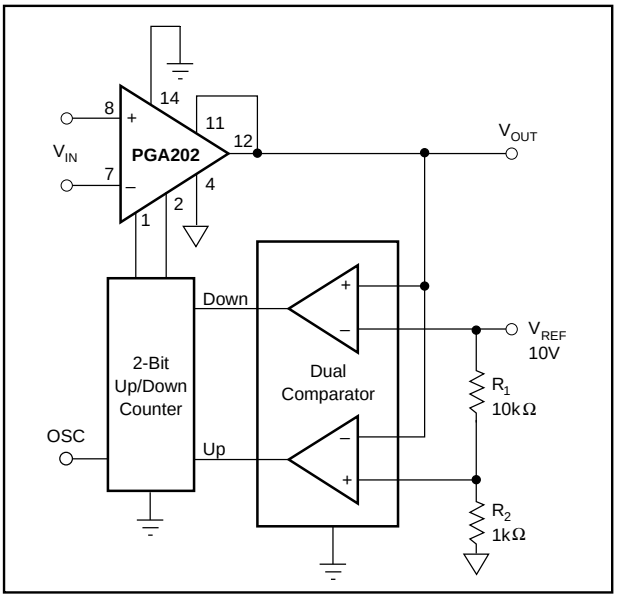


FIGURE 7. Auto Gain Ranging.

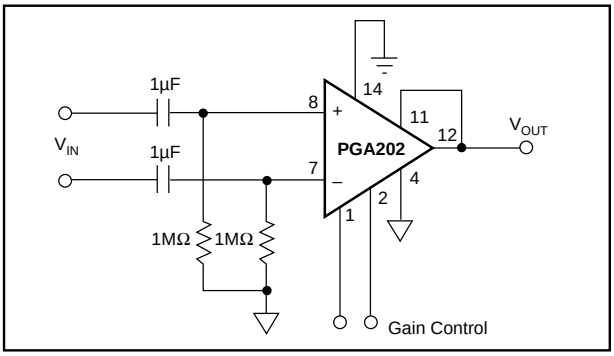


FIGURE 8. AC-Coupled Differential Amplifier for Frequencies Above 0.16Hz.

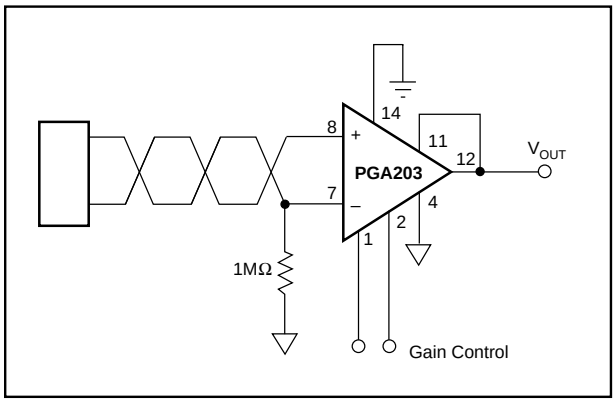


FIGURE 9. Floating Source Programmable Gain Instrumentation Amplifier.

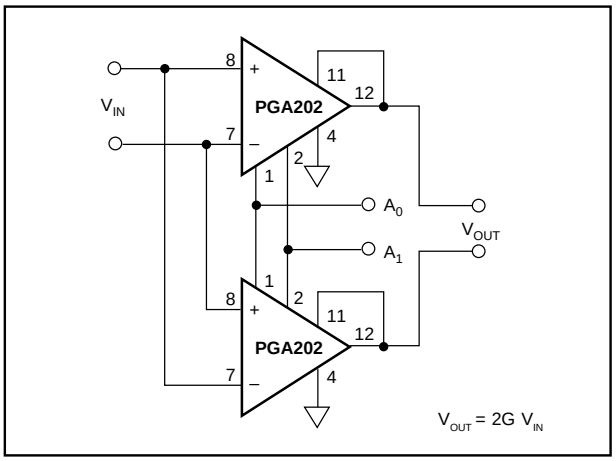


FIGURE 11. Programmable Differential In/Differential Out Amplifier.

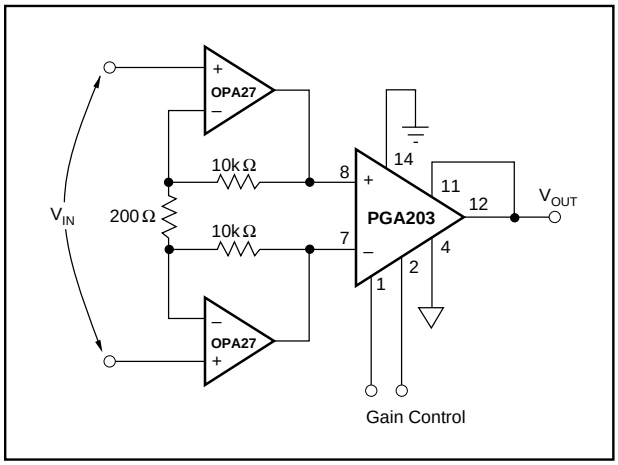


FIGURE 10. Low Noise Differential Amplifier with Gains of 100, 200, 400, 800.

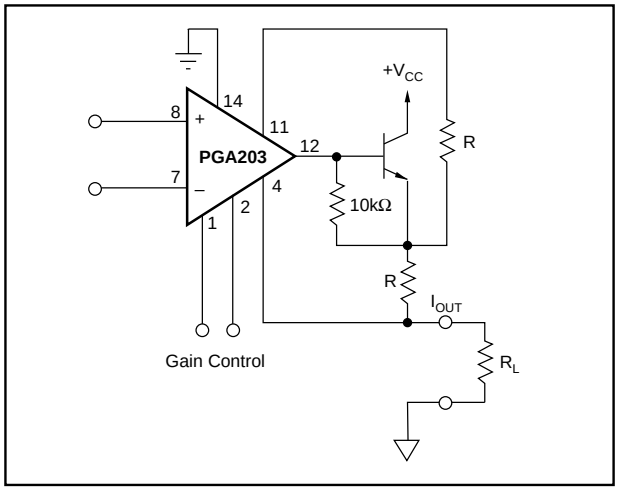


FIGURE 12. Programmable Current Source.

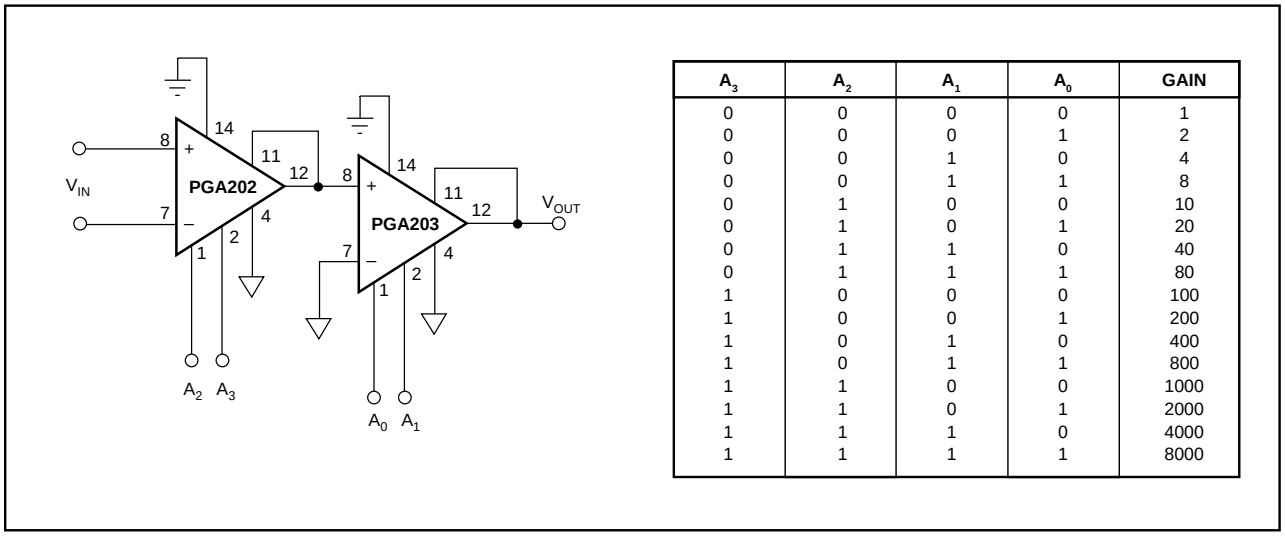


FIGURE 13. Cascaded Amplifiers.

A_3	A_2	A_1	A_0	GAIN
0	0	0	0	1
0	0	0	1	2
0	0	1	0	4
0	0	1	1	8
0	1	0	0	10
0	1	0	1	20
0	1	1	0	40
0	1	1	1	80
1	0	0	0	100
1	0	0	1	200
1	0	1	0	400
1	0	1	1	800
1	1	0	0	1000
1	1	0	1	2000
1	1	1	0	4000
1	1	1	1	8000

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PGA202KP	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	PGA202KP	Samples
PGA202KPG4	LIFEBUY	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	PGA202KP	
PGA203KP	ACTIVE	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	PGA203KP	Samples
PGA203KPG4	LIFEBUY	PDIP	N	14	25	RoHS & Green	NIPDAU	N / A for Pkg Type	-25 to 85	PGA203KP	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

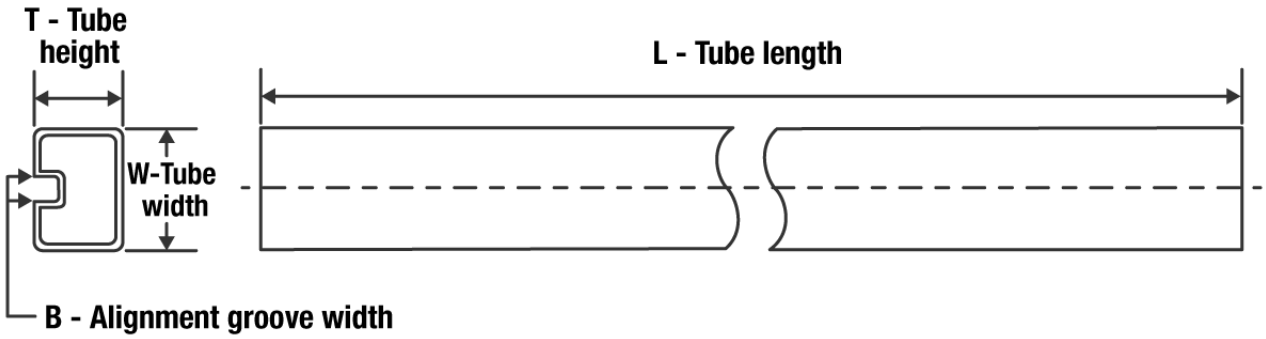
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
PGA202KP	N	PDIP	14	25	506	13.97	11230	4.32
PGA202KPG4	N	PDIP	14	25	506	13.97	11230	4.32
PGA203KP	N	PDIP	14	25	506	13.97	11230	4.32
PGA203KPG4	N	PDIP	14	25	506	13.97	11230	4.32

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265