

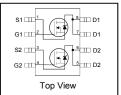
#### **Features**

- Advanced Planar Technology
- Ultra Low On-Resistance
- · Logic Level Gate Drive
- Dual N Channel MOSFET
- Surface Mount
- · Available in Tape & Reel
- 175°C Operating Temperature
- · Lead-Free, RoHS Compliant
- Automotive Qualified \*

## **Description**

Specifically designed for Automotive applications, these HEXFET® Power MOSFET's in a Dual SO-8 package utilize the lastest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of these Automotive qualified HEXFET Power MOSFET's are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

The efficient SO-8 package provides enhanced thermal characteristics and dual MOSFET die capability making it ideal in a variety of power applications. This dual, surface mount SO-8 can dramatically reduce board space and is also available in Tape & Reel.



V <sub>DSS</sub>	55V
R <sub>DS(on)</sub> typ.	0.043Ω
max.	0.050Ω
I <sub>D</sub>	5.1A



G	D	S
Gate	Drain	Source

Page part number   Backage Type		Standard Pack		Ordershie Bert Number	
Base part number	Package Type	Form Quantity		Orderable Part Number	
AUIRF7341Q	SO-8	Tape and Reel	4000	AUIRF7341QTR	

#### **Absolute Maximum Ratings**

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the specifications is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (TA) is 25°C, unless otherwise specified.

Symbol	Parameter	Max.	Units
$V_{DS}$	Drain-Source Voltage	55	V
I <sub>D</sub> @ T <sub>A</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	5.1	
$I_D @ T_A = 70^{\circ}C$	Continuous Drain Current, V <sub>GS</sub> @ 10V	4.2	Α
I <sub>DM</sub>	Pulsed Drain Current ①	42	
P <sub>D</sub> @T <sub>A</sub> = 25°C	Maximum Power Dissipation ③	2.4	10/
P <sub>D</sub> @T <sub>A</sub> = 70°C	Maximum Power Dissipation ③	1.7	W
	Linear Derating Factor	16	mW/°C
$V_{GS}$	Gate-to-Source Voltage	± 20	V
E <sub>AS</sub>	Single Pulse Avalanche Energy (Thermally Limited) ②	140	mJ
I <sub>AR</sub>	Avalanche Current	5.1	Α
E <sub>AR</sub>	Repetitive Avalanche Energy	See Fig.17, 18, 15a, 15b	mJ
$T_J$	Operating Junction and	-55 to + 175	00
T <sub>STG</sub>	Storage Temperature Range		°C

### **Thermal Resistance**

Symbol	Parameter	Тур.	Max.	Units
$R_{\theta JA}$	Junction-to-Ambient @		62.5	°C/W

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<sup>\*</sup>Qualification standards can be found at www.infineon.com



# Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Тур.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_{J}$	Breakdown Voltage Temp. Coefficient		0.052		V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
Б	Ctatia Drain to Course On Besistance		0.043	0.050		V <sub>GS</sub> = 10V, I <sub>D</sub> = 5.1A ③
$R_{DS(on)}$	Static Drain-to-Source On-Resistance		0.056	0.065	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 4.42A ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0		3.0	V	$V_{DS} = V_{GS}, I_{D} = 250 \mu A$
gfs	Forward Trans conductance	10.4			S	$V_{DS} = 10V, I_{D} = 5.2A$
ı	Drain-to-Source Leakage Current			2.0		$V_{DS}$ =44V, $V_{GS}$ = 0V
IDSS	Drain-to-Source Leakage Current			25	μA	$V_{DS} = 44V, V_{GS} = 0V, T_{J} = 150^{\circ}C$
I <sub>GSS</sub>	Gate-to-Source Forward Leakage			100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage			-100	IIA	$V_{GS} = -20V$

# Dynamic Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

$Q_g$	Total Gate Charge	 29	44		I <sub>D</sub> =5.2A
$Q_{gs}$	Gate-to-Source Charge	 2.9	4.4	nC	$V_{DS} = 44V$
$Q_{gd}$	Gate-to-Drain Charge	 7.3	11		V <sub>GS</sub> = 10V
$t_{d(on)}$	Turn-On Delay Time	 9.2			$V_{DD} = 28V$
t <sub>r</sub>	Rise Time	 7.7		no	I <sub>D</sub> = 1.0A
$t_{d(off)}$	Turn-Off Delay Time	31		ns	$R_G = 6.0\Omega$
t <sub>f</sub>	Fall Time	 12.5			V <sub>GS</sub> = 10V ③
$C_{iss}$	Input Capacitance	780			$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	 190		pF	V <sub>DS</sub> = 25V
$C_{rss}$	Reverse Transfer Capacitance	66			f = 1.0 MHz

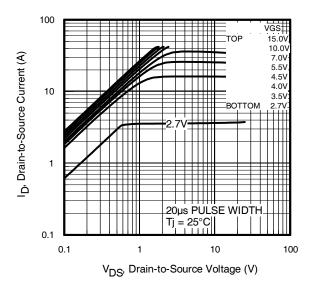
## **Diode Characteristics**

	Parameter	Min.	Тур.	Max.	Units	Conditions
	Continuous Source Current			2.4		MOSFET symbol
Is	(Body Diode)			2.4	_	showing the
ı	Pulsed Source Current			42	Α	integral reverse
I <sub>SM</sub>	(Body Diode) ①			42		p-n junction diode.
$V_{SD}$	Diode Forward Voltage			1.2	V	$T_J = 25^{\circ}C, I_S = 2.6A, V_{GS} = 0V ② ③$
t <sub>rr</sub>	Reverse Recovery Time		51	77	ns	$T_J = 25^{\circ}C$ , $I_F = 2.6A$ ,
$Q_{rr}$	Reverse Recovery Charge		76	114	nC	di/dt = 100A/µs ③

#### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ②  $V_{DD}$  =25V, Starting  $T_J$  = 25°C, L = 10.7mH,  $R_G$  = 25 $\Omega$ ,  $I_{AS}$  = 5.2A.
- 3 Pulse width  $\leq 300 \mu s$ ; duty cycle  $\leq 2\%$ .
- 4 Surface mounted FR-4 board,  $t \le 10 \text{sec.}$



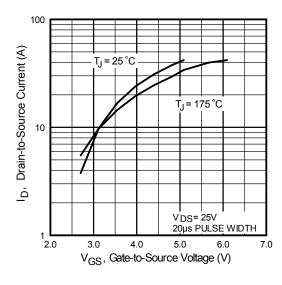


(V) treating 10 (10.00 to 10.00 to 10.0

100

Fig. 1 Typical Output Characteristics

Fig. 2 Typical Output Characteristics



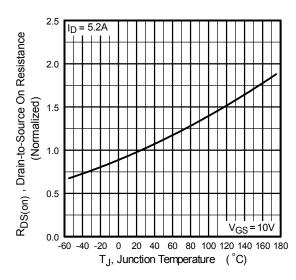
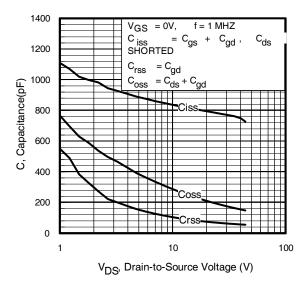


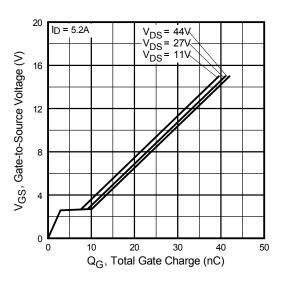
Fig. 3 Typical Transfer Characteristics

**Fig. 4** Normalized On-Resistance vs. Temperature





**Fig 5.** Typical Capacitance vs. Drain-to-Source Voltage



**Fig 6.** Typical Gate Charge vs. Gate-to-Source Voltage

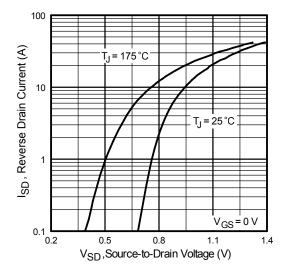


Fig. 7 Typical Source-to-Drain Diode Forward Voltage

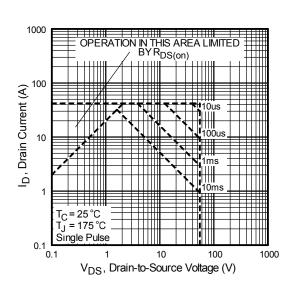


Fig 8. Maximum Safe Operating Area



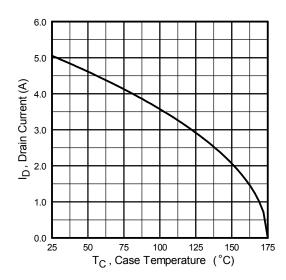


Fig 9. Maximum Drain Current vs. Case Temperature

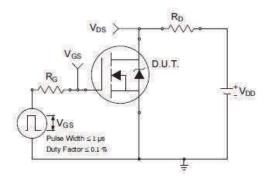


Fig 10a. Switching Time Test Circuit

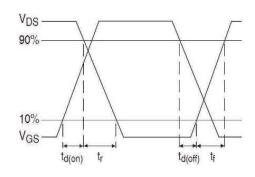


Fig 10b. Switching Time Waveforms

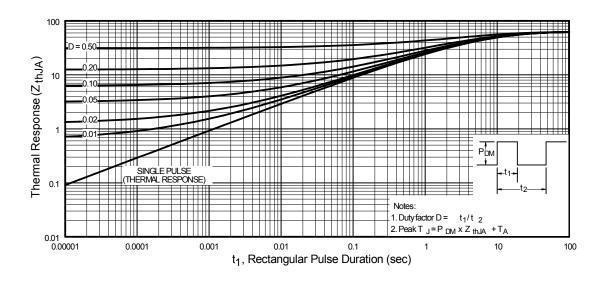


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient



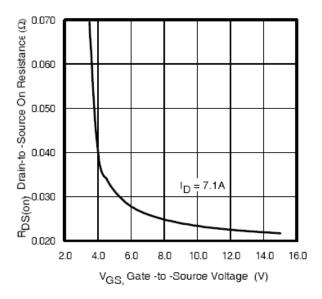


Fig 12. Typical On-Resistance Vs. Gate Voltage

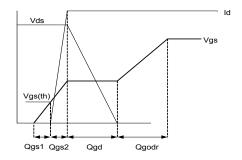


Fig 14a. Basic Gate Charge Waveform

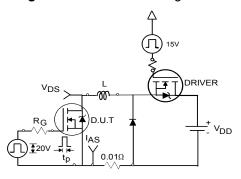


Fig 15a. Unclamped Inductive Test Circuit

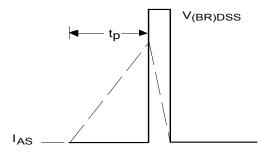


Fig 15b. Unclamped Inductive Waveforms

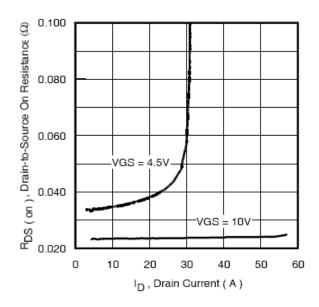


Fig 13. Typical On-Resistance Vs. Drain Current

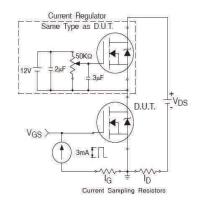


Fig 14b. Gate Charge Test Circuit

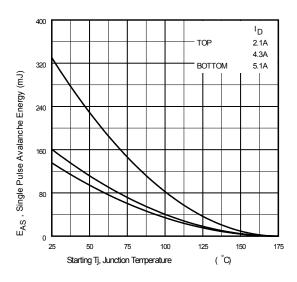


Fig 16. Maximum Avalanche Energy vs. Drain Current



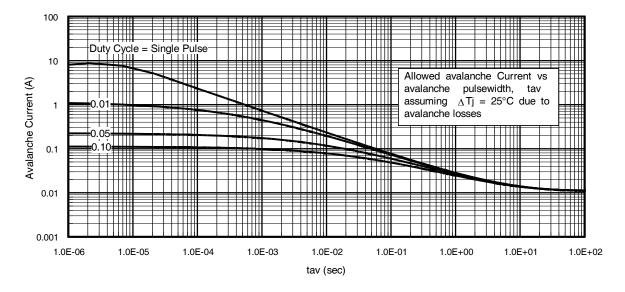
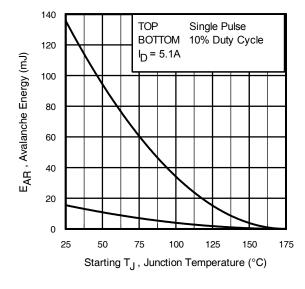


Fig 17. Typical Avalanche Current vs. Pulse width



**Fig 18.** Maximum Avalanche Energy vs. Temperature

Notes on Repetitive Avalanche Curves , Figures 17, 18: (For further info, see AN-1005 at www.infineon.com)

- Avalanche failures assumption:

  Durchy a thormal phonomenon and failure
  - Purely a thermal phenomenon and failure occurs at a temperature far in excess of T<sub>jmax</sub>. This is validated for every part type.
- 2. Safe operation in Avalanche is allowed as long as T<sub>jmax</sub> is not exceeded.
- 3. Equation below based on circuit and waveforms shown in Figures 15a, 15b.
- 4. PD (ave) = Average power dissipation per single avalanche pulse.
- BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
- 6. Iav = Allowable avalanche current.
- 7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 11, 17).

tav = Average time in avalanche.

D = Duty cycle in avalanche = tav ·f

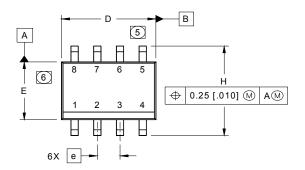
ZthJC(D, tav) = Transient thermal resistance, see Figures 11)

$$\begin{split} P_{D \; (ave)} &= 1/2 \; (\; 1.3 \cdot BV \cdot I_{av}) = \Delta T / \; Z_{thJC} \\ I_{av} &= 2\Delta T / \; [1.3 \cdot BV \cdot Z_{th}] \\ E_{AS \; (AR)} &= P_{D \; (ave)} \cdot t_{av} \end{split}$$

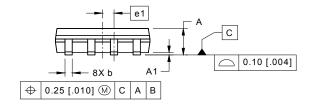
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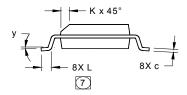


# **SO-8 Package Outline** (Dimensions are shown in millimeters (inches)



DIM	INC	HES	MILLIM	ETERS
DIIVI	MIN MAX		MIN	MAX
Α	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
С	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
Е	.1497	.1574	3.80	4.00
е	.050 B	ASIC	1.27 B	ASIC
e 1	.025 B	ASIC	0.635 E	BASIC
Н	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
у	0°	8°	0°	8°



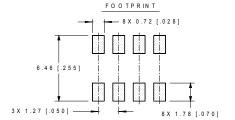


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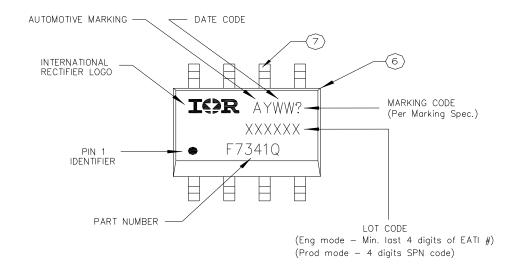
- CONTROLLING DIMENSION. MILLIMETERS [IN CHES].
   DIMENSIONS ARE SHOWN IN MILLIMETERS [IN CHES].

   OUTLINE CONFORMS TO JEDEC OUTLINE M S-012AA.

  DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS MOLD PROTRUSIONS NOT TO EXCEED 0.15 [.006].
- 6 DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS MOLD PROTRUSIONS NOT TO EXCEED 0.25 [.010].
- 7 DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.



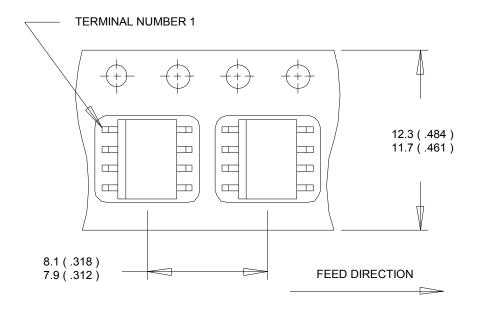
## **SO-8 Part Marking Information**



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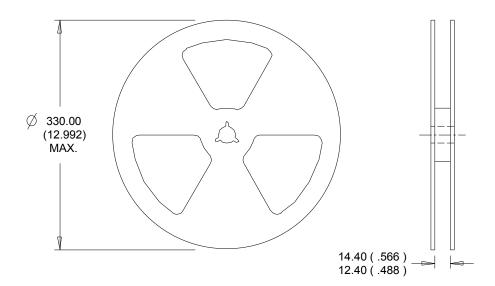


## SO-8 Tape and Reel (Dimensions are shown in millimeters (inches)



#### NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
- 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



## NOTES:

- 1. CONTROLLING DIMENSION: MILLIMETER.
- 2. OUTLINE CONFORMS TO EIA-481 & EIA-541.



#### **Qualification Information**

	ion inioniation						
		Automotive					
		(per AEC-Q101)					
Qualificat	tion Level	Comments: This part number(s) passed Automotive qualification. Infineon's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.					
Moisture	pisture Sensitivity Level SO-8 MSL1						
			Class M2 (+/- 200V) <sup>†</sup>				
	Machine Model		AEC-Q101-002				
FOD	Lluman Dady Madal	Class H1A (+/- 500V) <sup>†</sup>					
ESD	Human Body Model	AEC-Q101-001					
Charged Device Model		Class C5 (+/- 1125V) <sup>†</sup>					
		AEC-Q101-005					
RoHS Compliant Yes							

<sup>†</sup> Highest passing voltage.

## **Revision History**

Date	Comments					
3/10/2014 • Added "Logic Level Gate Drive" bullet in the features section on page 1						
3/10/2014	Updated data sheet with new IR corporate template					
9/30/2015	Updated datasheet with corporate template					
9/30/2013	Corrected ordering table on page 1.					

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