BLP10H630P; BLP10H630PG

Power LDMOS transistor

AMPLEON

Rev. 1 — 20 December 2016

Product data sheet

1. Product profile

1.1 General description

A 30 W LDMOS power transistor for broadcast and industrial applications in the HF to 1000 MHz band.

Table 1. Application information

Test signal	f	V _{DS}	PL	G _p	η _D
	(MHz)	(V)	(W)	(dB)	(%)
pulsed RF	720	50	30	18	72

1.2 Features and benefits

- Easy power control
- Integrated dual sided ESD protection enables class C operation and complete switch off of the transistor
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (HF to 1000 MHz)
- Compliant to Directive 2002/95/EC, regarding Restriction of Hazardous Substances (RoHS)

1.3 Applications

- Industrial, scientific and medical applications
- Broadcast transmitter applications

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outlin	ne Graphic symbol
BLP10H6	30P (SOT1223-2)	'	
1	gate 2	4 0	
2	gate 1	4 3	4
3	drain 1		
4	drain 2	pin 1 index	5
5	source	[1]	
		1 2	3
			aaa-003574
BLP10H6	30PG (SOT1224-2)		
1	gate 2	, ,	
2	gate 1	4 3	_
3	drain 1	□ ○ nin 1 index	
4	drain 2	pin 1 index	5
5	source	[1] 1 2	
			' 3
			aaa-003574

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package	Package				
	Name	Name Description Ve				
BLP10H630P	HSOP4F	plastic, heatsink small outline package; 4 leads (flat)	SOT1223-2			
BLP10H630PG	HSOP4	plastic, heatsink small outline package; 4 leads	SOT1224-2			

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	110	V
V_{GS}	gate-source voltage		-6	+11	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

^[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

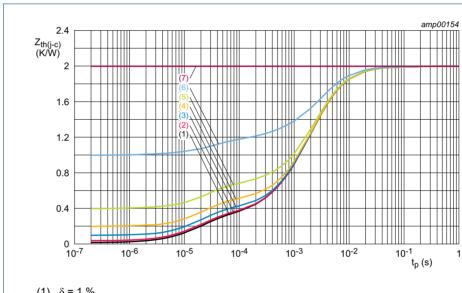
BLP10H630P_BLP10H630PG

Thermal characteristics 5.

Table 5. **Thermal characteristics**

Symbol	Parameter	Conditions		Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	T _j = 125 °C	[1][2]	2.0	K/W
Z _{th(j-c)}	transient thermal impedance from junction to case	T_j = 150 °C; t_p = 100 μs; δ = 20 %	[3]	0.68	K/W

- [1] T_i is the junction temperature.
- $R_{th(j-c)}$ is measured under RF conditions.
- See Figure 1.



- (1) $\delta = 1 \%$
- (2) $\delta = 2 \%$
- (3) $\delta = 5 \%$
- (4) $\delta = 10 \%$
- (5) $\delta = 20 \%$
- (6) $\delta = 50 \%$
- (7) $\delta = 100 \% (DC)$

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

Characteristics 6.

DC characteristics Table 6.

 T_i = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V _{(BR)DSS}	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 125 \mu\text{A}$	110	-	-	V
V _{GS(th)}	gate-source threshold voltage	V _{DS} = 10 V; I _D = 12.5 mA	1.25	1.9	2.25	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 50 \text{ V}; I_{D} = 5 \text{ mA}$	-	1.7	-	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 50 V	-	-	1.4	μΑ

BLP10H630P_BLP10H630PG

Table 6. DC characteristics ...continued

 T_i = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	2.0	-	Α
I _{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	140	nA
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 0.44 \text{ A}$	-	2.3	-	Ω

Table 7. AC characteristics

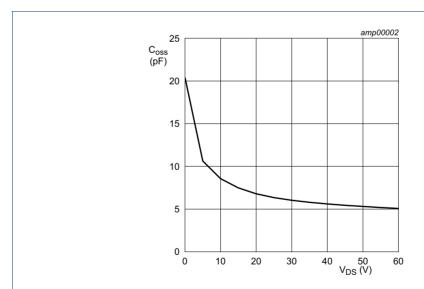
 T_i = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
C _{rs}	feedback capacitance	$V_{GS} = 0 \text{ V}; V_{DS} = 50 \text{ V}; f = 1 \text{ MHz}$	-	0.08	-	pF
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	15.0	-	pF
Coss	output capacitance	V _{GS} = 0 V; V _{DS} = 50 V; f = 1 MHz	-	5.3	-	pF

Table 8. RF characteristics

Test signal: pulsed RF; t_p = 100 μ s; δ = 20 %; f = 720 MHz; RF performance at V_{DS} = 50 V; I_{Dq} = 20 mA; T_{case} = 25 $^{\circ}$ C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	P _L = 30 W	16.8	18	-	dB
RLin	input return loss	P _L = 30 W	-	-17	-	dB
η_{D}	drain efficiency	P _L = 30 W	68	72	-	%



 V_{GS} = 0 V; f = 1 MHz.

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

7. Test information

7.1 Ruggedness in class-AB operation

The BLP10H630P and BLP10H630PG are capable of withstanding a load mismatch corresponding to VSWR > 40 : 1 through all phases under the following conditions: $V_{DS} = 50 \text{ V}$; $I_{Dq} = 20 \text{ mA}$; $P_L = 30 \text{ W pulsed}$; f = 720 MHz.

7.2 Impedance information

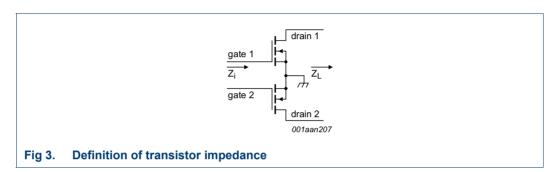


Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance; impedance info at V_{DS} = 50 V and P_L = 30 W.

f	Z _i	Z _L
(MHz)	(Ω)	(Ω)
720	13.8 – j37.6	32.4 + j47.0

7.3 Test circuit

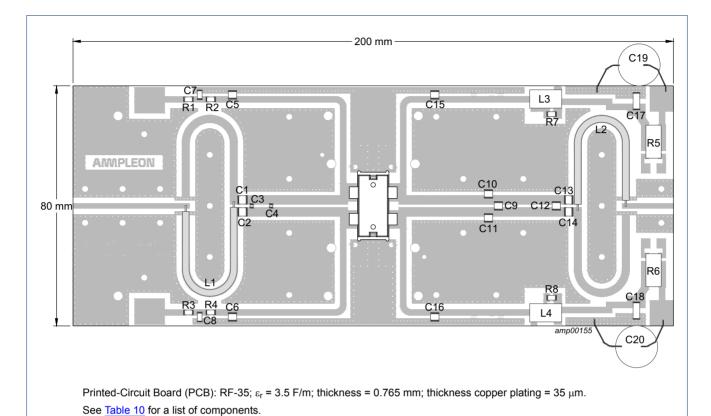


Table 10. List of components For test circuit see Figure 4.

Component layout for class-AB production test circuit

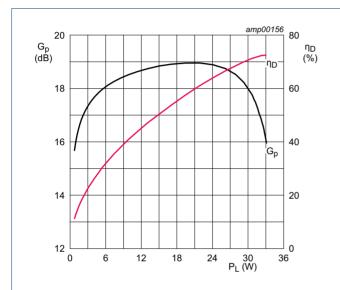
Component	Description	Value	Remarks
C1, C2	multilayer ceramic chip capacitor	33 pF	ATC 800B
C3	multilayer ceramic chip capacitor	4.3 pF	ATC 100A
C4	multilayer ceramic chip capacitor	4.3 pF	ATC 100A
C5, C6	multilayer ceramic chip capacitor	150 pF	ATC 100A
C7, C8	electrolytic capacitor	1 μF, 50 V	GRM32RR71H105KA01L
C9	multilayer ceramic chip capacitor	8.2 pF	ATC 800B
C10, C11	multilayer ceramic chip capacitor	12 pF	ATC 800B
C12	multilayer ceramic chip capacitor	7.5 pF	ATC 800B
C13, C14	multilayer ceramic chip capacitor	33 pF	ATC 800B
C15, C16	multilayer ceramic chip capacitor	150 pF	ATC 800B
C17, C18	multilayer ceramic chip capacitor	4.7 μF, 100 V	TDK: C5750X7R2A475KT/A
C19, C20	electrolytic capacitor	1000 μF, 63 V	Vishay
L1	coaxial balun	L = 64.8 mm	EZ_86_TP_M17
L2	coaxial balun	L = 64.8 mm	EZ_86_TP_M17
L3, L4	inductor	90 nH	132-9SMGL

Fig 4.

Table 10. List of components ...continued For test circuit see Figure 4.

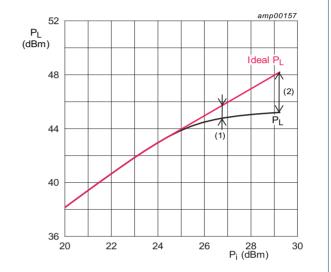
Component	Description	Value	Remarks
R1, R2, R3, R4	resistor	4.7 Ω	SMD 1206
R5, R6	resistor	50 mΩ, 5 W	FC4L110R010FER
R7, R8	resistor	7.5 Ω	SMD 1206

7.4 Graphical data



 V_{DS} = 50 V; I_{Dq} = 20 mA; f = 720 MHz; t_p = 100 μs ; δ = 20 %.

Fig 5. Power gain and drain efficiency as function of output power; typical values



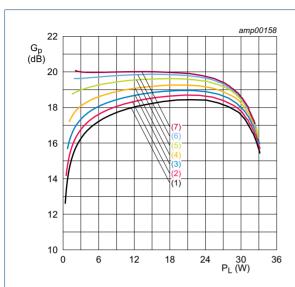
 V_{DS} = 50 V; I_{Dq} = 20 mA; f = 720 MHz; t_p = 100 μs ; δ = 20 %.

- (1) $P_{L(1dB)} = 44.8 \text{ dBm}$ (30 W) at $P_i = 26.8 \text{ dBm}$
- (2) $P_{L(3dB)} = 45.2 \text{ dBm}$ (33.1 W) at $P_i = 29.2 \text{ dBm}$

Fig 6. Output power as a function of input power; typical values

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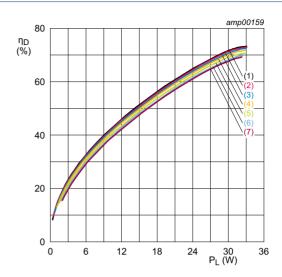
Power LDMOS transistor



 V_{DS} = 50 V; f = 720 MHz; t_p = 100 μ s; δ = 20 %.

- (1) $I_{Dq} = 5 \text{ mA}$
- (2) $I_{Dq} = 10 \text{ mA}$
- (3) $I_{Dq} = 20 \text{ mA}$
- (4) $I_{Dq} = 40 \text{ mA}$
- (5) $I_{Dq} = 80 \text{ mA}$
- (6) $I_{Dq} = 120 \text{ mA}$
- (7) $I_{Dq} = 150 \text{ mA}$

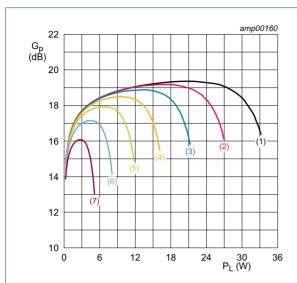
Fig 7. Power gain as a function of output power; typical values



 V_{DS} = 50 V; f = 720 MHz; t_p = 100 μ s; δ = 20 %.

- (1) $I_{Dq} = 5 \text{ mA}$
- (2) $I_{Dq} = 10 \text{ mA}$
- (3) $I_{Dq} = 20 \text{ mA}$
- (4) $I_{Dq} = 40 \text{ mA}$
- (5) $I_{Dq} = 80 \text{ mA}$
- (6) $I_{Dq} = 120 \text{ mA}$
- (7) $I_{Dq} = 150 \text{ mA}$

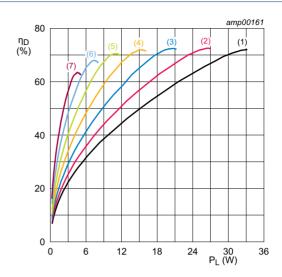
Fig 8. Drain efficiency as a function of output power; typical values



 I_{Dq} = 20 mA; f = 720 MHz; t_p = 100 $\mu s;$ δ = 20 %.

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$
- (4) $V_{DS} = 35 \text{ V}$
- (5) $V_{DS} = 30 \text{ V}$
- (6) $V_{DS} = 25 \text{ V}$
- (7) $V_{DS} = 20 \text{ V}$

Fig 9. Power gain as a function of output power; typical values



 I_{Dq} = 20 mA; f = 720 MHz; t_p = 100 μ s; δ = 20 %.

- (1) $V_{DS} = 50 \text{ V}$
- (2) $V_{DS} = 45 \text{ V}$
- (3) $V_{DS} = 40 \text{ V}$
- (4) $V_{DS} = 35 V$
- (5) $V_{DS} = 30 \text{ V}$ (6) $V_{DS} = 25 \text{ V}$
- (7) $V_{DS} = 20 \text{ V}$

Fig 10. Drain efficiency as a function of output power; typical values

8. Package outline

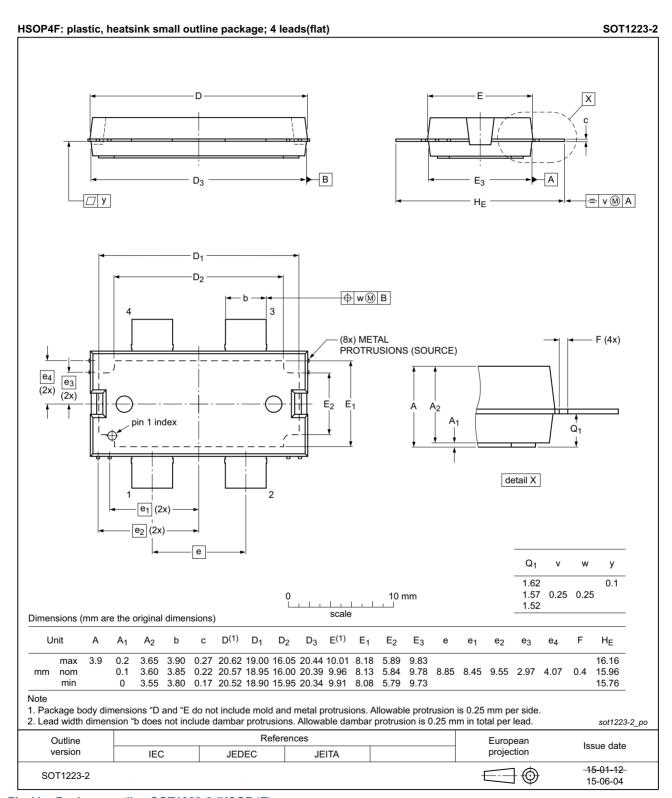


Fig 11. Package outline SOT1223-2 (HSOP4F)

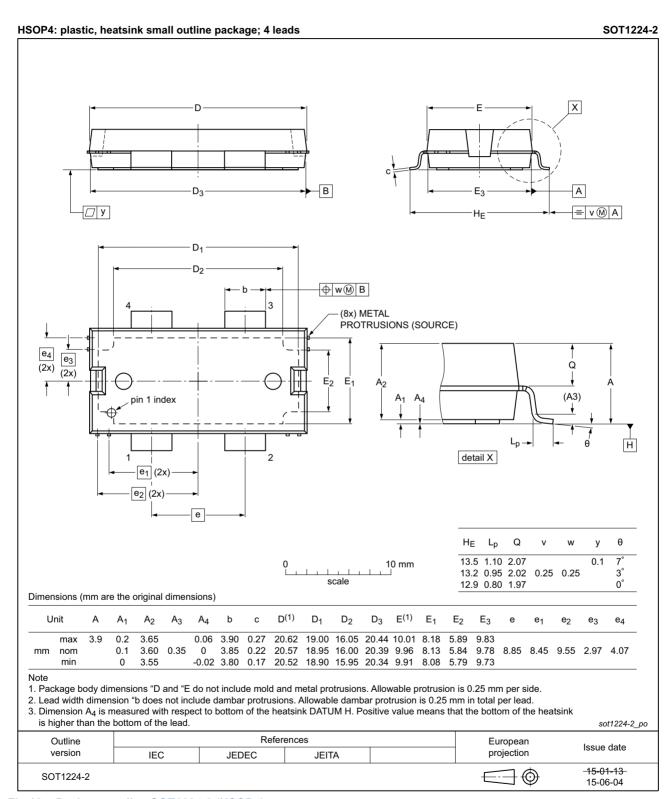


Fig 12. Package outline SOT1224-2 (HSOP4)

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C1 [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	1C 2

- [1] CDM classification C1 is granted to any part that passes after exposure to an ESD pulse of 250 V, but fails after exposure to an ESD pulse of 500 V.
- [2] HBM classification 1C is granted to any part that passes after exposure to an ESD pulse of 1000 V, but fails after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
HF	High Frequency
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MTF	Median Time to Failure
SMD	Surface Mounted Device
VSWR	Voltage Standing-Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLP10H630P_BLP10H630PG v.1	20161220	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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- [2] The term 'short data sheet' is explained in section "Definitions"
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BLP10H630P; BLP10H630PG

Power LDMOS transistor

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BLP10H630P; BLP10H630PG

Power LDMOS transistor

14. Contents

1	Product profile	1
1.1	General description	1
1.2	Features and benefits	1
1.3	Applications	1
2	Pinning information	2
3	Ordering information	2
4	Limiting values	2
5	Thermal characteristics	3
6	Characteristics	3
7	Test information	5
7.1	Ruggedness in class-AB operation	5
7.2	Impedance information	
7.3	Test circuit	
7.4	Graphical data	7
8	Package outline	. 10
9	Handling information	. 12
10	Abbreviations	
11	Revision history	. 12
12	Legal information	. 13
12.1	Data sheet status	. 13
12.2	Definitions	. 13
12.3	Disclaimers	. 13
12.4	Trademarks	. 14
13	Contact information	. 14
1/	Contants	15

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