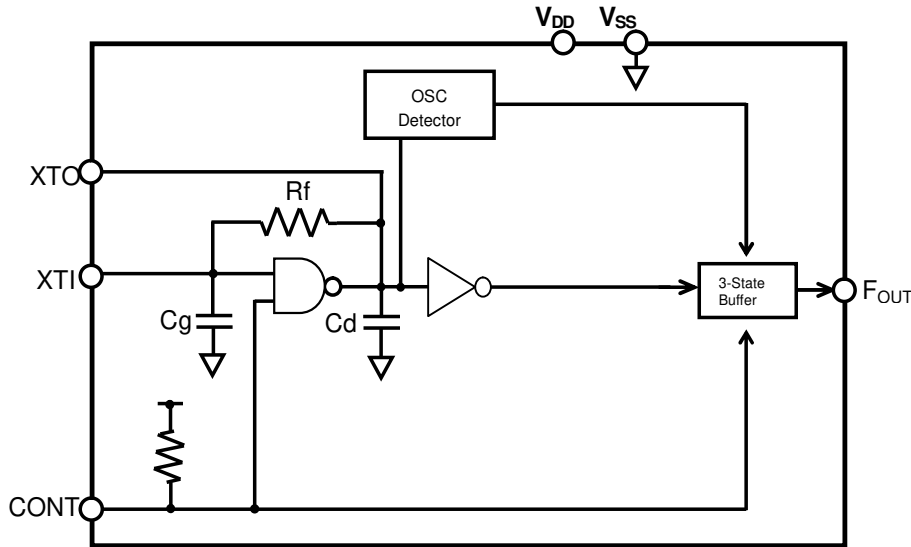
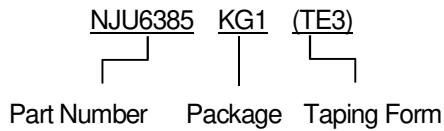




## ■BLOCK DIAGRAM



## ■PRODUCT NAME INFORMATION

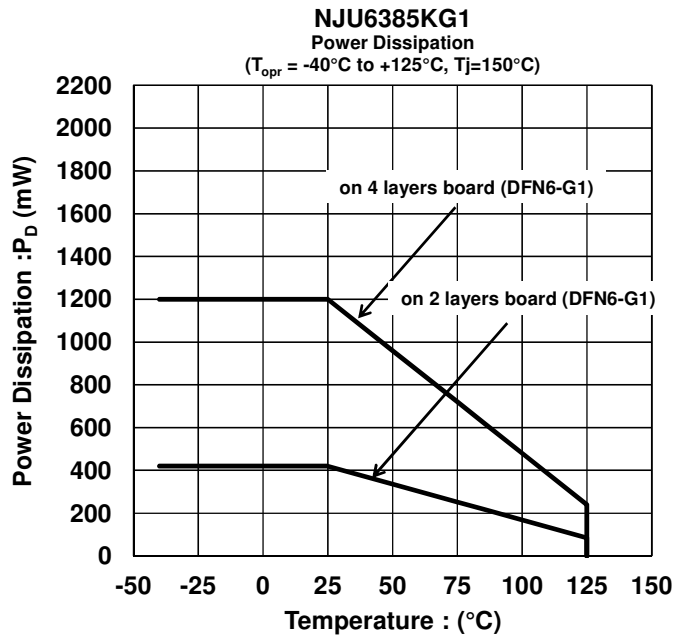


## ■ABSOLUTE MAXIMUM RATINGS <sup>(1)</sup>

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	$V_{DD}$	-0.6 to +6.0	V
Input Voltage	$V_{IN}$	-0.6 to $+V_{DD}+0.6$ and $\leq 6.0V$	V
Output Voltage	$V_O$	-0.6 to $V_{DD}+0.6$	V
Input Terminal Current	$I_{IN}$	$\pm 10$	mA
Output Terminal Current	$I_O$	$\pm 25$	mA
Power Dissipation ( $T_a=25^\circ C$ ) DFN6-G1(ESON6-G1) <sup>(2)</sup>	$P_D$	(2-layer / 4-layer) 420 / 1200	mW
Junction Temperature	$T_{jmax}$	+150	$^\circ C$
Operating Temperature Range	$T_{opr}$	-40 to +125	$^\circ C$
Storage Temperature Range	$T_{stg}$	-55 to +150	$^\circ C$

- (1) If the LSI used condition above the absolute maximum ratings, the LSI may be destroyed. Use beyond the electric characteristics conditions will cause mal-function and poor reliability.
- (2) Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 2Layers FR-4, with Exposed Pad)  
 Mounted on glass epoxy board. (101.5×114.5×1.6mm: based on EIA/JEDEC standard, 4Layers FR-4, with Exposed Pad)  
 \*For 4Layers: Applying 99.5×99.5mm inner Cu area and a thermal via hole to a board based on JEDEC standard JESD51-5

## ■POWER DISSIPATION vs. AMBIENT TEMPERATURE



## ■ELECTRICAL CHARACTERISTICS<sup>(4)</sup>

( $T_a=25^{\circ}\text{C}$ )

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Supply Voltage	$V_{DD}$	$f_{osc}=50\text{MHz}$	1.62	-	3.63	V
Input Voltage	$V_{IN}$	CONT	0	-	3.63	V
Output Voltage	$V_{OUT}$	$F_{OUT}$	0	-	$V_{DD}$	V
Output Frequency Stability	$df/f$	$V_{DD}\pm 10\%$	-	$\pm 1$	-	ppm

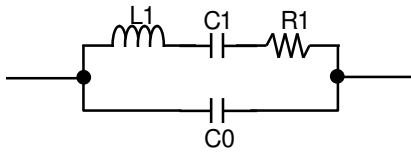
(V<sub>DD</sub>=1.62 to 3.63V, V<sub>SS</sub>=0V, T<sub>a</sub>=25°C)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT	
Operating Current	I <sub>DD</sub>	f <sub>0</sub> =49.152MHz No load TEST CIRCUIT(1) <sup>(3)</sup> F <sub>OUT</sub> =49.152MHz	V <sub>DD</sub> =1.8V	-	1.8	2.9	mA
			V <sub>DD</sub> =2.5V	-	3.3	4.8	
			V <sub>DD</sub> =3.3V	-	5.5	7.7	
		f <sub>0</sub> =49.152MHz C <sub>L</sub> =15pF TEST CIRCUIT(1) <sup>(3)</sup> F <sub>OUT</sub> =49.152MHz	V <sub>DD</sub> =1.8V	-	3.1	4.1	
			V <sub>DD</sub> =2.5V	-	5.1	6.6	
			V <sub>DD</sub> =3.3V	-	7.9	9.9	
Stand-by Current	I <sub>STB</sub>	TEST CIRCUIT(1) <sup>(3)</sup> CONT=V <sub>SS</sub>	V <sub>DD</sub> =1.8V	-	3.0	25.0	μA
			V <sub>DD</sub> =2.5V	-	5.0	30.0	
			V <sub>DD</sub> =3.3V	-	9.0	35.0	
H Level Output Voltage	V <sub>OH</sub>	TEST CIRCUIT(2) <sup>(3)</sup>	V <sub>DD</sub> -0.4	-	-	V	
L Level Output Voltage	V <sub>OL</sub>	TEST CIRCUIT(2) <sup>(3)</sup>	-	-	0.4	V	
H Level Input Voltage	V <sub>IH</sub>	TEST CIRCUIT(3) <sup>(3)</sup>	0.7V <sub>DD</sub>	-	-	V	
L Level Input Voltage	V <sub>IL</sub>	TEST CIRCUIT(3) <sup>(3)</sup>	-	-	0.3V <sub>DD</sub>	V	
Input Current	I <sub>IN</sub>	TEST CIRCUIT(4) <sup>(3)</sup> , V <sub>DD</sub> =1.62V, CONT=V <sub>DD</sub>	-	-	+65	nA	
		TEST CIRCUIT(4) <sup>(3)</sup> , V <sub>DD</sub> =1.62V, CONT=V <sub>SS</sub>	-	-	-0.5	μA	
		TEST CIRCUIT(4) <sup>(3)</sup> , V <sub>DD</sub> =3.63V, CONT=V <sub>DD</sub>	-	-	+150	nA	
		TEST CIRCUIT(4) <sup>(3)</sup> , V <sub>DD</sub> =3.63V, CONT=V <sub>SS</sub>	-10	-	-	μA	
3-state Off Leakage Current	I <sub>OZ</sub>	TEST CIRCUIT(5) <sup>(3)</sup> CONT=V <sub>SS</sub> , F <sub>OUT</sub> =V <sub>DD</sub> or V <sub>SS</sub>	-	-	±0.1	μA	
Feedback Resistance	R <sub>f</sub>		35	50	65	kΩ	
Built-In Oscillator Capacitance	C <sub>g</sub>	f <sub>OSC</sub> =50MHz	-	8	-	pF	
	C <sub>d</sub>	f <sub>OSC</sub> =50MHz	-	17	-	pF	
Oscillation Frequency	F <sub>OSC</sub>	Recommendation <sup>(4)</sup>	-	-	50	MHz	
Output Signal Symmetry	SYM	C <sub>L</sub> =15pF, @V <sub>DD</sub> /2, TEST CIRCUIT(1) <sup>(3)</sup>	45	50	55	%	
Phase Noise	SSB	f <sub>OSC</sub> =49.152MHz V <sub>DD</sub> =1.8V	10Hz Offset	-	-103	-	dBc /Hz
			1kHz Offset	-	-158	-	
			Floor	-	-166	-	
		f <sub>OSC</sub> =49.152MHz V <sub>DD</sub> =3.3V	10Hz Offset	-	-103	-	
			1kHz Offset	-	-163	-	
			Floor	-	-172	-	
Output Signal rise Time	tr	TEST CIRCUIT(1) <sup>(3)</sup> 0.1V <sub>DD</sub> to 0.9V <sub>DD</sub>	V <sub>DD</sub> =1.8V	-	3.1	4.7	ns
			V <sub>DD</sub> ≥ 2.5V	-	1.8	2.7	ns
Output Signal fall Time	tf	TEST CIRCUIT(1) <sup>(3)</sup> 0.9V <sub>DD</sub> to 0.1V <sub>DD</sub>	V <sub>DD</sub> =1.8V	-	2.8	4.2	ns
			V <sub>DD</sub> ≥ 2.5V	-	1.8	2.7	ns
Output Disable Time	t <sub>POZ</sub>	TEST CIRCUIT(6) <sup>(3)</sup>	-	-	200	ns	
Output Enable Time	t <sub>PZO</sub>	TEST CIRCUIT(6) <sup>(3)</sup>	-	-	1	ms	
Oscillation Start-Up Time	t <sub>OSC</sub>	TEST CIRCUIT(1) <sup>(3)</sup>	-	-	1	ms	

(3) Decoupling capacitor over than 0.01μF ceramic capacitor should be connected between V<sub>DD</sub> and V<sub>SS</sub> due to the stabilized operation for the circuit.

(4) NJR's standard crystal is used for measurement of the oscillation frequency range and it does not guarantee oscillation. (Refer to EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUITS)

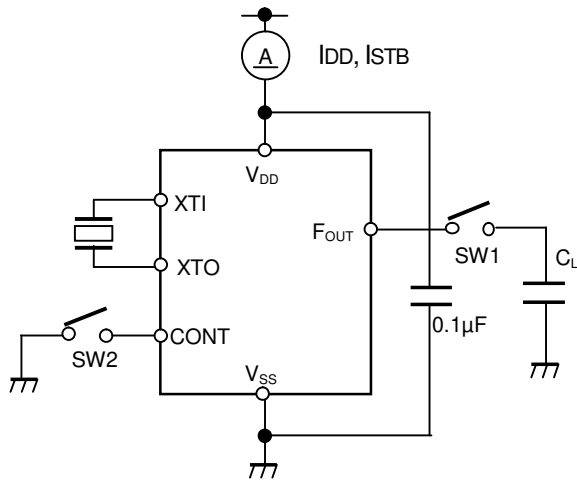
■EXAMPLE OF CRYSTAL PARAMETERS FOR MEASUREMENT CIRCUITS



f [MHz]	R1 [ $\Omega$ ]	L1 [mH]	C1 [fF]	C0 [pF]
49.152	17.7	3.83	2.74	1.23

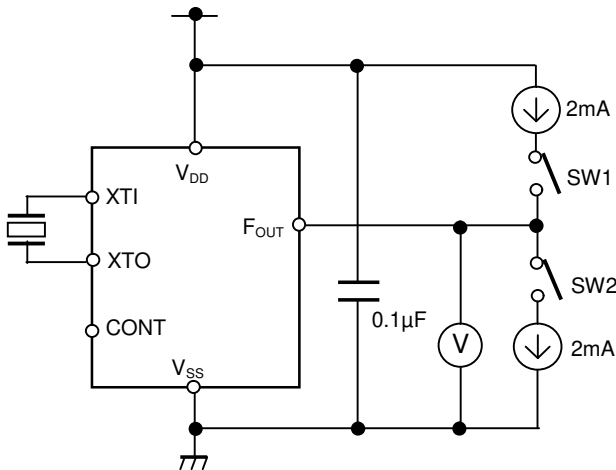
## ■ TYPICAL TEST CIRCUIT

(1) Operating Current, Stand-by Current, Output Signal rise / Fall Time, Oscillation Start-Up Time



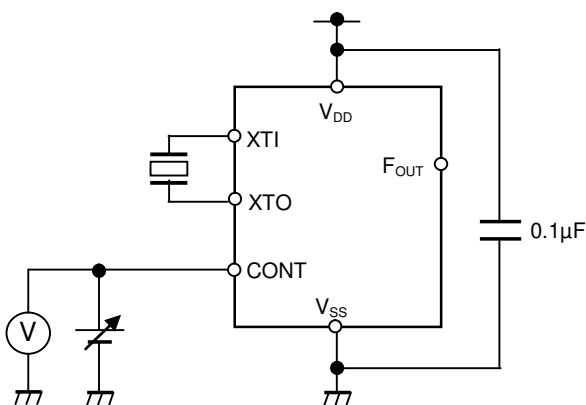
PARAMETER	SW1	SW2
$I_{DD} (C_L=0pF)$	OFF	OFF
$I_{DD} (C_L=15pF)$	ON	OFF
ISTB	ON or OFF	ON
SYM, tr, tf	ON	OFF
tosc	ON	OFF

(2) High-level / Low-level Output Voltage ( $V_{OH} / V_{OL}$ )



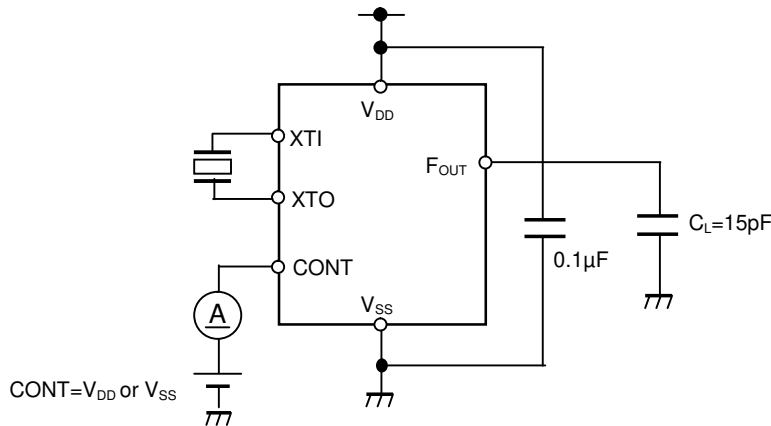
PARAMETER	SW1	SW2
$V_{OH}$	OFF	ON
$V_{OL}$	ON	OFF

(3) High-level / Low-level Input Voltage ( $V_{IH} / V_{IL}$ )

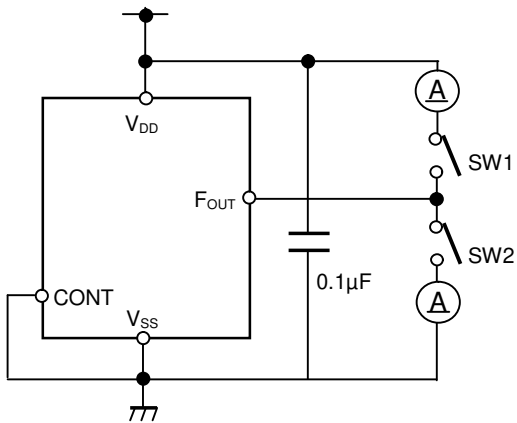


PARAMETER	FOUT
$CONT > 0.7V_{DD}$	Oscillation
$CONT \leq 0.3V_{DD}$	Stop

### (4) Input Current ( $I_{IN}$ )

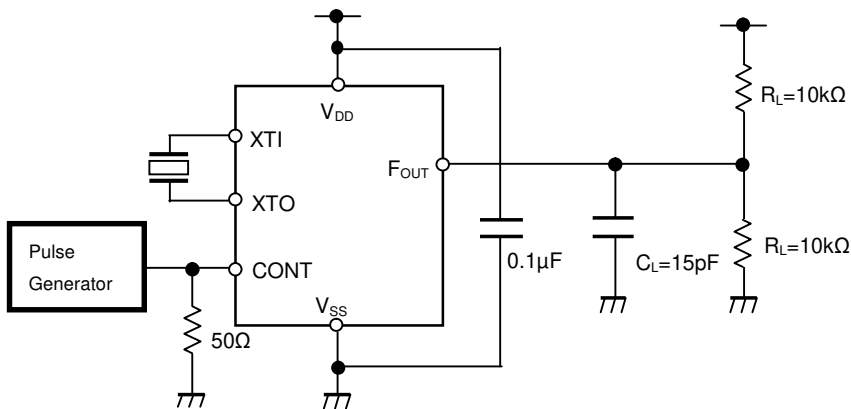


### (5) 3-State Off Leakage Current ( $I_{OZH}$ / $I_{OZL}$ )



PARAMETER	SW1	SW2
$I_{OZH}$	OFF	ON
$I_{OZL}$	ON	OFF

### (6) Output Disable Time, Output Enable Time ( $t_{POZ}$ / $t_{PZO}$ )



## ■TIMING CHART

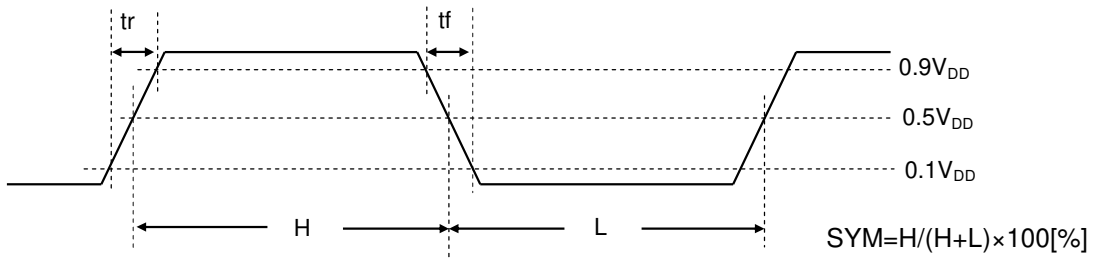


Fig.1 Output Signal Rise Time:  $t_r$ , Output Signal Fall Time:  $t_f$ , Output Symmetry: SYM

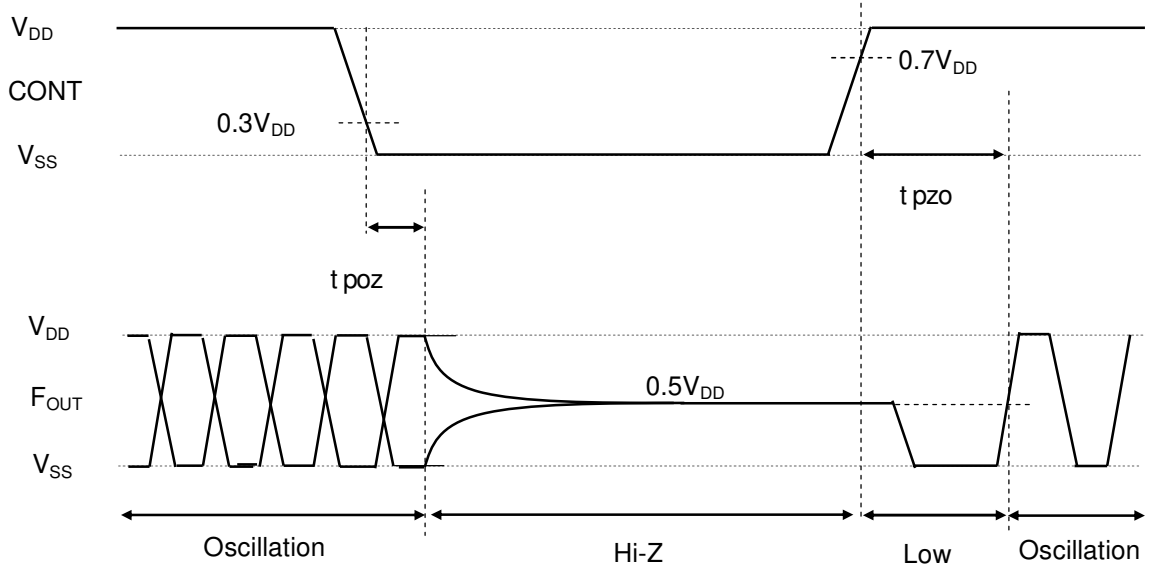


Fig.2 Output Disable time:  $t_{poz}$ , Output Enable time:  $t_{poz}$ .

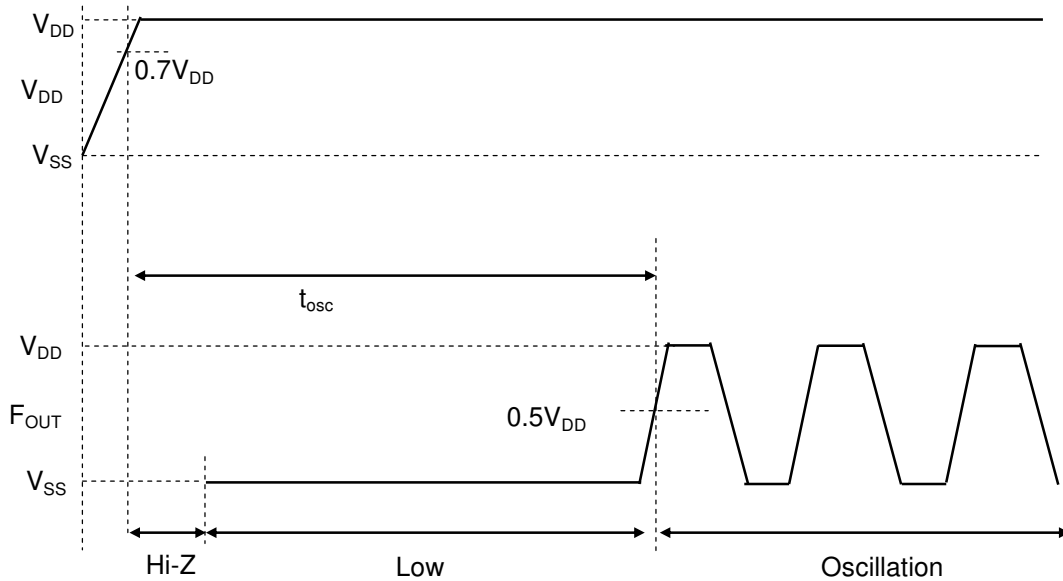
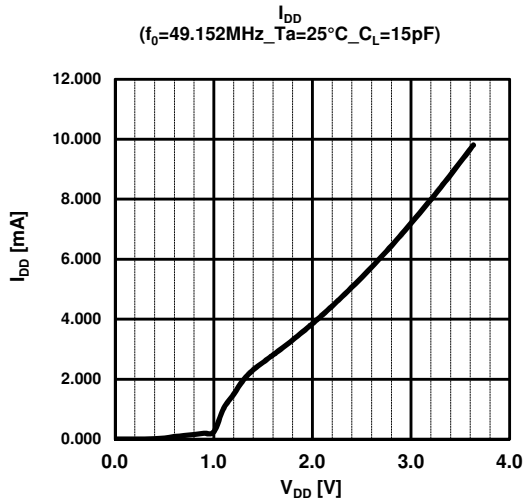


Fig.3 Oscillation Start time:  $t_{osc}$

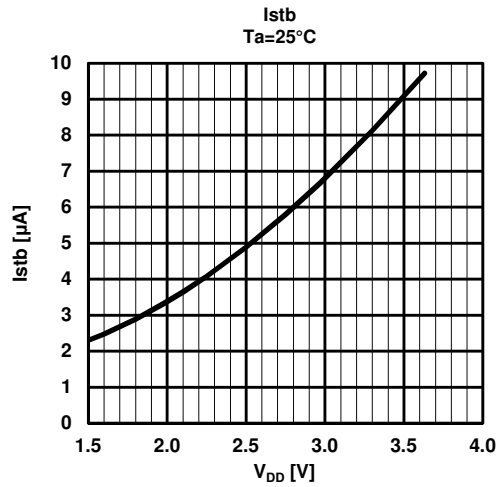


## ■ TYPICAL CHARACTERISTICS

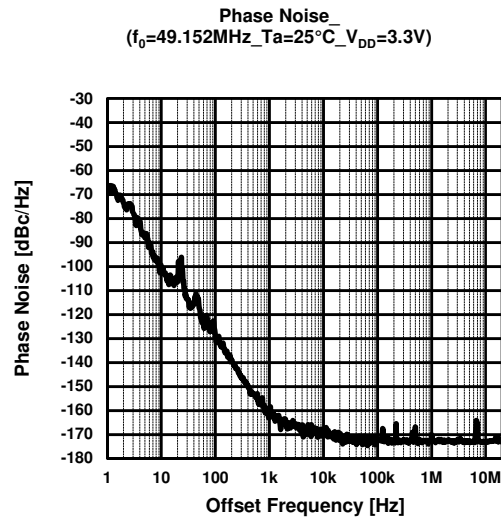
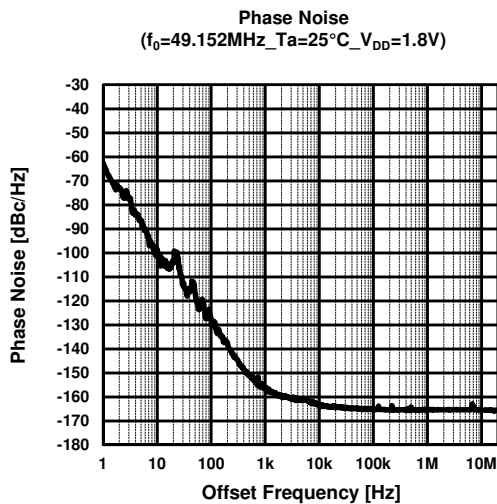
### • Operating Current



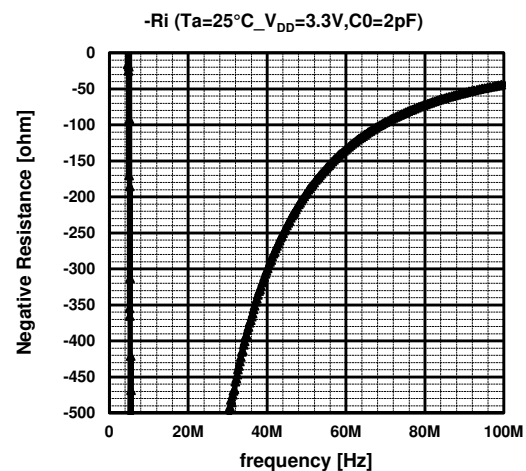
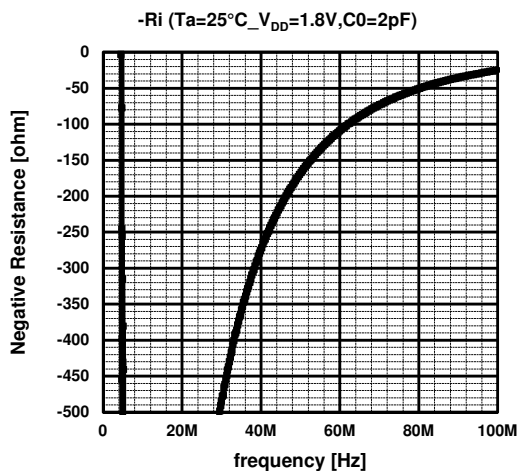
### • Stand-by Current



### • Phase Noise

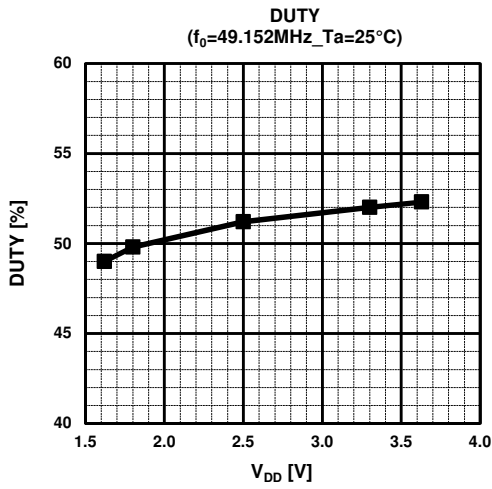


### • Negative Resistance

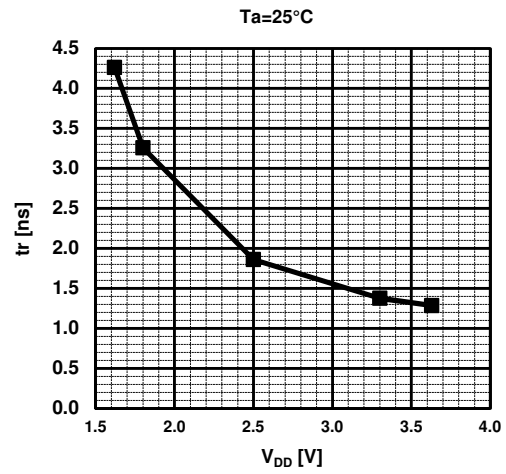


Note; A negative resistance 3 to 5 times the equivalent series resistance is said to be required for sufficient oscillation margin.

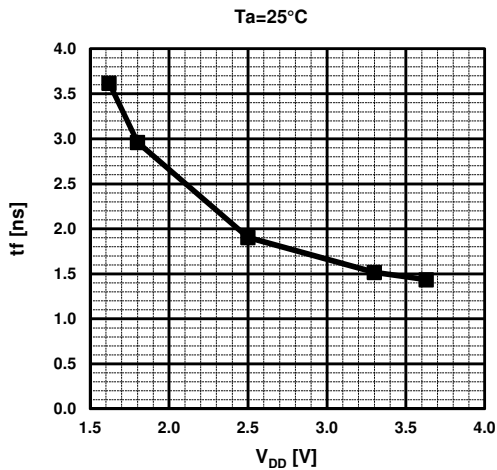
• Output Signal Symmetry



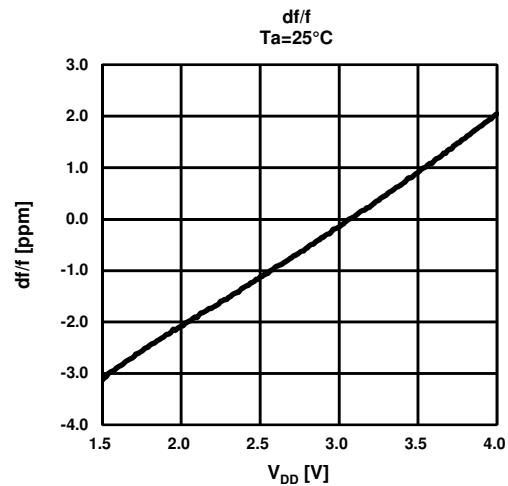
• Output Signal rise Time



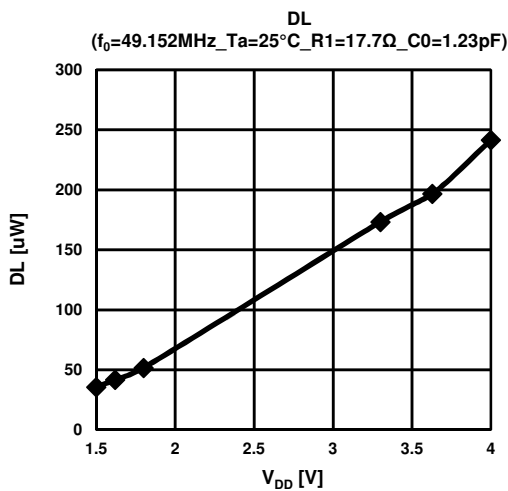
• Output Signal fall Time



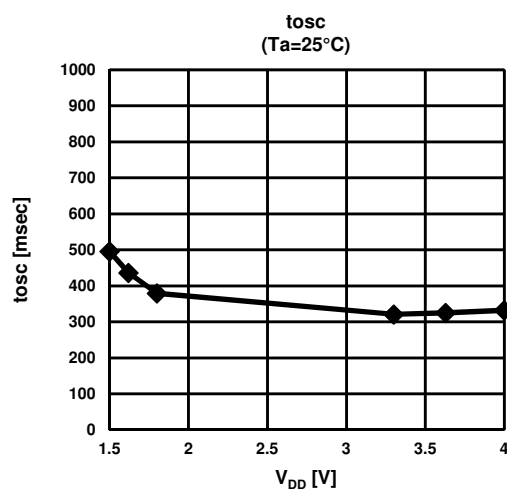
• Output Frequency Stability



• Drive Level



• Oscillation Start-Up Time



## Application Note

### FUNCTIONAL DESCRIPTION

•Standby Function

When CONT Terminal is “Low”, the F<sub>OUT</sub> Terminal output is High impedance.

CONT	F <sub>OUT</sub>	Oscillator
High(Open)	Frequency output	Normal operation
Low	High impedance	Stop

When not using Stand-by function, CONT terminal is recommended to connect to V<sub>DD</sub>.

•Built-in Variable Pull-up Resistance of CONT terminal

The built-in pull-up resistance value of CONT Terminal changes in response to the input level. When CONT is “Low” level, the pull-up resistance value is large to reduce the current consumption by the resistance. When CONT is open or connected to V<sub>DD</sub>, the pull-up resistance value is small to decrease the input susceptibility to external noise. It works to prevent an unexpectedly stopping of the output by external noise.

### Choice of crystal at notice

Standard crystal unit example

	Dxx2520xx
Frequency Range	30 to 54 MHz
Overtone Order	Fundamental

Equivalent Series Resistance	50Ω max.
Drive Level	10μW (Max. 200μW)
Load Capacitance	8, 12, 15 pF

■ This range is related to crystal oscillation IC.

Equivalent Series Resistance: Equivalent resistance of crystal unit when series resonance.( refer to perspective of -R<sub>i</sub> )

Drive Level: Loading condition of crystal resonator, which is determined by electric current or power.

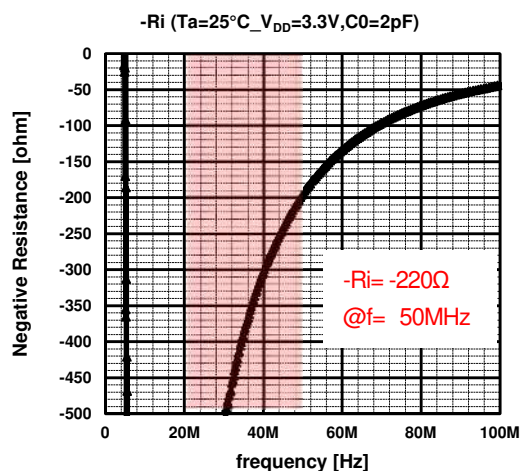
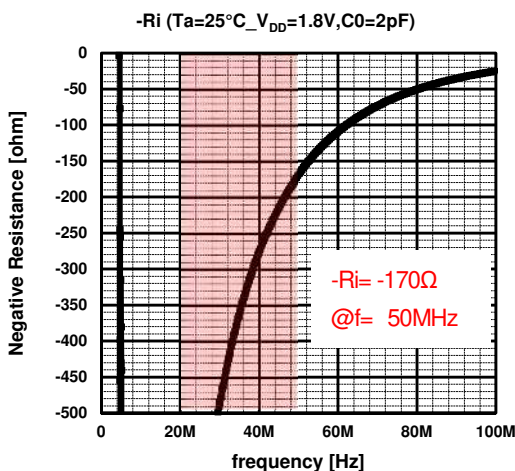
( refer to perspective of drive level )

Load Capacitance: The effective external capacitance that determines the resonance frequency of a crystal resonator.

( refer to A formula of load capacitance. )

### Perspective of -R<sub>i</sub>

■ :NJU6385 Oscillation Frequency Range.( 20MHz to 50MHz )

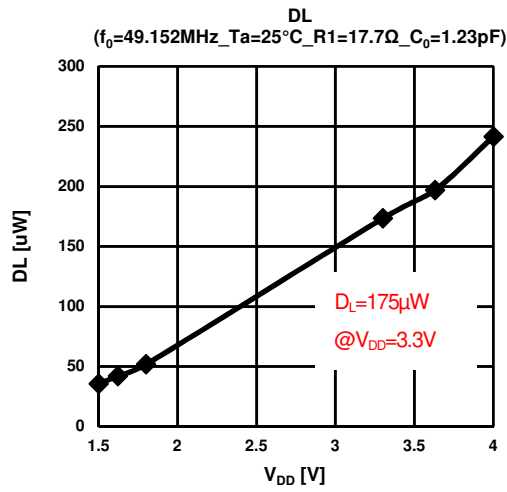


Note: A negative resistance 3 to 5 times the equivalent series resistance is said to be required for sufficient oscillation margin.

### Perspective of Drive Level

According to graph,  $D_L = 175\mu W$  at  $V_{DD} = 3.3V$ ,  $f = 49.1592MHz$

We recommend the high drive level crystal unit. example  $200\mu W$  [max.]



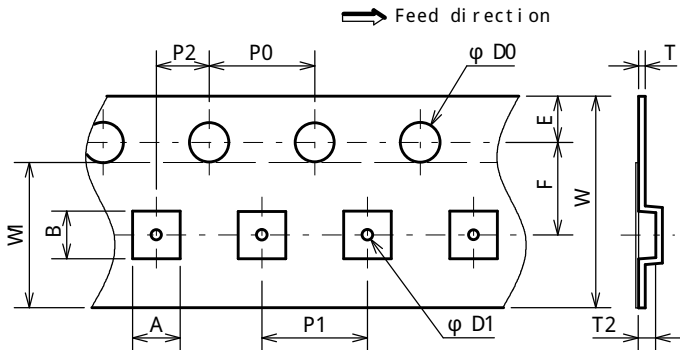
A formula of Load Capacitance. ( In case of internal capacitance of NJU6385 )

$$C_L = C_g \times C_d / ( C_g + C_d ) = 8pF \times 17pF / ( 8pF + 17pF ) \approx \underline{5.44pF} \quad \leftarrow \text{Load Capacitance of crystal unit.}$$



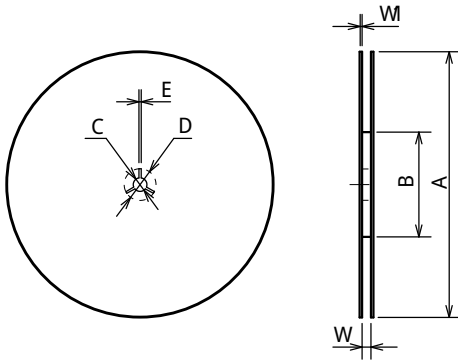
### PACKING SPEC

#### TAPING DIMENSIONS



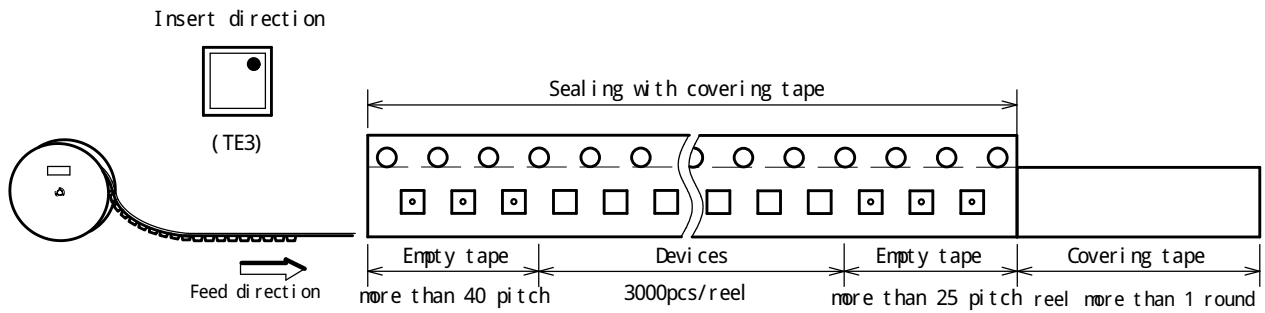
SYMBOL	DI MENSION	REMARKS
A	1.85± 0.05	BOTTOM DI MENSION
B	1.85± 0.05	BOTTOM DI MENSION
D0	1.5 <sup>+0.1</sup> <sub>0</sub>	
D1	0.5± 0.1	
E	1.75± 0.1	
F	3.5± 0.05	
P0	4.0± 0.1	
P1	4.0± 0.1	
P2	2.0± 0.05	
T	0.25± 0.05	
T2	0.65± 0.05	
W	8.0± 0.2	
Wt	5.5	THICKNESS 0.1max

#### REEL DIMENSIONS

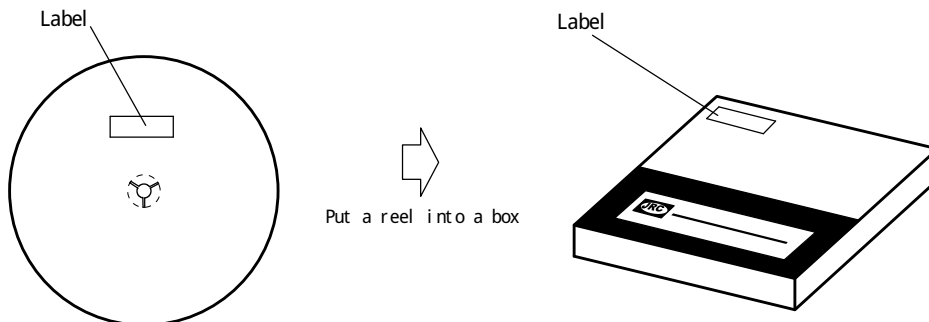


SYMBOL	DI MENSION
A	φ 180 <sup>0</sup> <sub>-1.5</sub>
B	φ 60 <sup>+1</sup> <sub>0</sub>
C	φ 13± 0.2
D	φ 21± 0.8
E	2± 0.5
W	9 <sup>+0.3</sup> <sub>0</sub>
Wt	1.2

#### TAPING STATE

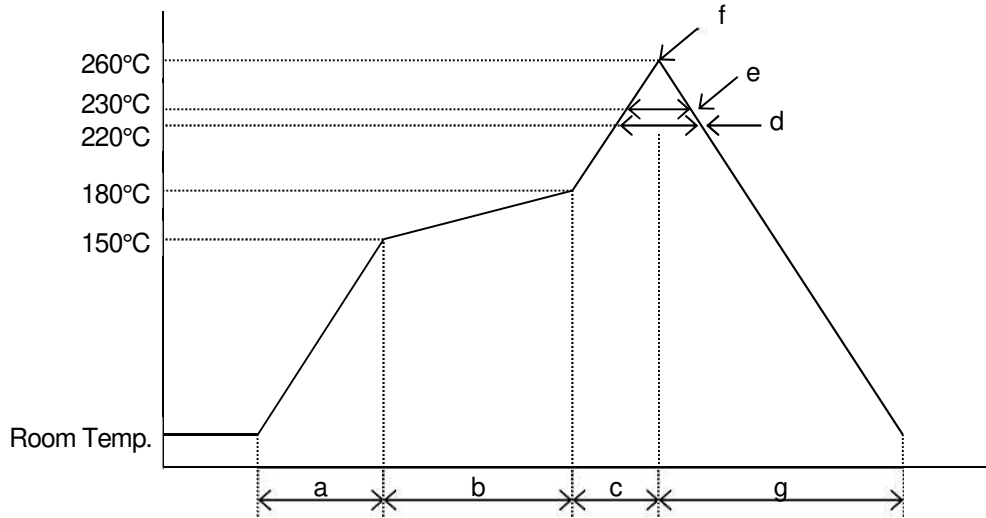


#### PACKING STATE



**RECOMMENDED MOUNTING METHOD**

\*Recommended reflow soldering procedure



- a: Temperature ramping rate : 1 to 4°C/s
- b: Pre-heating temperature : 150 to 180°C  
time : 60 to 120s
- c: Temperature ramp rate : 1 to 4°C/s
- d: 220°C or higher time : Shorter than 60s
- e: 230°C or higher time : Shorter than 40s
- f: Peak temperature : Lower than 260°C
- g: Temperature ramping rate : 1 to 6°C/s

\*The temperature indicates at the surface of mold package.

**REVISION HISTORY**

Date	Revision	Changes
24.Apr.2018	Ver.0	First edition
06.Jun.2018	Ver.1	P.6, P.7 ■ TYPICAL TEST CIRCUIT : Replacement of TYPICAL CIRCUIT
		P.8 ■ TIMING CHART: Unification of terms. ( Change to SYM from DUTY)
12.Feb.2019	Ver.2	P.11, P.12 ■ Application Note: In addition, Chose select crystal unit
13.Oct.2020	Ver.3	P.2 ■ BLOCK DIAGRAM: In addition, V <sub>DD</sub> and V <sub>SS</sub> terminals. ■ ABSOLUTE MAXIMUM RATINGS: UNIT: Output Voltage is replace to mA to V PARAMETER: The Output Terminal Input Voltage replace to Output Current
		P.4 ■ ELECTRICAL CHARACTERISTICS: 3-state Off Leakage Current: The Maximum value is change to ±0.1μA(Max.).
14.Oct.2020	Ver.4	P.1 ■ TERMINAL DISCREPTION: CONT: In Addition, ( f <sub>0</sub> )
		P.4 ■ ELECTRICAL CHARACTERISTICS: Output Signal Symmetry condition: In Addition, TEST CIRCUIT(1)(3).

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9. The product specifications and descriptions listed in this datasheet are subject to change at any time, without notice.

