16-Channel, 16-Bit, ES-PWM LED Driver with Full Self-Diagnosis for LED Lamp with 7-Bit DC and 7-Bit Global BC

Check for Samples: TLC5948

FEATURES

- **16 Constant-Current Sink Output Channels**
- **Sink Current Capability with Max DC/BC Data:**
  - **2 mA to 45 mA (V_{CC} ≤ 3.6 V)**
  - **2 mA to 60 mA (V_{CC} > 3.6 V)**
- **Dot Correction (DC):**
  - **7-Bit (128 Steps) with 0% to 100% Range**
- **Global Brightness Control (BC):**
  - **7-Bit (128 Steps) with 25% to 100% Range**
- **Grayscale Control (GS) with Enhanced Spectrum or Conventional PWM:**
  - **16-Bit (65,536 Steps)**
- **LED Power-Supply Voltage: Up to 10 V**
- **VCC: 3.0 V to 5.5 V**
- **Constant-Current Accuracy:**
  - **Channel-to-Channel: ±0.6% (typ), ±2% (max)**
  - **Device-to-Device: ±1% (typ), ±4% (max)**
- **Data Transfer Rate: 33 MHz**
- **Grayscale Control Clock: 33 MHz**
- **Auto Display Repeat/Auto Data Refresh**
- **Display Timing Reset**
- **Power-Save Mode to Minimize VCC Current**
- **LOD/LSD with Invisible Detection Mode (IDM)**
- **Output Leakage Detection (OLD)**
- **Current Reference Terminal Short Flag (ISF)**
- **Thermal Shutdown (TSD) and Error Flag (TEF)**
- **Pre-Thermal Warning (PTW)**
- **Four-Channel Grouped Delay Switching to Prevent Inrush Current**
- **Operating Temperature: –40°C to +85°C**

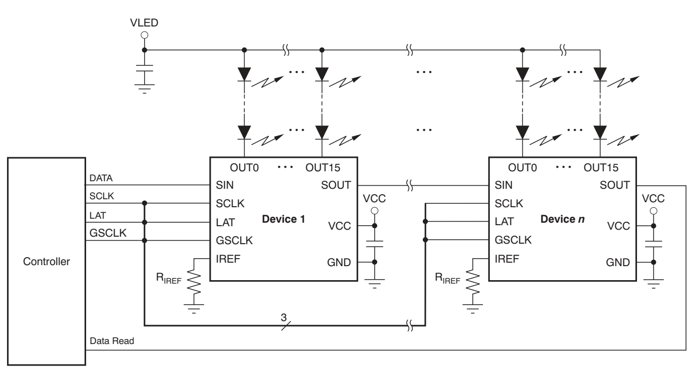
APPLICATIONS

- **LED Video Displays**
- **LED Signboards**

DESCRIPTION

The TLC5948 is a 16-channel, constant-current sink LED driver. Each channel has an individually-adjustable, pulse width modulation (PWM) grayscale (GS) brightness control with 65,536 steps and 128 steps of constant-current dot correction (DC). DC adjusts brightness deviation between channels. All channels have a 128-step global brightness control (BC). BC adjusts brightness deviation with other LED drivers. GS, DC, and BC data are accessible via a serial interface port.

The TLC5948 has six error flags: LED open detection (LOD), LED short detection (LSD), output leakage detection (OLD), reference current terminal short flag detection (ISF), pre-thermal warning (PTW), and thermal error flag (TEF). The error detection results can be read via a serial interface port.



Typical Application Circuit (Multiple Daisy-Chained TLC5948s)

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
TLC5948	SSOP/QSOP-24	DBQ	TLC5948DBQR	Tape and Reel, 2500
			TLC5948DBQ	Tube, 50
	HTSSOP-24 PowerPAD™	PWP	TLC5948PWPR	Tape and Reel, 2000
			TLC5948PWP	Tube, 60

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder at www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

Over operating free-air temperature range, unless otherwise noted.

		VALUE		UNIT
		MIN	MAX	
Voltage(2)	VCC	–0.3	+6.0	V
	SIN, SCLK, LAT, GSCLK, IREF	–0.3	V_{CC} + 0.3	V
	SOUT	–0.3	V_{CC} + 0.3	V
	OUT0 to OUT15	–0.3	+11	V
Current	OUT0 to OUT15		+70	mA
Temperature	Operating junction, T_J (max)		+150	°C
	Storage, T_{stg}	–55	+150	°C
Electrostatic discharge ratings	Human body model (HBM)		4000	V
	Charged device model (CDM)		2000	V

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under R*ecommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods my affect device reliability.
(2) All voltages are with respect to device ground terminal.

THERMAL INFORMATION

THERMAL METRIC(1)		TLC5948		UNITS
		DBQ	PWP	
		24 PINS	24 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	80.4	39.9	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	44.2	23.2	
θ_{JB}	Junction-to-board thermal resistance	33.5	21.5	
ψ_{JT}	Junction-to-top characterization parameter	8.8	0.6	
ψ_{JB}	Junction-to-board characterization parameter	33.2	21.3	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	N/A	3.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

RECOMMENDED OPERATING CONDITIONS

At T_A = –40°C to +85°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5948 MIN	TLC5948 NOM	TLC5948 MAX	UNIT
DC Characteristics: V_{CC} = 3 V to 5.5 V						
V_{CC}	Supply voltage		3.0		5.5	V
V_O	Voltage applied to output	OUT0 to OUT15			10	V
V_{IH}	High-level input voltage	SIN, SCLK, LAT, GSCLK	0.7 × V_{CC}		V_{CC}	V
V_{IL}	Low-level input voltage	SIN, SCLK, LAT, GSCLK	GND		0.3 × V_{CC}	V
I_{OH}	High-level output current	SOUT			–2	mA
I_{OL}	Low-level output current	SOUT			2	mA
I_{OLC}	Constant output sink current	OUT0 to OUT15, 3 V ≤ V_{CC} ≤ 3.6 V			45	mA
		OUT0 to OUT15, 3.6 V < V_{CC} ≤ 5.5 V			60	mA
T_A	Operating free-air temperature range		–40		+85	°C
T_J	Operating junction temperature range		–40		+125	°C
AC Characteristics: V_{CC} = 3 V to 5.5 V						
$f_{CLK\ (SCLK)}$	Data shift clock frequency	SCLK			33	MHz
$f_{CLK\ (GSCLK)}$	Grayscale control clock frequency	GSCLK			33	MHz
t_{WH0}	Pulse duration	SCLK	10			ns
t_{WL0}		SCLK	10			ns
t_{WH1}		GSCLK	10			ns
t_{WL1}		GSCLK	10			ns
t_{WH2}		LAT	30			ns
t_{SU0}	Setup time	SIN↑↓ to SCLK↑	5			ns
t_{SU1}		LAT↑ to SCLK↑	120			ns
t_{SU2}		LAT↑ for BLANK bit '0' set to GSCLK↑	50			ns
t_{SU3}		LAT↑ for GS data written to GSCLK↑ when display time reset mode is enabled	100			ns
t_{H0}	Hold time	SCLK↑ to SIN↑↓	5			ns
t_{H1}		SCLK↑ to LAT↑	5			ns

ELECTRICAL CHARACTERISTICS

At V_{CC} = 3 V to 5.5 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS		TLC5948 MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (SOUT)	I_{OH} = –2 mA		V_{CC} – 0.4		V_{CC}	V
V_{OL}	Low-level output voltage (SOUT)	I_{OL} = 2 mA				0.4	V
V_{LOD0}	LED open detection threshold	All OUT*n* = on, detection voltage code = 0h		0.25	0.30	0.35	V
V_{LOD1}		All OUT*n* = on, detection voltage code = 1h		0.55	0.6	0.65	V
V_{LOD2}		All OUT*n* = on, detection voltage code = 2h		0.85	0.9	0.95	V
V_{LOD3}		All OUT*n* = on, detection voltage code = 3h		1.15	1.2	1.25	V
V_{LSD0}	LED short detection threshold	All OUT*n* = on, detection voltage code = 0h		0.30 × V_{CC}	0.35 × V_{CC}	0.40 × V_{CC}	V
V_{LSD1}		All OUT*n* = on, detection voltage code = 1h		0.40 × V_{CC}	0.45 × V_{CC}	0.50 × V_{CC}	V
V_{LSD2}		All OUT*n* = on, detection voltage code = 2h		0.50 × V_{CC}	0.55 × V_{CC}	0.60 × V_{CC}	V
V_{LSD3}		All OUT*n* = on, detection voltage code = 3h		0.60 × V_{CC}	0.65 × V_{CC}	0.70 × V_{CC}	V
V_{IREF}	Reference voltage output	R_{IREF} = 1.1 kΩ		1.17	1.20	1.23	V
I_{IN}	Input current (SIN, SCLK, LAT, GSCLK)	V_{IN} = V_{CC} or GND		–1		1	µA
I_{CC0}	Supply current (V_{CC})	SIN/SCLK/LAT/GSCLK = GND, BLANK = 1, GS*n* = FFFFh, DC*n*/BC = 7Fh, V_{OUTn} = 0.8 V, R_{IREF} = open (all outputs off)			1.5	3	mA
I_{CC1}		SIN/SCLK/LAT/GSCLK = GND, BLANK = 1, GS*n* = FFFFh, DC*n*/BC = 7Fh, V_{OUTn} = 0.8 V, R_{IREF} = 2.2 kΩ (all outputs off, I_{OUTn} = 23.1 mA target)			5	7	mA
I_{CC2}		SIN/SCLK/LAT = GND, BLANK = 0, auto display repeat enabled, GSCLK = 33 MHz, GS*n* = FFFFh, DC*n*/BC = 7Fh, V_{OUTn} = 0.8 V, R_{IREF} = 2.2 kΩ (I_{OUT} = 23.1 mA target)			7	9	mA
I_{CC3}		SIN/SCLK/LAT = GND, BLANK = 0, auto display repeat enabled, GSCLK = 33 MHz, GS*n* = FFFFh, DC*n*/BC = 7Fh, V_{OUTn} = 0.8 V, R_{IREF} = 1.1 kΩ (I_{OUT} = 46.1 mA target)			11	14	mA
I_{CC4}		V_{CC} = 5.0 V, SIN/SCLK/LAT = GND, BLANK = 0, auto display repeat enabled, GSCLK = 33 MHz, GS*n* = FFFFh, DC*n*/BC = 7Fh, V_{OUTn} = 0.8 V, R_{IREF} = 0.91 kΩ (I_{OUT} = 55.8 mA target)			13	18	mA
I_{CC5}		V_{CC} = 5.0 V, SIN/SCLK/LAT/GSCLK = GND, BLANK = 0, auto display repeat enabled, GS*n* = 0000h, DC*n*/BC = 7Fh, in power-save mode, V_{OUTn} = 0.8 V, R_{IREF} = 0.91 kΩ (I_{OUT} = 55.8 mA target)			10	40	µA
I_{OLC0}	Constant output sink current (OUT0 to OUT15)	All OUT*n* = on, DC*n*/BC = 7Fh, V_{OUTn} = V_{OUTfix} = 0.8 V, R_{IREF} = 1.1 kΩ, T_A = +25°C (I_{OLCn} = 46.1 mA target)		43.4	46.1	48.8	mA
I_{OLC1}		V_{CC} = 5.0 V, All OUT*n* = on, DC*n*/BC = 7Fh, V_{OUTn} = V_{OUTfix} = 0.8 V, R_{IREF} = 0.91 kΩ, T_A = +25°C (I_{OLCn} = 55.8 mA target)		52.5	55.8	59.1	mA
I_{OLKG0}	Output leakage current (OUT0 to OUT15)	All OUT*n* = off, BLANK = 1, V_{OUTn} = V_{OUTfix} = 10 V, R_{IREF} = 1.1 kΩ	T_J = +25°C			0.1	µA
I_{OLKG1}			T_J = +85°C(1)			0.2	µA
I_{OLKG2}			T_J = +125°C(1)		0.3	0.8	µA

(1) Not tested; specified by design.

ELECTRICAL CHARACTERISTICS (continued)

At V_{CC} = 3 V to 5.5 V and T_A = –40°C to +85°C. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5948 MIN	TLC5948 TYP	TLC5948 MAX	UNIT
ΔI_{OLC0}	Constant-current error (channel-to-channel, OUT0 to OUT15)(2)	All OUT*n* = on, DC*n*/BC = 7Fh, V_{OUTn} = V_{OUTfix} = 0.8 V, R_{IREF} = 1.1 kΩ, T_A = +25°C (I_{OUTn} = 46.1 mA target)		±0.6	±2	%
ΔI_{OLC1}	Constant-current error (device-to-device, OUT0 to OUT15)(3)	All OUT*n* = on, DC*n*/BC = 7Fh, V_{OUTn} = V_{OUTfix} = 0.8 V, R_{IREF} = 1.1 kΩ, T_A = +25°C (I_{OUTn} = 46.1 mA target)		±1	±4	%
ΔI_{OLC2}	Line regulation (OUT0 to OUT15)(4)	V_{CC} = 3.0 V to 5.5 V, all OUT*n* = on, DC*n*/BC = 7Fh, V_{OUTn} = V_{OUTfix} = 0.8 V, R_{IREF} = 1.1 kΩ (I_{OUTn} = 46.1 mA target)		±0.1	±1	%/V
ΔI_{OLC3}	Load regulation (OUT0 to OUT15)(5)	All OUT*n* = on, DC*n*/BC = 7Fh, V_{OUTn} = 0.8 V to 3.0 V, V_{OUTfix} = 0.8 V, R_{IREF} = 1.1 kΩ (I_{OUTn} = 46.1 mA target)		±0.1	±1	%/V
T_{TEF}	Thermal error flag threshold	Junction temperature(6)	150	165	180	°C
T_{HYS}	Thermal error flag hysteresis	Junction temperature(6)	5	10	20	°C
T_{PTW}	Pre-thermal warning threshold	Junction temperature(6)	125	138	150	°C

(2) The deviation of each output from the average of OUT0 to OUT15 constant-current. Deviation is calculated by the formula:

$$\Delta(\%) = 100 \times \left(\frac{I_{OLC(n)}}{\left[\frac{(I_{OLC(0)} + I_{OLC(1)} + \cdots + I_{OLC(14)} + I_{OLC(15)})}{16}\right]} - 1 \right)$$

where n = 0 to 15.

(3) The deviation of the OUT0 to OUT15 constant-current average from the ideal constant-current value. Deviation is calculated by the formula:

$$\Delta(\%) = 100 \times \left(\frac{\left[\frac{(I_{OLC(0)} + I_{OLC(1)} + \cdots I_{OLC(14)} + I_{OLC(15)})}{16}\right] - \text{(Ideal Output Current)}}{\text{Ideal Output Current}} \right)$$

Ideal current is calculated by the formula:

$$I_{OLCn(IDEAL)}\ (\text{mA}) = 42.3 \times \left(\frac{1.20}{R_{IREF}} \right)$$

(4) Line regulation is calculated by the formula:

$$\Delta(\%/V) = \left(\frac{(I_{OLC(n)} \text{ at } V_{CC} = 5.5\ V) - (I_{OLC(n)} \text{ at } V_{CC} = 3.0\ V)}{(I_{OLC(n)} \text{ at } V_{CC} = 3.0\ V)} \right) \times \frac{100}{5.5\ V - 3.0\ V}$$

where n = 0 to 15.

(5) Load regulation is calculated by the equation:

$$\Delta(\%/V) = \times \left(\frac{(I_{OLC(n)} \text{ at } V_{OUTn} = 3\ V) - (I_{OLC(n)} \text{ at } V_{OUTn} = 0.8\ V)}{(I_{OLC(n)} \text{ at } V_{OUTn} = 0.8\ V)} \right) \times \frac{100}{3\ V - 0.8\ V}$$

where n = 0 to 15.

(6) Not tested; specified by design.

SWITCHING CHARACTERISTICS (See Figure 4, Figure 5, and Figure 8 through Figure 11)

At V_{CC} = 3 V to 5.5 V, T_A = –40°C to +85°C, C_L = 15 pF, R_L = 82 Ω, R_{IREF} = 1.1 kΩ, and V_{LED} = 5.0 V. Typical values at V_{CC} = 3.3 V and T_A = +25°C, unless otherwise noted.

PARAMETER		TEST CONDITIONS	TLC5948 MIN	TLC5948 TYP	TLC5948 MAX	UNIT
t_{R0}	Rise time	SOUT			5	ns
t_{R1}	Rise time	OUT*n*, DC*n*/BC = 7Fh		13		ns
t_{F0}	Fall time	SOUT			5	ns
t_{F1}	Fall time	OUT*n*, DC*n*/BC = 7Fh		23		ns
t_{D0}	Propagation delay	SCLK↑ to SOUT↑↓		15	25	ns
t_{D1}	Propagation delay	LAT↑ for BLANK = 1 set to OUT0/7/8/15 off		40	75	ns
t_{D2}	Propagation delay	GSCLK↑ to OUT0/7/8/15 on/off with DC*n*/BC = 7Fh	5	36	65	ns
t_{D3}	Propagation delay	GSCLK↑ to OUT1/6/9/14 on/off with DC*n*/BC = 7Fh	20	62	97	ns
t_{D4}	Propagation delay	GSCLK↑ to OUT2/5/10/13 on/off with DC*n*/BC = 7Fh	35	88	129	ns
t_{D5}	Propagation delay	GSCLK↑ to OUT3/4/11/12 on/off with DC*n*/BC = 7Fh	50	114	161	ns
t_{D6}	Propagation delay	LAT↑ to power-save mode by writing data for OUT*n* off with BLANK = 1 and PSMODE = 110			200	ns
t_{D7}	Propagation delay	SCLK↑ to normal mode with PSMODE = 101 or LAT ↑ to normal mode by writing GS data for OUT*n* on with BLANK = 1 and PSMODE = 110			50	μs
t_{ON_ERR}	Output on-time error(1)	t_{OUTON} – t_{GSCLK}, GS*n* = 0001h, GSCLK = 33 MHz, DC*n*/BC = 7Fh, T_A = +25°C	–20		10	ns

(1) Output on-time error (t_{ON_ERR}) is calculated by the formula: $t_{ON\_ERR} = t_{OUT\_ON} – t_{GSCLK}$. t_{OUTON} is the actual on-time of the constant-current driver. t_{GSCLK} is the GSCLK period.

PARAMETER MEASUREMENT INFORMATION

PIN-EQUIVALENT INPUT AND OUTPUT SCHEMATIC DIAGRAMS

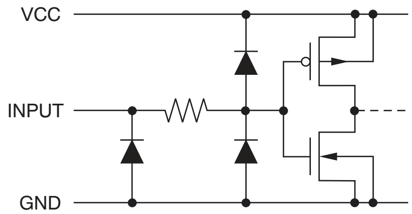


Figure 1. SIN, SCLK, LAT, GSCLK

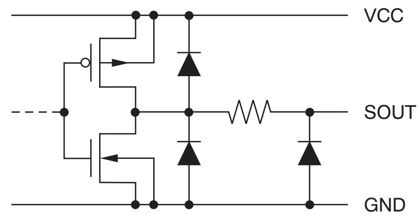
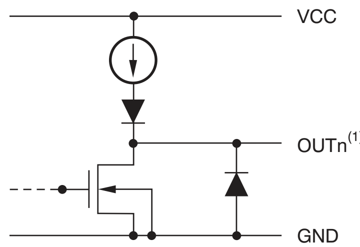


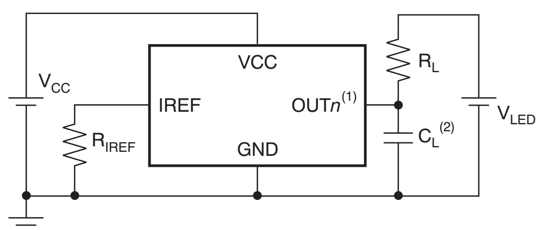
Figure 2. SOUT



(1) n = 0 to 15.

Figure 3. OUT0 Through OUT15

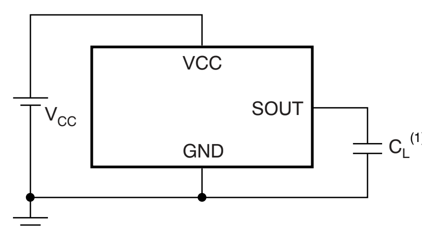
TEST CIRCUITS



(1) n = 0 to 15.

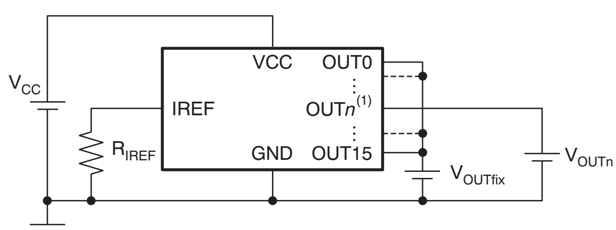
(2) C_L includes measurement probe and jig capacitance.

Figure 4. Rise Time and Fall Time Test Circuit for OUT*n*



(1) C_L includes measurement probe and jig capacitance.

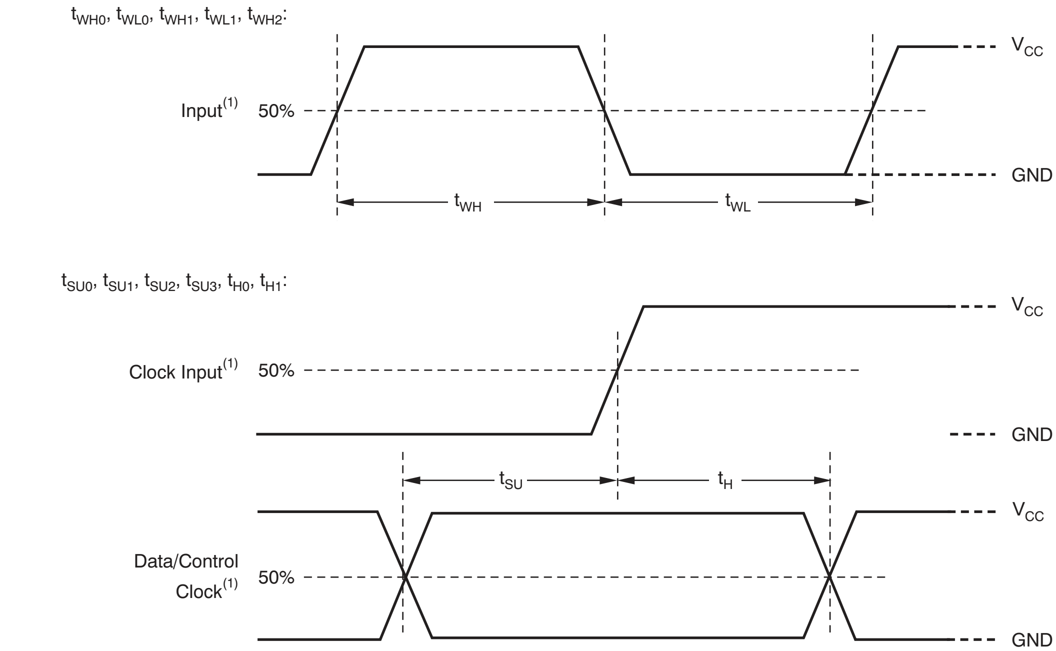
Figure 5. Rise Time and Fall Time Test Circuit for SOUT



(1) n = 0 to 15.

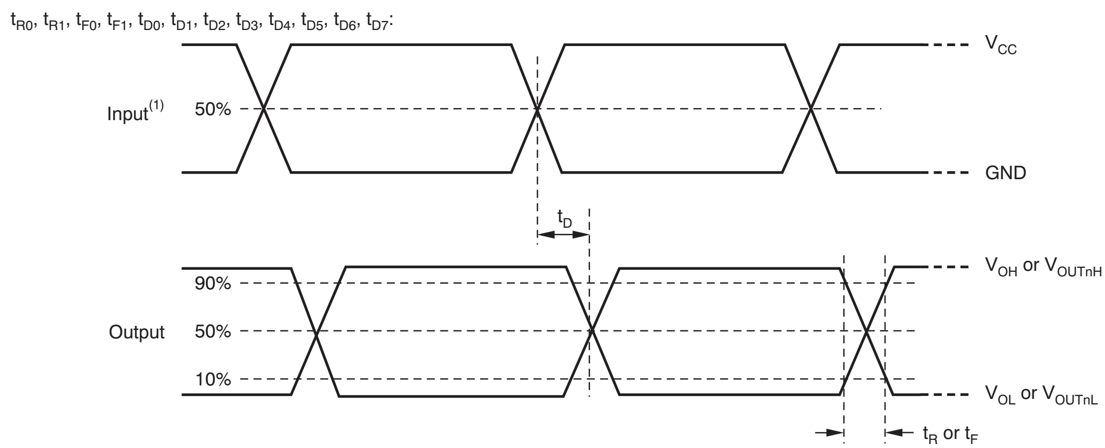
Figure 6. Constant-Current Test Circuit for OUT*n*

TIMING DIAGRAMS



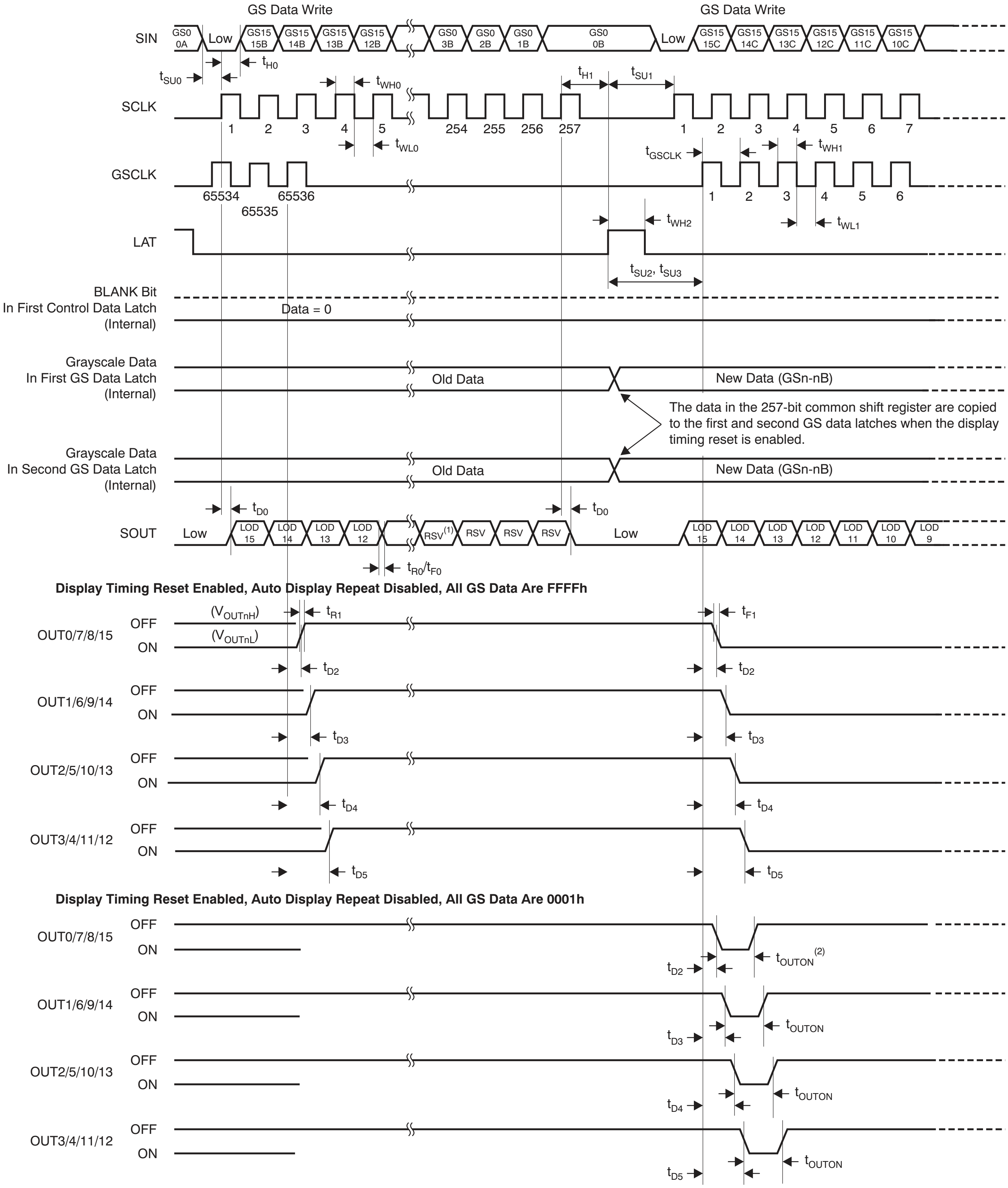
(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 7. Input Timing



(1) Input pulse rise and fall time is 1 ns to 3 ns.

Figure 8. Output Timing



(1) RSV = reserved.

(2) t_{OUTON} refers to $t_{ON\_ERR} = t_{OUTON} - t_{GSCLK}$.

Figure 9. Grayscale Data Write Timing

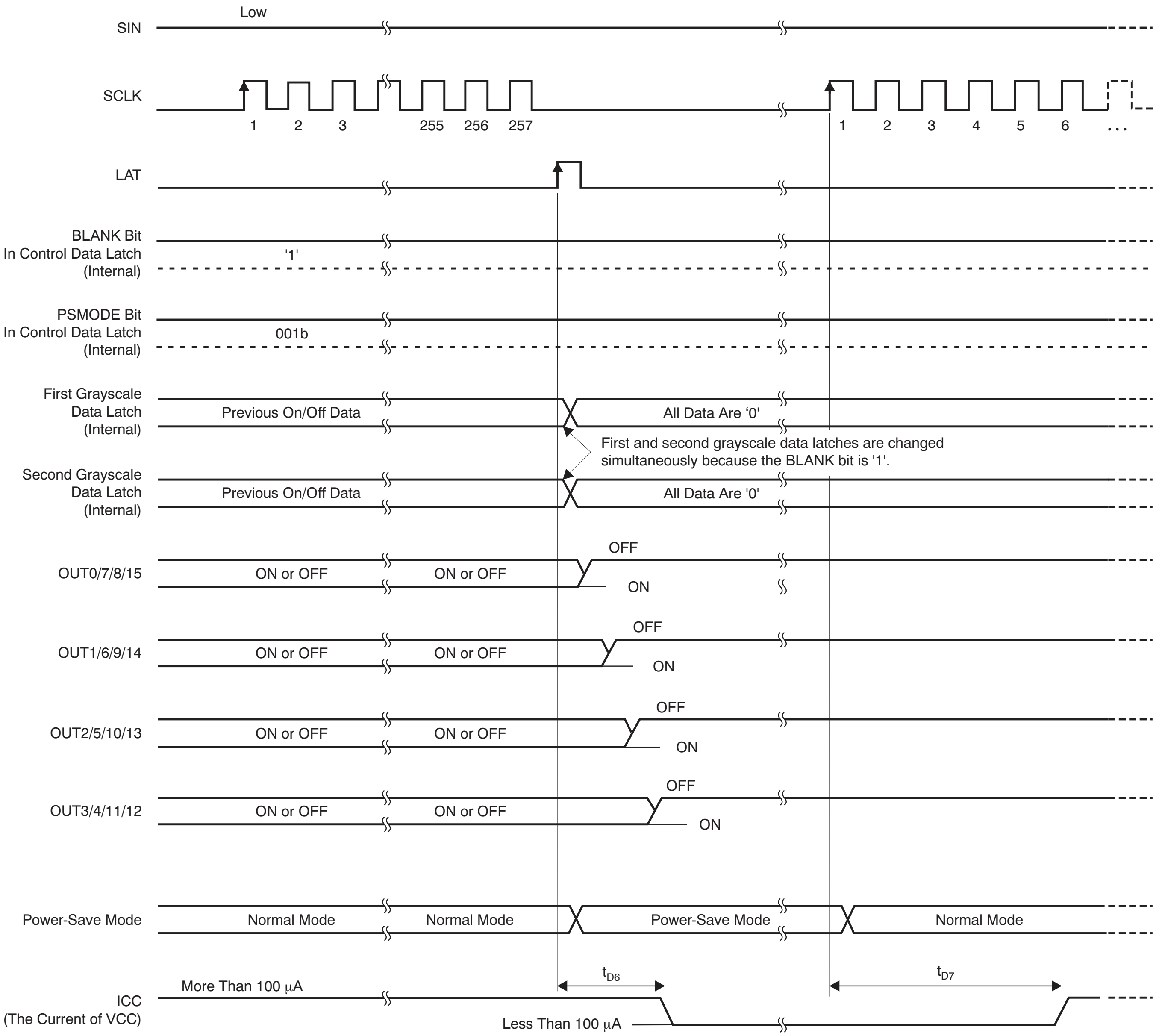
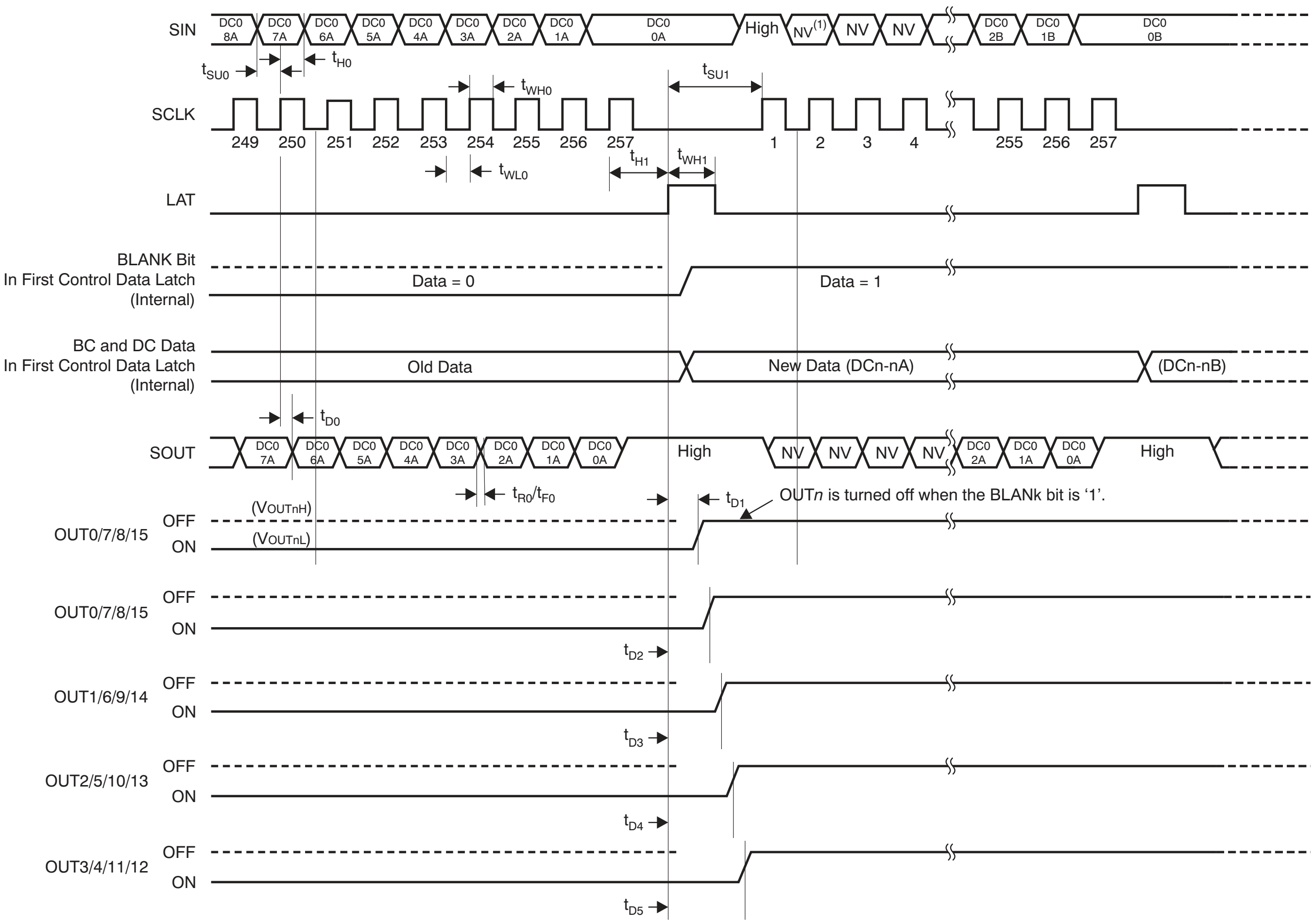


Figure 10. Power-Save Mode Timing

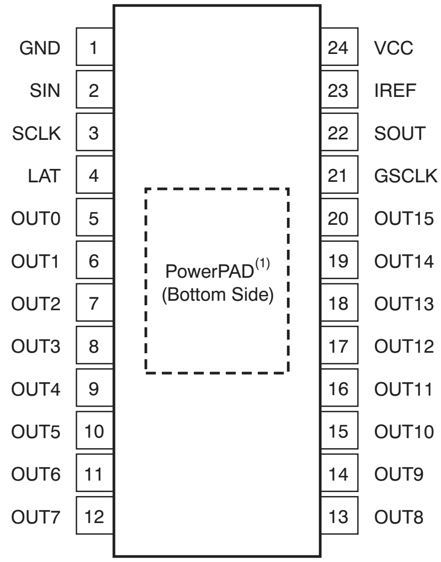


(1) NV = Not valid; these data are not used for any function.

Figure 11. Control Data Write Timing

PIN CONFIGURATION

DBQ, PWP PACKAGES
SSOP/QSOP-24, HTSSOP-24
(TOP VIEW)

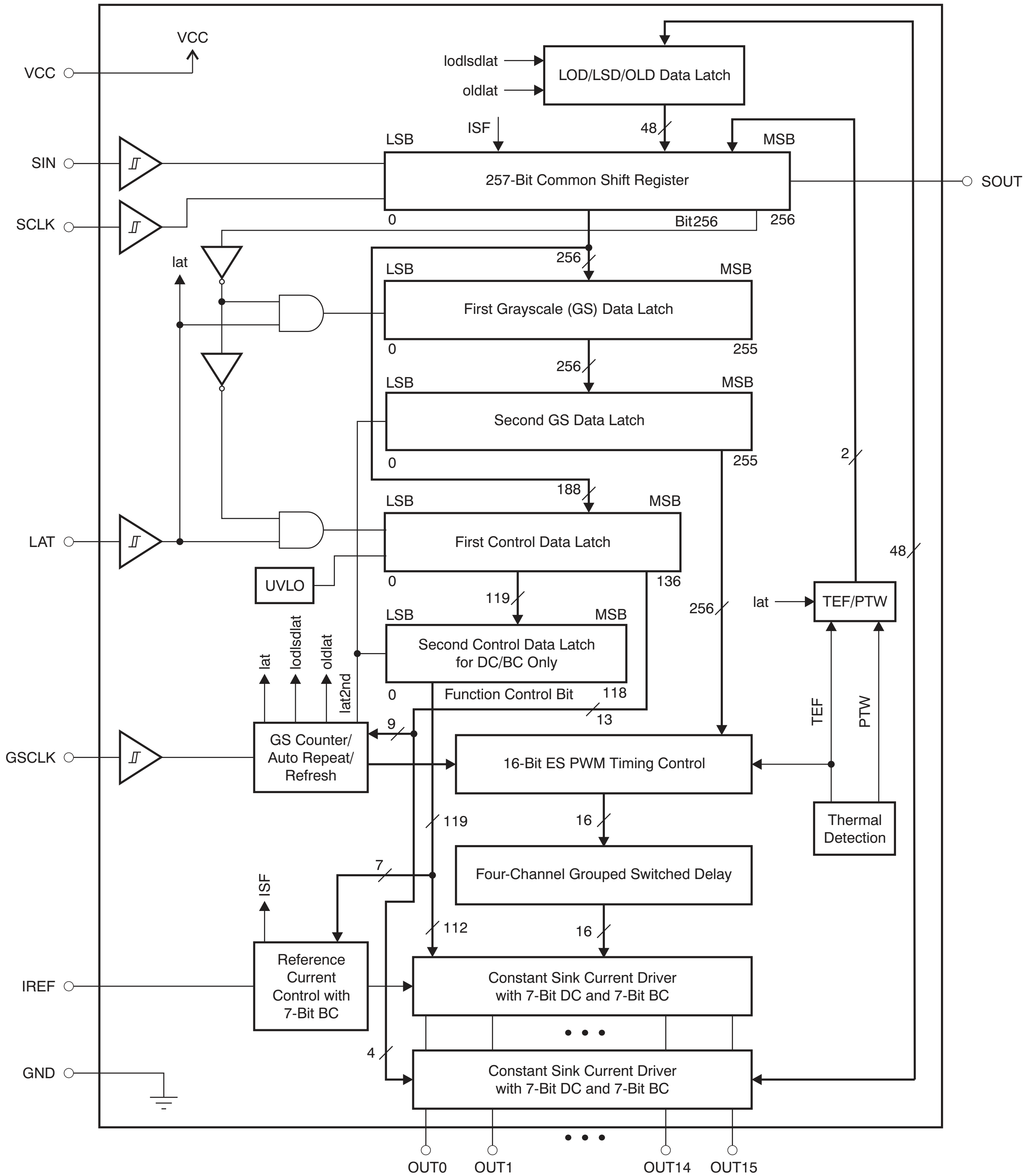


NOTE: PowerPAD is for PWP package only

PIN DESCRIPTIONS

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	—	Power ground
GSCLK	21	I	Grayscale (GS) pulse width modulation (PWM) reference clock control for OUT*n*. When BLANK = 0, each GSCLK rising edge increments the GS counter for PWM control. When BLANK = 0, all constant-current outputs (OUT0 to OUT15) are forced off, the GS counter is reset to '0', and the GS PWM timing controller is initialized.
IREF	23	I/O	Reference current terminal. A resistor connected between IREF to GND sets the maximum current for all constant-current outputs. When IREF is shorted to GND with low resistance, all constant-current outputs are forced off and the IREF short flag (ISF) bit in the status information data (SID) is set to '1'.
LAT	4	I	The LAT rising edge either latches the data from the 257-bit common shift register into the first GS data latch when the common shift register MSB is '0' or it latches the data into the first control data latch when the common shift register MSB is '1'. When the display timing reset bit (TMGRST) in the first control data latch is '1', the GS counter is initialized at the LAT signal for GS data writes. At the same time, the data in the 257-bit common shift register are copied to the first and second GS data latches simultaneously and the DC/BC data in the first control data latch are copied to the second data latch.
OUT0	5	O	Constant-current outputs. Multiple outputs can be configured in parallel to increase the constant-current capability. Different voltages can be applied to each output.
OUT1	6	O	
OUT2	7	O	
OUT3	8	O	
OUT4	9	O	
OUT5	10	O	
OUT6	11	O	
OUT7	12	O	
OUT8	13	O	
OUT9	14	O	
OUT10	15	O	
OUT11	16	O	
OUT12	17	O	
OUT13	18	O	
OUT14	19	O	
OUT15	20	O	
SCLK	3	I	Serial data shift clock. Data present on SIN are shifted to the LSB of the 257-bit common shift register with the rising edge of SCLK. Data in the shift register are shifted towards the MSB at each rising edge of SCLK. The MSB of the common shift register appear on SOUT.
SIN	2	I	Serial data input for the 257-bit common shift register
SOUT	22	O	Serial data output of the 257-bit common shift register. LED open detection (LOD), LED short detection (LSD), output leak detection (OLD), thermal error flag (TEF), and the IREF pin short flag (ISF) bit can be read out with SOUT as SID after the LAT rising edge. SOUT is connected to the 257-bit common shift register MSB. Data are clocked out at the rising edge of SCLK.
VCC	24	—	Power-supply voltage

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

At T_A = +25°C, unless otherwise noted.

REFERENCE RESISTOR vs OUTPUT CURRENT

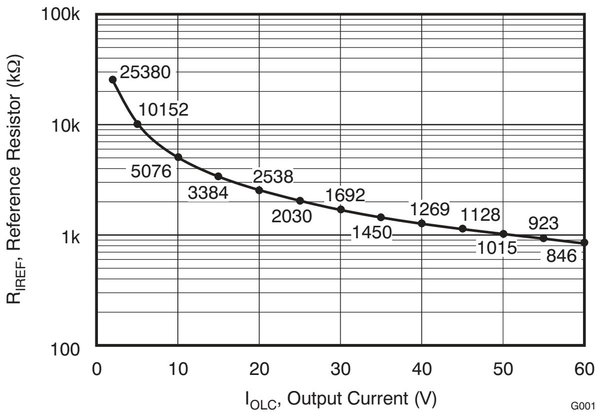


Figure 12.

OUTPUT CURRENT vs OUTPUT VOLTAGE (+3.3 V)

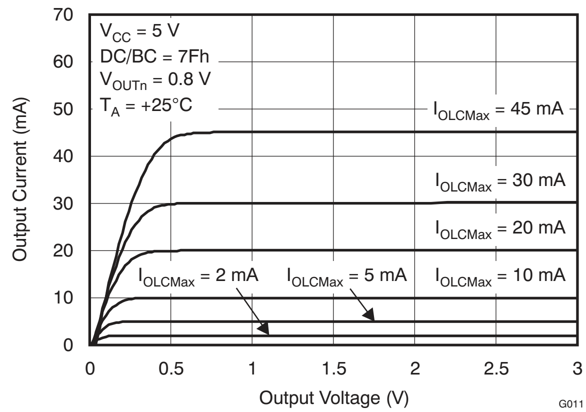


Figure 13.

OUTPUT CURRENT vs OUTPUT VOLTAGE (+5 V)

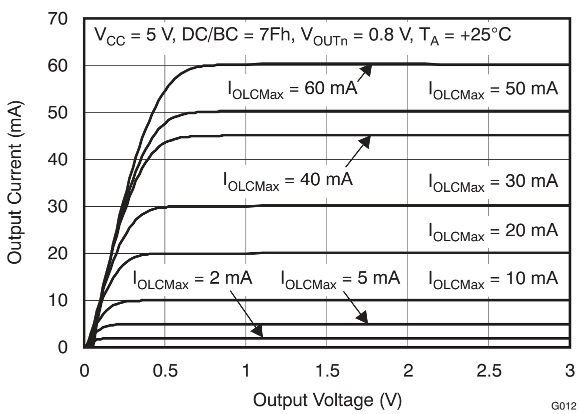


Figure 14.

OUTPUT CURRENT vs OUTPUT VOLTAGE (+3.3 V)

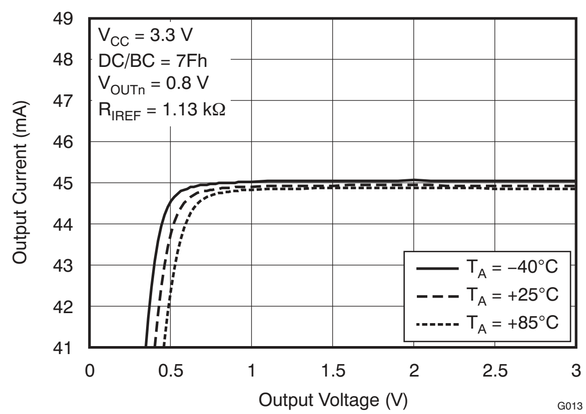


Figure 15.

OUTPUT CURRENT vs OUTPUT VOLTAGE (+5 V)

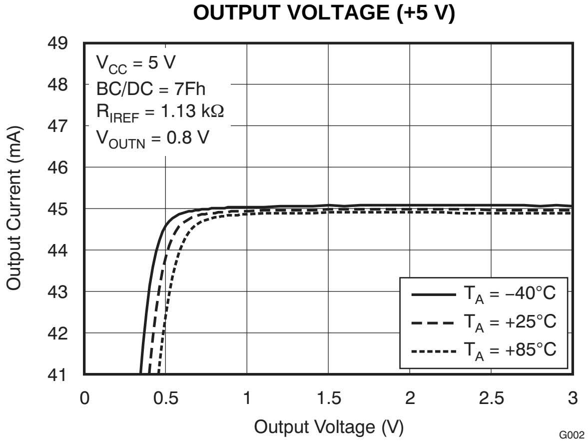


Figure 16.

CONSTANT-CURRENT ERROR vs OUTPUT CURRENT

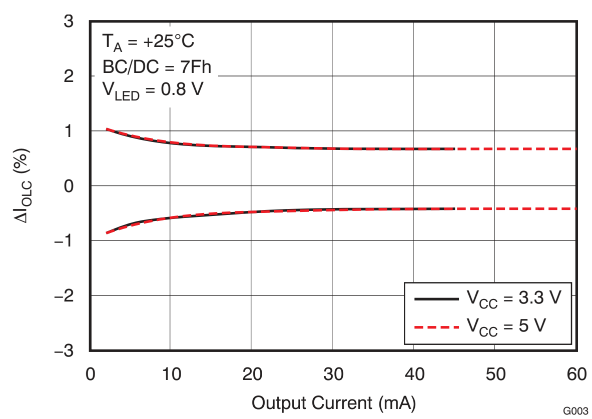


Figure 17.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

CONSTANT-CURRENT ERROR vs AMBIENT TEMPERATURE

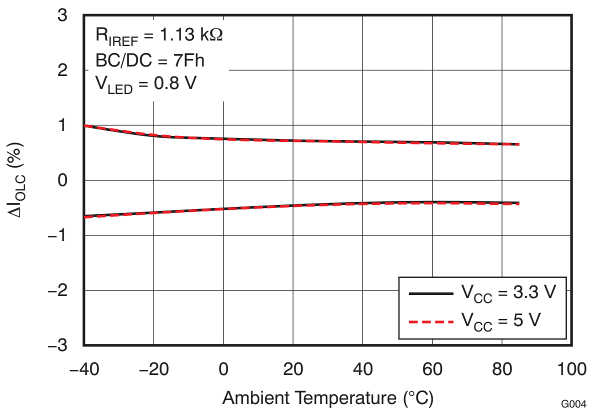


Figure 18.

DOT CORRECTION LINEARITY

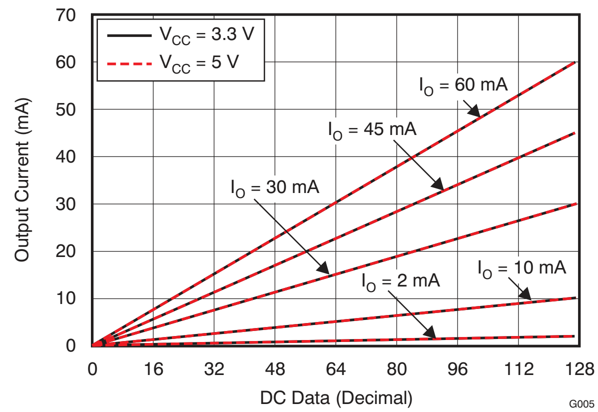


Figure 19.

GLOBAL BRIGHTNESS CONTROL LINEARITY

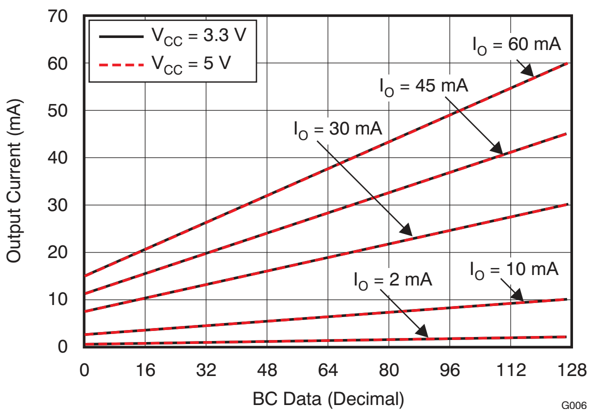


Figure 20.

SUPPLY CURRENT vs OUTPUT CURRENT

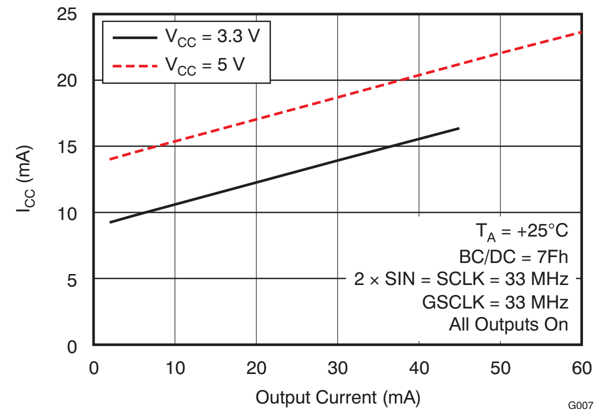


Figure 21.

SUPPLY CURRENT vs AMBIENT TEMPERATURE

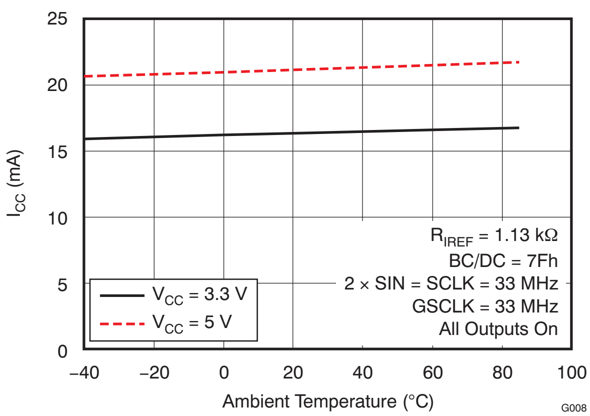


Figure 22.

SUPPLY CURRENT IN POWER-SAVE MODE vs AMBIENT TEMPERATURE

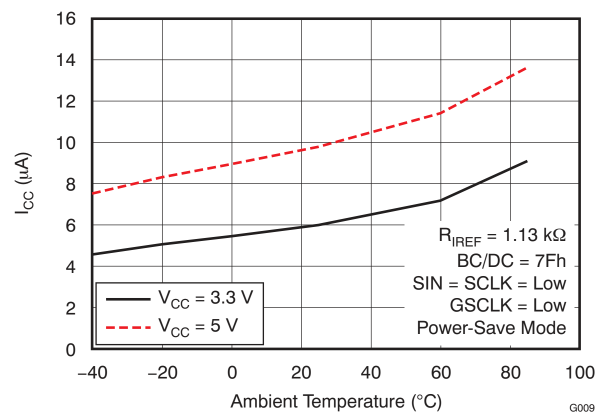


Figure 23.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C, unless otherwise noted.

CONSTANT-CURRENT OUTPUT VOLTAGE WAVEFORM

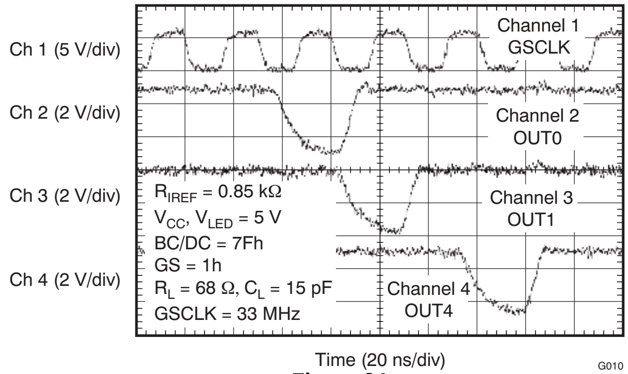


Figure 24.

DETAILED DESCRIPTION

MAXIMUM CONSTANT SINK CURRENT VALUE

The maximum output current value of each channel (I_{OLCMax}) is programmed by a single resistor (R_{IREF}) that is placed between the IREF and GND pins. The current value can be calculated by Equation 1:

$$R_{IREF} = \frac{V_{IREF}}{I_{OLCMax}} \times 42.3$$

Where:

V_{IREF} = the internal reference voltage on IREF (typically 1.20 V when the global brightness control data are at maximum)

I_{OLCMax} = 2 mA to 60 mA with DC*n*/BC = 7Fh (1)

I_{OLCMax} is the highest current for each output. Each output sinks I_{OLCMax} current when it is turned on and the dot correction (DC) data and the global brightness control (BC) data are set to the maximum value of 7Fh (127). Each output sink current can be reduced by lowering the DC and BC value.

R_{IREF} must be between 0.846 kΩ and 25.4 kΩ in order to hold I_{OLCMax} between 60 mA (typ) and 2 mA (typ). Otherwise, the output may be unstable. Output currents lower than 2 mA can be achieved by setting I_{OLCMax} to 2 mA or higher and then using dot correction or global brightness control to lower the output current.

Table 1 shows the characteristics of the constant-current sink versus the external resistor, R_{IREF}.

Table 1. Maximum Constant-Current Output versus External Resistor Value

I_{OLCMax} (mA)	R_{IREF} (kΩ, typ)
60 (V_{CC} > 3.6 V only)	0.846
55 (V_{CC} > 3.6 V only)	0.923
50 (V_{CC} > 3.6 V only)	1.02
45	1.13
40	1.27
35	1.45
30	1.70
25	2.03
20	2.53
15	3.38
10	5.08
5	10.2
2	25.4

DOT CORRECTION (DC) FUNCTION

The TLC5948 can individually adjust the output current of each channel (OUT0 to OUT15) by using dot correction (DC). The DC function allows the brightness deviations of the LEDs connected to each output to be individually adjusted. Each output DC is programmed with a 7-bit word, so the value is adjusted with 128 steps within the range of 0% to 100% of I_{OLCMax}. Equation 2 calculates the actual output current value as a function of R_{IREF}, DC value, and global brightness control (BC) value. DC data are programmed into the TLC5948 via the serial interface. When the device is powered on, the DC data in the first and second control data latches contain random data. Therefore, DC data must be written to the DC data latch before turning the constant-current outputs on. Table 2 summarizes the DC data value versus the set current value.

Table 2. DC Data versus Current Ratio and Set Current Value

DC DATA			BC DATA (Hex)	RATIO OF OUTPUT CURRENT TO I_{OLCMax} (%)	I_{OUT} (mA) (I_{OLCMax} = 45 mA, typical)	I_{OUT} (mA) (I_{OLCMax} = 2 mA, typical)
BINARY	DECIMAL	HEX				
000 0000	0	00	7F	0	0	0
000 0001	1	01	7F	0.8	0.35	0.02
000 0010	2	02	7F	1.6	0.71	0.03
—	—	—	—	—	—	—
111 1101	125	7D	7F	98.4	44.29	1.97
111 1110	126	7E	7F	99.2	44.65	1.98
111 1111	127	7F	7F	100.0	45.00	2.00

GLOBAL BRIGHTNESS CONTROL (BC) FUNCTION

The TLC5948 has the ability to adjust the output current of all constant-current outputs simultaneously. This function is called *global brightness control* (BC). The global BC for all outputs (OUT0 to OUT15) is programmed with a 7-bit word. The global BC adjusts all output currents in 128 steps from 25% to 100%, where 100% corresponds to the maximum output current set by R_{IREF}. Equation 2 calculates the actual output current as a function of R_{IREF}, DC value, and global BC value. BC data can be set via the serial interface. When the device is powered on, the BC data in the first and second control data latches contain random data. Therefore, BC data must be written to the BC data latch before turning the constant-current output on.

The output current value controlled by DC and BC can be calculated by Equation 2.

$$I_{OUTn} = 1/4 \times \left(I_{OLCMax} + \frac{3/4 \times I_{OLCMax} \times BC}{127} \times \frac{DCn}{127} \right)$$

Where:

I_{OLCMax} = the maximum constant-current value for each output determined by R_{IREF}

DC*n* = the dot correction value for each OUT*n* in the second control data latch (0h to 7Fh)

BC = the global brightness control value in the second control data latch (0h to 7Fh) (2)

Table 3 and Table 4 summarize the BC data versus the set current value.

Table 3. BC Data versus Constant-Current Ratio and Set Current Value

BC DATA			DC DATA (Hex)	RATIO OF OUTPUT CURRENT TO I_{OLCMax}(%)	I_{OUT} (mA) (I_{OLCMax}= 45 mA, typ)	I_{OUT} (mA) (I_{OLCMax}= 2 mA, typ)
BINARY	DECIMAL	HEX				
000 0000	0	00	7F	25.0	11.25	0.50
000 0001	1	01	7F	25.6	11.52	0.51
000 0010	2	02	7F	26.2	11.78	0.52
—	—	—	—	—	—	—
111 1101	125	7D	7F	98.8	44.47	1.98
111 1110	126	7E	7F	99.4	44.73	1.99
111 1111	127	7F	7F	100.0	45.00	2.00

Table 4. DC and BC Data versus Current Ratio and Set Current Value

BC DATA (Hex)	DC DATA (Hex)	RATIO OF OUTPUT CURRENT TO I_{OLCMax} (%)	I_{OUT} (mA) (I_{OLCMax} = 45 mA, typical)	I_{OUT} (mA) (I_{OLCMax} = 2 mA, typical)
00	3F	12.4	5.58	0.25
01	3F	12.7	5.71	0.25
02	3F	13.0	5.84	0.26
—	—	—	—	—
7D	3F	49.0	22.06	0.98
7E	3F	49.3	22.19	0.99
7F	3F	49.6	22.32	0.99

GRAYSCALE (GS) FUNCTION (PWM CONTROL)

The TLC5948 can adjust the brightness of each output channel using a pulse width modulation (PWM) control scheme. The architecture of 16 bits per channel results in 65,536 brightness steps, from 0% up to 100% brightness.

The PWM operation for OUT*n* is controlled by a 16-bit grayscale (GS) counter. The GS counter increments on each rising edge of the grayscale reference clock (GSCLK). The GS counter resets to 0000h when the BLANK bit in the first control data latch is set to '1'; the counter value is held at 0000h while the BLANK bit is '1', even if the GS clock input is toggled high and low.

The TLC5948 has two types of PWM control: conventional PWM control and enhanced spectrum (ES) PWM control. The conventional PWM control can be selected when the ESPWM bit in the first control data latch is '0'. The ES PWM control is selected when the ESPWM bit is '1'.

The on-time (t_{OUT_ON}) of each output (OUT*n*) can be calculated by Equation 3.

$$t_{OUT\_ON} = t_{GSCLK} \times GSn \quad (3)$$

Table 5 summarizes the GS data values versus the output on-time duty cycle. When the device powers up, the BLANK bit in the first control data latch is set to '1'. The 257-bit common shift register and the first and second GS data latches contain random data. Therefore, GS data must be written to the GS latches before the BLANK bit is set to '0'. All constant-current outputs are off when the BLANK bit is '1'.

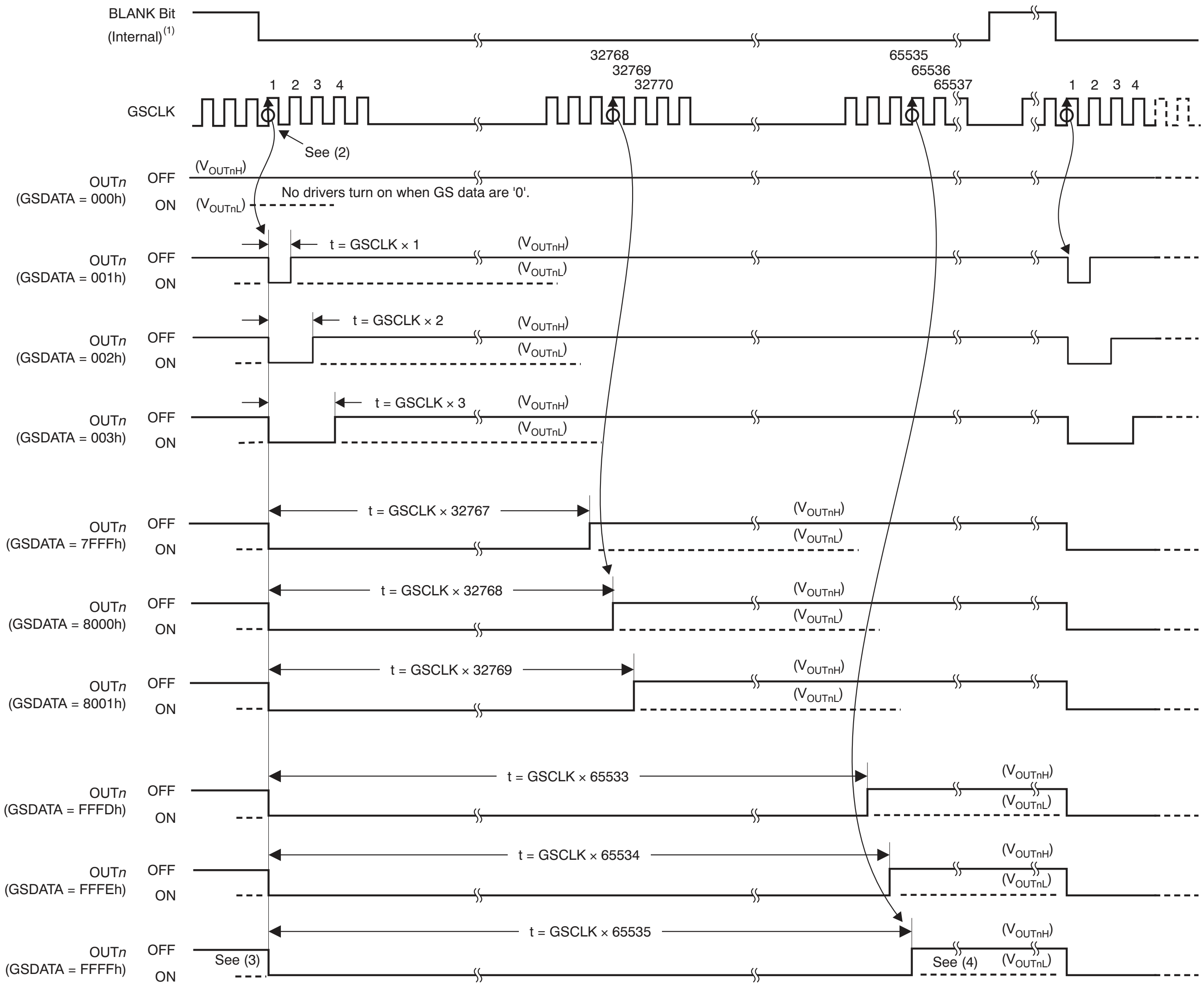
Table 5. Output Duty Cycle and On-Time versus GS Data

GS DATA			GS DATA		
DECIMAL	HEX	ON-TIME DUTY (%)	DECIMAL	HEX	ON-TIME DUTY (%)
0	0	0	32768	8000	50.001
1	1	0.002	32769	8001	50.002
2	2	0.003	32770	8002	50.004
3	3	0.005	32771	8003	50.005
—	—	—	—	—	—
8191	1FFF	12.499	40959	9FFF	62.499
8192	2000	12.500	40960	A000	62.501
8193	2001	12.502	40961	A001	62.502
—	—	—	—	—	—
16381	3FFD	24.996	49149	BFFD	74.997
16382	3FFE	24.997	49150	BFFE	74.998
16383	3FFF	24.999	49151	BFFF	75.000
16384	4000	25.000	49152	C000	75.001
16385	4001	25.002	49153	C001	75.003
16386	4002	25.003	49154	C002	75.004
16387	4003	25.005	49155	C003	75.006
—	—	—	—	—	—
24575	5FFF	37.499	57343	DFFF	87.500
24576	6000	37.501	57344	E000	87.501
24577	6001	37.502	57345	E001	87.503
—	—	—	—	—	—
32765	7FFD	49.996	65533	FFFD	99.997
32766	7FFE	49.998	65534	FFFE	99.998
32767	7FFF	49.999	65535	FFFF	100.000

Conventional PWM Control

In this PWM control, the GS clock is enabled when the BLANK bit is set to '0'. The first rising edge of a GS clock after the BLANK bit is set to '0' increments the GS counter by one and switches on all outputs with a non-zero GS value programmed into the second GS data latch. Each additional rising edge on a GS clock increases the corresponding GS counter by one.

The GS counter keeps track of the number of clock pulses from the GS clock inputs. Each output stays on while the counter is less than or equal to the programmed GS value. Each output turns off at the rising edge of the GS counter value when the counter becomes greater than the output grayscale latch value. Figure 25 shows the conventional PWM operation.



(1) The internal signal is generated when LAT inputs GS data with the display timing reset bit (TMGRST) set to '1'. This signal has the same function as a BLANK = 1 pulse. Furthermore, the signal is generated at the 65,536th GSCLK when the auto display repeat bit (DSPRPT) is set to '1'.

(2) The GS counter begins to count GSCLK pulses after the BLANK bit is set to '0' or when the LAT signal for the GS data write is input with the display time reset mode enabled.

(3) OUT*n* turns on at the first GSCLK rising edge except when GS data are '0' after the BLANK bit is set to '0' or when the LAT signal for the GS data write is input with the display time reset mode enabled.

(4) OUT*n* does not turn on again until BLANK is set to '1' once, except when the TMGRST or DSPRPT bits are '1'.

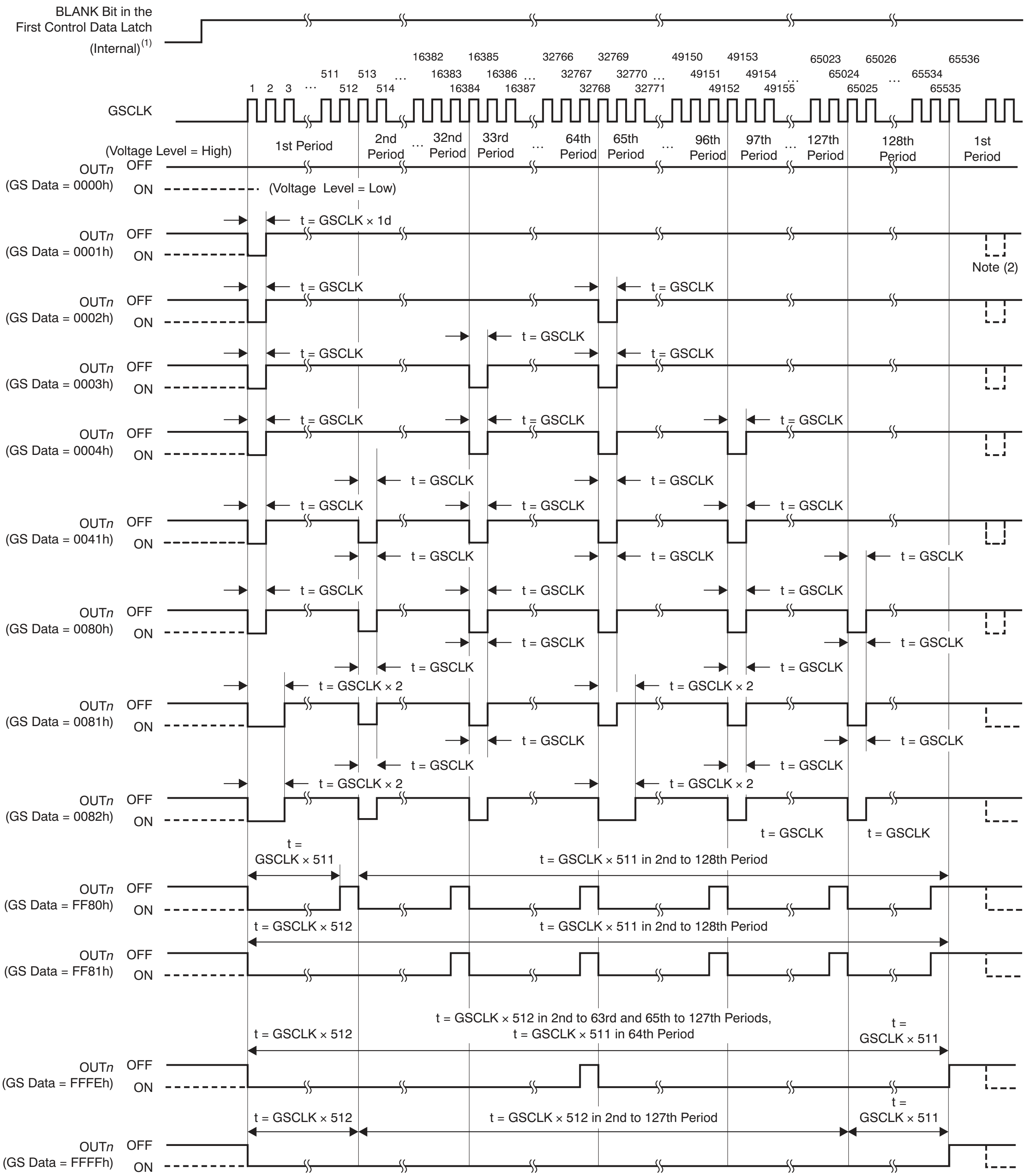
Figure 25. Conventional PWM Operation

Enhanced Spectrum (ES) PWM Control

In this PWM control, the total display period is divided into 128 display segments. The total display period is the time from the first grayscale clock (GSCLK) to the 65,536th grayscale clock input after the BLANK bit is set to '0'. Each display segment has a maximum of 512 grayscale clocks. The OUT*n* on-time changes, depending on the 16-bit grayscale data. Refer to Table 6 for the sequence of information and to Figure 26 for the timing information.

Table 6. ES PWM Drive Turn On-Time Length

GS DATA		
DECIMAL	HEX	OUT*n* DRIVER OPERATION
0	0000h	Does not turn on
1	0001h	Turns on for one GSCLK period in the first display segment
2	0002h	Turns on for one GSCLK period in the first and 65th display segments
3	0003h	Turns on for one GSCLK period in the first, 65th, and 33th display segments
4	0004h	Turns on for one GSCLK period in the first, 65th, 33th, and 97th display segments
5	0005h	Turns on for one GSCLK period in the first, 65th, 33th, 97th, and 17th display segments
6	0006h	Turns on for one GSCLK period in the first, 65th, 33th, 97th, 17th, and 81th display segments
—	—	The number of display segments where OUT*n* is turned on for one GSCLK is incremented by increasing the GS data in the following order: 1 > 65 > 33 > 97 > 17 > 81 > 49 > 113 > 9 > 73 > 41 > 105 > 25 > 89 > 57 > 121 > 5 > 69 > 37 > 101 > 21 > 85 > 53 > 117 > 13 > 77 > 45 > 109 > 29 > 93 > 61 > 125 > 3 > 67 > 35 > 99 > 19 > 83 > 51 > 115 > 11 > 75 > 43 > 107 > 27 > 91 > 59 > 123 > 7 > 71 > 39 > 103 > 23 > 87 > 55 > 119 > 15 > 79 > 47 > 111 > 31 > 95 > 63 > 127 > 2 > 66 > 34 > 98 > 18 > 82 > 50 > 114 > 10 > 74 > 42 > 106 > 26 > 90 > 58 > 122 > 6 > 70 > 38 > 102 > 22 > 86 > 54 > 118 > 14 > 78 > 46 > 110 > 30 > 94 > 62 > 126 > 4 > 68 > 36 > 100 > 20 > 84 > 52 > 116 > 12 > 76 > 44 > 108 > 28 > 92 > 60 > 124 > 8 > 72 > 40 > 104 > 24 > 88 > 56 > 120 > 16 > 80 > 48 > 112 > 32 > 96 > 64 > 128.
127	007Fh	Turns on for one GSCLK period in the first to 127th display segments, but does not turn on in the 128th display segment
128	0080h	Turns on for one GSCLK period in all display segments (first to 128th)
129	0081h	Turns on for two GSCLK periods in the first display period and for one GSCLK period in all other display periods
—	—	The number of display segments where OUT*n* is turned on for one GSCLK is incremented by increasing the GS data in the following order: 1 > 65 > 33 > 97 > 17 > 81 > 49 > 113 > 9 > 73 > 41 > 105 > 25 > 89 > 57 > 121 > 5 > 69 > 37 > 101 > 21 > 85 > 53 > 117 > 13 > 77 > 45 > 109 > 29 > 93 > 61 > 125 > 3 > 67 > 35 > 99 > 19 > 83 > 51 > 115 > 11 > 75 > 43 > 107 > 27 > 91 > 59 > 123 > 7 > 71 > 39 > 103 > 23 > 87 > 55 > 119 > 15 > 79 > 47 > 111 > 31 > 95 > 63 > 127 > 2 > 66 > 34 > 98 > 18 > 82 > 50 > 114 > 10 > 74 > 42 > 106 > 26 > 90 > 58 > 122 > 6 > 70 > 38 > 102 > 22 > 86 > 54 > 118 > 14 > 78 > 46 > 110 > 30 > 94 > 62 > 126 > 4 > 68 > 36 > 100 > 20 > 84 > 52 > 116 > 12 > 76 > 44 > 108 > 28 > 92 > 60 > 124 > 8 > 72 > 40 > 104 > 24 > 88 > 56 > 120 > 16 > 80 > 48 > 112 > 32 > 96 > 64 > 128.
255	00FFh	Turns on for two GSCLK periods in the first to 127th display segments and turns on one GSCLK period in the 128th display segment
256	0100h	Turns on for two GSCLK periods in all display segments (first to 128th)
257	0101h	Turns on for three GSCLK periods in the first display segments and for two GSCLK periods in all other display segments
—	—	The number of display segments where OUT*n* is turned on for one GSCLK is incremented by increasing the GS data in the following order: 1 > 65 > 33 > 97 > 17 > 81 > 49 > 113 > 9 > 73 > 41 > 105 > 25 > 89 > 57 > 121 > 5 > 69 > 37 > 101 > 21 > 85 > 53 > 117 > 13 > 77 > 45 > 109 > 29 > 93 > 61 > 125 > 3 > 67 > 35 > 99 > 19 > 83 > 51 > 115 > 11 > 75 > 43 > 107 > 27 > 91 > 59 > 123 > 7 > 71 > 39 > 103 > 23 > 87 > 55 > 119 > 15 > 79 > 47 > 111 > 31 > 95 > 63 > 127 > 2 > 66 > 34 > 98 > 18 > 82 > 50 > 114 > 10 > 74 > 42 > 106 > 26 > 90 > 58 > 122 > 6 > 70 > 38 > 102 > 22 > 86 > 54 > 118 > 14 > 78 > 46 > 110 > 30 > 94 > 62 > 126 > 4 > 68 > 36 > 100 > 20 > 84 > 52 > 116 > 12 > 76 > 44 > 108 > 28 > 92 > 60 > 124 > 8 > 72 > 40 > 104 > 24 > 88 > 56 > 120 > 16 > 80 > 48 > 112 > 32 > 96 > 64 > 128.
65479	FEFFh	Turns on for 511 GSCLK periods in the first to 127th display segments, but only turns on 510 GSCLK periods in the 128th display segment
65480	FF00h	Turns on for 511 GSCLK periods in all display segments (first to 128th)
65481	FF01h	Turns on for 512 GSCLK periods in the first display period and for 511 GSCLK periods in the second to 128th display segments
—	—	—
65534	FFFEh	Turns on for 512 GSCLK periods in the first to 63th and 65th to 127th display segments; also turns on 511 GSCLK periods in 64th and 128th display segments
65535	FFFFh	Turns on for 512 GSCLK periods in the first to 127th display segments but only turns on 511 GSCLK periods in the 128th display segment



(1) The internal signal is generated when LAT inputs GS data when the display timing reset bit (TMGRST) is set to '1'. This signal has the same function as BLANK = 1. Furthermore, the signal is generated at the 65,536th GSCLK when the auto display repeat bit (DSPRPT) is set to '1'.

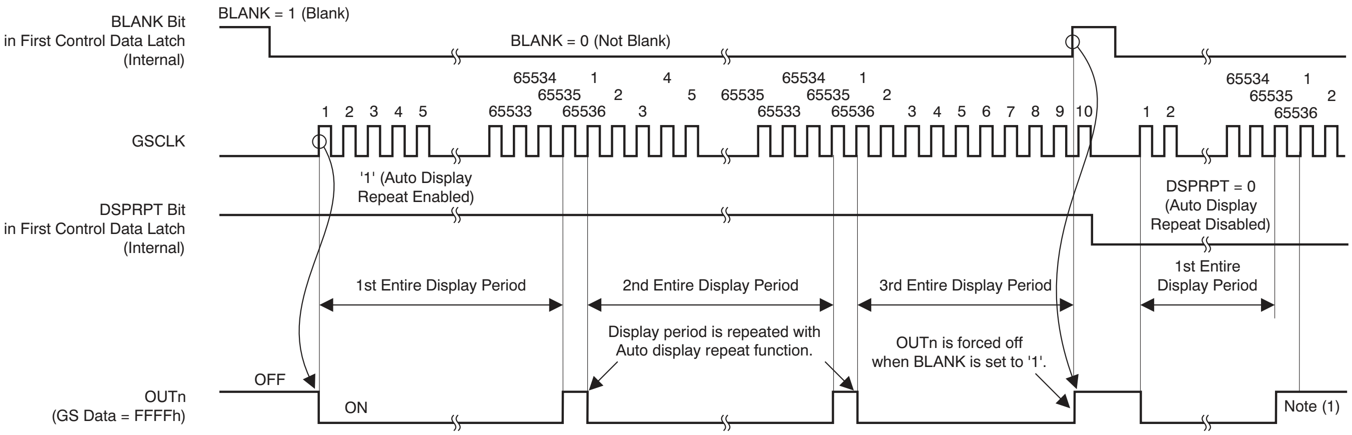
(2) When auto display repeat is on.

Figure 26. ES PWM Operation

Auto Display Repeat Function

This function can repeat the total display period as long as GSCLK is present, as shown in Figure 27. This function is switched on or off by the content of the DSPRPT bit in the first control data latch.

When the DSPRPT bit is '1', auto display repeat is enabled and the entire display period repeats automatically. When the DSPRPT bit is '0', auto display repeat is disabled and the entire display period executes only once after the BLANK bit is set to '0' or a rising signal for a GS data write occurs at LAT when the display timing reset is enabled.



(1) OUT*n* is not turned on until BLANK changes from '1' to '0' or until LAT changes from low to high for a GS data write with TMGRST = 1.

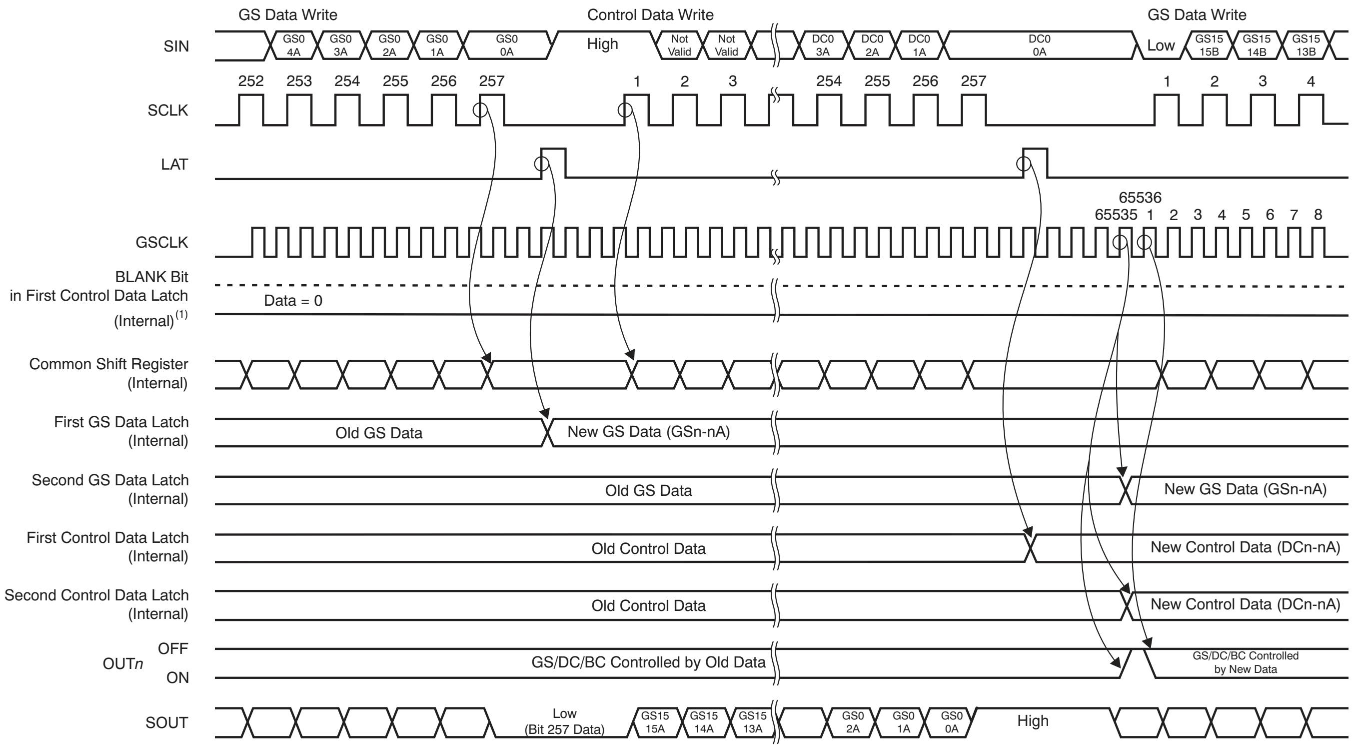
Figure 27. Auto Display Repeat Function

Auto Data Refresh Function

This function allows users to input grayscale (GS) data, dot correction (DC) data, and global brightness control (BC) data at any time without synchronizing the input to the display timing. If GS, DC, and BC data are sent during a display period, the input data are held in the first latch for each data register. The data are then transferred to the second latch when the 65,536th GSCLK occurs. The second latch data are used for the next display period. Figure 28 and Figure 29 show the timing of the auto data refresh function. However, when the BLANK bit in the first control data latch is set to '1' before the 65,536th GSCLK occurs, the first latch data uploads to the second latch immediately. Also, when a rising edge occurs at LAT while the BLANK bit is '1', the selected shift register data are transferred to the first and second latch at the same time. The data of bits 119-136 (BLANK, DSPRPT, TMGRST, ESPWM, LODVLT, LSDVLT, LATTMG, IDMENA, IDMRPT, IDMCUR, OLDEN, and PSMODE) in the control data latch update immediately whenever the data are written into the first latch.

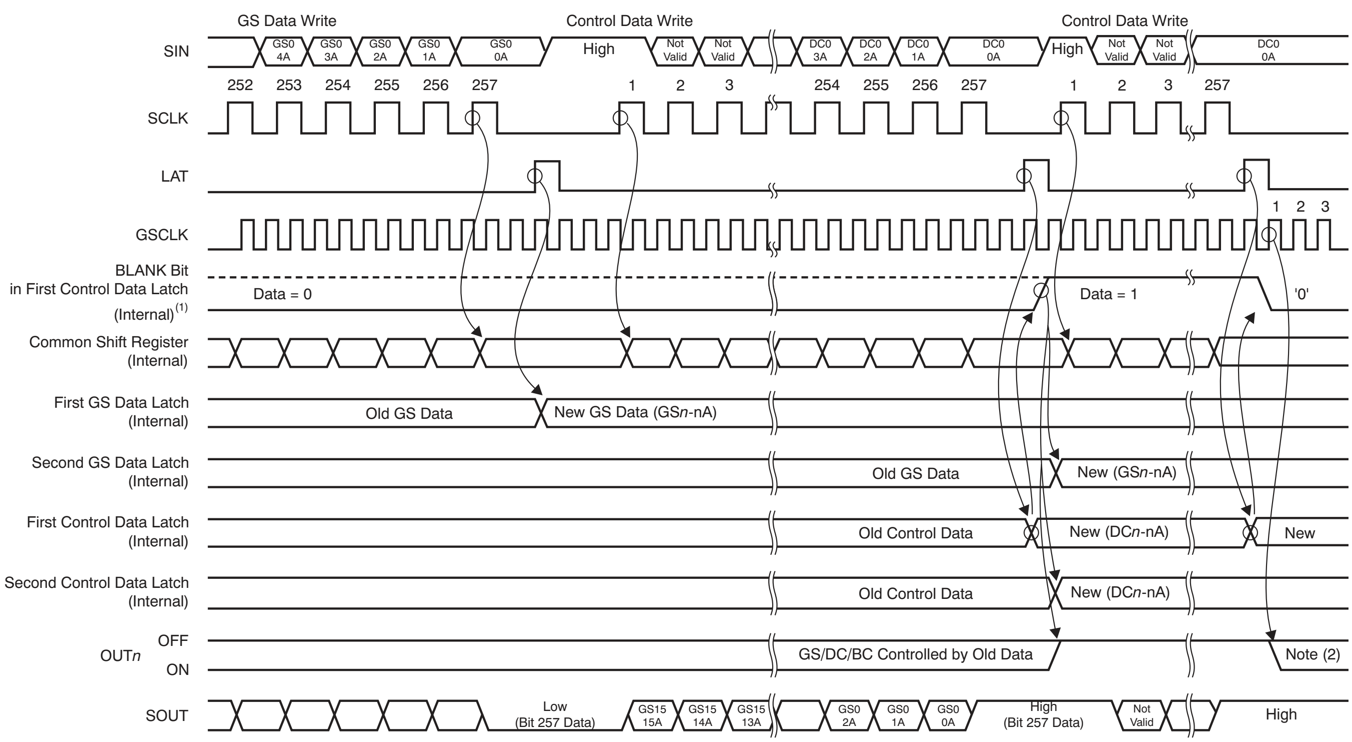
Display Timing Reset Function

The display timing reset function allows initializing the display timing using a rising signal for a GS data write at the LAT pin. This function can be switched on or off with the TMGRST bit in the first control data latch. When the TMGRST bit is '1', the GS counter is reset to '0' and all outputs are forced off at the LAT rising edge for a GS data write. Furthermore, the data in the 257-bit common shift register are copied to the first and second GS data latches at the same time. In addition, the DC/BC data in the first control data latch are transferred to the second data latch simultaneously. This configuration is identical to when the BLANK bit data changes from '0' to '1' and '1' to '0'. Therefore, the BLANK bit is not needed to control the display reset. PWM control resumes from the next GSCLK rising edge. When the TMGRST bit is '0', the GS counter is not reset and the outputs are not forced off even if a rising edge occurs at LAT.



(1) BLANK data does not change with Auto Display Repeat enabled.

Figure 28. Auto Data Refresh Function 1



(1) The value of the BLANK bit is changed after the rising edge at LAT pin.
(2) GS/DC/BC are controlled by new data.

Figure 29. Auto Data Refresh Function 2

REGISTER AND DATA LATCH CONFIGURATION

The TLC5948 has one common shift register and two pairs of data latches: the first and second grayscale (GS) data latches and the first and second control data latches. The common shift register is 257 bits long and the GS data latches are 256 bits long. The first control data latch is 137 bits long and the second latch is 119 bits long. When the MSB of the common shift register is '0', the least significant 256 bits from the common shift register are latched into the first GS data latch. When the MSB is '1', the data are latched into the first control data latch. Figure 30 shows the configuration of the common shift register and the latch configurations.

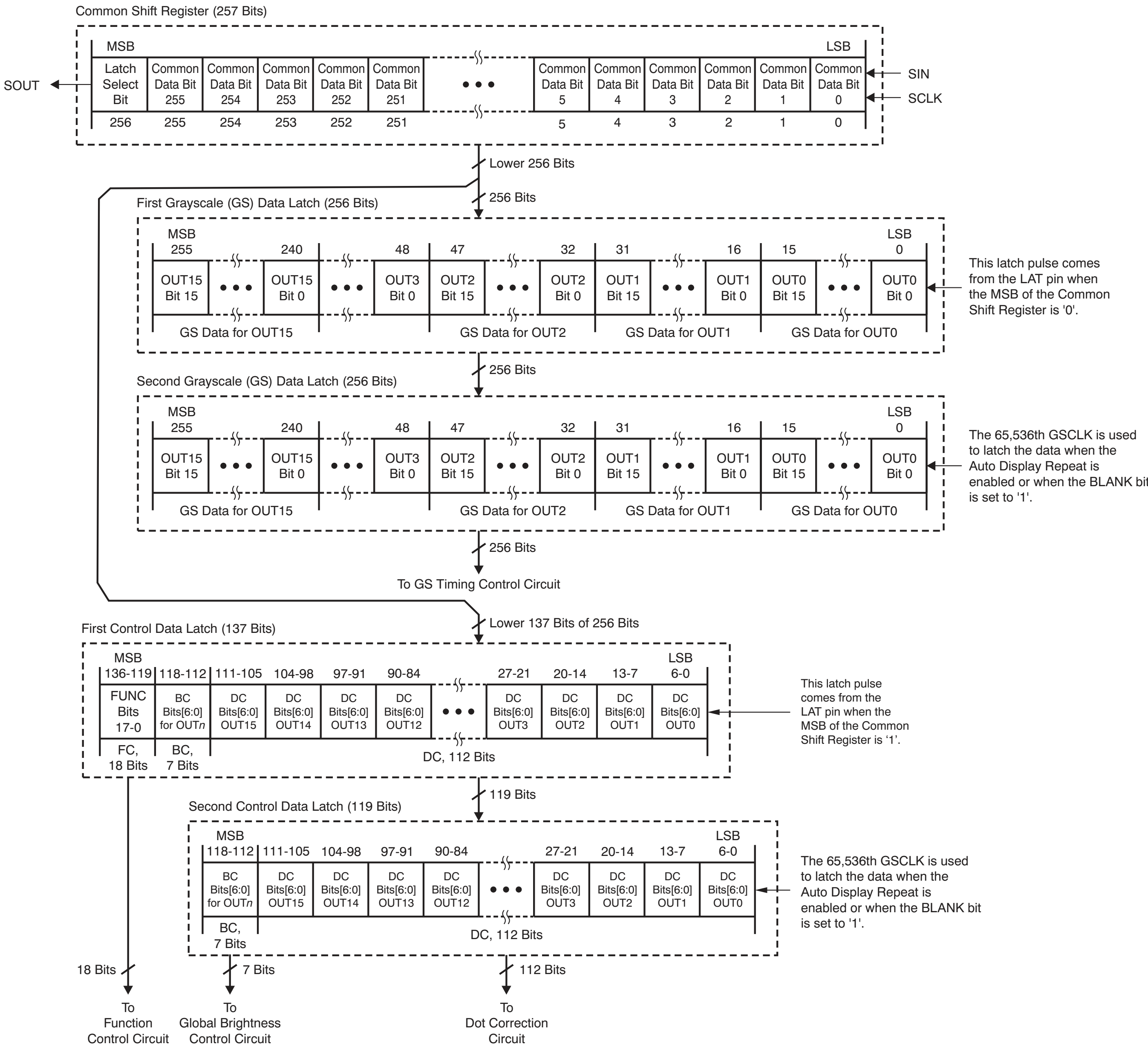


Figure 30. Common Shift Register and Control Data Latches Configuration

257-Bit Common Shift Register

The 257-bit common shift register is used to shift data from the SIN pin into the TLC5948. The data shifted into the register are used for GS, DC, and global BC functions. The LSB of the common shift register is connected to SIN and the MSB is connected to SOUT. On each rising edge of SCLK, the data on SIN are shifted into the LSB and all 257 bits are shifted towards the MSB. The register MSB is always connected to SOUT. When the device is powered up, the data in the 257-bit common shift register are random.

First and Second Grayscale Data Latch

The first and second grayscale (GS) data latches are each 256 bits long, and set the PWM timing for each constant-current output. The on-time of all constant-current outputs is controlled by the data in the second GS data latch. A LAT rising edge when the common shift register MSB is '0' shifts the least significant 256 bits of the common shift register into the first grayscale latch. The GS data from the first latch are copied into the second latch either when the 65,536th GSCLK occurs with the auto display repeat mode enabled, or a rising edge for a GS data write occurs at LAT with the display timing reset mode enabled, or the BLANK bit in the first control data latch are set to '1'.

When the device is powered up, the data in the first and second latches are random. Therefore, GS data must be written to the GS data latches before turning on the constant-current output. The first and second GS data latch configuration are shown in Figure 31. The data bit assignment is shown in Table 7.

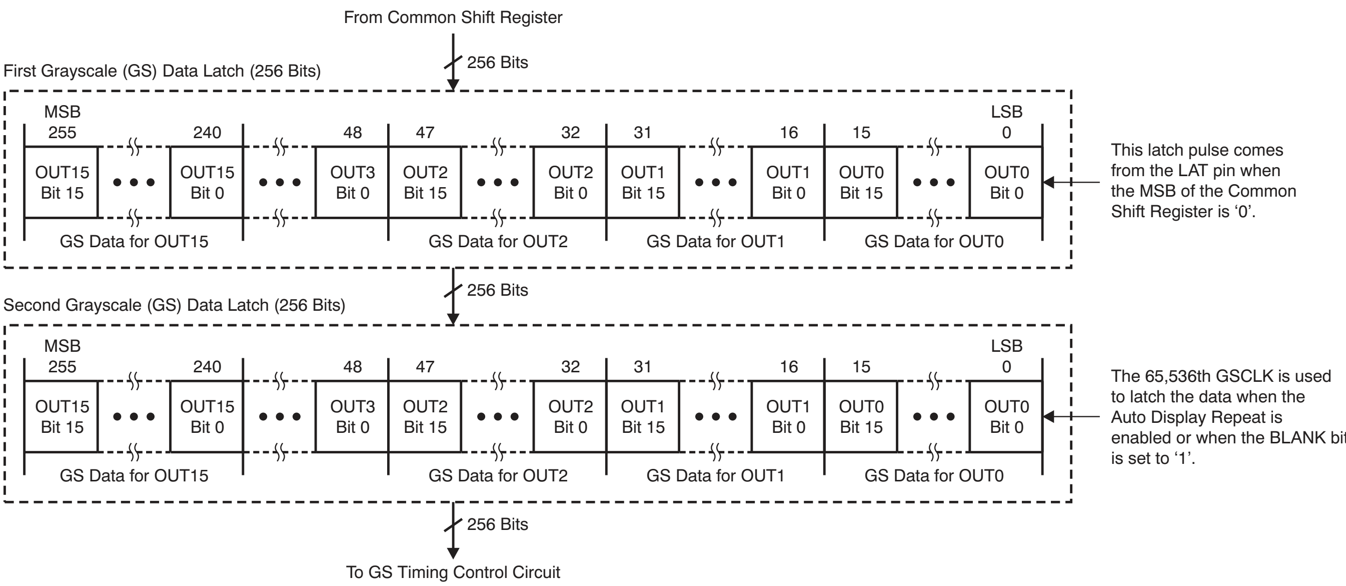


Figure 31. First and Second Grayscale Data Latch Configuration

Table 7. Grayscale Data Latch Bit Description

BIT NUMBER	BIT NAME	CONTROLLED CHANNEL	BIT NUMBER	BIT NAME	CONTROLLED CHANNEL
15-0	GSOUT0	Bits[15:0] for OUT0	143-128	GSOUT8	Bits[15:0] for OUT8
31-16	GSOUT1	Bits[15:0] for OUT1	159-144	GSOUT9	Bits[15:0] for OUT9
47-32	GSOUT2	Bits[15:0] for OUT2	175-160	GSOUT10	Bits[15:0] for OUT10
63-48	GSOUT3	Bits[15:0] for OUT3	191-176	GSOUT11	Bits[15:0] for OUT11
79-64	GSOUT4	Bits[15:0] for OUT4	207-192	GSOUT12	Bits[15:0] for OUT12
95-80	GSOUT5	Bits[15:0] for OUT5	223-208	GSOUT13	Bits[15:0] for OUT13
111-96	GSOUT6	Bits[15:0] for OUT6	239-224	GSOUT14	Bits[15:0] for OUT14
127-112	GSOUT7	Bits[15:0] for OUT7	255-240	GSOUT15	Bits[15:0] for OUT15

First and Second Control Data Latch

The first and second control data latches are 137 bits and 119 bits long, respectively. The first latch contains dot correction (DC) data, global brightness control (BC) data, and function control (FC) data; the second latch contains dot correction (DC) data and global brightness control (BC) data. The DC for each constant-current output and the BC for all constant-current outputs are controlled by the second control data latch. The control data into the first latch are set by the least significant 137 bits from the common shift register at the rising edge of LAT when the common shift register MSB is '1'. The 119 bits of DC and BC data from the first control data latch are copied to the second latch when the 65,536th GSCLK occurs or when the BLANK bit in the first control data latch are set to '1'.

When the device is powered up, the data in the first latch (except the BLANK and PSMODE bits of the FC bits) and second latch are random. Therefore, DC, BC and FC data must be written to the first and second control data latches before turning on the constant-current outputs. The default value of the BLANK bit is '1'. The first and second control data latch configurations are shown in Figure 32.

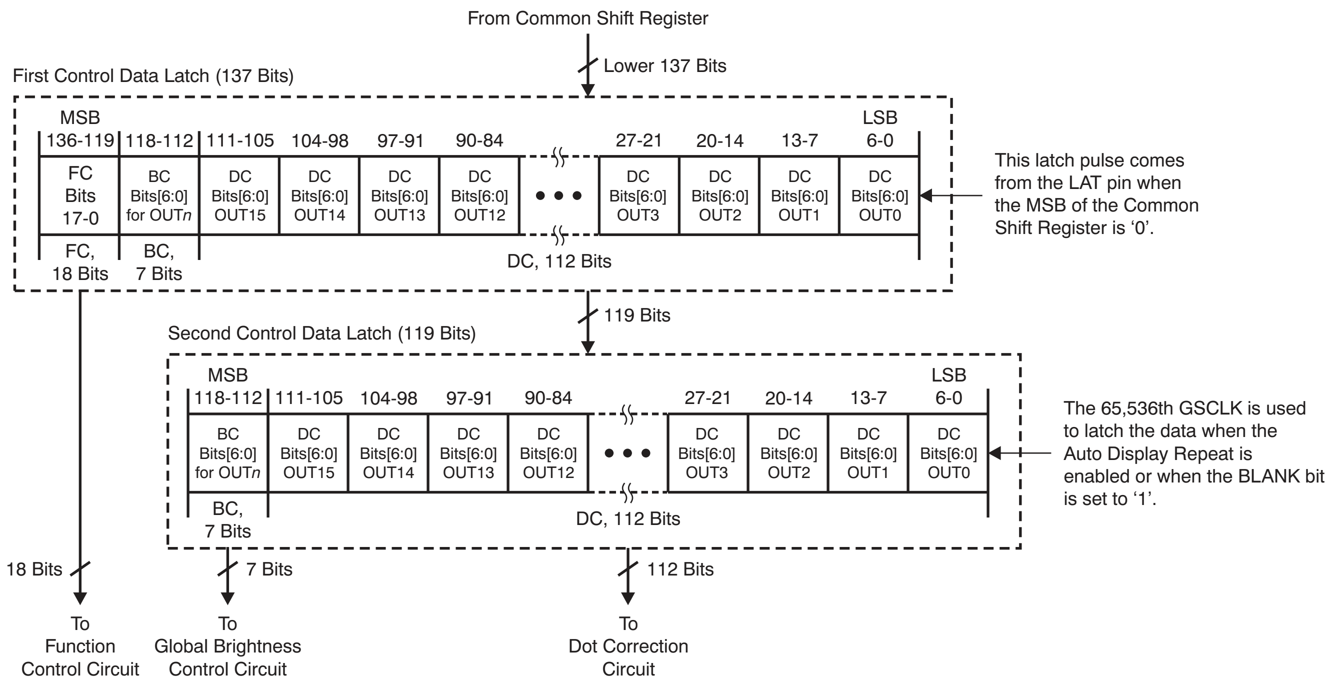


Figure 32. First and Second Control Data (DC/BC/FC) Latch Configulation

Dot Correction Data

The dot correction (DC) data is 112 bits long; the data for each constant-current output is controlled by seven bits. DC for each constant-current output is controlled by the second control data latch. Each DC value individually adjusts the output current for each constant-current output. As explained in the *Dot Correction (DC) Function* section, the DC values are used to adjust the output current from 0% to 100% of the maximum value.

The data bit assignment for dot correction in the first and second latches are shown in Table 8. Refer to Table 2 for a summary of the DC data value versus set current value.

Table 8. Dot Correction Data Bit Description

BIT NUMBER	BIT NAME	CONTROLLED CHANNEL	BIT NUMBER	BIT NAME	CONTROLLED CHANNEL
6-0	DCOUT0	DC bits[6:0] for OUT0	62-56	DCOUT8	DC bits[6:0] for OUT8
13-7	DCOUT1	DC bits[6:0] for OUT1	69-63	DCOUT9	DC bits[6:0] for OUT9
20-14	DCOUT2	DC bits[6:0] for OUT2	76-70	DCOUT10	DC bits[6:0] for OUT10
27-21	DCOUT3	DC bits[6:0] for OUT3	83-77	DCOUT11	DC bits[6:0] for OUT11
34-28	DCOUT4	DC bits[6:0] for OUT4	90-84	DCOUT12	DC bits[6:0] for OUT12
41-35	DCOUT5	DC bits[6:0] for OUT5	97-91	DCOUT13	DC bits[6:0] for OUT13
48-42	DCOUT6	DC bits[6:0] for OUT6	104-98	DCOUT14	DC bits[6:0] for OUT14
55-49	DCOUT7	DC bits[6:0] for OUT7	111-105	DCOUT15	DC bits[6:0] for OUT15

Global Brightness Control (BC) Data

The global brightness control (BC) data are seven bits long. The global brightness for all outputs is controlled by the second control data latch. The data are used to adjust the constant-current values for the 16 constant-current outputs. As explained in the *Global Brightness Control (BC) Function* section, the BC values are used to adjust the output current from 25% to 100% of the maximum value. The data bit assignment for the global BC in the first and second latches is shown in Table 9. Table 3 summarizes the BC data value versus set current value.

Table 9. Global Brightness Control Data Bit Assignment in the Cotrol Data Latch

BIT NUMBER	BIT NAME	CONTROLLED CHANNEL
118-112	BC	BC bits[6:0} for all channels (OUT0-OUT15)

Function Control (FC) Data Latch

The function control (FC) data latch is 13 bits long. This latch enables the constant-current outputs, enables the auto display repeat and display timing reset functions, and sets the PWM control mode and the LOD/LSD/OLD data latch timing. Each function is selected by the first control data latch. When the device is powered on, the data of the FC data in the first control data latch are random (except the BLANK and PSMODE bits) in order to disable all constant-current outputs. The FC data bit assignment in the first control data latch is shown in Table 10.

Table 10. Function Control Data Latch Bit Description

BIT NUMBER	BIT NAME	DEFAULT VALUE (Binary)	DESCRIPTION
119	BLANK	1	Constant-current output blank bit 0 = On, 1 = Off When this bit is '0', all constant-current outputs are controlled by the GS PWM timing controller. When this bit is '1', all constant-current outputs (OUT0-OUT15) are forced off. The grayscale counter is reset to '0', and the GS PWM timing controller is initialized. When the device is powered on, this bit is set to '1'.
120	DSPRPT	—	Auto display repeat mode enable bit 0 = Disabled, 1 = Enabled When this bit is '0', the auto display repeat function is disabled. Each constant-current output is turned on and off for one display period after the BLANK bit is set to '0'. When this bit is '1', each output is repeated every 65536 GS clocks. When the device is powered on, this bit is random.
121	TMGRST	—	Display timing reset mode enable bit 0 = Disabled, 1 = Enabled When this bit is '1', the GS counter is reset to '0' and all outputs are forced off at the LAT rising edge for GS data write. This function is identical to the BLANK bit. Therefore, a BLANK bit data change is not needed to control the outputs from a controller. PWM control resumes from the next GSCLK rising edge. When this bit is '0', the GS counter is not reset and the outputs are not forced off even if a rising edge occurs at LAT. When the device is powered on, this bit is random.
122	ESPWM	—	ES-PWM mode enable bit 0 = Disabled, 1 = Enabled When this bit is '1', ES-PWM control mode is selected. When this bit is '0', the conventional PWM control mode is selected. If the TLC5948 is used for multiplexing a drive, the conventional PWM mode should be selected to prevent excess on/off switching. When the device is powered on, this bit is not random.
123, 124	LODVLT	—	LOD detection voltage selection bits LED open detection (LOD) detects a fault caused by an open LED by comparing the OUT*n* voltage to the LOD detection threshold voltage. The threshold voltage is selected with these bits. Table 11 shows the detect voltage truth table. When the device is powered on, this bit is random.
125, 126	LSDVLT	—	LSD detection voltage selection bits LED short detection (LSD) detects a fault caused by a shorted LED by comparing the OUT*n* voltage to the LSD detection threshold voltage. The threshold voltage is selected by these bits. Table 12 shows the detect voltage truth table. When the device is powered on, this bit is random.
127, 128	LATTMG	—	LOD/LSD data reading timing selection bits The LOD/LSD data reading time is selected by these bits. When DSPRPT is '1' and IDMRPT is '0', LOD/LSD data are loaded to the LOD/LSD data latch only once after new GS data are written into the second GS data latch. Table 13 shows the data load timing truth table. When the device is powered on, this bit is random.

Table 10. Function Control Data Latch Bit Description (continued)

BIT NUMBER	BIT NAME	DEFAULT VALUE (Binary)	DESCRIPTION
129	IDMENA	—	Invisible detection mode (IDM) enable bit 0 = Disabled, 1 = Enabled When this bit is '1', LED open detection (LOD) and LED short detection (LSD) check the LED status with very small current sinking at OUT*n* in a specific display segment. LOD and LSD can be checked even if OUT*n* is off. The current value is set by the IDMCUR bits (bits[132:131]) and the time is set by the LATTMG bits (bits[128:127]) in the function control data latch. Furthermore, the IDM operation is repeated every display period with auto display mode enabled when the IDMRPT bit (bit 130) is set to '1'. When this bit is '0', IDM is disabled. Therefore, LOD and LSD check the status of the LEDs at power-up only. When the device is powered on, this bit is random.
130	IDMRPT	—	Invisible detection mode (IDM) repeat bit 0 = Not repeated, 1 = Repeat When this bit is '1', IDM operation is repeated every display period with the auto display mode enabled. LOD and LSD check the LED status at OUT*n* every display period even if OUT*n* is off. When this bit is '0', IDM is not repeated. Therefore, LOD and LSD check the status of the LEDs once after the BLANK bit is changed from '1' to '0'. Otherwise, LAT is input for a GS write when TMGRST is '1' or the GS counter is reset at power-up once at the time programmed by LATTMG. IDM is disabled when IDMENA is set to '0' even if this bit is '1'. When the device is powered on, this bit is random.
131, 132	IDMCUR	—	Invisible detection mode (IDM) current select bits The OUT*n* sink current for IDM can be selected with these bits. Table 14 shows the current truth table. When the device is powered on, these bits are random.
133	OLDENA	—	Output leak detection mode (OLD) enable bit 0 = Disabled, 1 = Enabled When this bit is '1', output leak detection (OLD) checks the LED status with a small current sourced through OUT*n* in a display segment. OLD checks OUT*n* with GS data '0' only. When OUT*n* current leakage is detected, the OLD bit that corresponds to the leaking output is set to '1' in status information data (SID). When IDMENA is '1', OLD operation is disabled even if the OLDENA bit is set to '1' because OLD cannot get a correct result when IDM is enabled. When this bit is '0', OLD is not checked and all OLD bits in SID are set to '0'. OLD data are loaded into the OLD data latch at the 65535th GS clock. OLD data in SID may show the result of the previous display period, depending on the LAT input timing. When the device is powered on, this bit is random.
134-136	PSMODE	111	Power-save mode (PSM) selection bits The power-save mode is selected with these bits. Table 15 and Table 16 show the PSM truth tables. When the device is powered on, these bits are all set to '1'.

Table 11. LOD Threshold Voltage Truth Table

LODVLT		LED OPEN DETECTION (LOD) THRESHOLD VOLTAGE
BIT 124	BIT 123	
0	0	VLOD0 (0.3 V, typ)
0	1	VLOD1 (0.6 V, typ)
1	0	VLOD2 (0.9 V, typ)
1	1	VLOD3 (1.2 V, typ)

Table 12. LSD Threshold Voltage Truth Table

LSDVLT		LED SHORT DETECTION (LSD) THRESHOLD VOLTAGE
BIT 126	BIT 125	
0	0	VLSD0 (0.35 × VCC, typ)
0	1	VLSD1 (0.45 × VCC, typ)
1	0	VLSD2 (0.55 × VCC, typ)

Table 12. LSD Threshold Voltage Truth Table (continued)

LSDVLT		
BIT 126	**BIT 125**	**LED SHORT DETECTION (LSD) THRESHOLD VOLTAGE**
1	1	VLSD3 (0.65 × VCC, typ)

Table 13. LOD/LSD Data Latch Time Truth Table

LATTMG		
BIT 128	**BIT 127**	**LOD/LSD DATA LATCH TIMING**
0	0	17th GSCLK after BLANK bit is changed to '0' or GS counter is reset.(1)
0	1	33rd GSCLK after BLANK bit is changed to '0' or GS counter is reset.(1)
1	0	65th GSCLK after BLANK bit is changed to '0' or GS counter is reset.(1)
1	1	129th GSCLK after BLANK bit is changed to '0' or GS counter is reset.(1)

(1) When DSPRPT is '1' and IDMRPT is '0', the resulting LOD/LSD data are loaded to the LOD/LSD data latch only once after new GS data are written into the second GS data latch.

Table 14. IDM Sink Current Truth Table

IDMCUR		
BIT 132	**BIT 131**	**INVISIBLE DETECTION MODE (IDM) SINK CURRENT**
0	0	2 µA (typ)
0	1	10 µA (typ)
1	0	20 µA (typ)
1	1	1 mA (typ)

Table 15. PSM Select Truth Table: Bits[135:134]

PSMODE		
BIT 135	**BIT 134**	**POWER-SAVE MODE (PSM) FUNCTION**
0	0	Power-save mode is disabled in every condition
0	1	When all '0's are written into the second GS data latch, the device goes into power-save mode. When a rising edge at SCLK occurs, the device goes to normal operation and starts to control the output current. However, it takes some recovery time (t_{D7}) to resume normal operation after an SCLK rising edge.
1	0	When all '0's are written into the second GS data latch, the device goes into power-save mode. When the data (except all '0's) are written into the second GS data latch, the device goes to normal operation and starts to control the output current. However, it takes some recovery time (t_{D7}) to resume normal operation after the data changes.
1 (default)	1 (default)	Power-save mode is enabled in every condition. When the device is powered up, this mode is selected.

Table 16. PSM Select Truth Table: Bit[136]

PSMODE	
BIT 136	**POWER-SAVE MODE (PSM) FUNCTION**
0	The GSCLK signal is used for GS timing control in the same manner as in normal mode even if the device is in power-save mode.
1 (default)	When the device is in power-save mode, the GSCLK signal is forced low internally and GS timing control logic is not operational in order to reduce power consumption. However, if the lower two bits of PSMODE (bits[135:134]) are set to '0', the GSCLK signal is not forced low because the PSM is disabled. When the device is powered up, this mode is selected.

STATUS INFORMATION DATA (SID)

The status information data (SID) contain the status of the LED open detection (LOD), LED short detection (LSD), output leakage detection (OLD), pre-thermal warning (PTW), thermal error flag (TEF), and IREF short flag (ISF). When the LAT rising edge for a GS data write is input, the SID overwrite the common shift register data after the data in the common shift register are copied to the GS latch. If the MSB of the common shift register is '1', the SID data are not copied to the common shift register.

After being copied into the common shift register, new SID data cannot be copied until at least one new bit of data is written into the common shift register. Otherwise, the LAT signal is ignored. To recheck SID without changing the GS data, reprogram the common shift register with the same data currently programmed into the GS latch. When LAT goes high, the GS data do not change, but the SID data are loaded into the common shift register. LOD, LSD, OLD, PTW, TEF, and ISF are shifted out of SOUT with each rising edge of SCLK. The SID load configuration and SID read timing are shown in Figure 33 and Table 17, respectively.

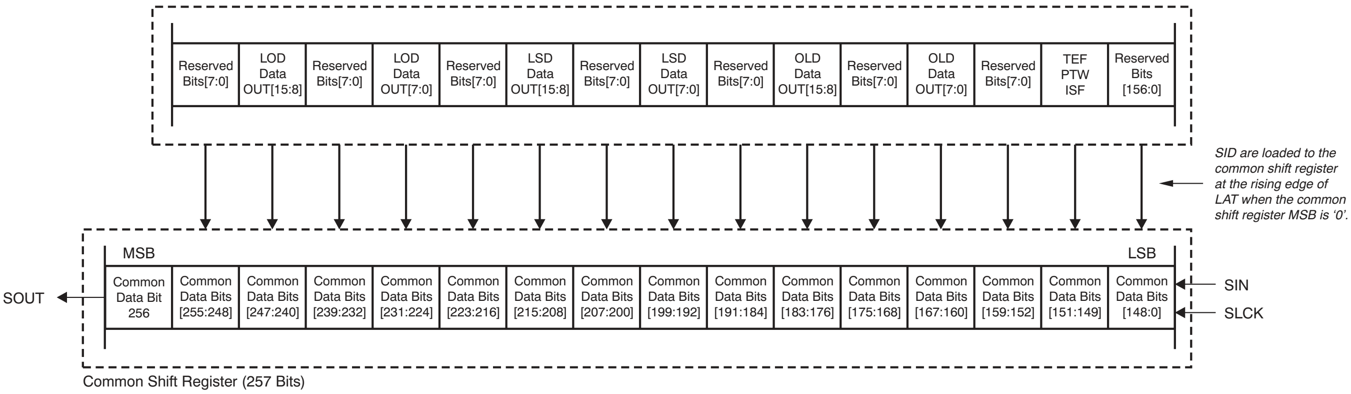


Figure 33. SID Load Configuration

Table 17. SID Load Description

COMMON SHIFT REGISTER BIT NUMBER	LOADED SID DESCRIPTION
256	No data loaded
[255:248]	Reserved
[247:240]	LED open detection (LOD) data of OUT[15:8] The bit assignment of the output channels is: Bit 240 = OUT8 LOD Bit 241 = OUT9 LOD … Bit 246 = OUT14 LOD Bit 247 = OUT15 LOD 0 = Normal operation 1 = LED is open or connected to GND with low resistance
[239:232]	Reserved
[231:224]	LED open detection (LOD) data of OUT[7:0] The bit assignment of the output channels is: Bit 224 = OUT0 LOD Bit 225 = OUT1 LOD … Bit 230 = OUT6 LOD Bit 231 = OUT7 LOD Bit data meaning 0 = Normal operation 1 = LED is open or connected to GND with low resistance
[223:216]	Reserved

Table 17. SID Load Description (continued)

COMMON SHIFT REGISTER BIT NUMBER	LOADED SID DESCRIPTION
[215:208]	LED short detection (LSD) data of OUT[15:8] The bit assignment of the output channels is: Bit 208 = OUT8 LSD Bit 209 = OUT9 LSD … Bit 214 = OUT14 LSD Bit 215 = OUT15 LSD 0 = Normal operation 1 = LED is shorted
[207:200]	Reserved
[199:192]	LED short detection (LSD) data of OUT[7:0] The bit assignment of the output channels is: Bit 192 = OUT0 LSD Bit 193 = OUT1 LSD … Bit 198 = OUT6 LSD Bit 199 = OUT7 LSD 0 = Normal operation 1 = LED is shorted
[191:184]	Reserved
Bits[183:176]	Output leak detection (OLD) data of OUT[15:8] The bit assignment of the output channels is: Bit 176 = OUT8 OLD Bit 177 = OUT9 OLD … Bit 182 = OUT14 OLD Bit 183 = OUT15 OLD 0 = Normal operation 1 = Output current leaks to GND when the output is off
Bits[175:168]	Reserved
Bits[167:160]	Output leak detection (OLD) data of OUT[7:0] The bit assignment of the output channels is: Bit 160 = OUT0 OLD Bit 161 = OUT1 OLD … Bit 166 = OUT6 OLD Bit 167 = OUT7 OLD 0 = Normal operation 1 = LED current leaks to GND when the output is off
Bits[159:152]	Reserved
Bit 151	Thermal error flag (TEF) data 0 = Normal operation 1 = Higher temperature condition than TEF detected temperature range
Bit 150	Pre-thermal warning (PTW) data 0 = Normal operation 1 = Higher temperature condition than PTW detected temperature range
Bit 149	IREF short flag (ISF) data, 1-bit data 0 = Normal operation 1 = IREF terminal connected to GND with low resistance
Bits[148:0]	Reserved

LED OPEN DETECTION (LOD)

LOD detects a fault caused by an LED open circuit or a short from OUT*n* to ground with low resistance, by comparing the OUT*n* voltage to the LOD detection threshold voltage. If the OUT*n* voltage is lower than the threshold voltage (set by the LODVLT bits in the first control data latch) when OUT*n* is on, that output LOD bit is set to '1' to indicate an open LED. Otherwise, the LOD bit is set to '0'. LOD data are only valid for outputs that are programmed to be on at time of the LOD data read selected by the LATTMG bits in the first control data latch. LOD data are latched into the LOD data latch at the time LOD data are read, as selected by LATTMG. LOD data for outputs programmed to be off at the LOD latch timing are always '0' when IDM is not enabled.

LED SHORT DETECTION (LSD)

LSD data detect a fault caused by a shorted LED by comparing the OUT*n* voltage to the LSD detection threshold voltage level set by LSDVLT in the first control data latch. If the OUT*n* voltage is higher than the programmed voltage when OUT*n* is on, the corresponding output LSD bit is set to '1' to indicate a shorted LED. Otherwise, the LSD bit is set to '0'. LSD data are only valid for outputs that are programmed to be on at the time when the LSD data are read, as selected by the LATTMG bits in the first control data latch. LSD data are latched into the LSD data latch at the time when the LSD data are read, as selected by LATTMG. LSD data for outputs programmed to be off at the LSD latch timing are always '0' when IDM is not enabled.

OUTPUT LEAKAGE DETECTION (OLD)

Output leakage detection (OLD) detects a fault caused by a short with high resistance from OUT*n* to GND by comparing the OUT*n* voltage to the LSD detection threshold voltage when the output is off. A small current is sourced from OUT*n* to detect LED leakage. OLD operation can be disabled by the OLDENA bit. Also, OLD is disabled when the invisible detection mode (IDM) is enabled (see the *Invisible Detection Mode* section). If the OUT*n* voltage is lower than the programmed LSD threshold voltage, the corresponding output OLD bit is set to '1' to indicate a leaking LED. Otherwise, the OLD bit is set to '0'. The OLD result is valid for disabled outputs only. The OLD data are latched into the OLD data latch at the end of the display period or when BLANK is changed to '1'. Also, the OLD data are latched when the GS data are written if the display timing reset is enabled. OLD data always read '0' when the output GS is not '0', or when OLD is disabled.

INVISIBLE DETECTION MODE (IDM)

Invisible detection mode (IDM) can detect LOD and LSD without dependency upon GS data. When the IDM bit in the function control data latch is set, OUT*n* starts sinking the current set by the IDMCUR bits in the function control latch at the first GSCLK; the IDM sink current is turned off at the GSCLK programmed by LATTMG. When the IDM current is turned off, LOD and LSD data are latched into the LOD/LSD data latch. During the IDM timing, the original PWM control continues. When the IDM bit in the control data latch is set to '0', the OUT*n* on/off timing is only controlled by GS data.

LOD/LSD data are not valid for approximately 1 μs after the constant-current output turns on. Therefore, GS data must be set to turn on the output for at least 1 μs. Furthermore, the LOD/LSD latch timing bits (LATTMG) should be set as shown in Equation 4:

$$\text{The number of GSCLK to obtain valid LOD/LSD} = 1\ \mu s / T_{GSCLK} \quad (4)$$

where:

- T_{GSCLK} = one GSCLK period

If the GSCLK frequency is 33 MHz, the outputs must be on for 33 GSCLK periods or more. Therefore, the LATTMG bits can only be set to 01, 10, or 11b. If the GSCLK frequency is 2 MHz, the outputs must be on for two GSCLK periods or more. In this case, the LATTMG bits can be set to any pattern.

When LOD/LSD data must be read with invisible brightness, the LATTMG bits should be set to the minimum data larger than the calculated number of GSCLK periods defined by Equation 4. IDM does not work in power-save mode. Figure 34 shows the LOD/LSD/OLD/IDM circuit and Table 18 shows a truth table for LOD, LSD, and OLD. IDM operation timing is shown in Figure 35.

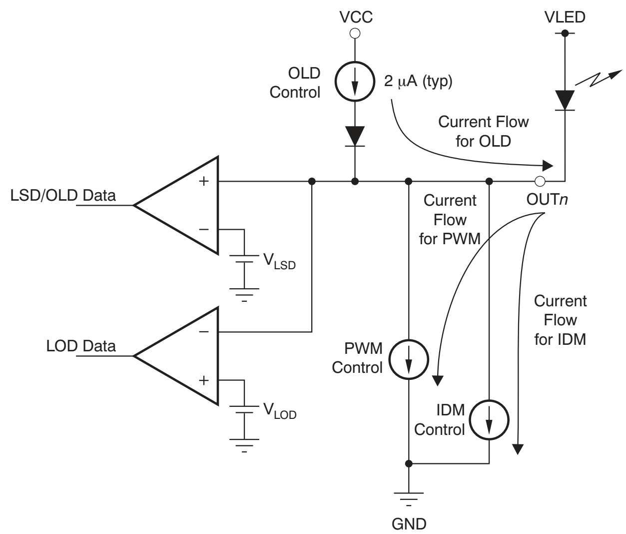
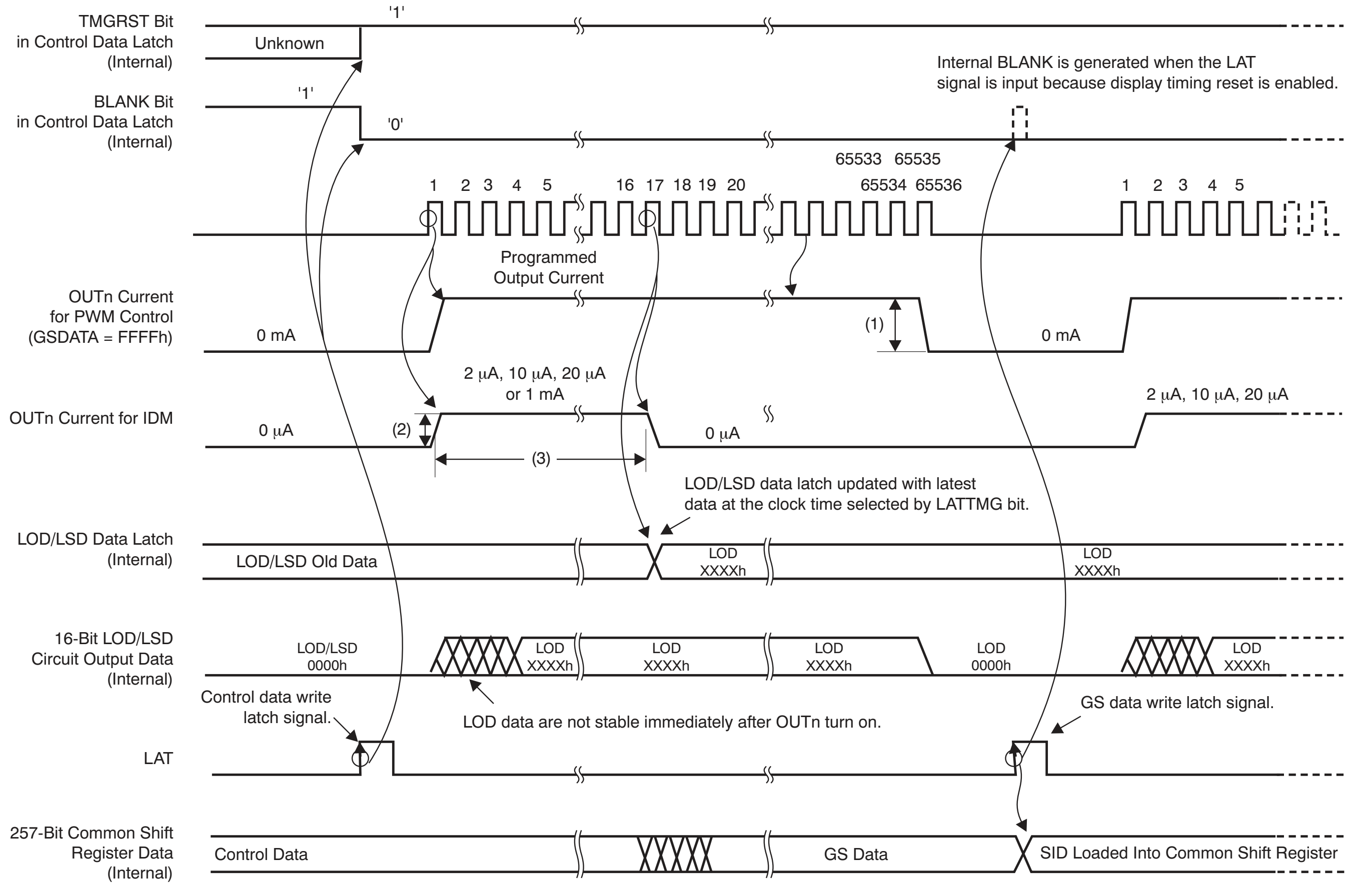


Figure 34. LOD/LSD/OLD/IDM Circuit

Table 18. LOD/LSD/OLD/ISF/PTW/TEF Truth Table

SID DATA	CONDITION					
	LOD	LSD	OLD	ISF	PTW	TEF
0	LED is not opened ($V_{OUTn} > V_{LOD}$)	LED is not shorted ($V_{OUTn} \le V_{LSD}$)	OUT*n* does not leak to GND ($V_{OUTn} > V_{LSD}$ when constant-current output off and OUT*n* source current on)	IREF terminal is not shorted	Device temperature is lower than pre-thermal warning temperature (temperature ≤ T_{PTW})	Device temperature is lower than thermal shutdown threshold temperature (temperature ≤ T_{TEF})
1	LED is open or shorted to GND ($V_{OUTn} \le V_{LOD}$)	LED is shorted between anode and cathode, or shorted to higher voltage side ($V_{OUTn} > V_{LSD}$)	Current leaks from OUT*n* to internal GND, or OUT*n* is shorted to external GND with high impedance ($V_{OUTn} \le V_{LSD}$ when constant-current output off and OUT*n* source current on)	IREF terminal is shorted to GND with low impedance and OUT*n* are forced off	Device temperature is higher than pre-thermal warning temperature (temperature > T_{PTW})	Device temperature is higher than thermal shutdown threshold temperature and driver is forced off (temperature > T_{TEF})



(1) Set the current with the external resistor and DC/BC data.
(2) Select the output current with the IDMCUR bit in the control data latch.
(3) Select clock time with the LATTMG bit in the control data latch.

Figure 35. PWM and IDM Operation Timing

POWER-SAVE MODE (PSM)

The power-save mode control bits are assigned in the function control data latch. The device dissipation current becomes 10 μA (typ.) in this mode. When the two lower bits in PSMODE are '01', '10', or '11', the power-save mode is enabled. When the lower two bits are '01' or '10', if all '0' data are written in the second GS data latch, the TLC5948 goes into power-save mode. When a rising edge is generated at SCLK with the lower two PSMODE bits (bits[135:134]) set to '01', the device leaves PSM for normal operation. OUT*n* are turned on at the first GSCLK of the next display period after the device has left PSM. Figure 36 shows the power-save mode timing diagram.

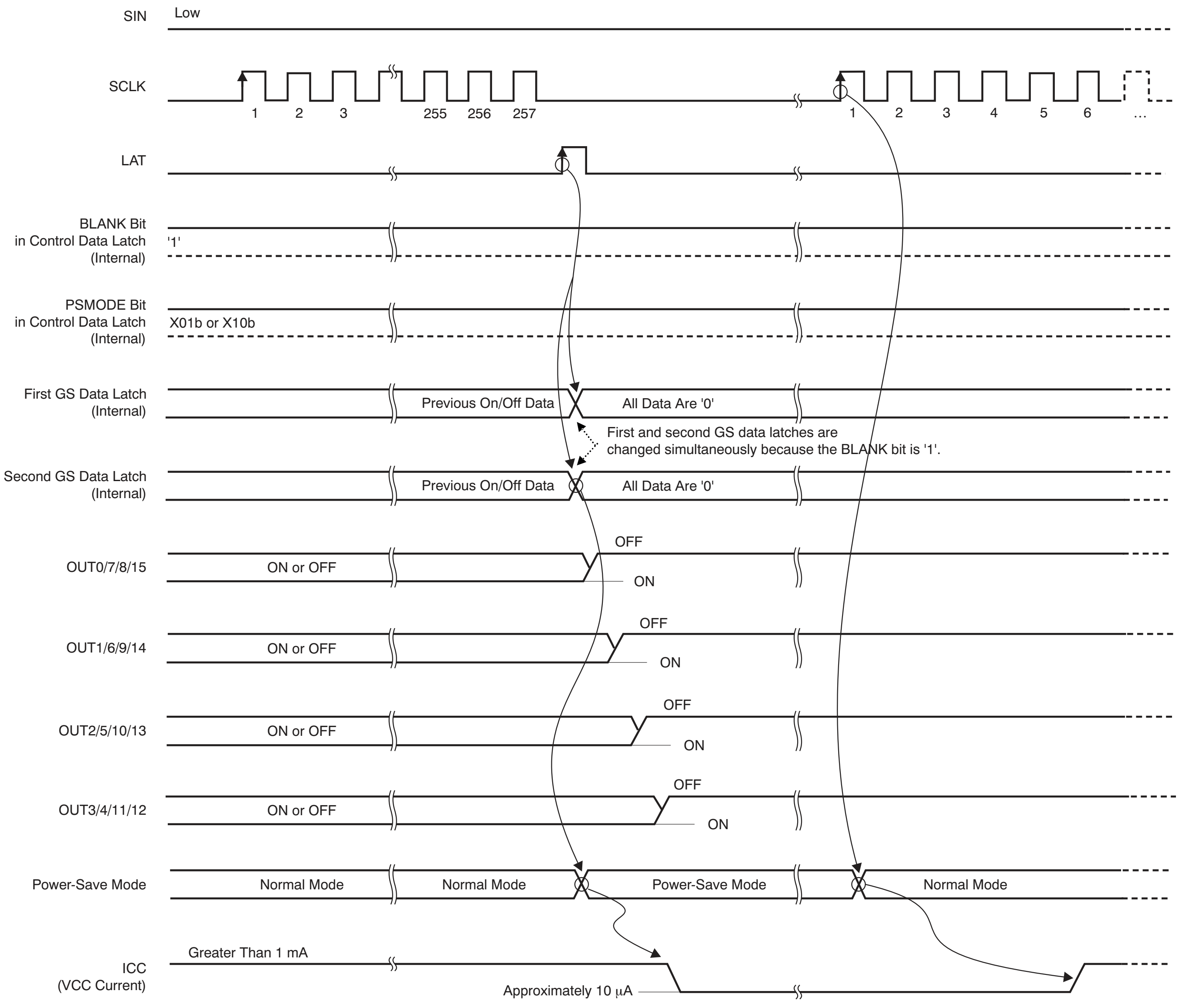


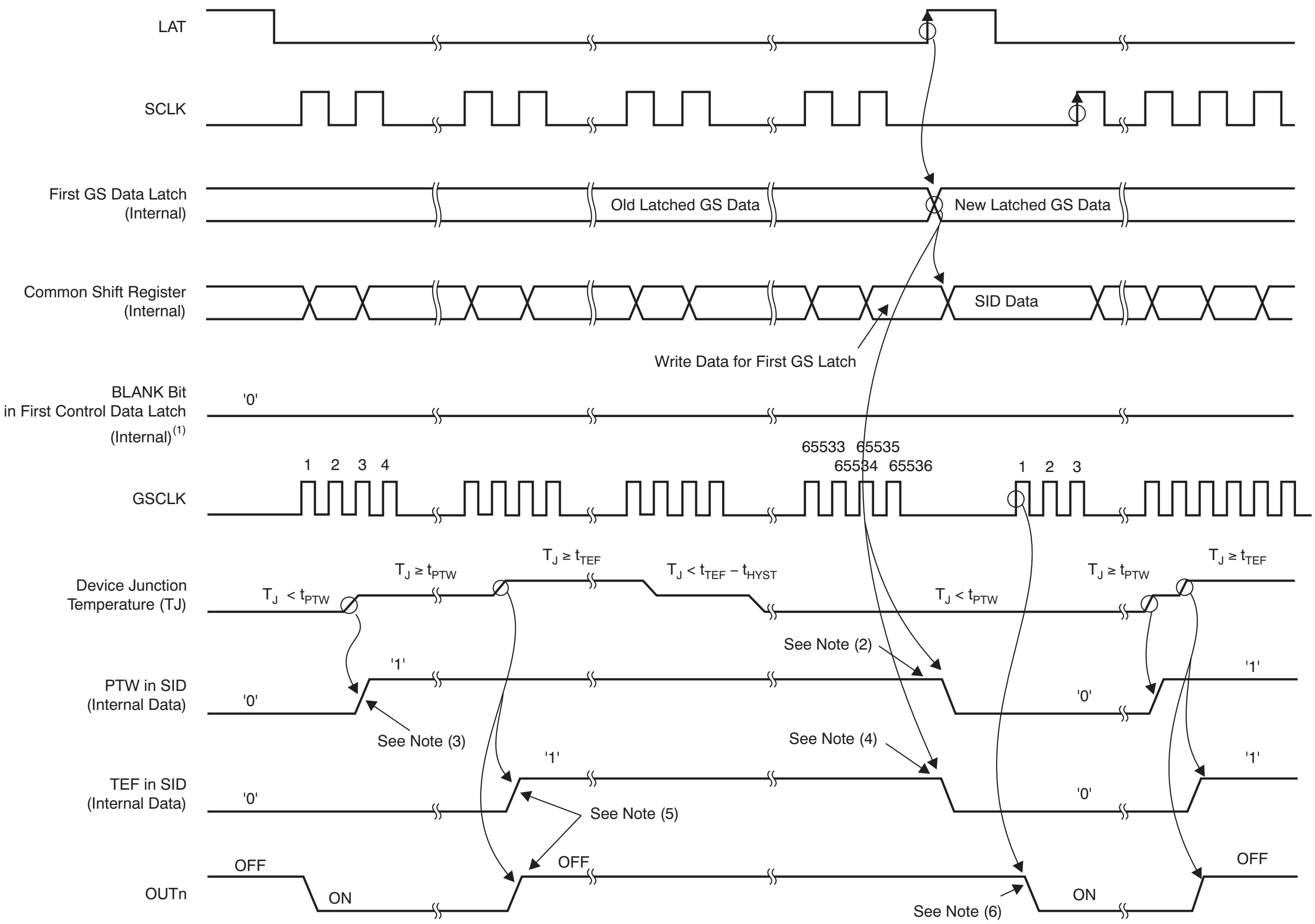
Figure 36. Power-Save Mode Timing (Bits 135 and 134 = 01)

CURRENT REFERENCE (IREF PIN) SHORT FLAG (ISF)

The ISF function indicates that the IREF terminal is shorted with low impedance to GND. The ISF bit in the SID is set to '1' during this condition. Then all outputs, OUT*n*, are forced off. See Table 18 for the ISF truth table.

PRE-THERMAL WARNING (PTW)

The PTW function indicates that the device junction temperature is high. The PTW in the SID is set to '1' while the device junction temperature exceeds the temperature threshold (T_{PTW} = +138°C, typ); however, the outputs are not forced off. When the PTW is set, the device temperature should be reduced by lowering the power dissipated in it to avoid a forced shutdown by the thermal shutdown circuit. This reduction can be accomplished by lowering the values of the GS, DC, or BC data. When the device junction temperature drops below the T_{PTW} temperature, the PTW bit in the SID is set to '0'. Figure 37 shows a timing diagram; see Table 18 for the PTW truth table.



(1) This internal signal is reset when LAT is input for the GS write with the display timing reset enabled.

(2) The PTW bit in SID is reset to '0' at the LAT rising edge for a GS data write if the device junction temperature is below t_{PTW}.

(3) The PTW bit is set to '1' when the device junction temperature is greater than t_{PTW}.

(4) The TEF bit in SID is reset to '0' at the LAT rising edge for a GS data write if the device junction temperature is below t_{TEF}.

(5) OUT0 to OUT15 are forced off when T_J exceeds t_{TEF}. Furthermore, the TEF bit is set to '1' at the same time.

(6) OUT0 to OUT15 are turned on at the first GSCLK rising edge if the device junction temperature is below t_{TEF} with BLANK set to '0'.

Figure 37. PTW/TEF/TSD Timing

THERMAL SHUTDOWN (TSD) AND THERMAL ERROR FLAG (TEF)

The thermal shutdown (TSD) function turns off all constant-current outputs on the device when the junction temperature (T_J) exceeds the threshold (T_{TEF} = +165°C, typ) and sets the thermal error flag (TEF) to '1'. All outputs are latched off when TEF is set to '1' and remain off at least until the next GS cycle starts and the junction temperature drops below (T_{TEF} – T_{HYST}). TEF remains '1' until a rising edge at LAT occurs and the temperature is reduced. TEF is set to '0' once the junction temperature drops below (T_{TEF} – T_{HYST}), but the output does not turn on until the first GSCLK in the next display period occurs even if TEF is set to '0'. See Figure 37 for a timing diagram; Table 18 shows the truth table for TEF.

NOISE REDUCTION

Large surge currents may flow through the device and the board on which the device is mounted if all 16 outputs turn on simultaneously at the start of each GS cycle. These large current surges could introduce detrimental noise and electromagnetic interference (EMI) into other circuits. The TLC5948 turns the outputs on with delay for each group independently to provide a soft-start feature. The output current sinks are grouped into four groups in each color group. The first output group that is turned on/off are OUT0/7/8/15; the second output group is OUT1/6/9/14; the third output group is OUT2/5/10/13; and the fourth output group is OUT3/4/11/12. Each output group is turned on and off sequentially with a small delay between the groups. However, each output on/off is controlled by the GS clock.

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/ Ball Finish	MSL Peak Temp [3]	Samples (Requires Login)
TLC5948DBQ	ACTIVE	SSOP/QSOP	DBQ	24	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLC5948DBQR	ACTIVE	SSOP/QSOP	DBQ	24	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLC5948PWP	ACTIVE	HTSSOP	PWP	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	
TLC5948PWPR	ACTIVE	HTSSOP	PWP	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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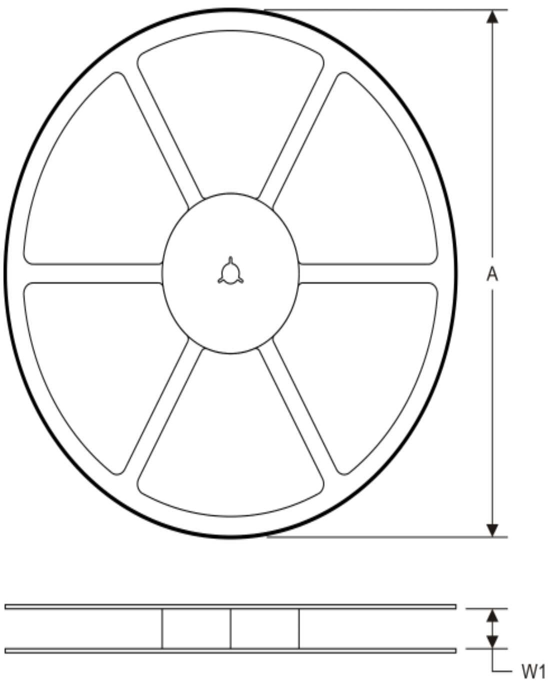
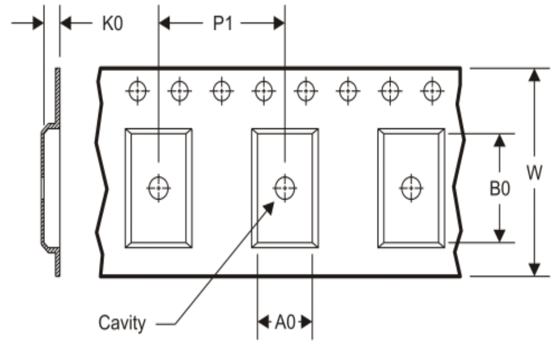
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



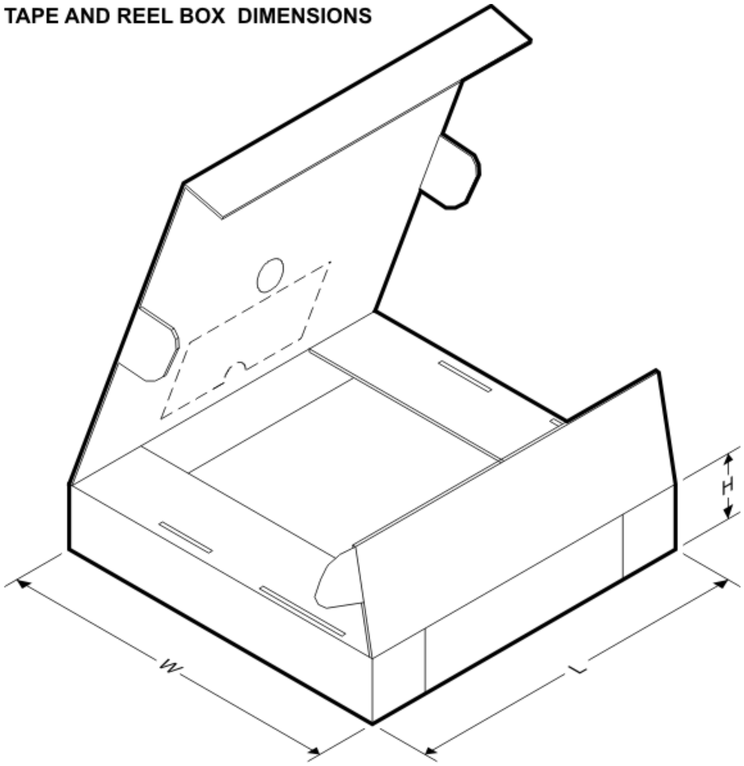
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC5948DBQR	SSOP/ QSOP	DBQ	24	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
TLC5948PWPR	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

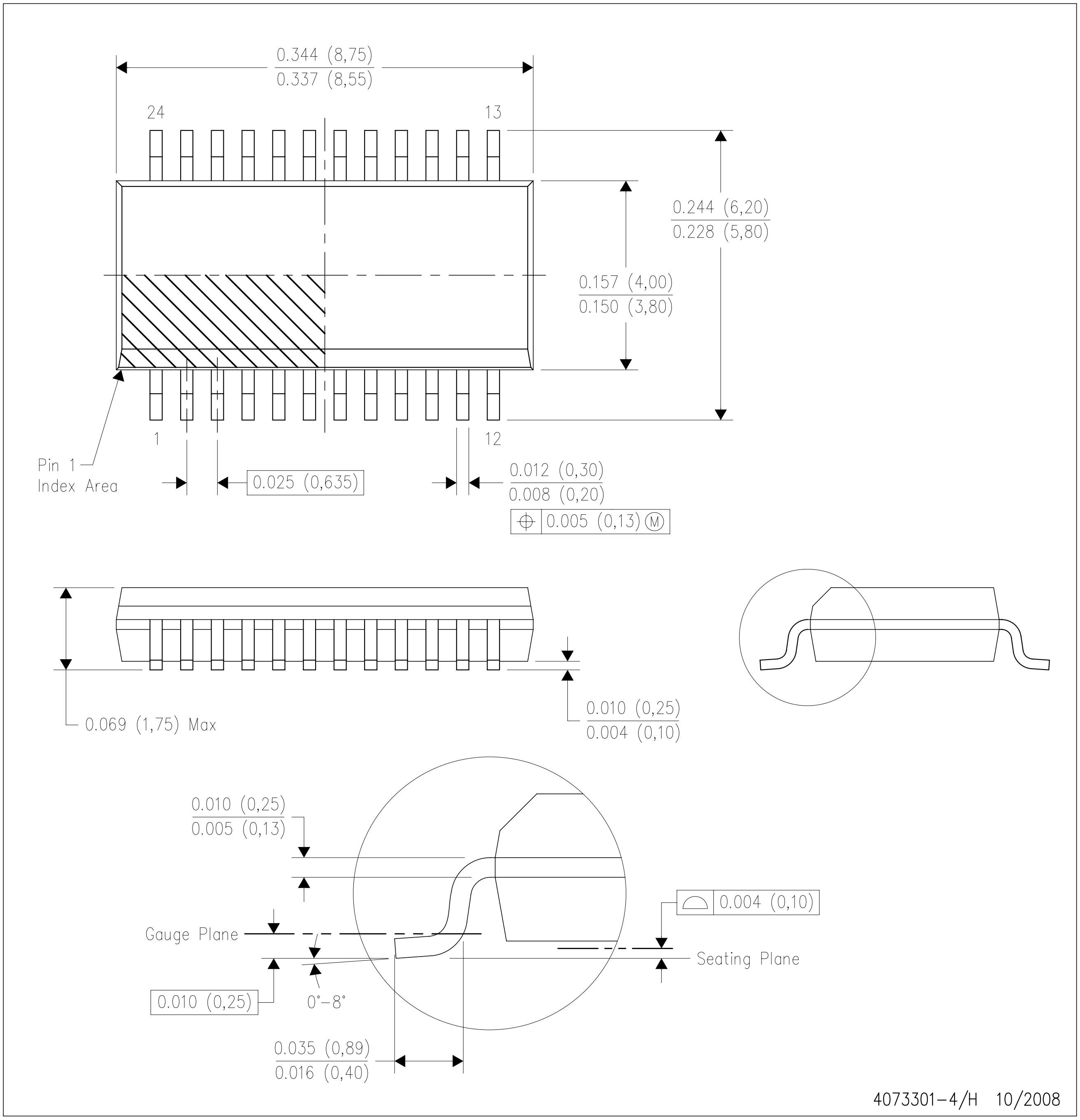
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

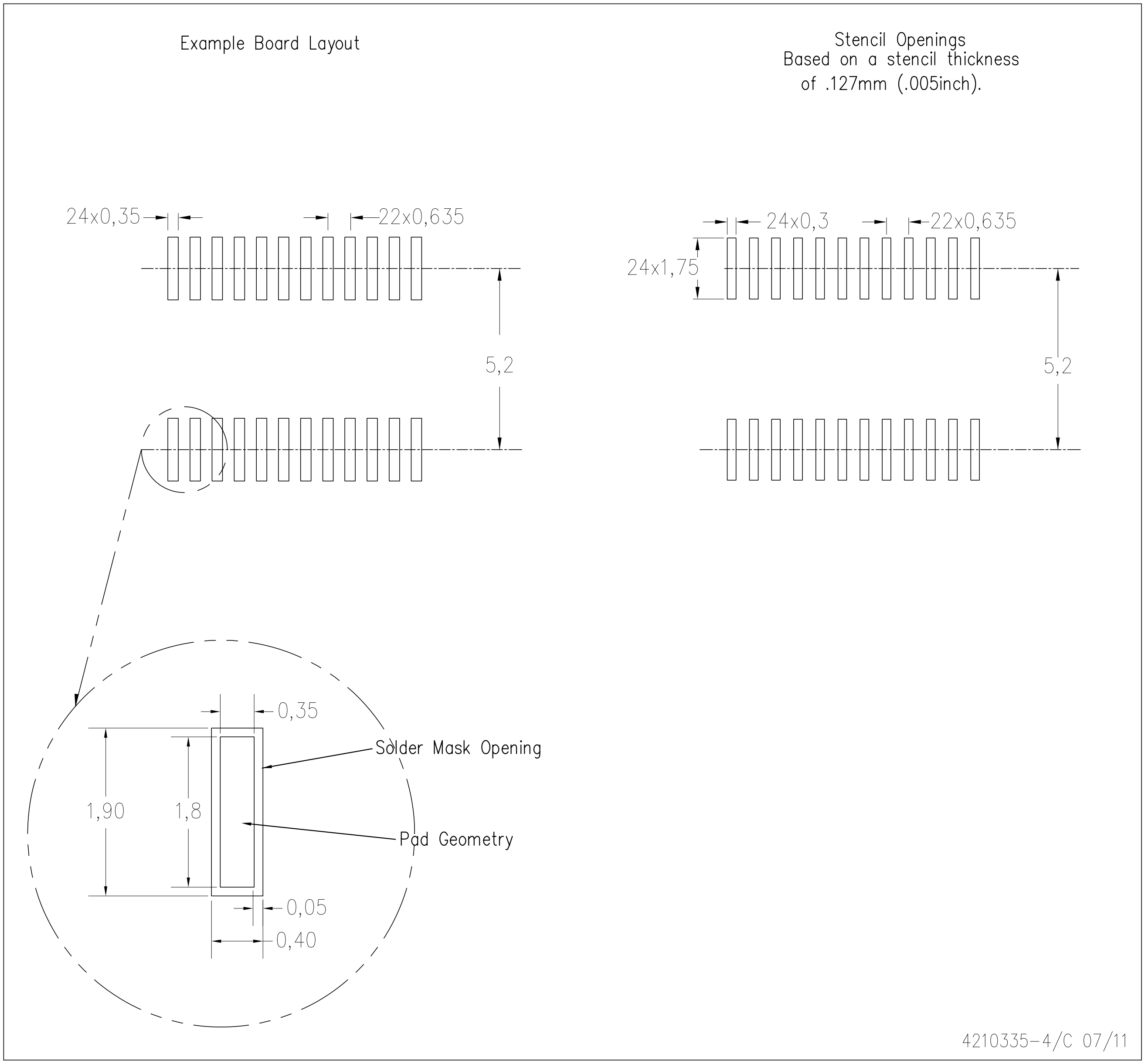
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC5948DBQR	SSOP/QSOP	DBQ	24	2500	346.0	346.0	33.0
TLC5948PWPR	HTSSOP	PWP	24	2000	346.0	346.0	33.0

DBQ (R–PDSO–G24) PLASTIC SMALL–OUTLINE PACKAGE



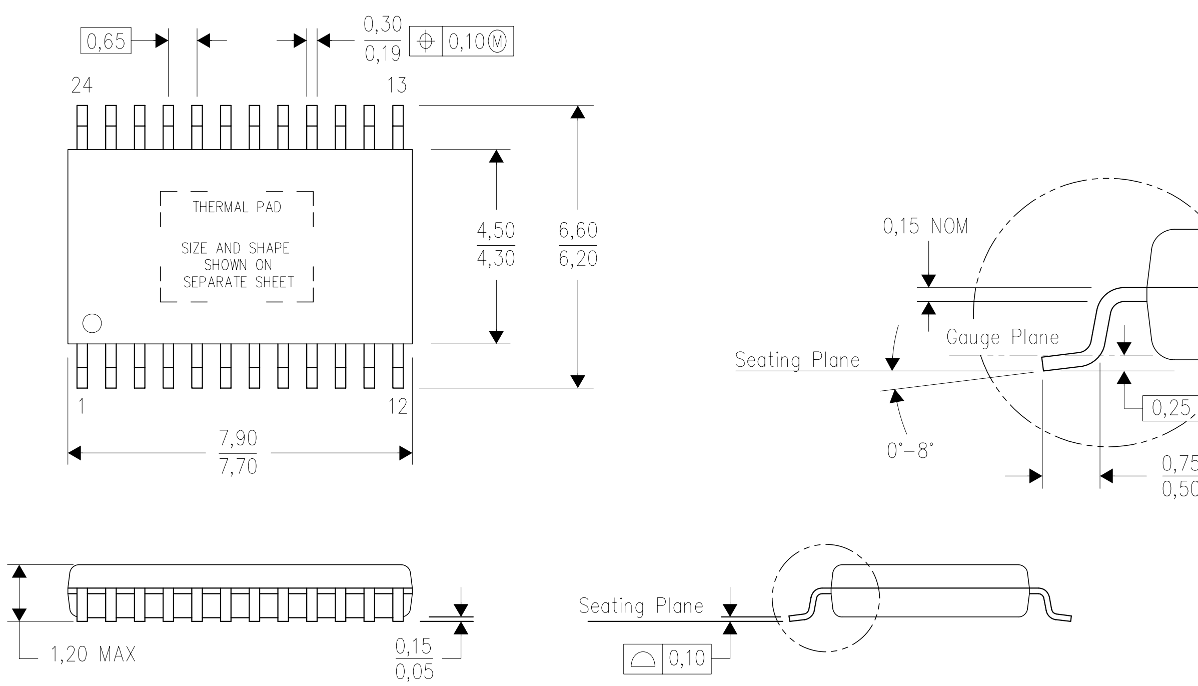
NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15) per side.
- D. Falls within JEDEC MO–137 variation AE.

DBQ (R–PDSO–G24) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

PWP (R–PDSO–G24)　　　　PowerPAD™ PLASTIC SMALL OUTLINE



4073225-5/I 05/11

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusions. Mold flash and protrusion shall not exceed 0.15 per side.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- E. Falls within JEDEC MO–153

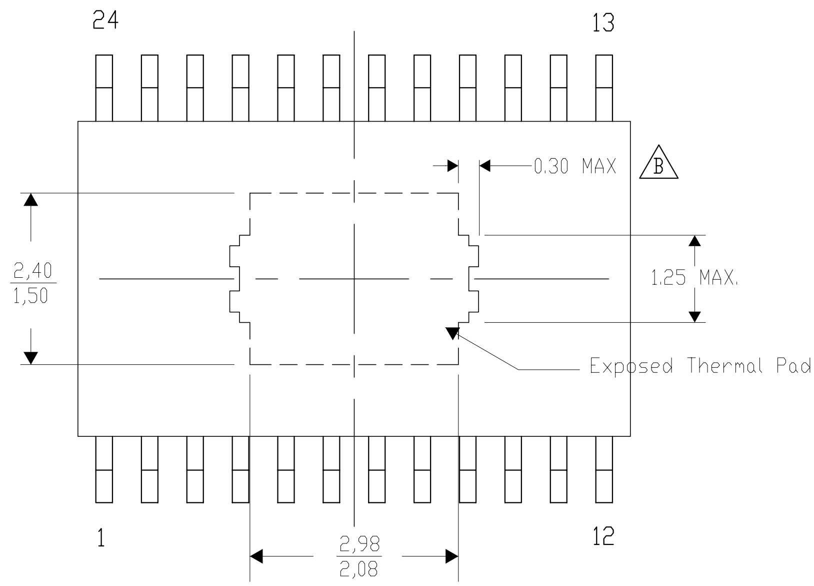
PWP (R-PDSO-G24) PowerPAD™ SMALL PLASTIC OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Top View

Exposed Thermal Pad Dimensions

4206332-28/Y 10/11

NOTE: A. All linear dimensions are in millimeters

B. Exposed tie strap features may not be present.

PowerPAD is a trademark of Texas Instruments