

EMIPAK 1B PressFit Power Module

800 V Half Controlled Single Phase Bridge, 20 A

600 V PFC and Half Bridge MOSFET, 40 A



EMIPAK 1B
(package example)



RoHS
COMPLIANT

FEATURES

- E series power MOSFET with fast body diode
- MOAT and SiC diode technology
- Thyristor phase control
- Exposed Al₂O₃ substrate with low thermal resistance
- Low input capacitance
- Low switching and conduction losses
- Ultra low gate charge Q_g
- Low internal inductances
- Qualified using AQG324 guideline as reference
- PressFit pins locking technology
PATENT(S): www.vishay.com/patents
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

DESCRIPTION

The EMIPAK 1B package is easy to use thanks to the PressFit pins. The exposed substrate provides improved thermal performance.

The optimized layout also helps to minimize stray parameters, allowing for better EMI performance.

| PRIMARY CHARACTERISTICS | |
|--|--|
| HALF CONTROLLED SINGLE PHASE BRIDGE | |
| I _O at T _{SINK} = 115 °C | 20 A |
| D1, D2 | |
| V _{RRM} | 800 V |
| V _{FM} typical at 20 A | 1.10 V |
| SCR1, SCR2 | |
| V _{RRM} /V _{DRM} | 800 V |
| V _{TM} typical at 20 A | 1.29 V |
| QB1 - QB2 - QB3 MOSFET | |
| V _{DSS} | 600 V |
| R _{DS(on)} typical at I _C = 40 A | 37 mΩ |
| I _D at T _{SINK} = 39 °C | 40 A |
| D3 SILICON CARBIDE CLAMP DIODE | |
| V _{RRM} | 600 V |
| V _{FM} typical at 30 A | 1.72 V |
| I _F at T _C = 46 °C | 30 A |
| Type | Modules - MOSFET |
| Package | EMIPAK 1B |
| Circuit configuration | Half controlled input bridge plus MOSFET boost PFC leg and MOSFET half bridge inverter |

PATENT(S): www.vishay.com/patents

This Vishay product is protected by one or more United States and international patents.



| ABSOLUTE MAXIMUM RATINGS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) | | | | |
|--|-------------------|---|-------------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MAX. | UNITS |
| Operating junction temperature | T_J | | 150 | °C |
| Storage temperature range | T_{Stg} | | -40 to +150 | |
| RMS isolation voltage | V_{ISOL} | $T_J = 25\text{ }^\circ\text{C}$, all terminals shorted, $f = 50\text{ Hz}$, $t = 1\text{ s}$ | 3500 | V |
| HALF CONTROLLED SINGLE PHASE BRIDGE | | | | |
| Maximum DC output current of bridge | I_O | $T_{SINK} = 25\text{ }^\circ\text{C}$ | 44 | A |
| | | $T_{SINK} = 80\text{ }^\circ\text{C}$ | 31 | |
| One-cycle non-repetitive on-state peak or forward current | I_{FSM}/I_{TSM} | 10 ms sine or 6 ms rectangular pulse, $T_J = 150\text{ }^\circ\text{C}$, no voltage reapplied | 273 | |
| Maximum I^2t for fusing | I^2t | 10 ms sine pulse, no voltage reapplied | 374 | A^2s |
| Maximum $I^2\sqrt{t}$ for fusing | $I^2\sqrt{t}$ | $t = 0.1\text{ ms}$ to 10 ms , no voltage reapplied | 3740 | $A^2\sqrt{s}$ |
| Value of threshold voltage | $V_{F(TO)}$ | $T_J = 150\text{ }^\circ\text{C}$ | 1.04 | V |
| Slope resistance | r_t | $T_J = 150\text{ }^\circ\text{C}$ | 38.9 | $m\Omega$ |
| Repetitive peak reverse diode | V_{RRM} | | 800 | V |
| Repetitive peak direct and reverse thyristor | V_{RRM}/V_{DRM} | | 800 | V |
| Maximum critical rate of rise of off-state voltage - thyristor | dV/dt | $V_{DRM} = 80\%$ of rated voltage, $T_J = 125\text{ }^\circ\text{C}$ | 500 | $V/\mu s$ |
| Maximum non-repetitive rate of rise of turned on current - thyristor | dI/dt | $T_J = 125\text{ }^\circ\text{C}$ | 150 | $A/\mu s$ |
| QB1 - QB2 - QB3 MOSFET | | | | |
| Drain to source voltage | V_{DSS} | | 600 | V |
| Gate to source voltage | V_{GS} | | ± 30 | |
| Pulsed drain current | I_{DM} | $V_{GS} = 10\text{ V}$ | 135 | A |
| Continuous drain current | I_D | $T_{SINK} = 25\text{ }^\circ\text{C}$ | 42 | A |
| | | $T_{SINK} = 80\text{ }^\circ\text{C}$ | 32 | |
| Power dissipation | P_D | $T_{SINK} = 25\text{ }^\circ\text{C}$ | 174 | W |
| | | $T_{SINK} = 80\text{ }^\circ\text{C}$ | 97 | |
| Single pulse avalanche energy | E_{AS} | $L = 10\text{ mH}$, $I_{AS} = 23\text{ A}$, $T_J = 25\text{ }^\circ\text{C}$ | 2645 | mJ |
| Pulsed source current (body diode) | I_{SM} | | 135 | A |
| D3 SILICON CARBIDE CLAMP DIODE | | | | |
| Cathode to anode voltage | V_{RRM} | | 600 | V |
| Single pulse forward current | I_{FSM} | 10 ms sine or 6 ms rectangular pulse, $T_J = 25\text{ }^\circ\text{C}$ | 234 | A |
| Diode continuous forward current | I_F | $T_{SINK} = 25\text{ }^\circ\text{C}$ | 33 | A |
| | | $T_{SINK} = 80\text{ }^\circ\text{C}$ | 23 | |
| Power dissipation | P_D | $T_{SINK} = 25\text{ }^\circ\text{C}$ | 96 | W |
| | | $T_{SINK} = 80\text{ }^\circ\text{C}$ | 54 | |



| ELECTRICAL SPECIFICATIONS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) | | | | | | |
|---|--------------------------------|---|------|-------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNITS |
| INPUT SINGLE PHASE BRIDGE | | | | | | |
| D1, D2 | | | | | | |
| Forward voltage drop | V_{FM} | $I_F = 20\text{ A}$ | - | 1.10 | 1.32 | V |
| | | $I_F = 20\text{ A}, T_J = 150\text{ }^\circ\text{C}$ | - | 1.02 | - | |
| Breakdown voltage | V_{BR} | $I_R = 500\text{ }\mu\text{A}$ | 800 | - | - | V |
| Reverse leakage current | I_{RM} | $V_R = 800\text{ V}$ | - | 0.7 | 100 | μA |
| | | $V_R = 800\text{ V}, T_J = 150\text{ }^\circ\text{C}$ | - | 0.7 | - | mA |
| SCR1, SCR2 | | | | | | |
| Peak on state voltage | V_{TM} | $I_{TM} = 20\text{ A}$ | - | 1.29 | 1.70 | V |
| | | $I_{TM} = 20\text{ A}, T_J = 150\text{ }^\circ\text{C}$ | - | 1.24 | - | |
| Breakdown voltage | V_{RRM}/V_{DRM} | $I_R = 500\text{ }\mu\text{A}$ | 800 | - | - | V |
| Reverse and direct leakage current | I_{RM}/I_{DM} | $V_R = 800\text{ V}$ | - | 1.0 | 100 | μA |
| | | $V_R = 800\text{ V}, T_J = 150\text{ }^\circ\text{C}$ | - | 4.5 | - | mA |
| QB1 - QB2 - QB3 MOSFET | | | | | | |
| Drain to source breakdown voltage | BV_{DSS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | 600 | - | - | m Ω |
| Drain to source on resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}, I_D = 40\text{ A}$ | - | 37 | 48 | |
| | | $V_{GS} = 10\text{ V}, I_D = 40\text{ A}, T_J = 150\text{ }^\circ\text{C}$ | - | 87 | - | |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | 1.8 | 2.7 | 4.4 | V |
| Temperature coefficient of threshold voltage | $\Delta V_{GS(th)}/\Delta T_J$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ (25 °C to 125 °C) | - | -11.4 | - | mV/°C |
| Forward transconductance | g_{fs} | $V_{DS} = 20\text{ V}, I_D = 40\text{ A}$ | - | 48 | - | S |
| Transfer characteristics | V_{GS} | $V_{DS} = 20\text{ V}, I_D = 40\text{ A}$ | - | 5.3 | - | V |
| Zero gate voltage drain current | I_{DSS} | $V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}$ | - | 0.7 | 10 | μA |
| | | $V_{GS} = 0\text{ V}, V_{DS} = 600\text{ V}, T_J = 150\text{ }^\circ\text{C}$ | - | 1.1 | - | mA |
| Gate to source leakage current | I_{GSS} | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ | - | - | ± 150 | nA |
| QB1 - QB2 - QB3 MOSFET BODY DIODE | | | | | | |
| Source-to-drain voltage drop | V_{SD} | $I_{SD} = 40\text{ A}, V_{GS} = 0\text{ V}$ | - | 0.92 | 1.32 | V |
| D3 SILICON CARBIDE CLAMP DIODE | | | | | | |
| Forward voltage drop | V_{FM} | $I_F = 30\text{ A}$ | - | 1.72 | 1.98 | V |
| | | $I_F = 30\text{ A}, T_J = 150\text{ }^\circ\text{C}$ | - | 2.37 | - | |
| Breakdown voltage | V_{BR} | $I_R = 1.5\text{ mA}$ | 600 | - | - | V |
| Reverse leakage current | I_{RM} | $V_R = 600\text{ V}$ | - | 0.6 | 300 | μA |
| | | $V_R = 600\text{ V}, T_J = 150\text{ }^\circ\text{C}$ | - | 4.2 | - | |

| TRIGGERING ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) | | | | |
|--|-------------|---|--------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | VALUES | UNITS |
| SCR1, SCR2 | | | | |
| Maximum peak gate power | P_{GM} | | 8.0 | W |
| Maximum average gate power | $P_{G(AV)}$ | | 2.0 | W |
| Maximum peak gate current | I_{GM} | | 1.5 | A |
| Maximum peak negative gate voltage | V_{GM} | | 10 | V |
| Maximum gate voltage required to trigger | V_{GT} | $T_J = 25\text{ }^\circ\text{C}$, anode supply = 6 V resistive load | 2.0 | V |
| | | $T_J = 125\text{ }^\circ\text{C}$, anode supply = 6 V resistive load | 0.75 | |
| Maximum gate current required to trigger | I_{GT} | $T_J = 25\text{ }^\circ\text{C}$, anode supply = 6 V resistive load | 45 | mA |
| | | $T_J = 125\text{ }^\circ\text{C}$, anode supply = 6 V resistive load | 14 | |
| Maximum gate voltage that will not trigger | V_{GD} | $T_J = 125\text{ }^\circ\text{C}$, 100 % V_{DRM} applied | 0.2 | V |
| Maximum gate current that will not trigger | I_{GD} | $T_J = 125\text{ }^\circ\text{C}$, 100 % V_{DRM} applied | 1.0 | mA |



| SWITCHING ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) | | | | |
|---|----------|-----------------------------------|--------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | VALUES | UNITS |
| SCR1, SCR2 | | | | |
| Typical turn-on time | t_{gt} | $T_J = 25\text{ }^\circ\text{C}$ | 0.9 | μs |
| Typical reverse recovery time | t_{rr} | $T_J = 125\text{ }^\circ\text{C}$ | 4 | |
| Typical turn-off time | t_g | $T_J = 125\text{ }^\circ\text{C}$ | 110 | |

| SWITCHING CHARACTERISTICS ($T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted) | | | | | | |
|---|--------------|--|------|------|------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | MIN. | TYP. | MAX. | UNITS |
| QB1 MOSFET with D3 CLAMP DIODE | | | | | | |
| Total gate charge (turn-on) | Q_g | $I_D = 32\text{ A}$, $V_{DS} = 480\text{ V}$, $V_{GS} = 10\text{ V}$ | - | 240 | - | nC |
| Gate to source charge (turn-on) | Q_{gs} | | - | 58 | - | |
| Gate to drain charge (turn-on) | Q_{gd} | | - | 96 | - | |
| Turn-on switching loss | E_{ON} | $I_D = 40\text{ A}$, $V_{DD} = 450\text{ V}$, $V_{GS} = +10\text{ V} / -10\text{ V}$, $R_g = 10\text{ }\Omega$, $L = 500\text{ }\mu\text{H}$ | - | 0.53 | - | mJ |
| Turn-on delay time | $t_{d(on)}$ | | - | 43 | - | ns |
| Rise time | t_r | | - | 26 | - | |
| Turn-off switching loss | E_{OFF} | | - | 0.19 | - | mJ |
| Turn-off delay time | $t_{d(off)}$ | | - | 160 | - | ns |
| Fall time | t_f | | - | 18 | - | |
| Turn-on switching loss | E_{ON} | $I_D = 40\text{ A}$, $V_{DD} = 450\text{ V}$, $V_{GS} = +10\text{ V} / -10\text{ V}$, $R_g = 10\text{ }\Omega$, $L = 500\text{ }\mu\text{H}$, $T_J = 125\text{ }^\circ\text{C}$ | - | 0.63 | - | mJ |
| Turn-on delay time | $t_{d(on)}$ | | - | 39 | - | ns |
| Rise time | t_r | | - | 29 | - | |
| Turn-off switching loss | E_{OFF} | | - | 0.23 | - | mJ |
| Turn-off delay time | $t_{d(off)}$ | | - | 162 | - | ns |
| Fall time | t_f | | - | 19 | - | |
| Input capacitance | C_{iss} | $V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$ | - | 7500 | - | pF |
| Output capacitance | C_{oss} | | - | 378 | - | |
| Reverse transfer capacitance | C_{rss} | | - | 5 | - | |
| Reverse bias safe operating area | RBSOA | $T_J = 150\text{ }^\circ\text{C}$, $I_D = 100\text{ A}$, $V_{DD} = 400\text{ V}$, $V_P = 600\text{ V}$, $R_g = 10\text{ }\Omega$, $V_{GS} = +10\text{ V} / 0\text{ V}$ | | | | |
| QB2 - QB3 MOSFET | | | | | | |
| Total gate charge (turn-on) | Q_g | $I_D = 32\text{ A}$, $V_{DS} = 480\text{ V}$, $V_{GS} = 10\text{ V}$ | - | 240 | - | nC |
| Gate-source charge | Q_{gs} | | - | 58 | - | |
| Gate-drain charge | Q_{gd} | | - | 96 | - | |
| Turn-off switching loss | E_{OFF} | $I_D = 40\text{ A}$, $V_{DD} = 450\text{ V}$, $V_{GS} = +10\text{ V} / -10\text{ V}$, $R_g = 10\text{ }\Omega$, $L = 500\text{ }\mu\text{H}$ | - | 0.17 | - | mJ |
| Turn-off delay time | $t_{d(off)}$ | | - | 157 | - | ns |
| Fall time | t_f | | - | 18 | - | |
| Turn-off switching loss | E_{OFF} | $I_D = 40\text{ A}$, $V_{DD} = 450\text{ V}$, $V_{GS} = +10\text{ V} / -10\text{ V}$, $R_g = 10\text{ }\Omega$, $L = 500\text{ }\mu\text{H}$, $T_J = 125\text{ }^\circ\text{C}$ | - | 0.19 | - | mJ |
| Turn-off delay time | $t_{d(off)}$ | | - | 164 | - | ns |
| Fall time | t_f | | - | 19 | - | |
| Input capacitance | C_{iss} | $V_{GS} = 0\text{ V}$, $V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$ | - | 7500 | - | pF |
| Output capacitance | C_{oss} | | - | 378 | - | |
| Reverse transfer capacitance | C_{rss} | | - | 5 | - | |
| Reverse bias safe operating area | RBSOA | $T_J = 150\text{ }^\circ\text{C}$, $I_D = 150\text{ A}$, $V_{DD} = 400\text{ V}$, $V_P = 600\text{ V}$, $R_g = 10\text{ }\Omega$, $V_{GS} = +10\text{ V} / 0\text{ V}$ | | | | |
| QB1 - QB2 - QB3 MOSFET BODY DIODE | | | | | | |
| Diode reverse recovery time | t_{rr} | $V_R = 200\text{ V}$, $T_J = 25\text{ }^\circ\text{C}$, $I_S = 40\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$ | - | 211 | - | ns |
| Diode reverse recovery current | I_{rr} | | - | 17 | - | A |
| Diode reverse recovery charge | Q_{rr} | | - | 1775 | - | nC |
| D3 SILICON CARBIDE CLAMP DIODE | | | | | | |
| Total capacitive charge | Q_C | $V_R = 600\text{ V}$, $I_F = 30\text{ A}$, $di/dt = 500\text{ A}/\mu\text{s}$ | - | 75 | - | nC |



| INTERNAL NTC - THERMISTOR SPECIFICATIONS | | | | |
|--|--------------------|---|------------|-------|
| PARAMETER | SYMBOL | TEST CONDITIONS | VALUE | UNITS |
| Resistance | R25 | T _C = 25 °C | 5000 | Ω |
| | R100 | T _C = 100 °C | 493 ± 5 % | |
| B-value | B _{25/50} | R ₂ = R ₂₅ exp. [B _{25/50} (1/T ₂ - 1/(298.15K))] | 3375 ± 5 % | K |
| Maximum operating temperature | | | 220 | °C |
| Dissipation constant | | | 2 | mW/°C |
| Thermal time constant | | | 8 | s |

| THERMAL AND MECHANICAL SPECIFICATIONS | | | | | |
|---|-------------------|------|------|------|-------|
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNITS |
| INPUT SINGLE PHASE BRIDGE - Junction to sink thermal resistance (per diode) ⁽¹⁾ | R _{thJS} | - | 1.28 | - | °C/W |
| INPUT SINGLE PHASE BRIDGE - Junction to sink thermal resistance (per thyristor) ⁽¹⁾ | | - | 1.11 | - | |
| QB1 - QB2 - QB3 MOSFET - Junction to sink thermal resistance (per switch) ⁽¹⁾ | | - | 0.64 | - | |
| D3 SILICON CARBIDE CLAMP DIODE - Junction to sink thermal resistance (per diode) ⁽¹⁾ | | - | 1.07 | - | |
| Case to sink thermal resistance (per module) ⁽¹⁾ | | - | 0.1 | - | |
| Mounting torque (M4) | | 2 | - | 3 | Nm |
| Weight | | - | 28 | - | g |

Note

⁽¹⁾ Mounting surface flat, smooth, and greased, λ_{grease} = 0.67 W/mK

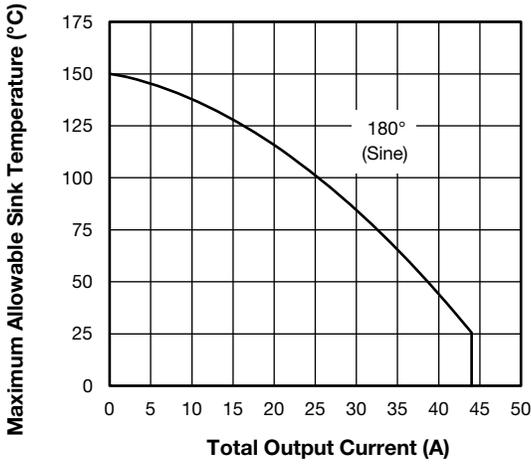


Fig. 1 - Current Rating Characteristics

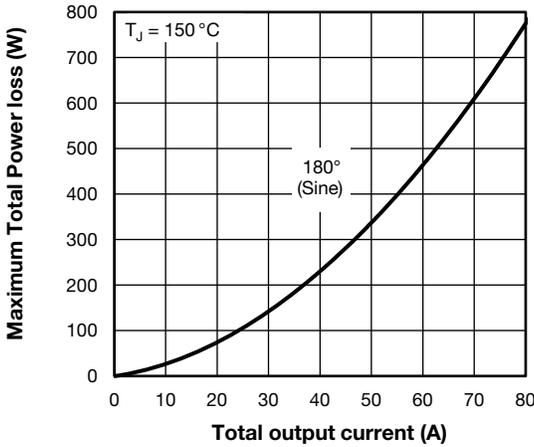


Fig. 2 - Total Power Loss Characteristics

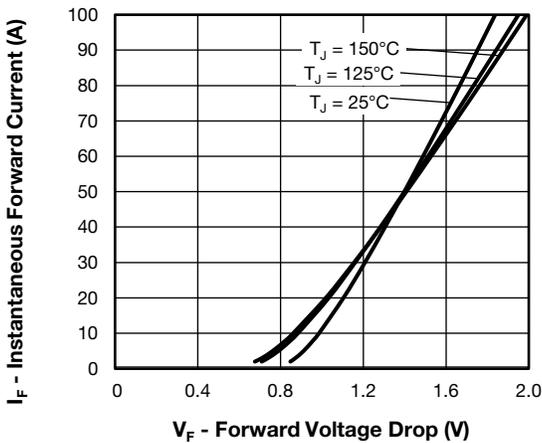


Fig. 3 - Typical D1 - D2 Forward Voltage Drop vs. Instantaneous Forward Current

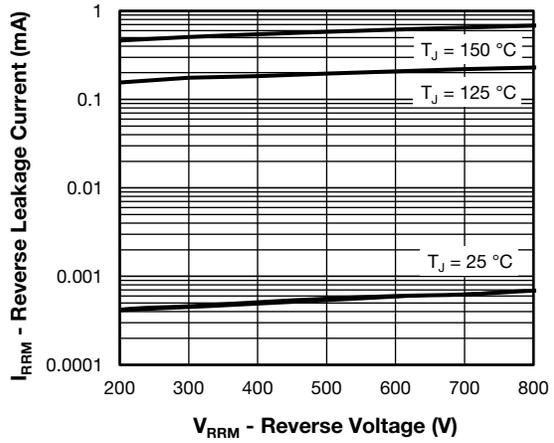


Fig. 4 - Typical D1 - D2 Reverse Current vs. Reverse Voltage

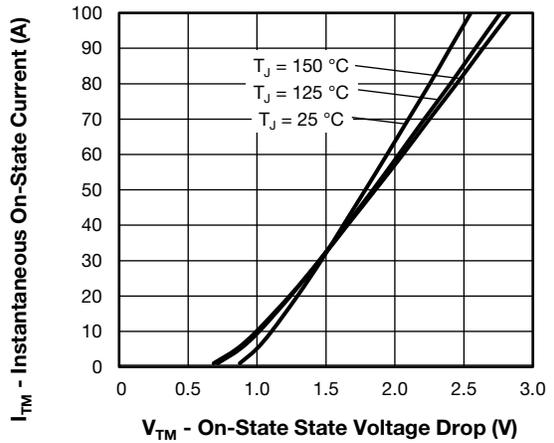


Fig. 5 - Typical Scr1 - Scr2 On-State Voltage Drop vs. Instantaneous On-State Current

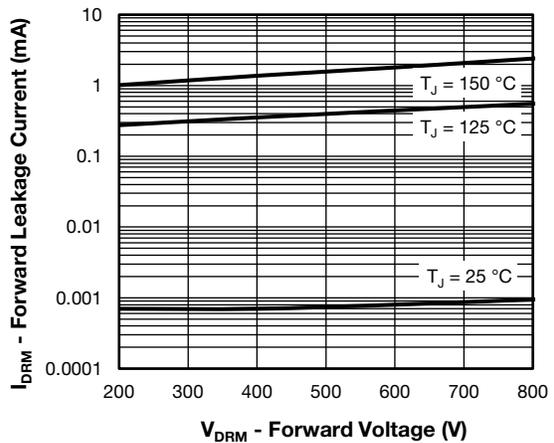


Fig. 6 - Typical Scr1 - Scr2 Forward Leakage Current vs. Direct Blocking Voltage

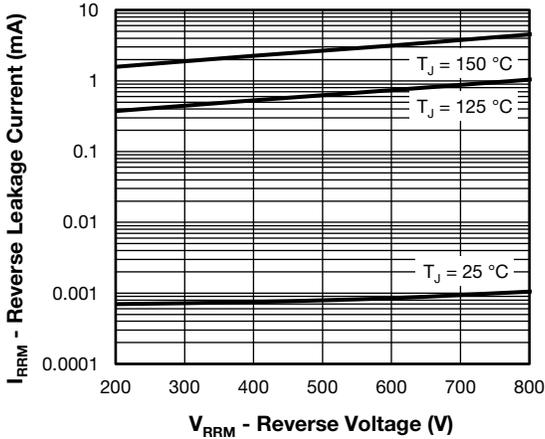


Fig. 7 - Typical Scr1 - Scr2 Reverse Leakage Current vs. Reverse Blocking Voltage

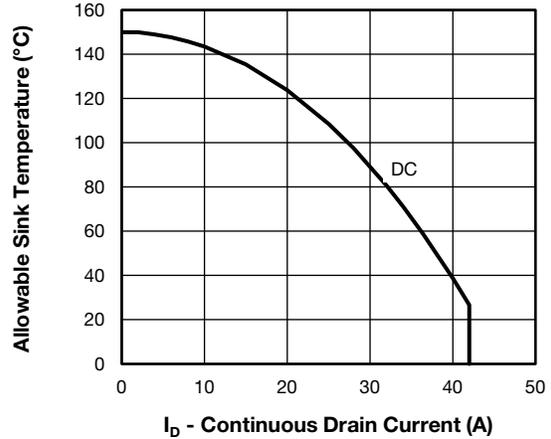


Fig. 10 - Maximum QB1 - QB3 Continuous Drain Current vs. Sink Temperature

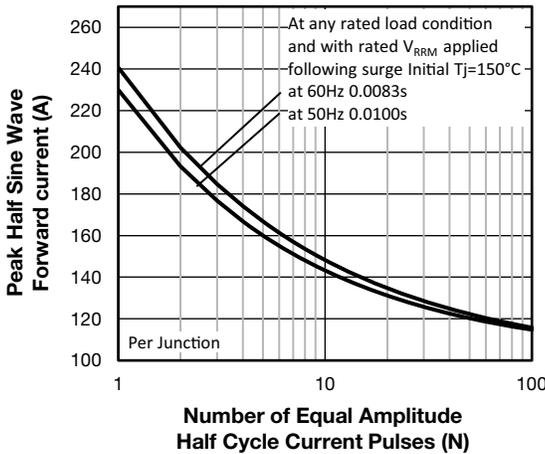


Fig. 8 - Maximum Non-Repetitive Surge Current vs. Number of Current Pulses

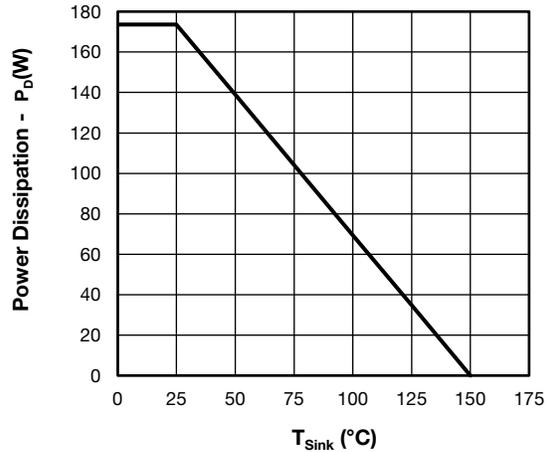


Fig. 11 - QB1 - QB3 Power Dissipation Curve

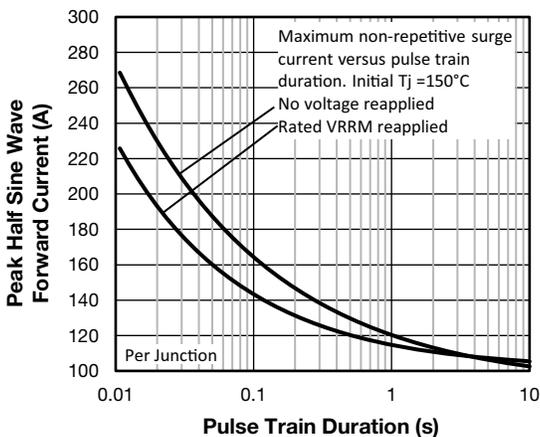


Fig. 9 - Maximum Non-Repetitive Surge Current vs. Pulse Train Duration

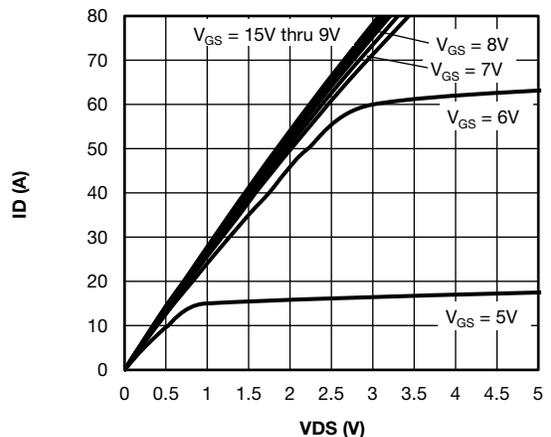


Fig. 12 - Typical QB1 - QB3 Drain to Source Current Output Characteristics at $T_J = 25\text{ °C}$

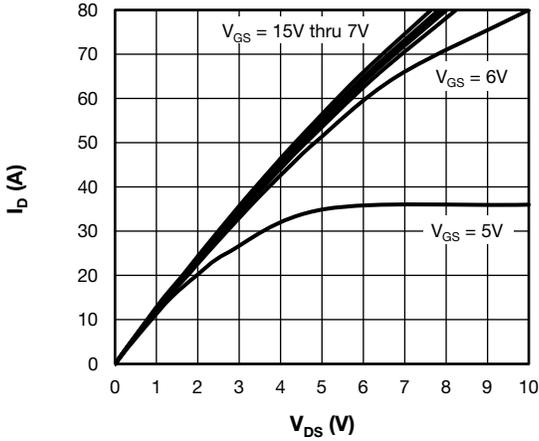


Fig. 13 - Typical QB1 - QB3
Drain to Source Current Output Characteristics at $T_J = 150\text{ }^\circ\text{C}$

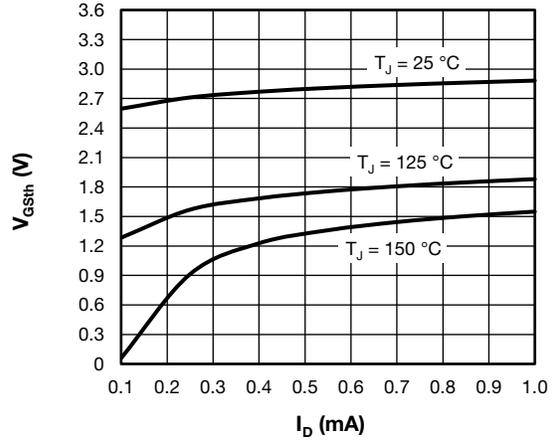


Fig. 16 - Typical QB1-QB3
Gate Threshold Voltage Characteristics

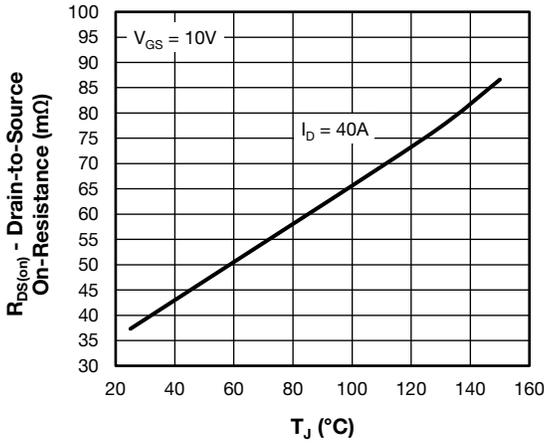


Fig. 14 - Typical QB1 - QB3
Drain-to-Source On-Resistance vs. Temperature

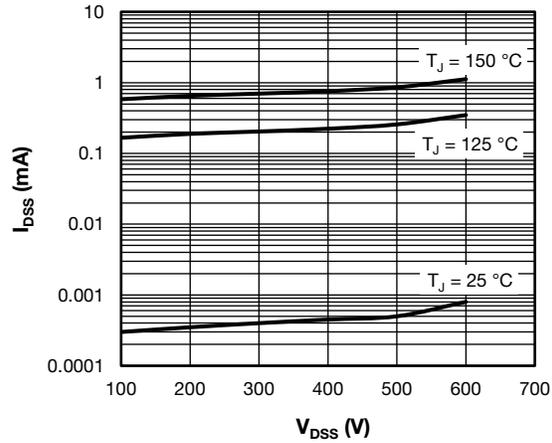


Fig. 17 - Typical QB1 - QB3
Zero Gate Voltage Drain Current

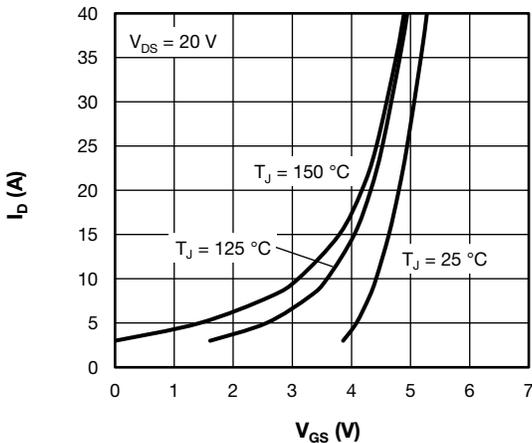


Fig. 15 - Typical QB1 - QB3
Transfer Characteristics

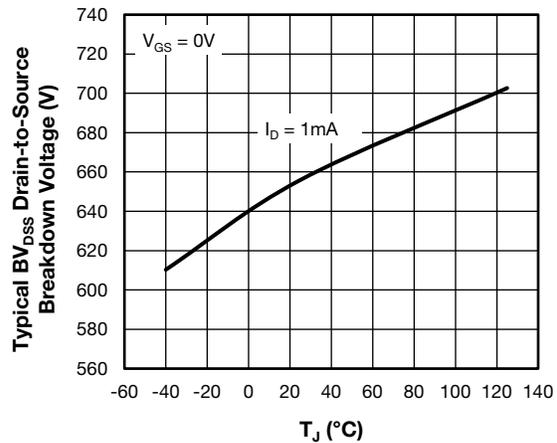


Fig. 18 - Typical QB1 - QB3
Drain to Source Breakdown Voltage vs. Temperature

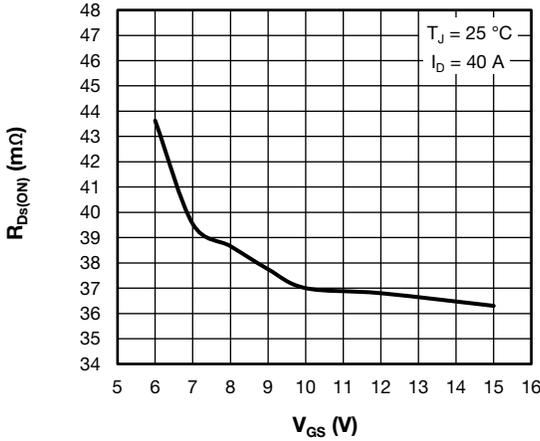


Fig. 19 - Typical QB1 - QB3
Drain - State Resistance vs. Gate-to-Source Voltage

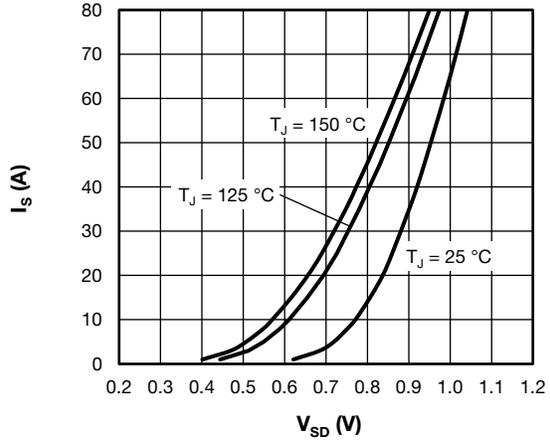


Fig. 22 - Typical QB1 - QB3
Body Diode Source-to-Drain Current Characteristics

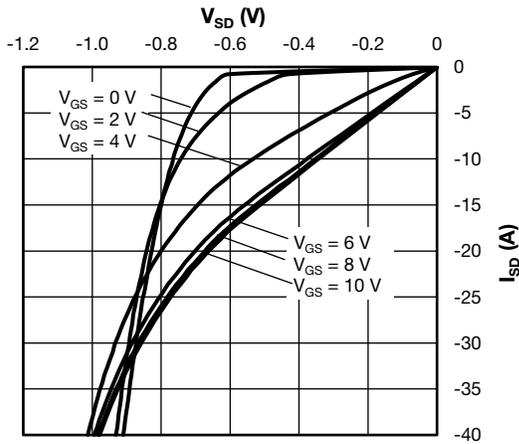


Fig. 20 - Typical QB1 - QB3
Source-to-Drain Current Characteristics at $T_J = 125\text{ °C}$

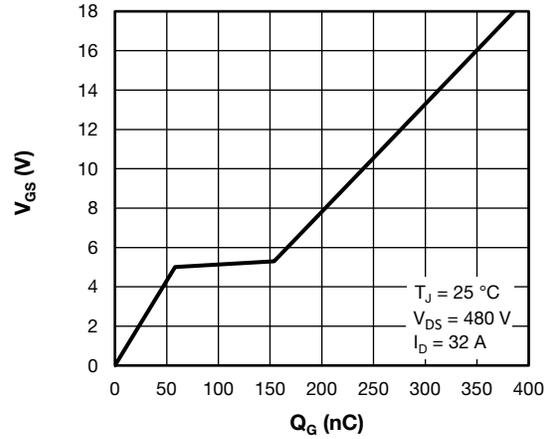


Fig. 23 - Typical QB1 - QB3
Gate charge vs. Gate-to-Source Voltage

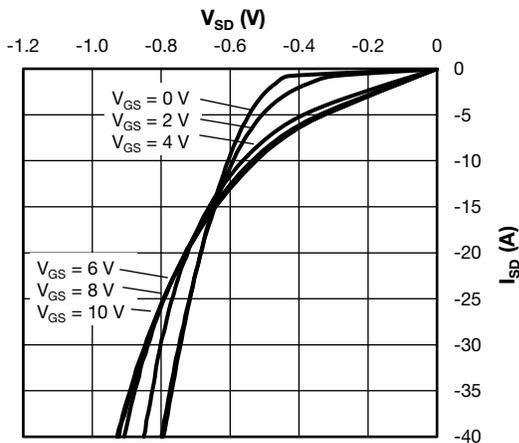


Fig. 21 - Typical QB1 - QB3
Source-to-Drain Current Characteristics at $T_J = 125\text{ °C}$

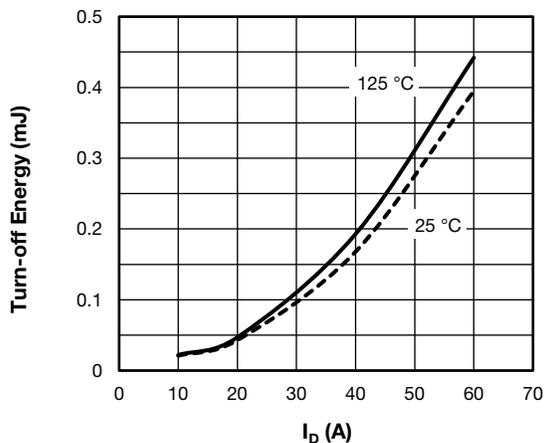


Fig. 24 - Typical QB2 - QB3 Turn-off Energy Loss vs. I_D
 $V_{DD} = 450\text{ V}$, $R_g = 10\text{ }\Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\text{ }\mu\text{H}$

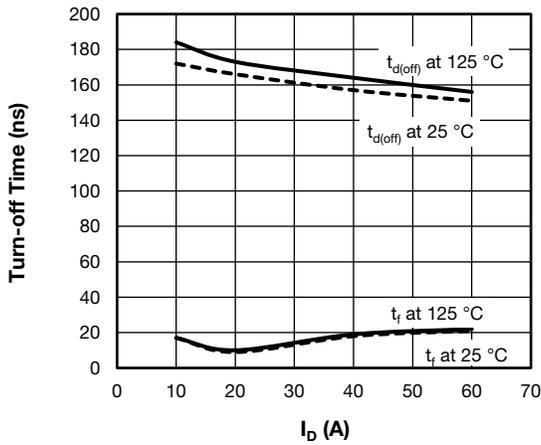


Fig. 25 - Typical QB2-QB3 Turn-off Switching Time vs I_D
 $V_{DD} = 450\text{ V}$, $R_g = 10\ \Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

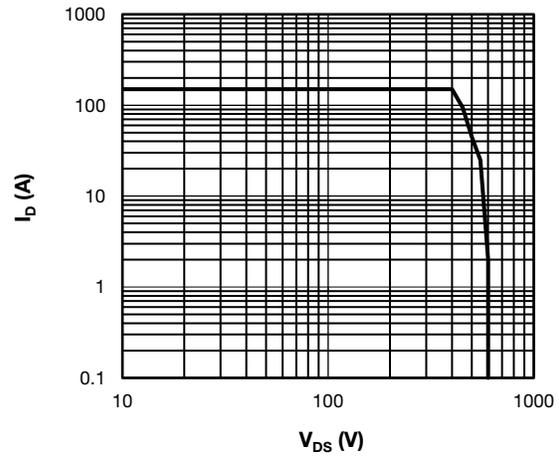


Fig. 28 - QB2 - QB3 MOSFET Reverse BIAS SOA
 $T_J = 150\ ^\circ\text{C}$, $V_{GS} = 10\text{ V}$

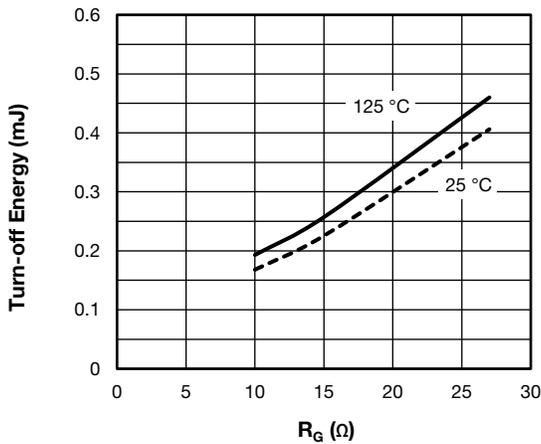


Fig. 26 - Typical QB2-QB3 Turn-off Energy Loss vs R_g
 $V_{DD} = 450\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

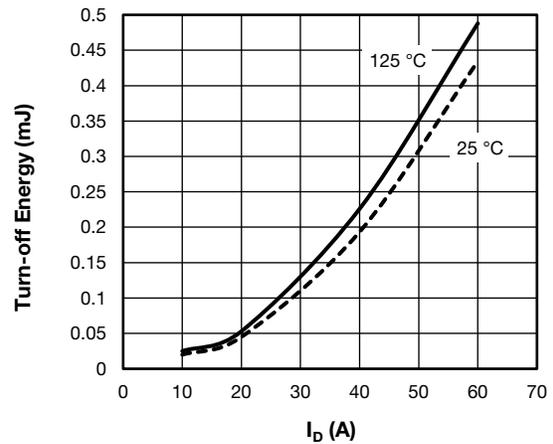


Fig. 29 - Typical QB1 Turn-off Energy Loss vs. I_D
 $V_{DD} = 450\text{ V}$, $R_g = 10\ \Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

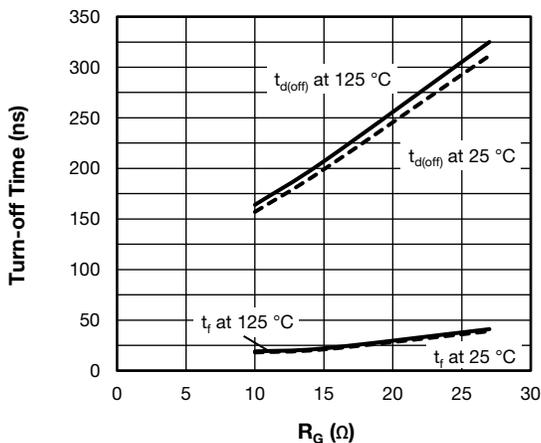


Fig. 27 - Typical QB2-QB3 Turn-off Switching Time vs R_g
 $V_{DD} = 450\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

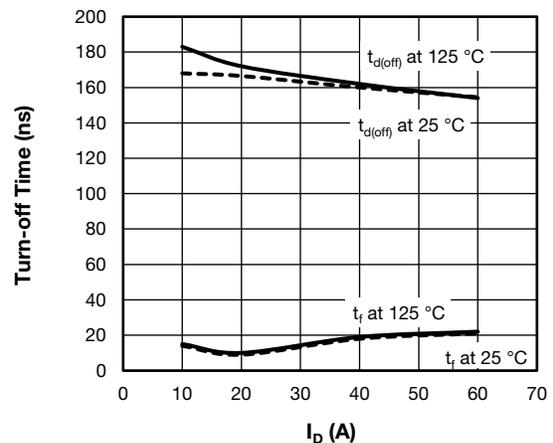


Fig. 30 - Typical QB1 Turn-off Switching Time vs. I_D
 $V_{DD} = 450\text{ V}$, $R_g = 10\ \Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

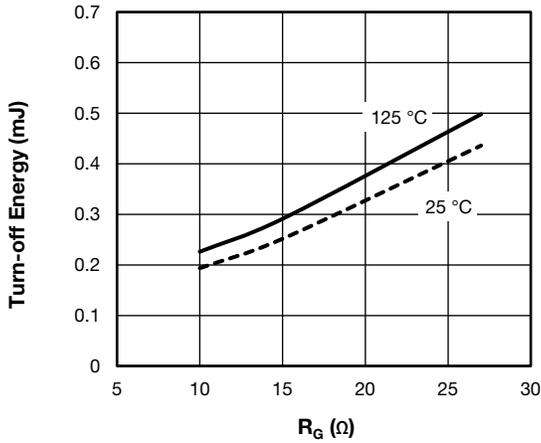


Fig. 31 - Typical QB1 Turn-off Energy Loss vs. R_g
 $V_{DD} = 450\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

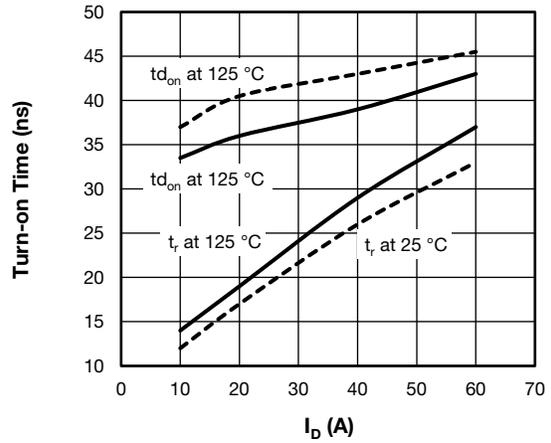


Fig. 34 - Typical QB1 Turn-on Switching Time vs. I_D
 $V_{DD} = 450\text{ V}$, $R_g = 10\ \Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

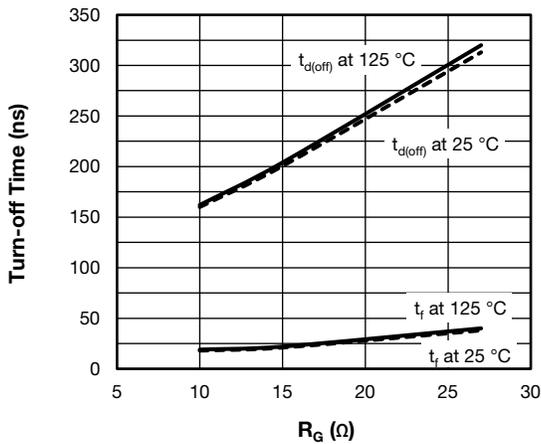


Fig. 32 - Typical QB1 Turn-off Switching Time vs. R_g
 $V_{DD} = 450\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

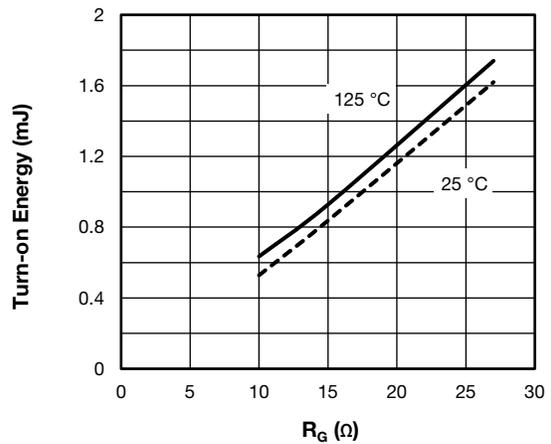


Fig. 35 - Typical QB1 Turn-on Energy Loss vs. R_g
 $V_{DD} = 450\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

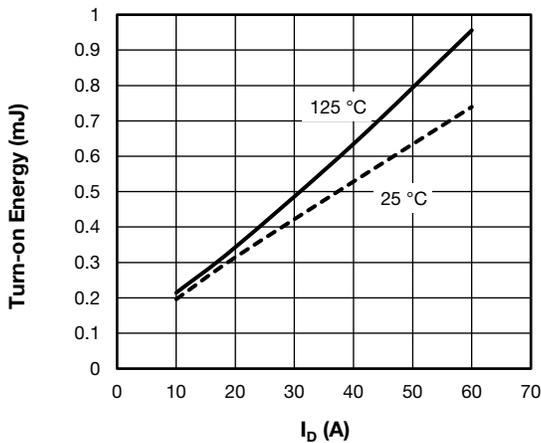


Fig. 33 - Typical QB1 Turn-on Energy Loss vs. I_D
 $V_{DD} = 450\text{ V}$, $R_g = 10\ \Omega$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

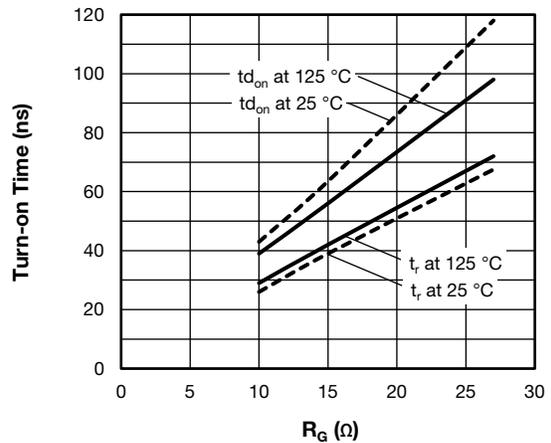


Fig. 36 - Typical QB1 Turn-on Switching Time vs. R_g
 $V_{DD} = 450\text{ V}$, $I_D = 40\text{ A}$, $V_{GS} = \pm 10\text{ V}$, $L = 500\ \mu\text{H}$

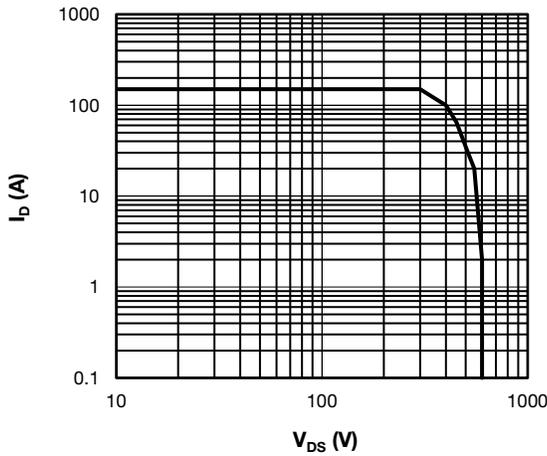


Fig. 37 - QB1 MOSFET Reverse BIAS SOA
 $T_J = 150\text{ }^\circ\text{C}$, $V_{GS} = 10\text{ V}$

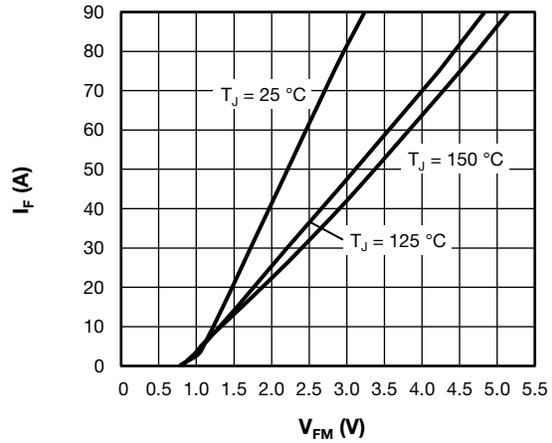


Fig. 39 - Typical D3 Diode Forward Characteristics

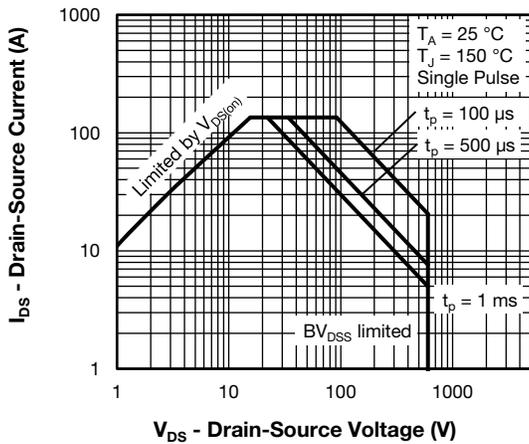


Fig. 38 - QB1 - QB3 Safe Operating Area

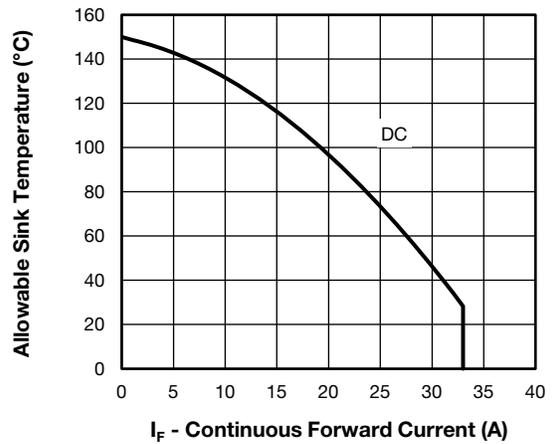


Fig. 40 - Maximum D3 Diode Continuous Forward Current vs. Sink Temperature

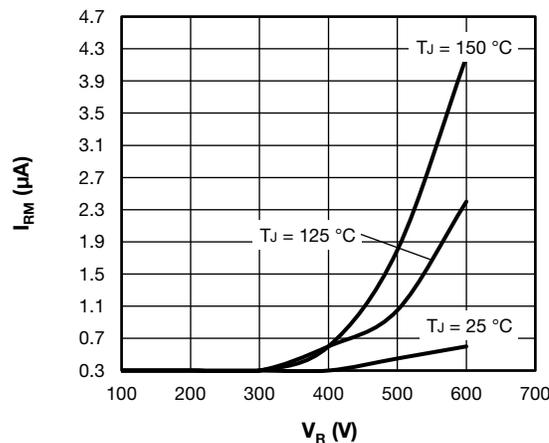


Fig. 41 - Typical D3 Diode Reverse Leakage Current

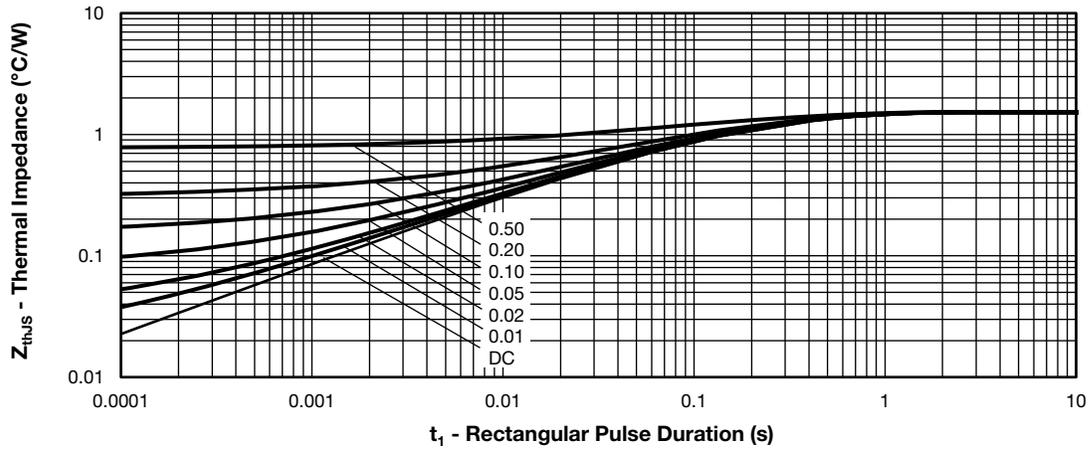


Fig. 42 - Maximum D1 - D2 Z_{thJS} Thermal Impedance Characteristic

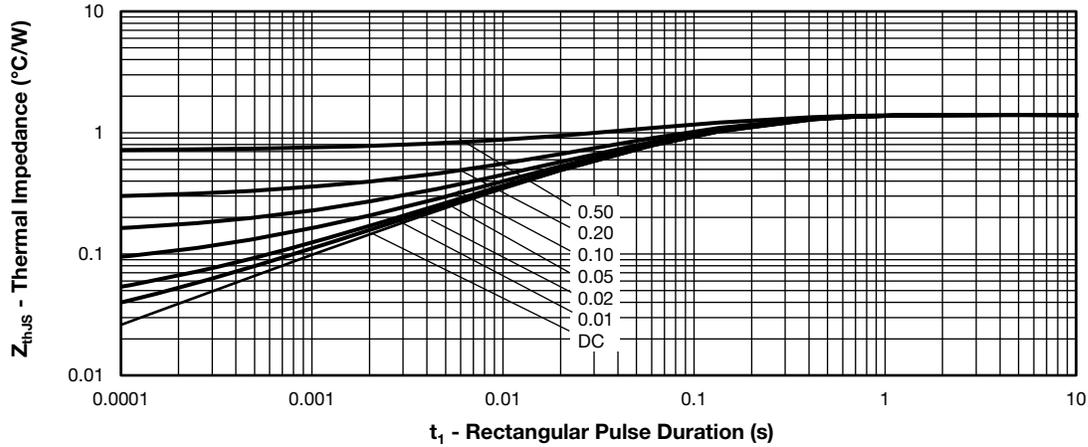


Fig. 43 - Maximum Scr1 - Scr2 Z_{thJS} Thermal Impedance Characteristic

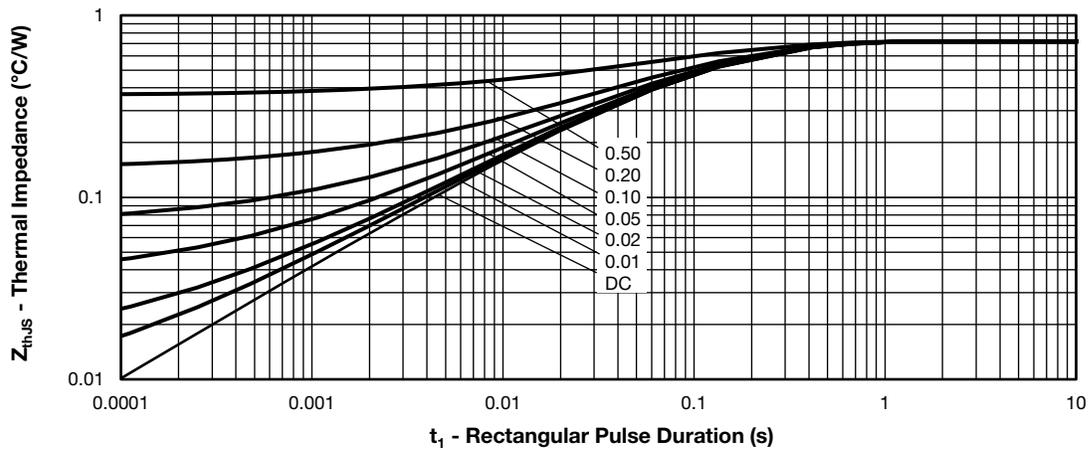


Fig. 44 - Maximum QB1 - QB3 Z_{thJS} Thermal Impedance Characteristic

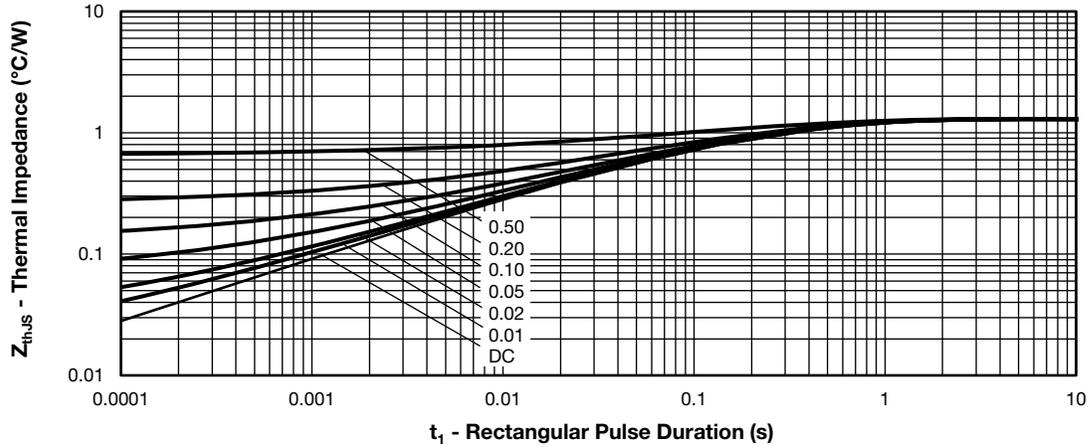


Fig. 45 - Maximum D3 Z_{thJS} Thermal Impedance Characteristics

ORDERING INFORMATION TABLE

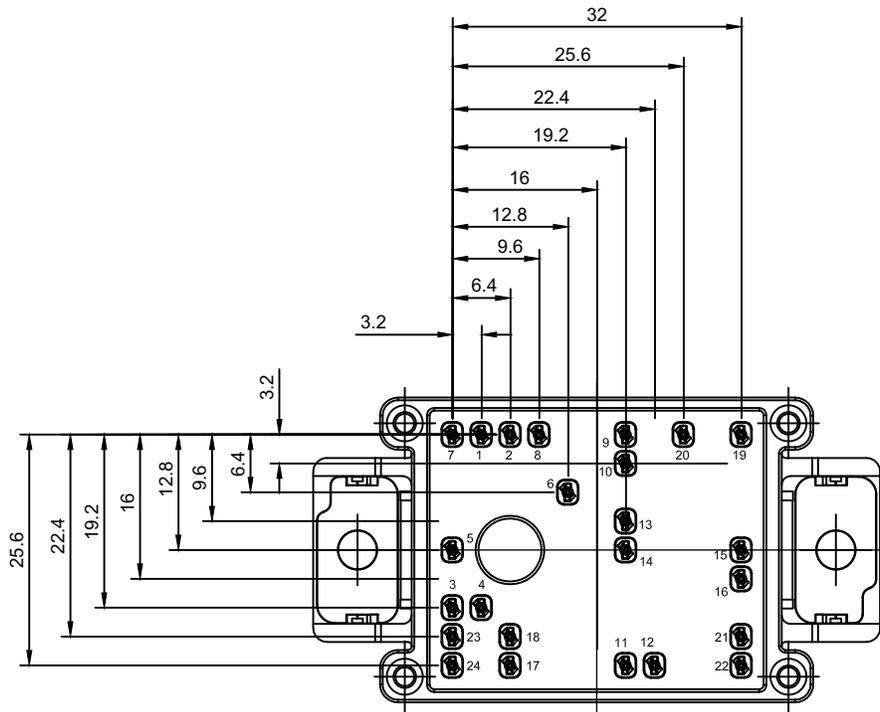
| | | | | | | | |
|-------------|------------|-----------|----------|------------|----------|-----------|----------|
| Device code | VS- | EN | M | 040 | M | 60 | P |
| | ① | ② | ③ | ④ | ⑤ | ⑥ | ⑦ |

- 1** - Vishay Semiconductors product
- 2** - Package indicator (EN = EMIPAK 1B)
- 3** - Circuit configuration (M = Half controlled input bridge plus MOSFET boost PFC leg and MOSFET half bridge inverter)
- 4** - Current rating (040 = 40 A)
- 5** - Switch die technology (M = SiC diodes + Power MOSFET + MOAT)
- 6** - Voltage rating (60 = 600 V)
- 7** - Diode technology (P = SiC diodes + MOAT + SCR)

| CIRCUIT CONFIGURATION | | |
|--|----------------------------|-----------------|
| CIRCUIT | CIRCUIT CONFIGURATION CODE | CIRCUIT DRAWING |
| Half controlled input bridge plus MOSFET boost PFC leg and MOSFET half bridge inverter | M | |



PACKAGE



LINKS TO RELATED DOCUMENTS

| | |
|------------------|--|
| Dimensions | www.vishay.com/doc?95558 |
| Application Note | www.vishay.com/doc?95580 |



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