

# EPC2107 – Enhancement-Mode GaN Power Transistor Half-Bridge with Integrated Synchronous Bootstrap

$V_{DS}$ , 100 V

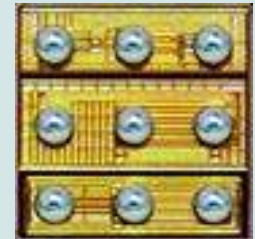
$R_{DS(on)}$ , 390 mΩ

$I_D$ , 1.7 A



Gallium Nitride’s exceptionally high electron mobility and low temperature coefficient allows very low  $R_{DS(on)}$ , while its lateral device structure and majority carrier diode provide exceptionally low  $Q_G$  and zero  $Q_{RR}$ . The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings					
DEVICE	PARAMETER		VALUE	UNIT	
Q1 & Q2	$V_{DS}$	Drain-to-Source Voltage (Continuous)	100	V	
		Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120		
	$I_D$	Continuous ( $T_A = 25^\circ\text{C}$ , $R_{\theta JA} = 60^\circ\text{C/W}$ )	1.7	A	
		Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300 \mu\text{s}$ )	3.8		
	$V_{GS}$	Gate-to-Source Voltage	6	V	
		Gate-to-Source Voltage	-4		
	$T_J$	Operating Temperature	-40 to 150	°C	
	$T_{STG}$	Storage Temperature	-40 to 150		
	Q3	$V_{DS}$	Drain-to-Source Voltage (Continuous)	100	V
			Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
$I_D$		Continuous ( $T_A = 25^\circ\text{C}$ , $R_{\theta JA} = 100^\circ\text{C/W}$ )	0.5	A	
		Pulsed ( $25^\circ\text{C}$ , $T_{PULSE} = 300 \mu\text{s}$ )	0.5		
$V_{GS}$		Gate-to-Source Voltage	6	V	
		Operating Temperature	-40 to 150		
$T_J$		Storage Temperature	-40 to 150	°C	
$T_{STG}$		Storage Temperature	-40 to 150		



EPC2107 eGaN® ICs are supplied only in passivated die form with solder bumps  
Die Size: 1.35 mm x 1.35 mm

### Applications

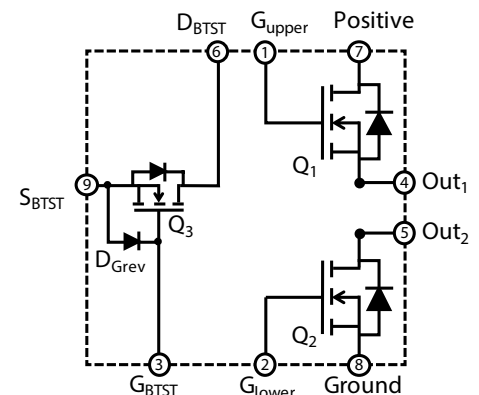
- High Frequency DC-DC Conversion
- Class-D Audio
- Wireless Power (Highly Resonant and Inductive)

### Benefits

- Ultra High Efficiency
- Ultra Low  $R_{DS(on)}$
- Ultra Low  $Q_G$
- Ultra Small Footprint

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	6	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	33	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	81	

Note 1:  $R_{\theta JA}$  is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board. See [https://epc-co.com/epc/documents/product-training/Appnote\\_Thermal\\_Performance\\_of\\_eGaN\\_FETs.pdf](https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf) for details



EPC2107 – Detailed Schematic

Static Characteristics ( $T_j = 25^\circ\text{C}$  unless otherwise stated)

DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1 & Q2	$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 0.3\text{ mA}$	100			V
	$I_{DSS}$	Drain-Source Leakage	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$		0.05	0.25	mA
	$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.1	1	mA
		Gate-to-Source Reverse Leakage	$V_{GS} = -4\text{ V}$		0.05	0.25	mA
	$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 0.1\text{ mA}$	0.8	1.6	2.5	V
	$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 2\text{ A}$		250	390	m $\Omega$
	$V_{SD}$	Source-Drain Forward Voltage	$I_S = 0.5\text{ A}, V_{GS} = 0\text{ V}$		2.5		V
Q3	$BV_{DSS}$	Drain-to-Source Voltage	$V_{GS} = 0\text{ V}, I_D = 0.125\text{ mA}$	100			V
	$I_{DSS}$	Drain-Source Leakage	$V_{DS} = 80\text{ V}, V_{GS} = 0\text{ V}$		0.02	0.1	mA
	$I_{GSS}$	Gate-to-Source Forward Leakage	$V_{GS} = 5\text{ V}$		0.1	1	mA
	$V_F$	Source-Gate Forward Voltage	$I_F = 0.2\text{ mA}, V_{DS} = 0\text{ V}$			2.7	V
	$V_{GS(TH)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 0.1\text{ mA}$	0.8	1.7	2.5	V
	$R_{DS(on)}$	Drain-Source On Resistance	$V_{GS} = 5\text{ V}, I_D = 0.05\text{ A}$		2100	3300	m $\Omega$
	$V_{SD}$	Source-Drain Forward Voltage	$I_S = 0.1\text{ A}, V_{GS} = 0\text{ V}$		2.9		V

Dynamic Characteristics ( $T_j = 25^\circ\text{C}$  unless otherwise stated)

DEVICE	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Q1	$C_{ISS}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		21	25	pF
	$C_{RSS}$	Reverse Transfer Capacitance			0.2		
	$C_{OSS}$	Output Capacitance			9.2	14	
	$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		13		
	$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			18		
	$R_G$	Gate Resistance			0.7		$\Omega$
	$Q_G$	Total Gate Charge	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 2\text{ A}$		190	230	pC
	$Q_{GS}$	Gate to Source Charge	$V_{DS} = 50\text{ V}, I_D = 2\text{ A}$		77		
	$Q_{GD}$	Gate to Drain Charge			41		
	$Q_{G(TH)}$	Gate Charge at Threshold			49		
	$Q_{OSS}$	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		900	1350	
$Q_{RR}$	Source-Drain Recovery Charge			0			
Q2	$C_{ISS}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		21	25	pF
	$C_{RSS}$	Reverse Transfer Capacitance			0.2		
	$C_{OSS}$	Output Capacitance			14	21	
	$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		19		
	$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			25		
	$R_G$	Gate Resistance			0.7		$\Omega$
	$Q_G$	Total Gate Charge	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 2\text{ A}$		190	230	pC
	$Q_{GS}$	Gate to Source Charge	$V_{DS} = 50\text{ V}, I_D = 2\text{ A}$		77		
	$Q_{GD}$	Gate to Drain Charge			41		
	$Q_{G(TH)}$	Gate Charge at Threshold			49		
	$Q_{OSS}$	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		1250	1875	
$Q_{RR}$	Source-Drain Recovery Charge			0			
Q3	$C_{ISS}$	Input Capacitance	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		7	8.4	pF
	$C_{RSS}$	Reverse Transfer Capacitance			0.02		
	$C_{OSS}$	Output Capacitance			1.6	2.4	
	$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0\text{ V}$		2.2		
	$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			2.7		
	$R_G$	Gate Resistance			4.8		$\Omega$
	$Q_G$	Total Gate Charge	$V_{DS} = 50\text{ V}, V_{GS} = 5\text{ V}, I_D = 0.05\text{ A}$		44	55	pC
	$Q_{GS}$	Gate to Source Charge	$V_{DS} = 50\text{ V}, I_D = 0.05\text{ A}$		20		
	$Q_{GD}$	Gate to Drain Charge			4		
	$Q_{G(TH)}$	Gate Charge at Threshold			18		
	$Q_{OSS}$	Output Charge	$V_{DS} = 50\text{ V}, V_{GS} = 0\text{ V}$		134	200	
$Q_{RR}$	Source-Drain Recovery Charge			0			

Note 2:  $C_{OSS(ER)}$  is a fixed capacitance that gives the same stored energy as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Note 3:  $C_{OSS(TR)}$  is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 50%  $BV_{DSS}$ .

Figure 1a (Q1 & Q2): Typical Output Characteristics at 25°C

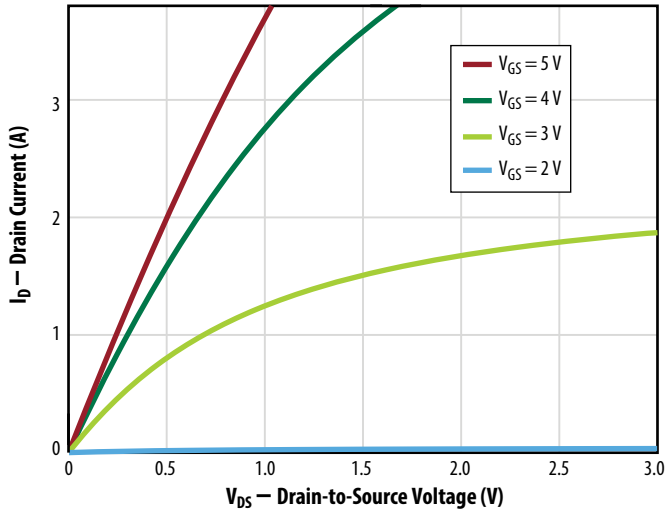


Figure 1b (Q3): Typical Output Characteristics at 25°C

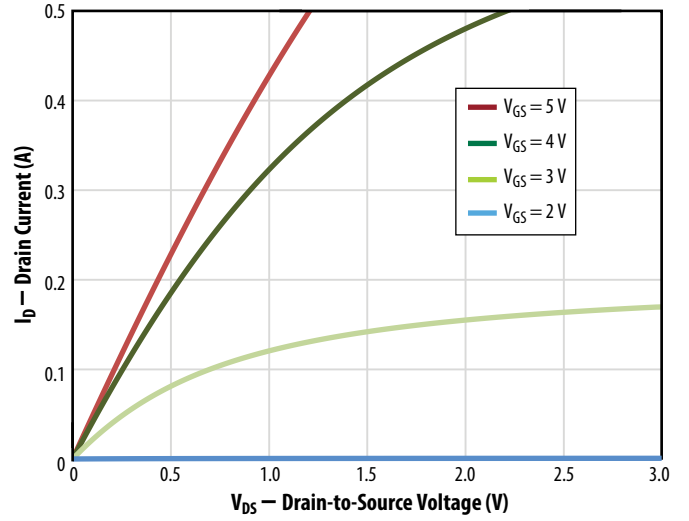


Figure 2a (Q1 & Q2): Transfer Characteristics

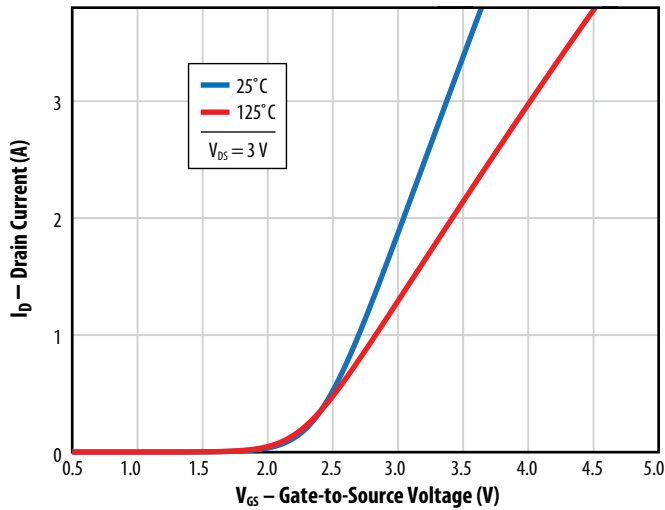


Figure 2b (Q3): Transfer Characteristics

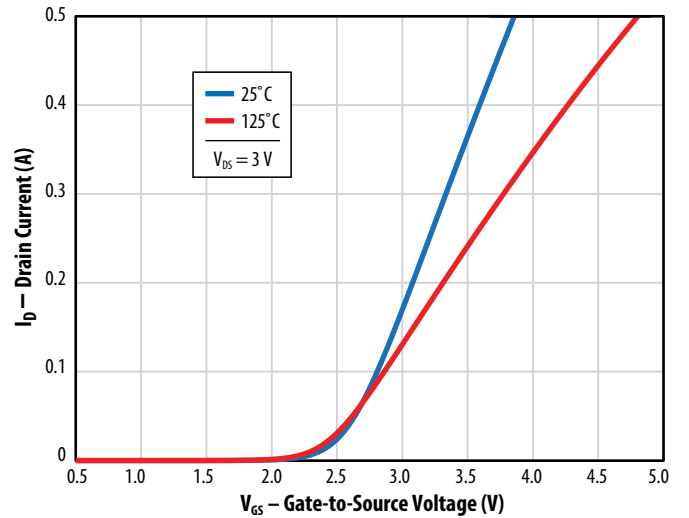


Figure 3a (Q1 & Q2):  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

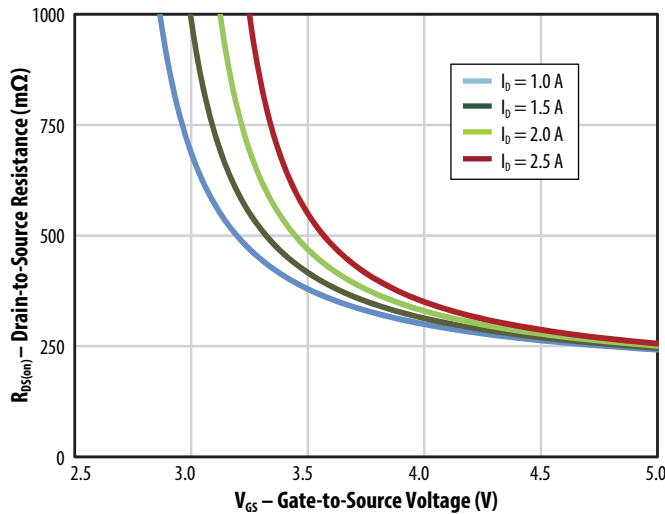


Figure 3b (Q3):  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Drain Currents

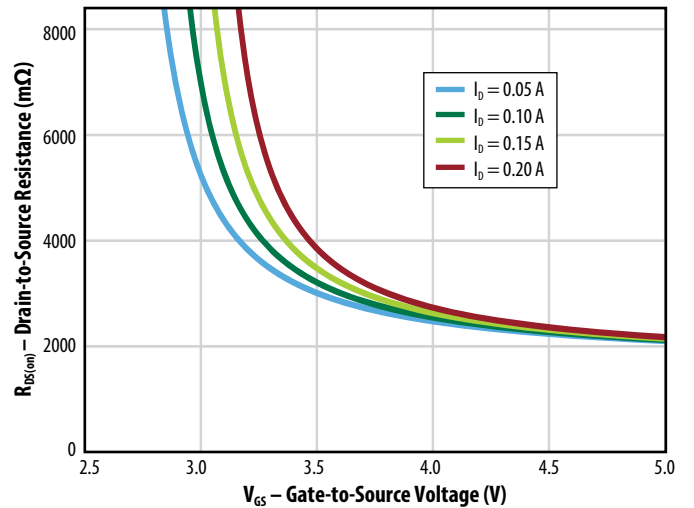


Figure 4a (Q1 & Q2):  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

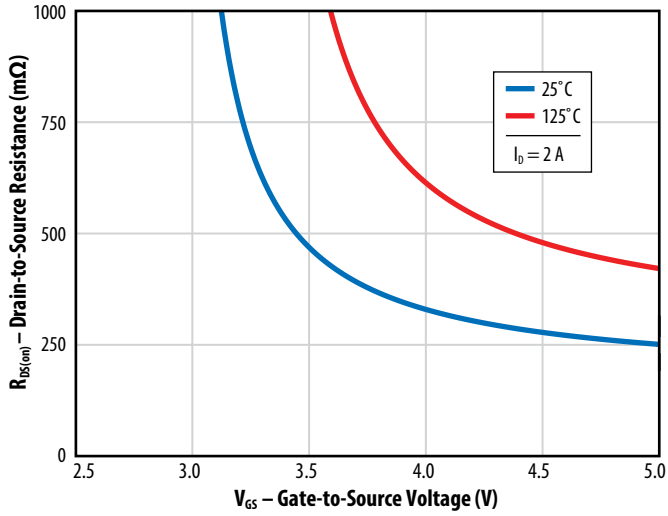


Figure 4b (Q3):  $R_{DS(on)}$  vs.  $V_{GS}$  for Various Temperatures

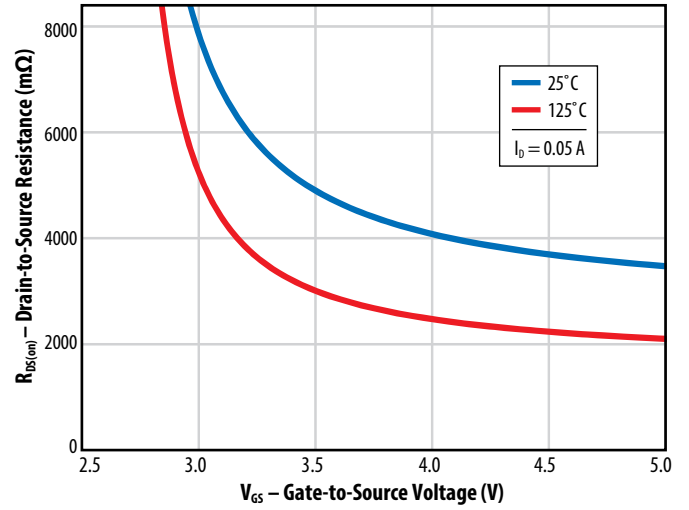


Figure 5a (Q1): Capacitance (Linear Scale)

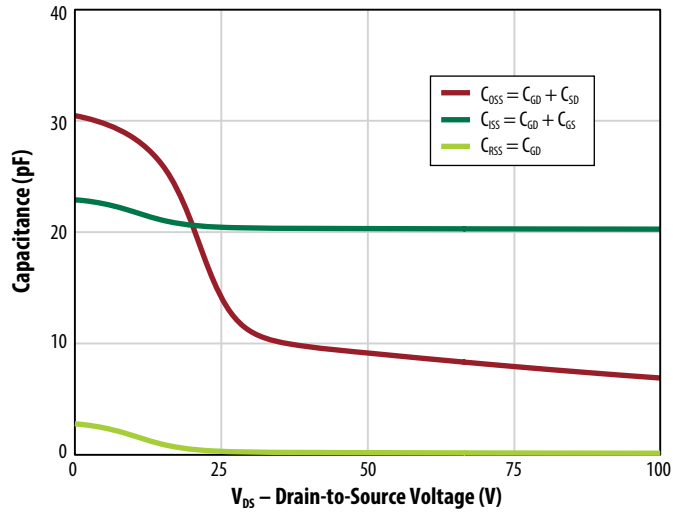


Figure 5b (Q1): Capacitance (Log Scale)

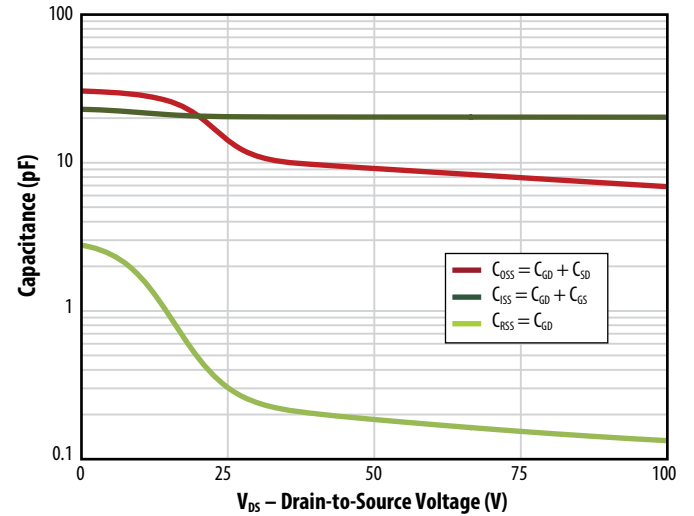


Figure 5c (Q2): Capacitance (Linear Scale)

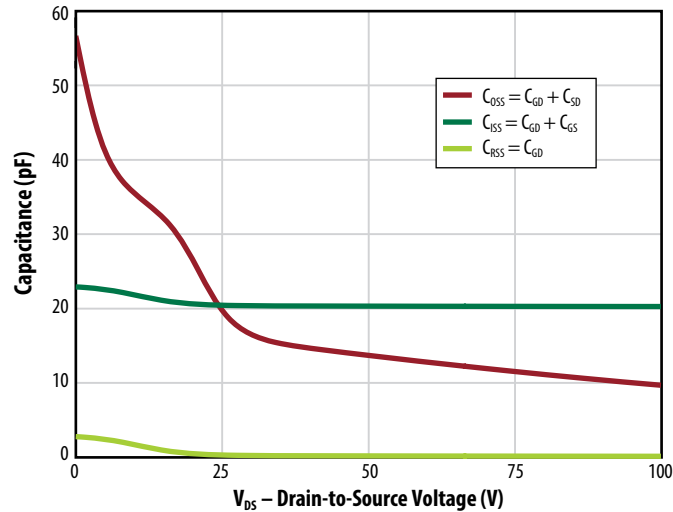


Figure 5d (Q2): Capacitance (Log Scale)

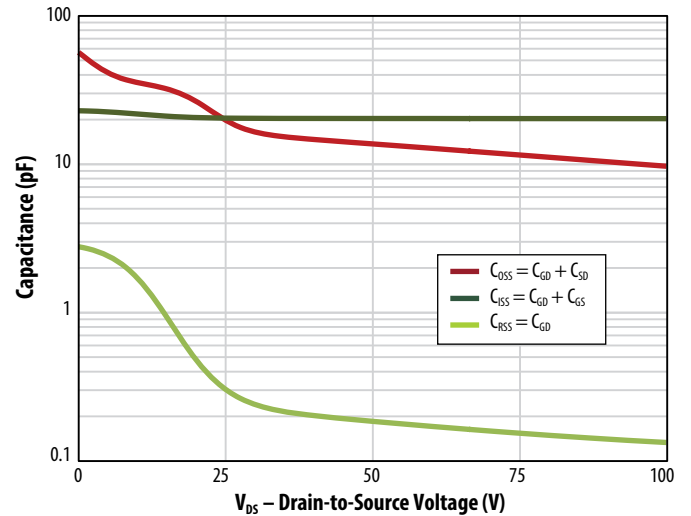


Figure 5e (Q3): Capacitance (Linear Scale)

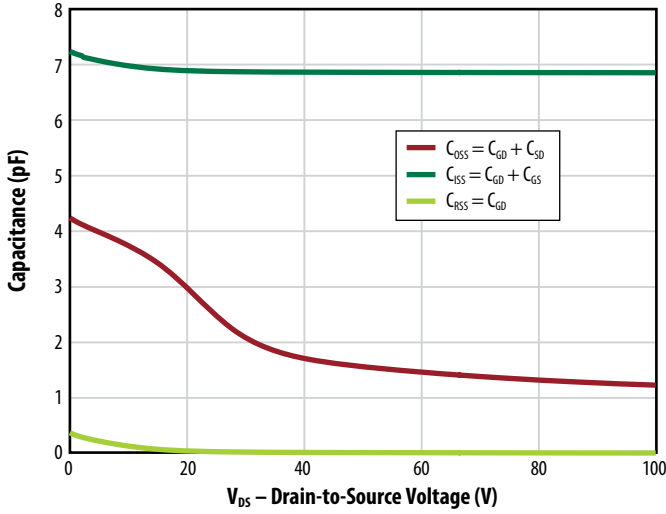


Figure 5f (Q3): Capacitance (Log Scale)

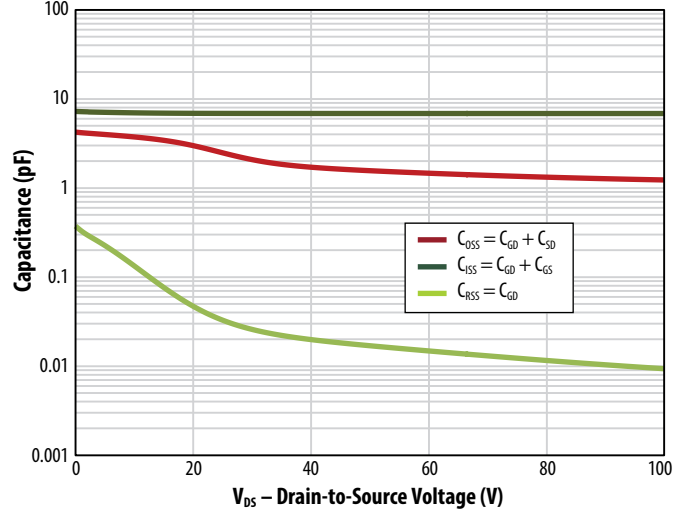


Figure 6a (Q1): Output Charge and  $C_{oss}$  Stored Energy

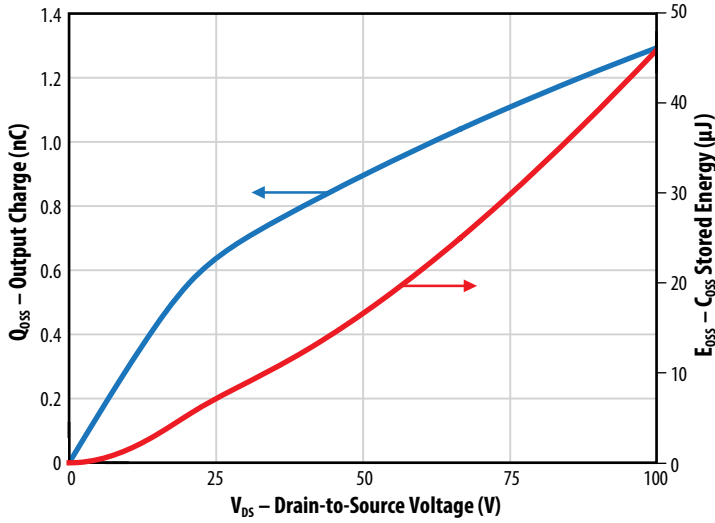


Figure 6b (Q2): Output Charge and  $C_{oss}$  Stored Energy

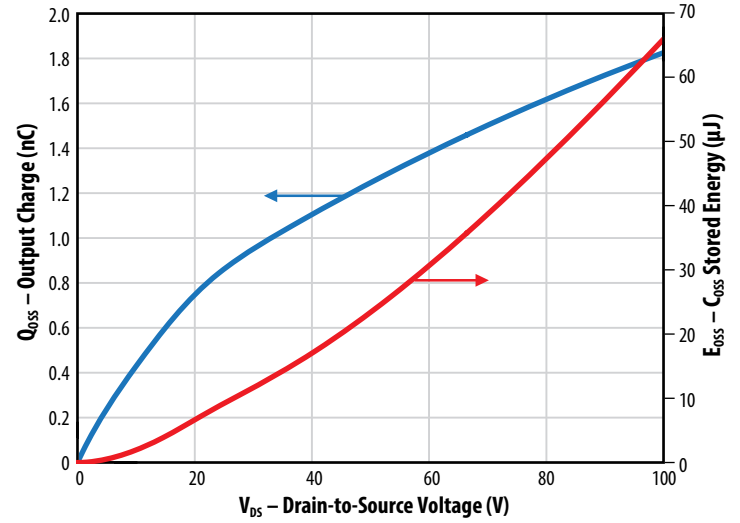


Figure 6c (Q3): Output Charge and  $C_{oss}$  Stored Energy

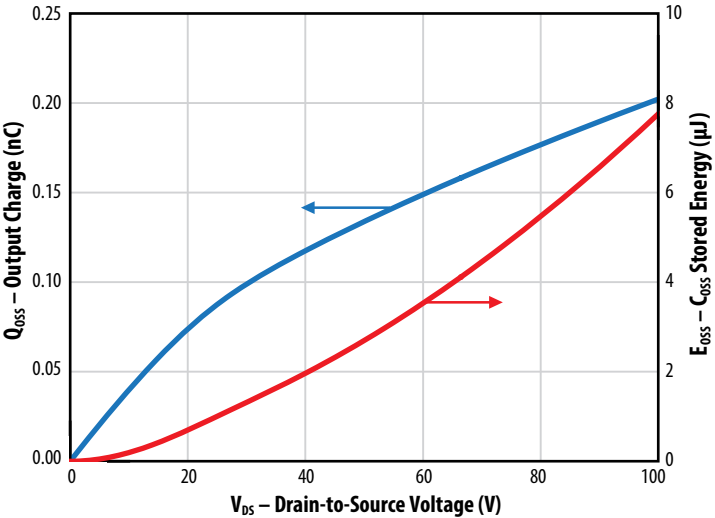


Figure 7a (Q1 & Q2): Gate Charge

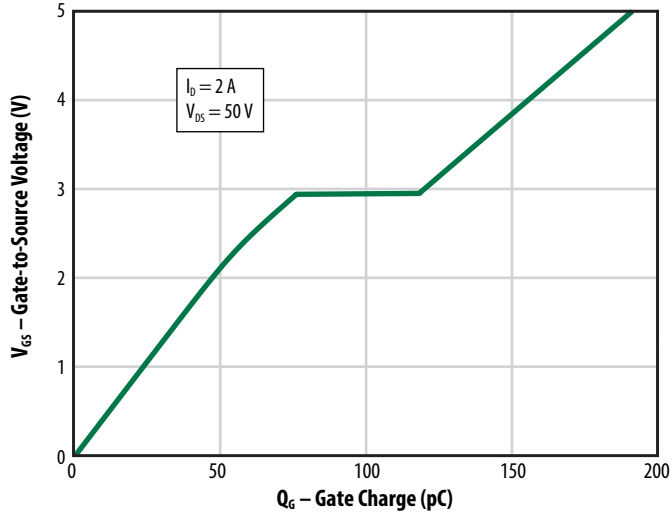


Figure 7b (Q3): Gate Charge

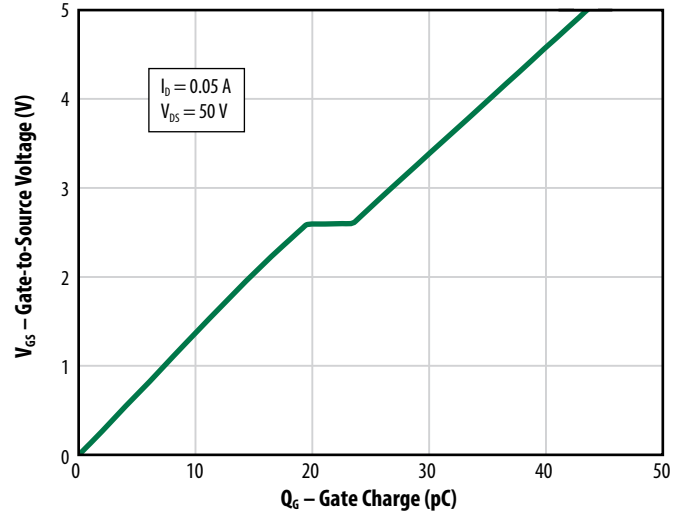


Figure 8a (Q1 & Q2): Reverse Drain-Source Characteristics

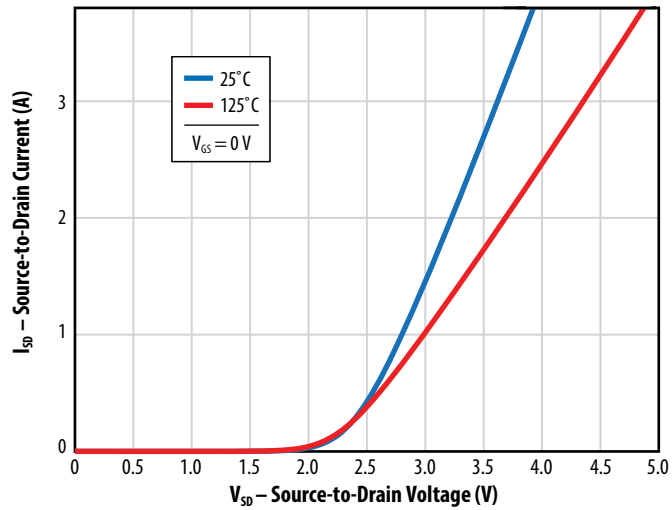


Figure 8b (Q3): Reverse Drain-Source Characteristics

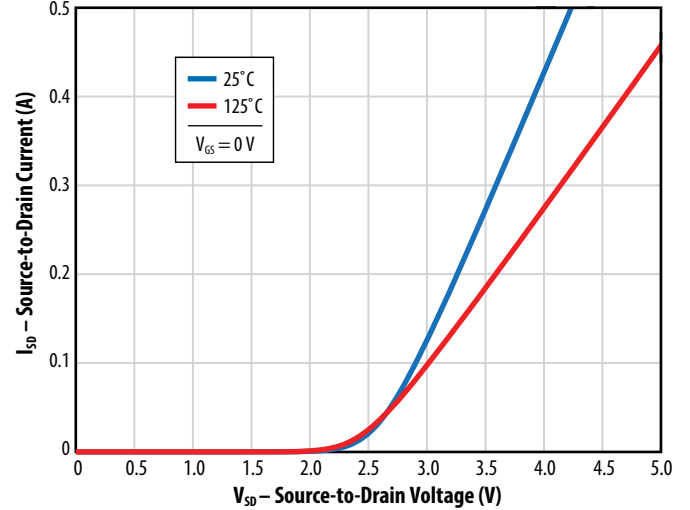


Figure 9a (Q1 & Q2): Normalized On-State Resistance vs. Temperature

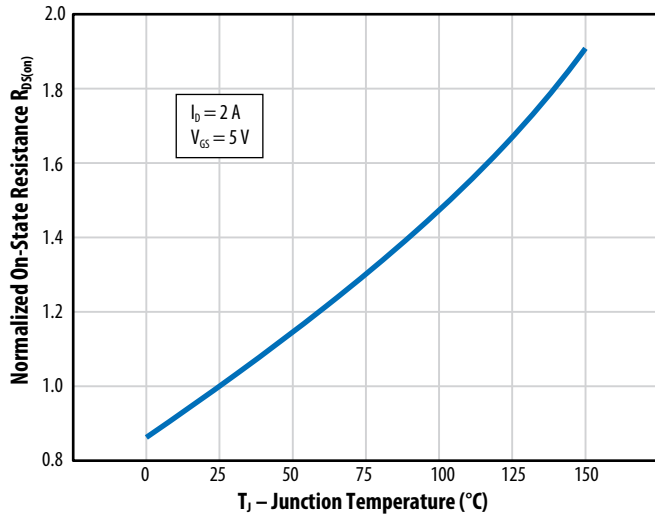
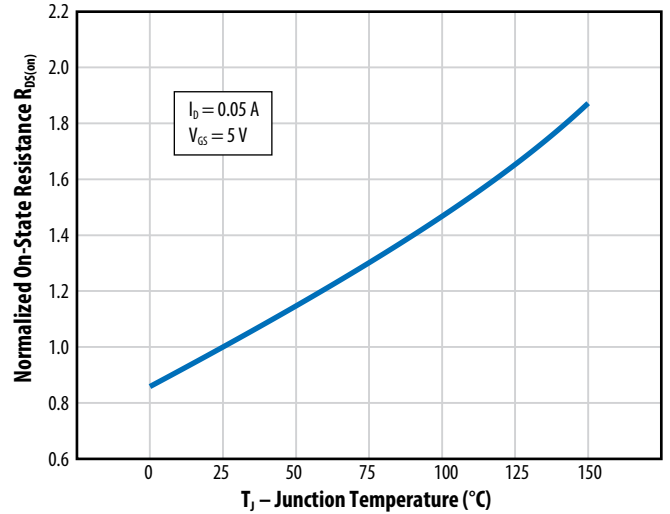
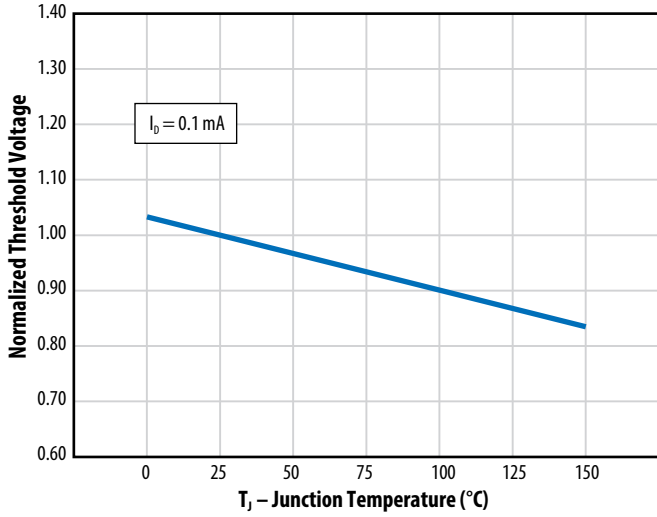


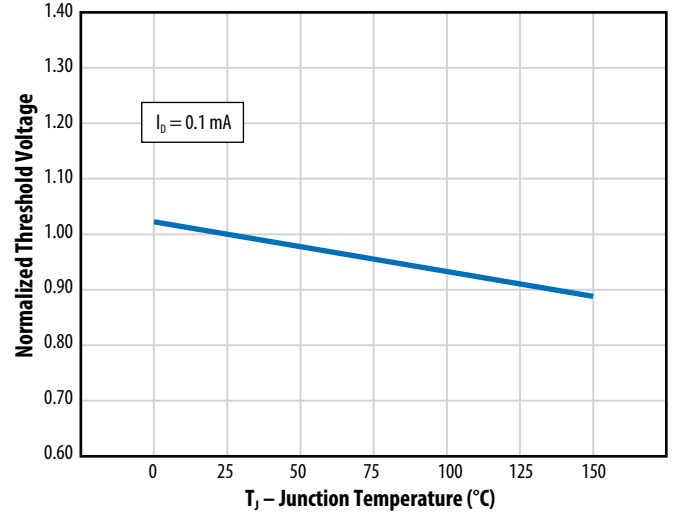
Figure 9b (Q3): Normalized On-State Resistance vs. Temperature



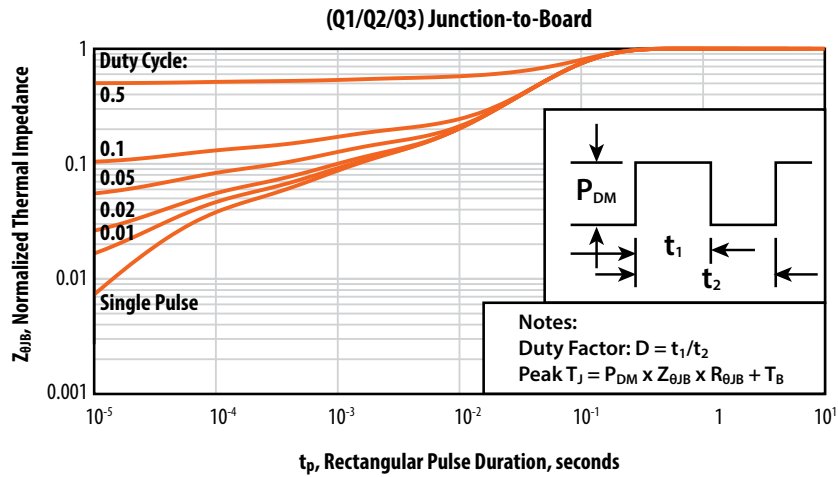
**Figure 10a (Q1 & Q2):**  
Normalized Threshold Voltage vs. Temperature



**Figure 10b (Q3):**  
Normalized Threshold Voltage vs. Temperature



**Figure 11a**  
Transient Thermal Response Curves



**Figure 11b**  
Transient Thermal Response Curves

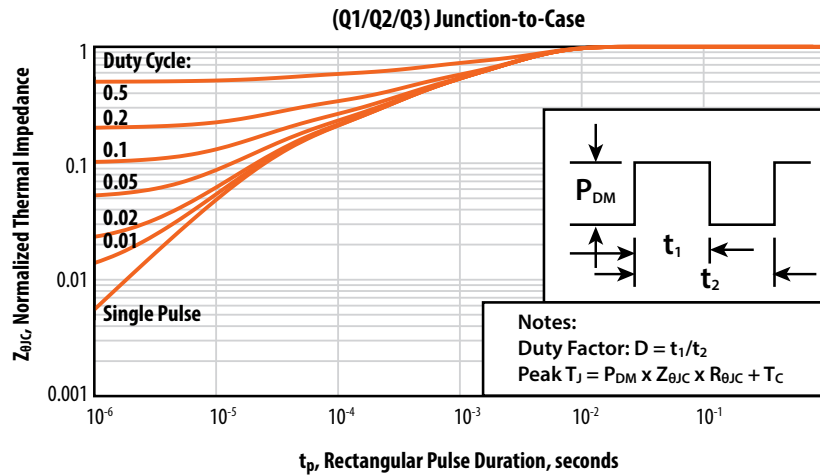


Figure 12 (Q1 & Q2): Safe Operating Area

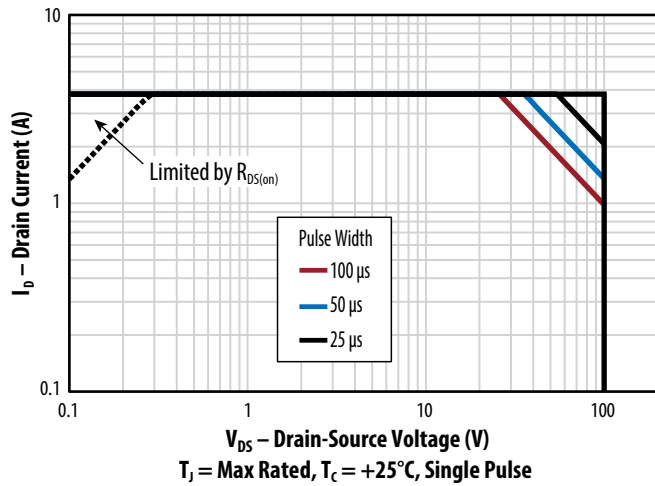


Figure 13 (Q3): Gate-Source Characteristics

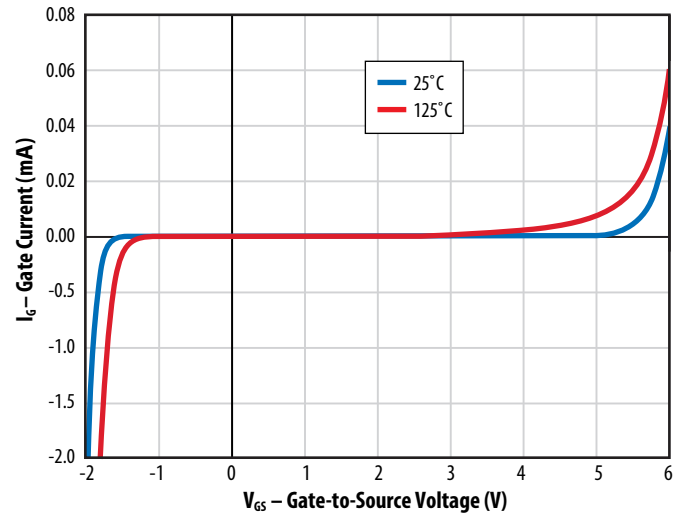
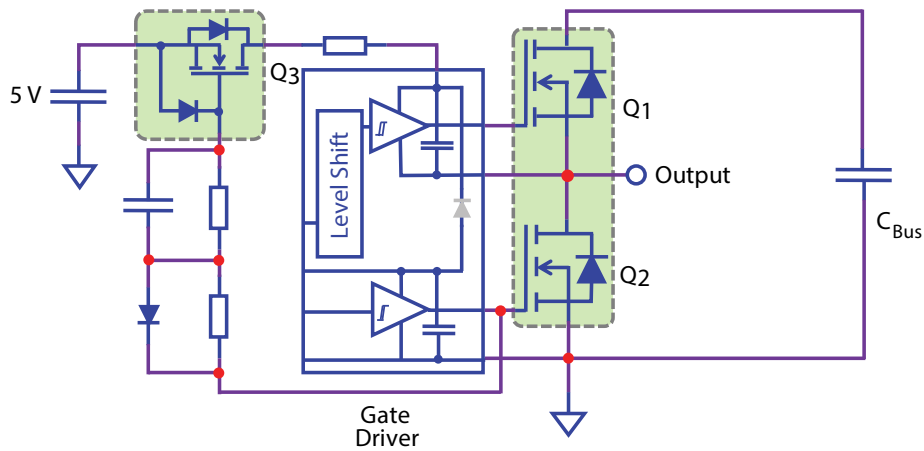


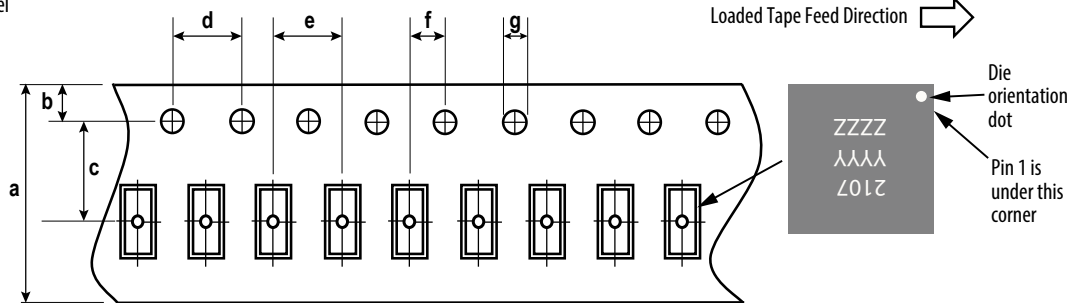
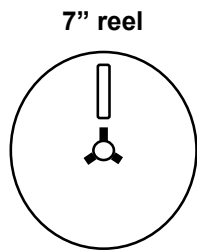
Figure 14: Typical Application Circuit





**TAPE AND REEL CONFIGURATION**

4mm pitch, 8mm wide tape on 7" reel

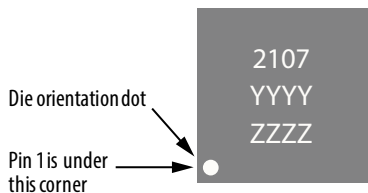


Die is placed into pocket solder bump side down (face side down)

Dimension (mm)	EPC2107 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

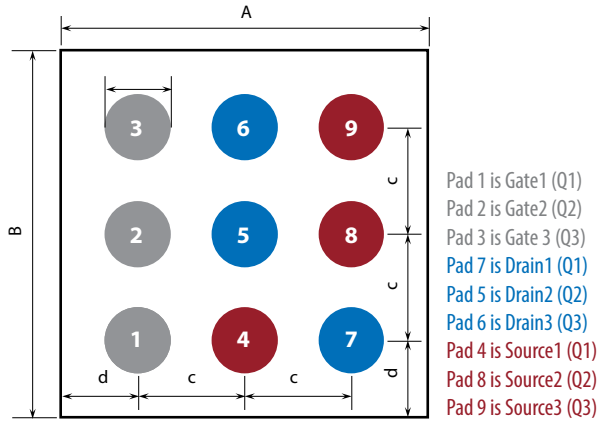
Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.  
 Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

**DIE MARKINGS**



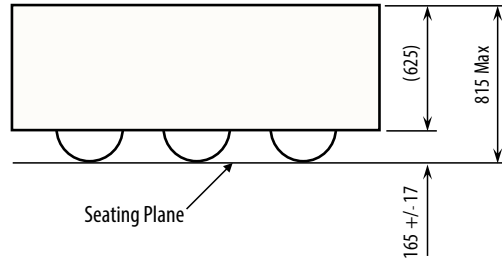
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2107	2107	YYYY	ZZZZ

**DIE OUTLINE**  
Solder Bump View

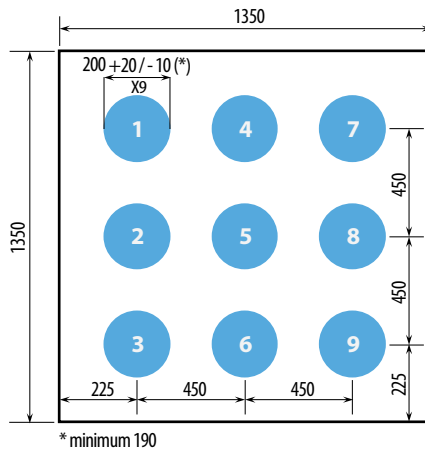


DIM	Micrometers		
	MIN	Nominal	MAX
A	1320	1350	1380
B	1320	1350	1380
c	450	450	450
d	210	225	240
e	187	208	229

Side View

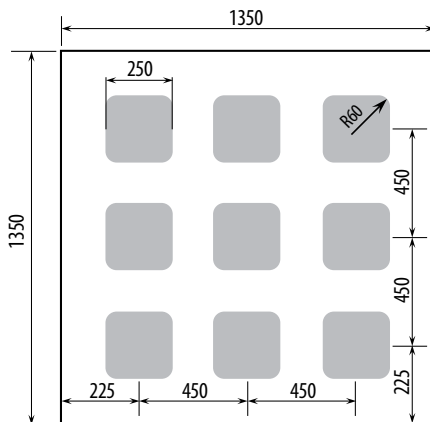


**RECOMMENDED LAND PATTERN**  
(measurements in  $\mu\text{m}$ )



The land pattern is solder mask defined  
Solder mask is 10  $\mu\text{m}$  smaller per side than bump

**RECOMMENDED STENCIL DRAWING**  
(measurements in  $\mu\text{m}$ )



Recommended stencil should be 4 mil (100  $\mu\text{m}$ ) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at  
<https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx>

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