

Dual 20 V N-Channel NexFET™ Power MOSFETs

FEATURES

- Common Source Connection
- Low Drain to Drain On-Resistance
- Space Saving SON 3.3 x 3.3 mm Plastic Package
- Optimized for 5 V Gate Drive
- Low Thermal Resistance
- Avalanche Rated
- Pb-Free Terminal Plating
- RoHS Compliant
- Halogen Free

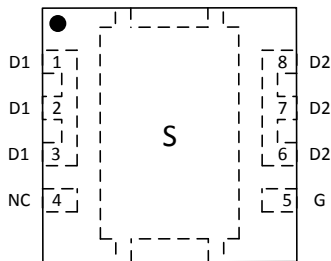
APPLICATIONS

- Adaptor or USB Input Protection for Notebook PCs and Tablets

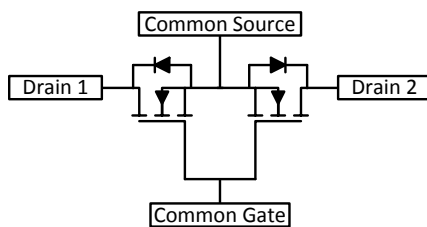
DESCRIPTION

The CSD85312Q3E is a 20 V common-source, dual N-channel device designed for adaptor or USB input protection. This SON 3.3 x 3.3 mm device has low drain to drain on-resistance that minimizes losses and offers low component count for space constrained multi-cell battery charging applications.

Top View



Circuit Image



PRODUCT SUMMARY

$T_A = 25^\circ\text{C}$		TYPICAL VALUE		UNIT
V_{DS}	Drain to Source Voltage	20		V
Q_g	Gate Charge Total (4.5 V)	11.7		nC
Q_{gd}	Gate Charge Gate to Drain	1.6		nC
$R_{DD(on)}$	Drain to Drain On Resistance (Q1 + Q2)	$V_{GS} = 4.5\text{ V}$	11.7	m Ω
		$V_{GS} = 8\text{ V}$	10.3	m Ω
$V_{GS(th)}$	Threshold Voltage	1.1		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD85312Q3E	SON 3.3 x 3.3 mm Plastic Package	13 Inch Reel	2500	Tape and Reel

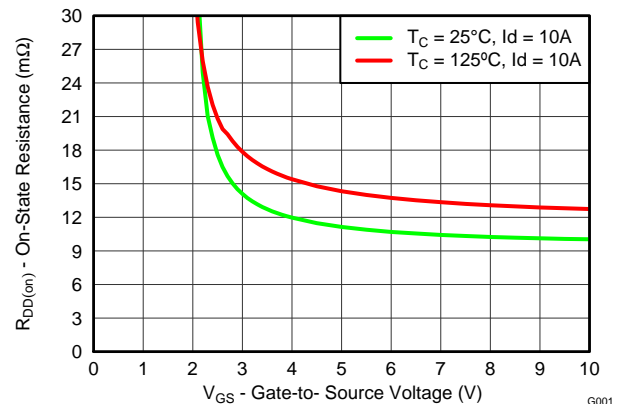
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$		VALUE	UNIT
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	+10/-8	V
I_D	Continuous Drain Current (Package Limited)	39	A
	Continuous Drain Current ⁽¹⁾	12	A
I_{DM}	Pulsed Drain Current ⁽²⁾	76	A
P_D	Power Dissipation	2.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, Single Pulse $I_D = 38\text{ A}, L = 0.1\text{ mH}, R_G = 25\ \Omega$	72	mJ

(1) Typical $R_{\theta JA} = 63^\circ\text{C/W}$ on 1 inch² (2 oz.) on 0.060 inch thick FR4PCB

(2) Pulse duration $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

V_{GS} vs. $R_{DD(on)}$



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	20			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0\text{ V}, V_{DS} = 16\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0\text{ V}, V_{GS} = +10/-8\text{ V}$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	0.85	1.10	1.40	V
$R_{DD(on)}$	Drain to Drain On Resistance (Q1 + Q2)	$V_{GS} = 4.5\text{ V}, I_D = 10\text{ A}$		11.7	14.0	$\text{m}\Omega$
		$V_{GS} = 8\text{ V}, I_D = 10\text{ A}$		10.3	12.4	$\text{m}\Omega$
g_{fs}	Transconductance	$V_{DS} = 10\text{ V}, I_D = 10\text{ A}$		99		S
Dynamic Characteristics⁽¹⁾						
C_{iss}	Input Capacitance	$V_{GS} = 0\text{ V}, V_{DS} = 10\text{ V}, f = 1\text{ MHz}$		1840	2390	pF
C_{oss}	Output Capacitance			492	640	pF
C_{rss}	Reverse Transfer Capacitance			31	40	pF
R_G	Series Gate Resistance			5.5	11	Ω
Q_g	Gate Charge Total (4.5 V)	$V_{DS} = 10\text{ V}, I_D = 10\text{ A}$		11.7	15.2	nC
Q_{gd}	Gate Charge Gate to Drain			1.6		nC
Q_{gs}	Gate Charge Gate to Source			3.5		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.8		nC
Q_{oss}	Output Charge	$V_{DS} = 10\text{ V}, V_{GS} = 0\text{ V}$		8.9		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 10\text{ V}, V_{GS} = 4.5\text{ V}, I_{DS} = 10\text{ A}, R_G = 2\ \Omega$		11		ns
t_r	Rise Time			27		ns
$t_{d(off)}$	Turn Off Delay Time			24		ns
t_f	Fall Time			6		ns
Diode Characteristics⁽¹⁾						
V_{SD}	Diode Forward Voltage	$I_{SD} = 10\text{ A}, V_{GS} = 0\text{ V}$		0.8	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DS} = 10\text{ V}, I_F = 10\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$		15		nC
t_{rr}	Reverse Recovery Time			23		ns

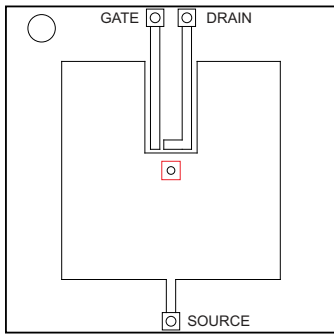
(1) All Dynamic and Diode Characteristics were measured with respect to one of the two drains, with the other left floating.

THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

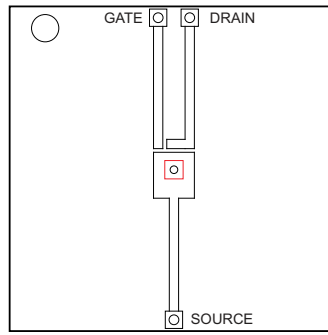
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			3.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			63	$^\circ\text{C}/\text{W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch² (6.45 cm²), 2-oz. (0.071 mm thick) Cu pad on a 1.5 inch × 1.5 inch (3.81 cm × 3.81 cm), 0.06 inch (1.52 mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1 inch² (6.45 cm²), 2 oz. (0.071 mm thick) Cu.



Max $R_{\theta JA} = 63^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of 2
oz. (0.071 mm thick)
Cu.

M0137-01



Max $R_{\theta JA} = 150^{\circ}\text{C/W}$
when mounted on a
minimum pad area of 2
oz. (0.071 mm thick)
Cu.

M0137-02

TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)

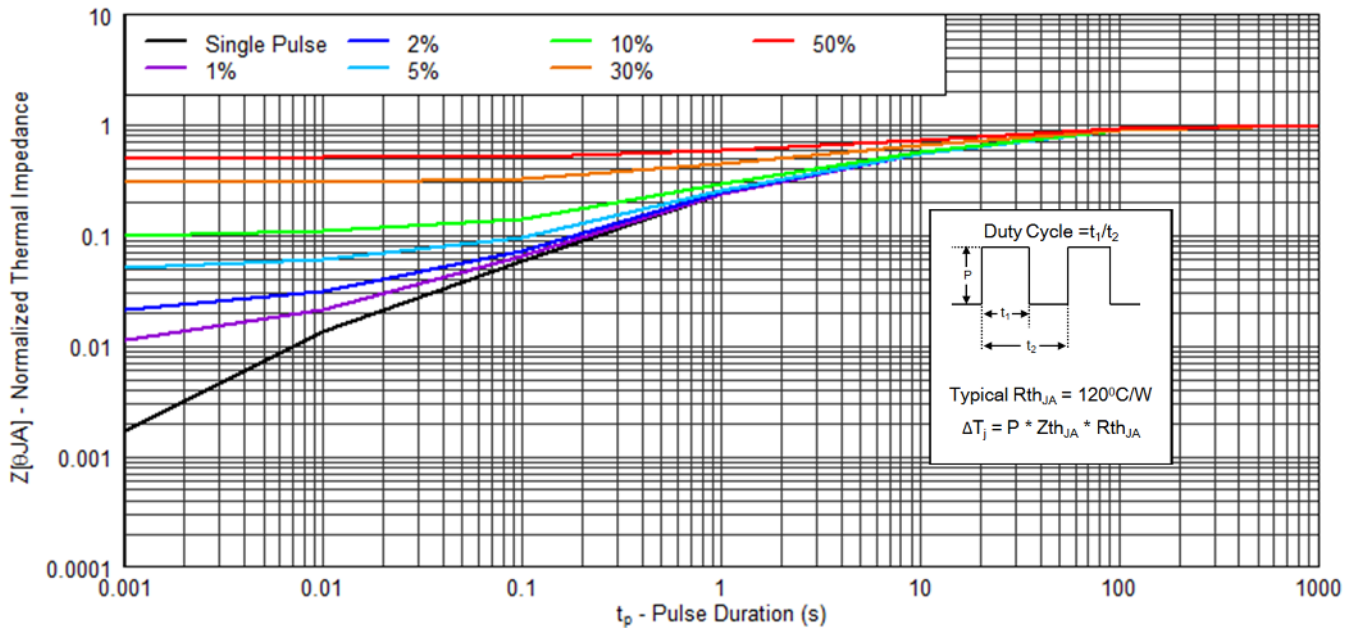


Figure 1. Transient Thermal Impedance

5201

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

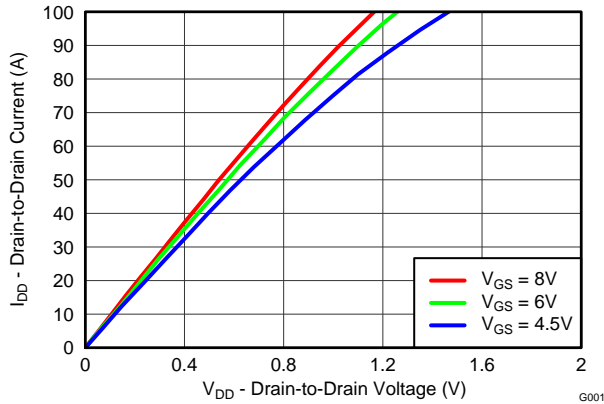


Figure 2. Saturation Characteristics

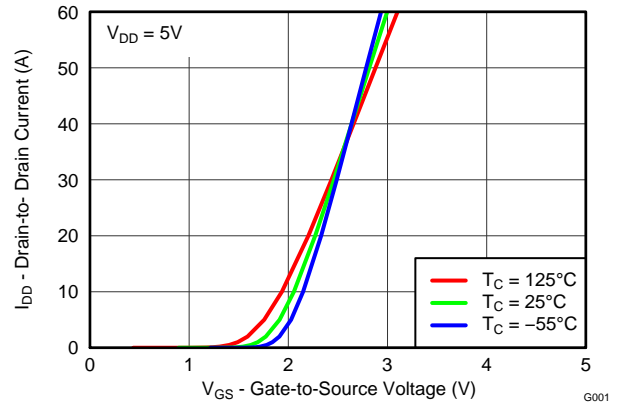


Figure 3. Transfer Characteristics

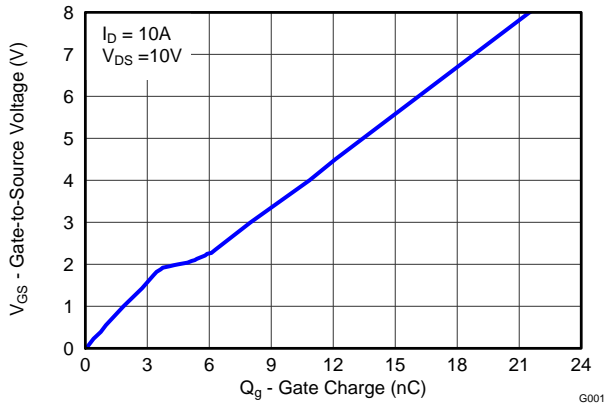


Figure 4. Gate Charge

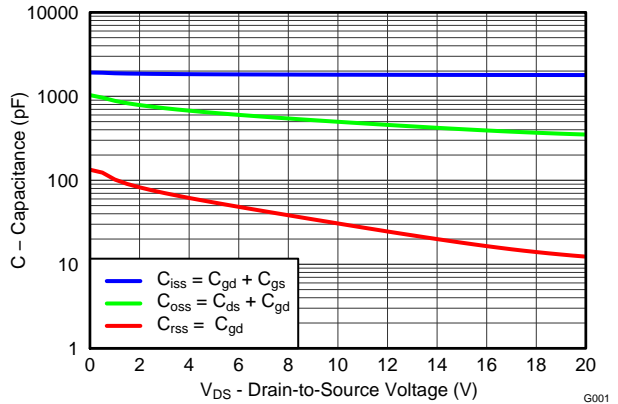


Figure 5. Capacitance

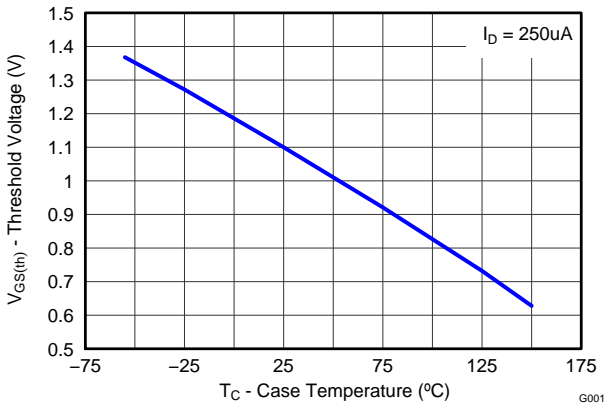


Figure 6. Threshold Voltage vs. Temperature

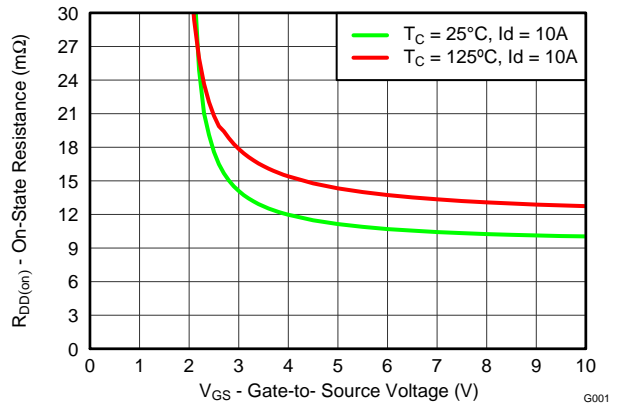


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

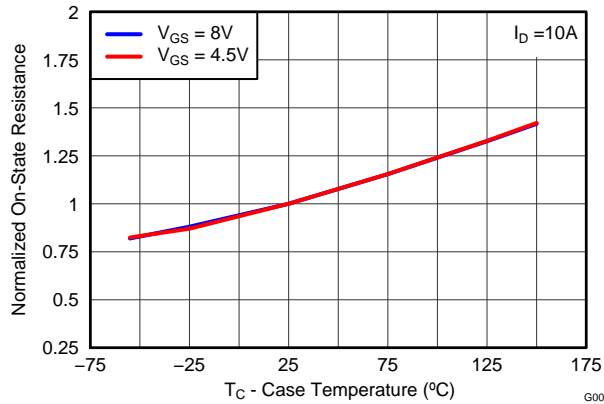


Figure 8. Normalized On-State Resistance vs. Temperature

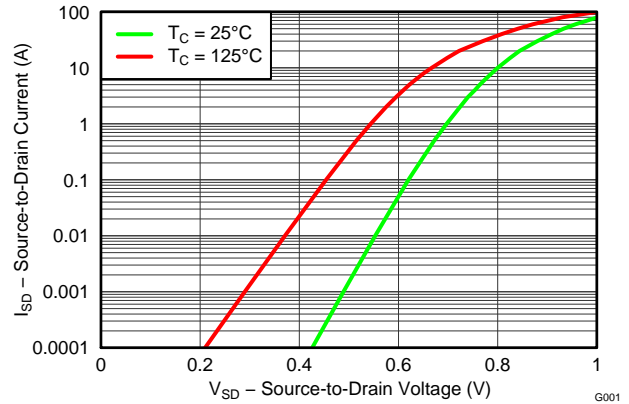


Figure 9. Typical Diode Forward Voltage

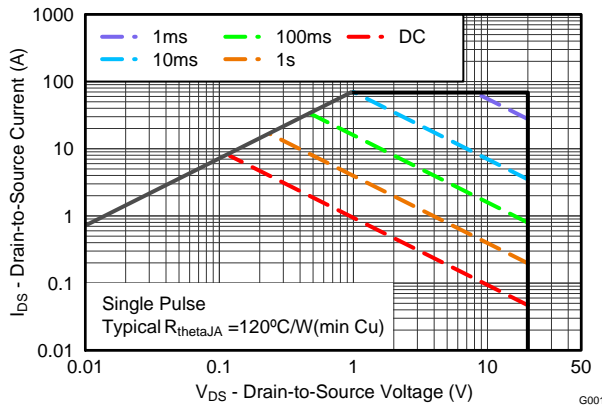


Figure 10. Maximum Safe Operating Area

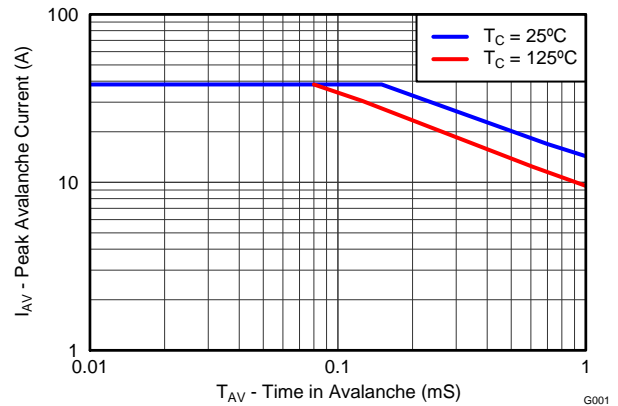


Figure 11. Single Pulse Unclamped Inductive Switching

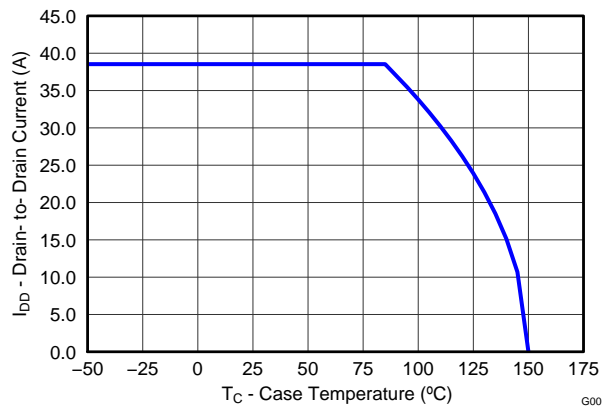


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

CSD85312Q3E Package Dimensions

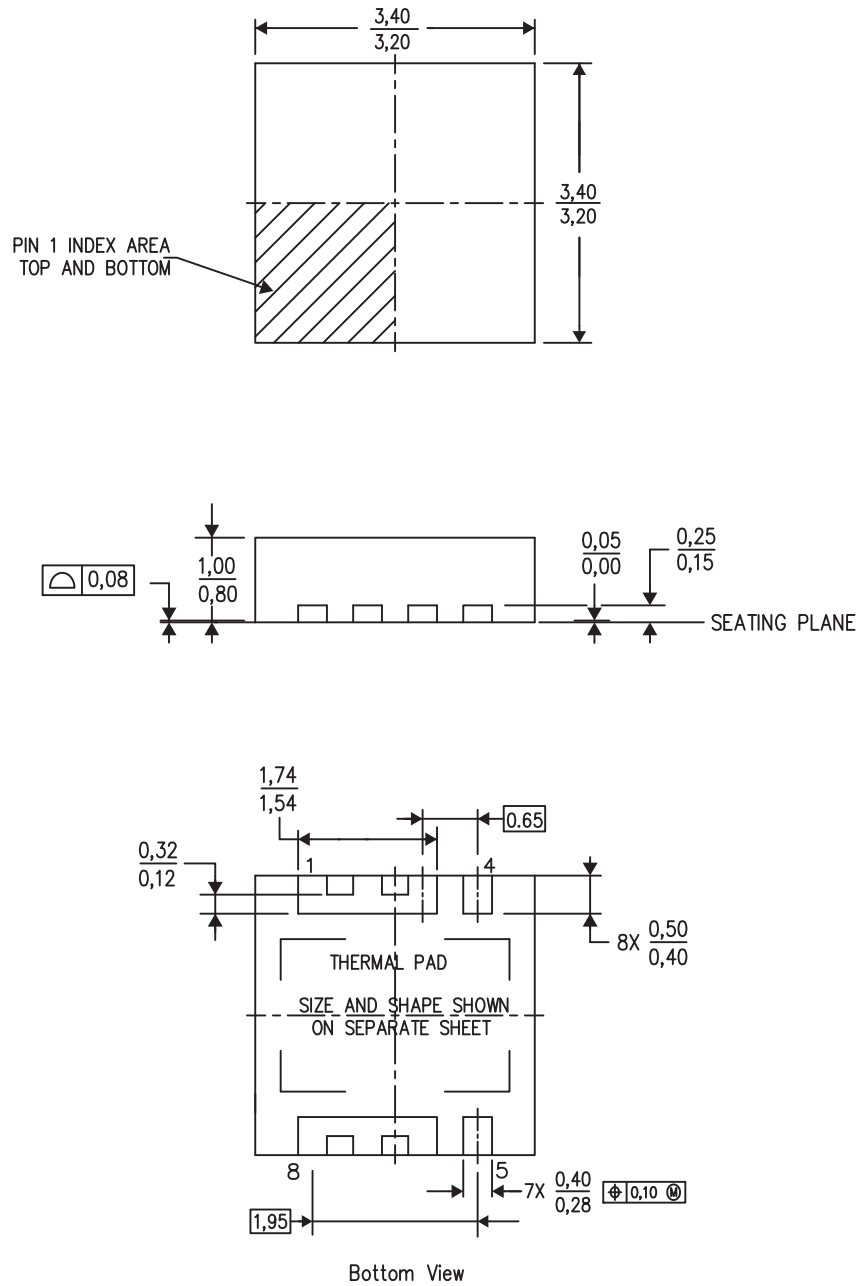
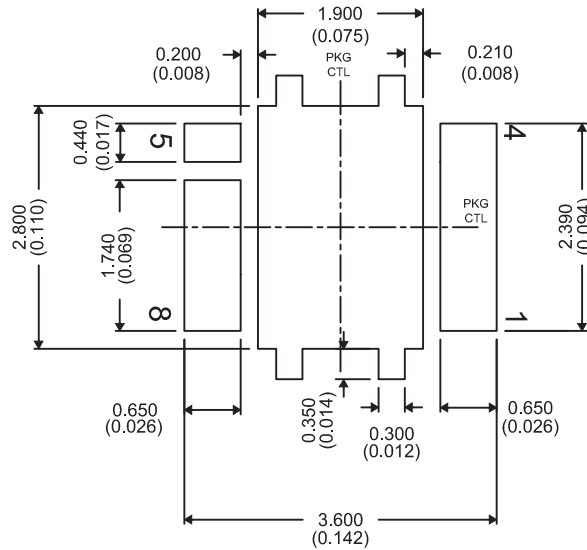


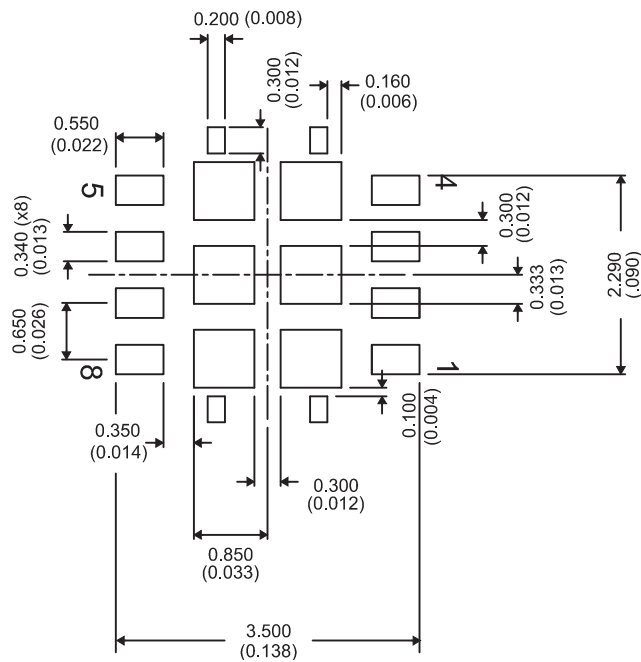
Table 1. Pin Configuration

Position	Designation
Pin 1 – 3	Drain 1
Pin 4	No Connect
Pin 5	Gate
Pin 6 – 8	Drain 2
Pin 9 (Thermal Pad)	Source

Recommended PCB Pattern



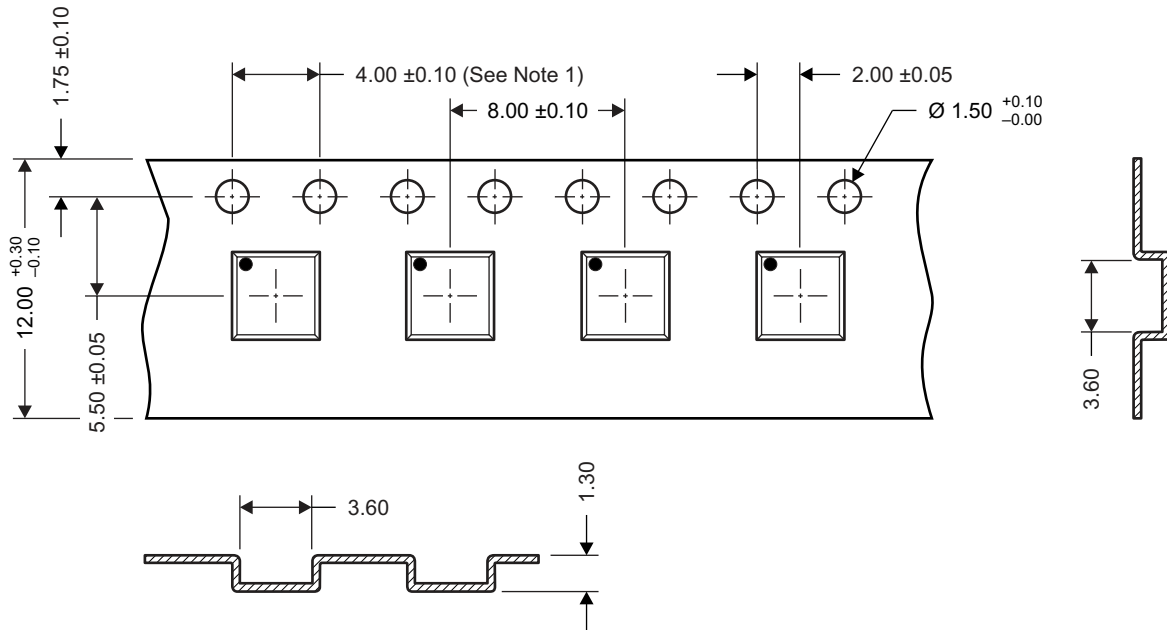
Recommended Stencil Opening



1. All Dimensions are in millimeters (inches)
2. Stencil Opening Thickness 4 mils

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q3E Tape and Reel Information



M0144-01

Notes:

1. 10 sprocket hole pitch cumulative tolerance ± 0.2
2. Camber not to exceed 1 mm IN 100 mm, noncumulative over 250 mm
3. Material: black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness: 0.30 ± 0.05 mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD85312Q3E	ACTIVE	VSON	DPA	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 150	85312E	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD85312Q3E	VSON	DPA	8	2500	330.0	12.4	3.6	3.6	1.2	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD85312Q3E	VSON	DPA	8	2500	346.0	346.0	33.0

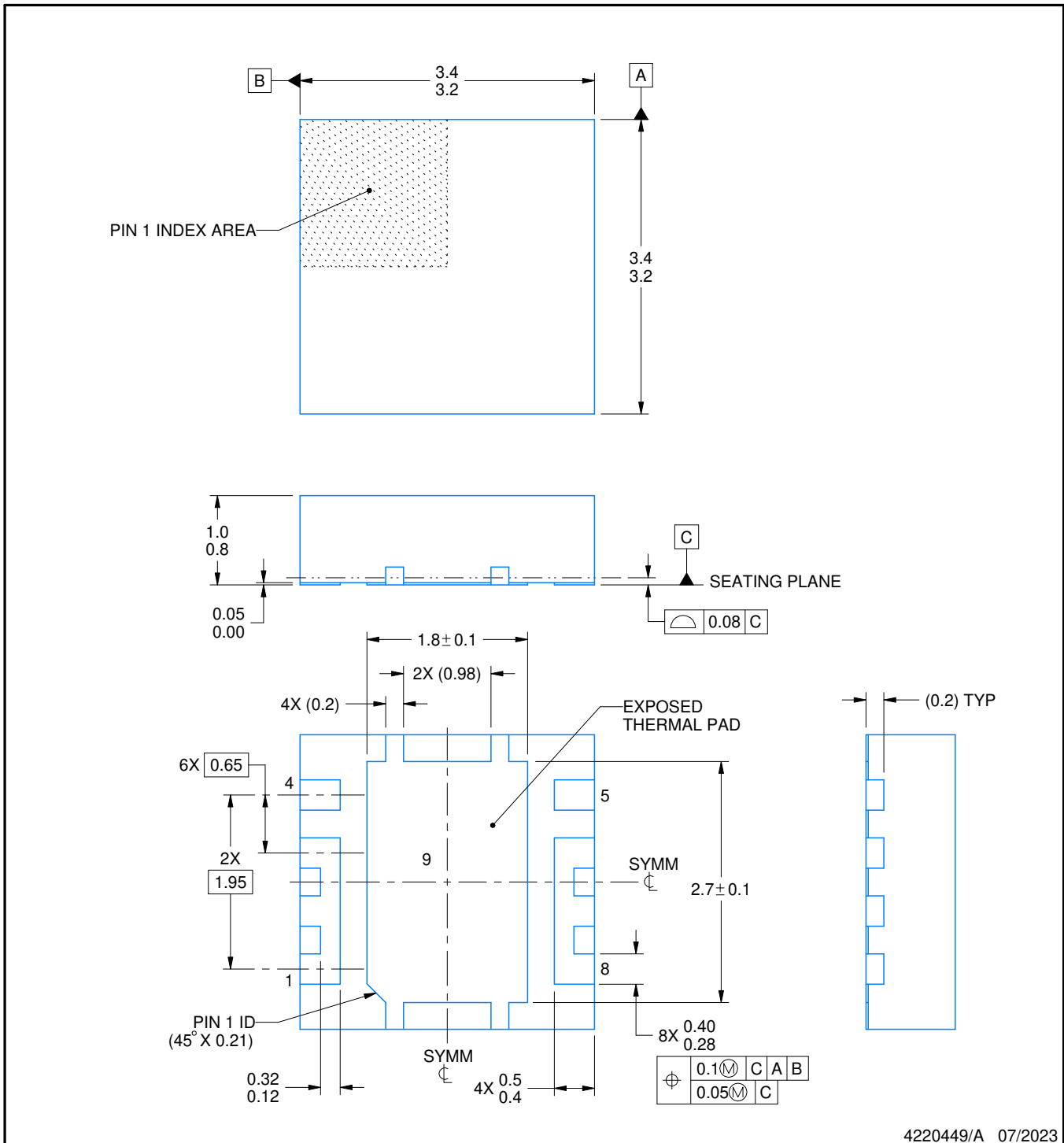
DPA0008A



PACKAGE OUTLINE

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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NOTES:

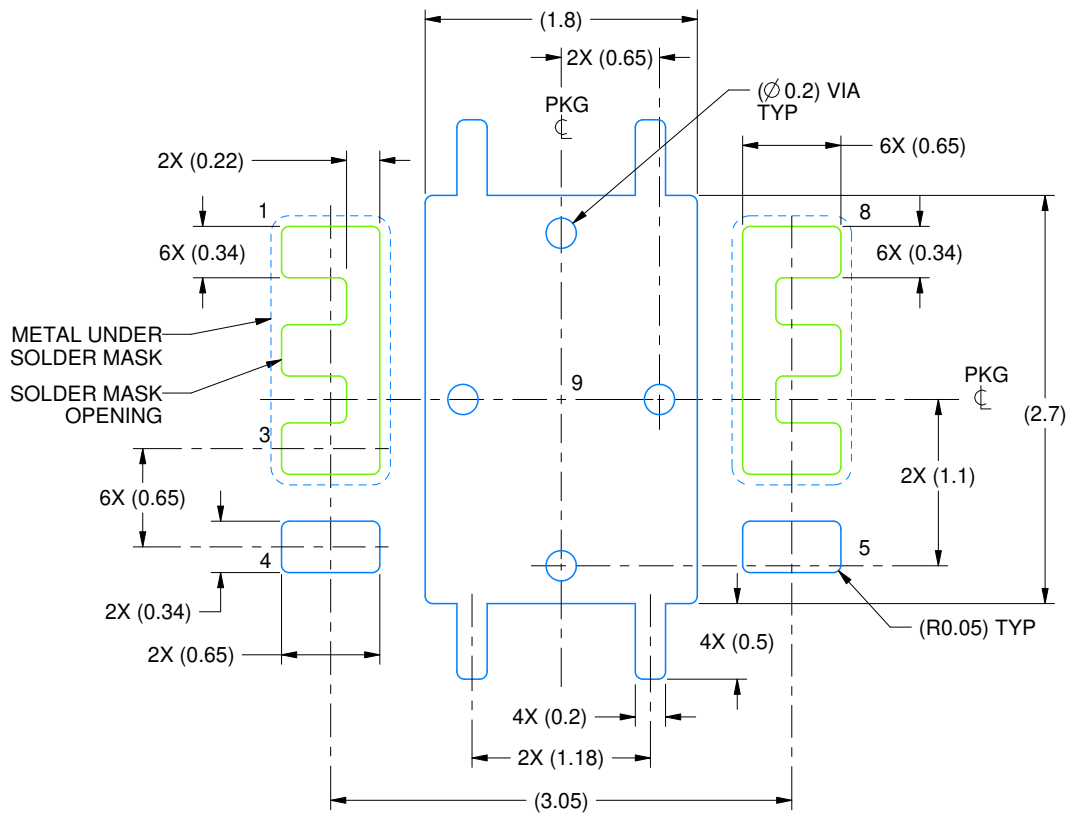
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

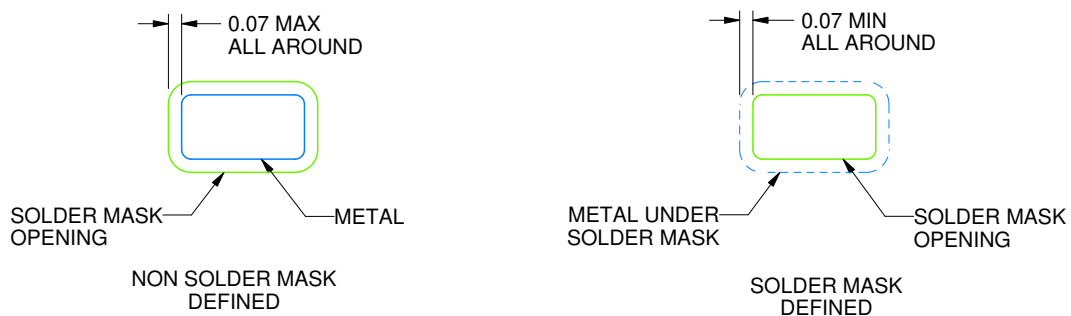
DPA0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

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NOTES: (continued)

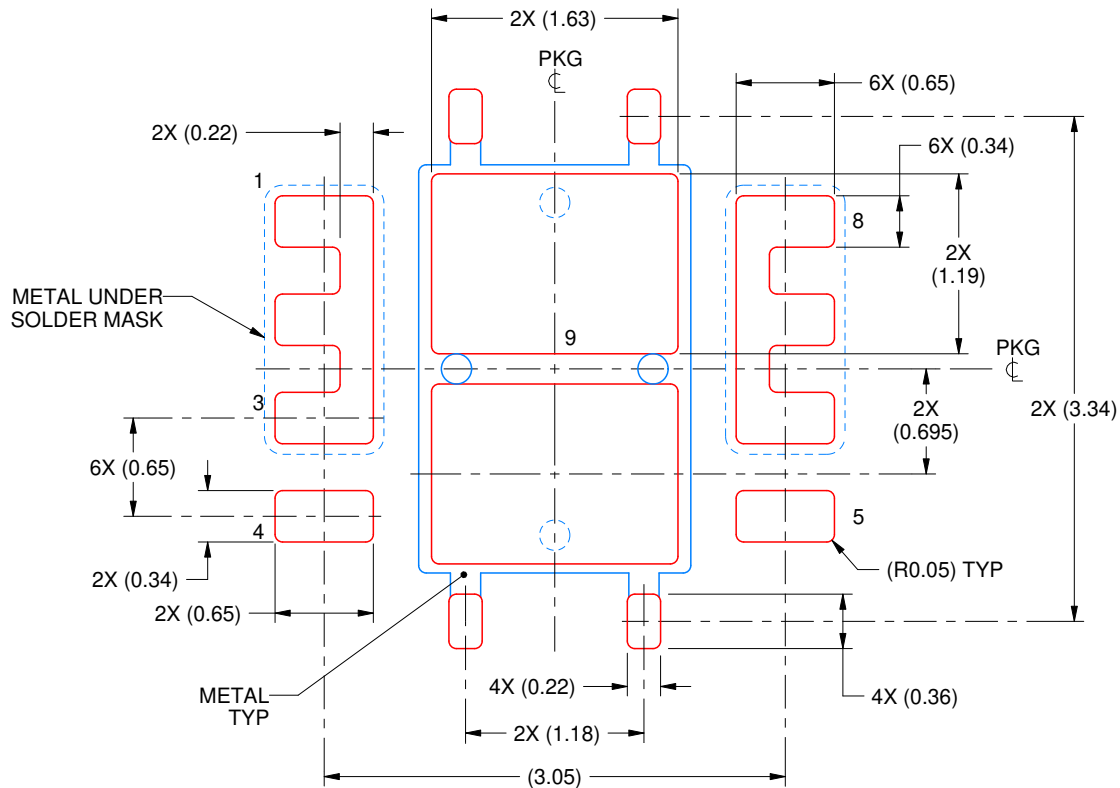
- This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
- Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.

EXAMPLE STENCIL DESIGN

DPA0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9
76% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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