



**CY7C1393JV18**  
**CY7C1394JV18**

# 18 Mbit DDR II SIO SRAM Two Word Burst Architecture

## Features

- 18 Mbit Density (1M x 18, 512K x 36)
- 300 MHz Clock for High Bandwidth
- Two word Burst for reducing Address Bus Frequency
- Double Data Rate (DDR) Interfaces (data transferred at 600 MHz) at 300 MHz
- Two Input Clocks (K and  $\bar{K}$ ) for Precise DDR Timing
  - SRAM uses rising edges only
- Two Input Clocks for Output Data (C and  $\bar{C}$ ) to Minimize Clock Skew and Flight Time mismatches
- Echo Clocks (CQ and  $\bar{CQ}$ ) simplify Data Capture in High Speed Systems
- Synchronous Internally self timed Writes
- DDR II operates with 1.5 cycle Read Latency when the DLL is enabled
- Operates similar to a DDR I Device with one Cycle Read Latency in DLL Off Mode
- 1.8V Core Power Supply with HSTL Inputs and Outputs
- Variable Drive HSTL Output Buffers
- Expanded HSTL Output Voltage (1.4V–V<sub>DD</sub>)
- Available in 165-Ball FBGA Package (13 x 15 x 1.4 mm)
- Offered in both Pb-free and non Pb-free packages
- JTAG 1149.1 compatible Test Access Port
- Delay Lock Loop (DLL) for Accurate Data Placement

## Configurations

CY7C1393JV18 – 1M x 18  
 CY7C1394JV18 – 512K x 36

## Selection Guide

Description		300 MHz	250 MHz	Unit
Maximum Operating Frequency		300	250	MHz
Maximum Operating Current	x18	865	725	mA
	x36	935	770	

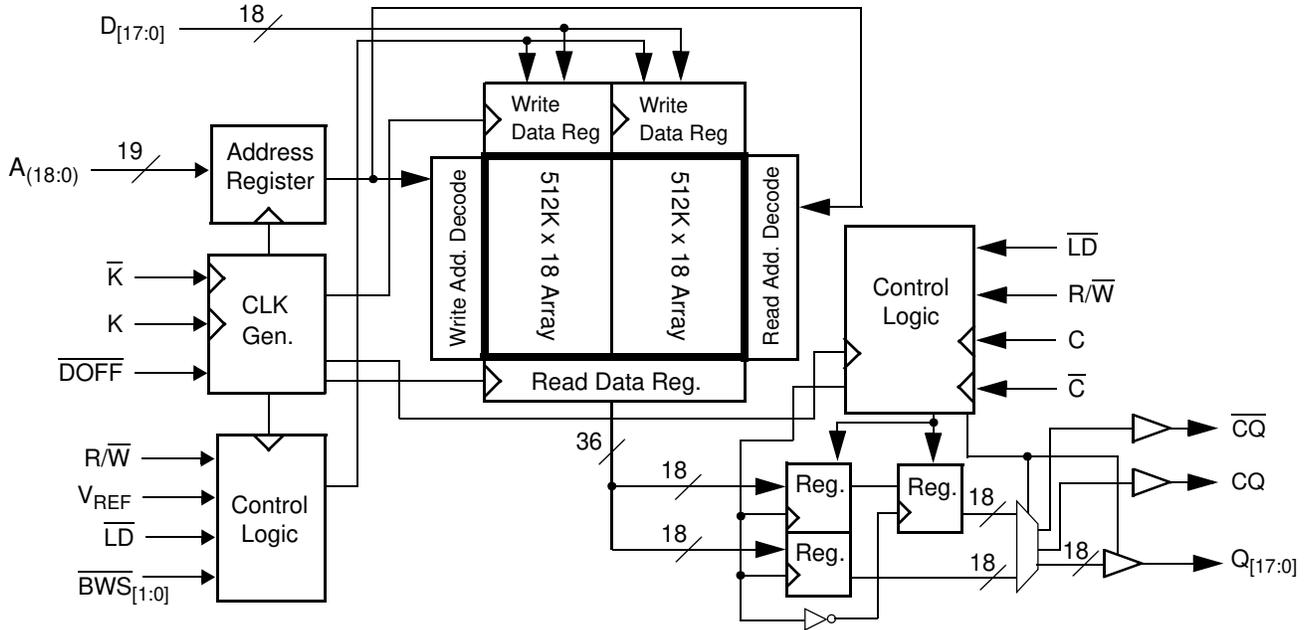
## Functional Description

The CY7C1393JV18, and CY7C1394JV18 are 1.8V Synchronous Pipelined SRAMs, equipped with Double Data Rate Separate IO (DDR II SIO) architecture. The DDR II SIO consists of two separate ports: the read port and the write port to access the memory array. The read port has data outputs to support read operations and the write port has data inputs to support write operations. The DDR II SIO has separate data inputs and data outputs to completely eliminate the need to 'turnaround' the data bus required with common IO devices. Access to each port is accomplished through a common address bus. Addresses for read and write are latched on alternate rising edges of the input (K) clock. Write data is registered on the rising edges of both K and  $\bar{K}$ . Read data is driven on the rising edges of C and  $\bar{C}$  if provided, or on the rising edge of K and  $\bar{K}$  if C or  $\bar{C}$  is not provided. Each address location is associated with two 18-bit words in the case of CY7C1393JV18, and two 36-bit words in the case of CY7C1394JV18 that burst sequentially into or out of the device.

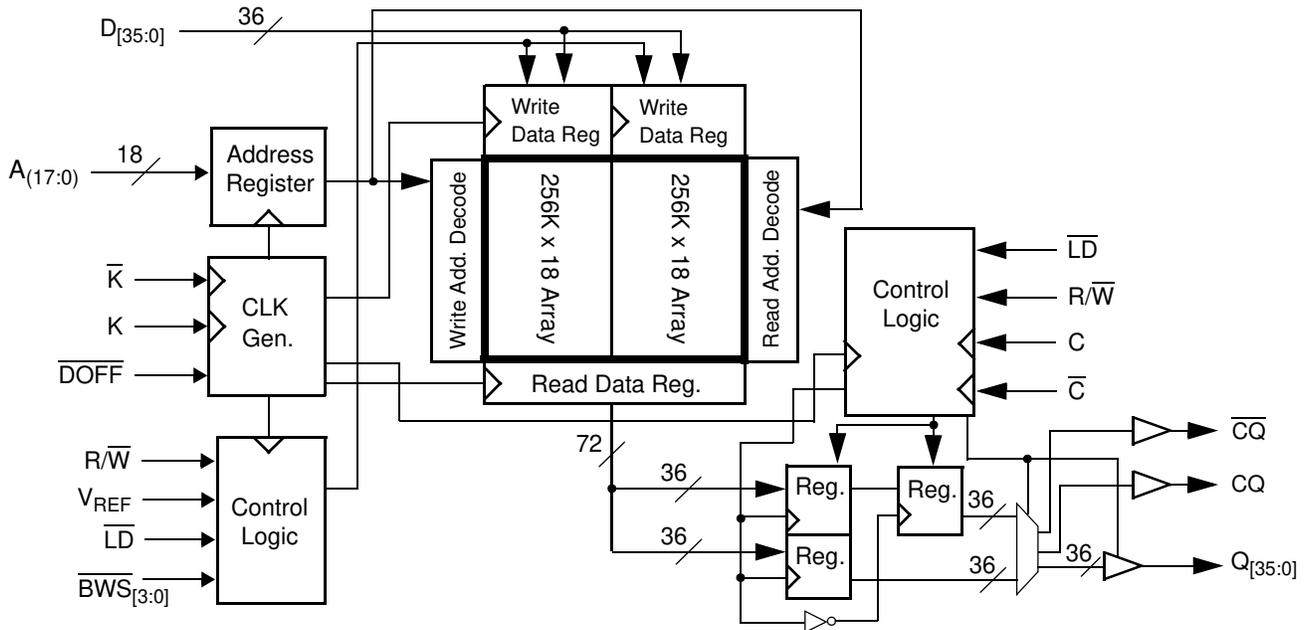
Asynchronous inputs include an output impedance matching input (ZQ). Synchronous data outputs are tightly matched to the two output echo clocks CQ/ $\bar{CQ}$ , eliminating the need to capture data separately from each individual DDR II SIO SRAM in the system design. Output data clocks (C/ $\bar{C}$ ) enable maximum system clocking and data synchronization flexibility.

All synchronous inputs pass through input registers controlled by the K or  $\bar{K}$  input clocks. All data outputs pass through output registers controlled by the C or  $\bar{C}$  (or K/ $\bar{K}$  in a single clock domain) input clocks. Writes are conducted with on-chip synchronous self timed write circuitry.

**Logic Block Diagram (CY7C1393JV18)**



**Logic Block Diagram (CY7C1394JV18)**



## Pin Configuration

The pin configurations for CY7C1393JV18, and CY7C1394JV18 follow. [1]

### 165-Ball FBGA (13 x 15 x 1.4 mm) Pinout

#### CY7C1393JV18 (1M x 18)

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	$\overline{\text{CQ}}$	NC/144M	NC/36M	$\text{R}/\overline{\text{W}}$	$\overline{\text{BWS}}_1$	$\overline{\text{K}}$	NC/288M	$\overline{\text{LD}}$	A	NC/72M	CQ
<b>B</b>	NC	Q9	D9	A	NC	K	$\overline{\text{BWS}}_0$	A	NC	NC	Q8
<b>C</b>	NC	NC	D10	$V_{\text{SS}}$	A	A	A	$V_{\text{SS}}$	NC	Q7	D8
<b>D</b>	NC	D11	Q10	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	NC	NC	D7
<b>E</b>	NC	NC	Q11	$V_{\text{DDQ}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{DDQ}}$	NC	D6	Q6
<b>F</b>	NC	Q12	D12	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	NC	Q5
<b>G</b>	NC	D13	Q13	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	NC	D5
<b>H</b>	$\overline{\text{DOFF}}$	$V_{\text{REF}}$	$V_{\text{DDQ}}$	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	$V_{\text{DDQ}}$	$V_{\text{REF}}$	ZQ
<b>J</b>	NC	NC	D14	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	Q4	D4
<b>K</b>	NC	NC	Q14	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	NC	D3	Q3
<b>L</b>	NC	Q15	D15	$V_{\text{DDQ}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{DDQ}}$	NC	NC	Q2
<b>M</b>	NC	NC	D16	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	NC	Q1	D2
<b>N</b>	NC	D17	Q16	$V_{\text{SS}}$	A	A	A	$V_{\text{SS}}$	NC	NC	D1
<b>P</b>	NC	NC	Q17	A	A	C	A	A	NC	D0	Q0
<b>R</b>	TDO	TCK	A	A	A	$\overline{\text{C}}$	A	A	A	TMS	TDI

#### CY7C1394JV18 (512K x 36)

	1	2	3	4	5	6	7	8	9	10	11
<b>A</b>	$\overline{\text{CQ}}$	NC/288M	NC/72M	$\text{R}/\overline{\text{W}}$	$\overline{\text{BWS}}_2$	$\overline{\text{K}}$	$\overline{\text{BWS}}_1$	$\overline{\text{LD}}$	NC/36M	NC/144M	CQ
<b>B</b>	Q27	Q18	D18	A	$\overline{\text{BWS}}_3$	K	$\overline{\text{BWS}}_0$	A	D17	Q17	Q8
<b>C</b>	D27	Q28	D19	$V_{\text{SS}}$	A	A	A	$V_{\text{SS}}$	D16	Q7	D8
<b>D</b>	D28	D20	Q19	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	Q16	D15	D7
<b>E</b>	Q29	D29	Q20	$V_{\text{DDQ}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{DDQ}}$	Q15	D6	Q6
<b>F</b>	Q30	Q21	D21	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	D14	Q14	Q5
<b>G</b>	D30	D22	Q22	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	Q13	D13	D5
<b>H</b>	$\overline{\text{DOFF}}$	$V_{\text{REF}}$	$V_{\text{DDQ}}$	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	$V_{\text{DDQ}}$	$V_{\text{REF}}$	ZQ
<b>J</b>	D31	Q31	D23	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	D12	Q4	D4
<b>K</b>	Q32	D32	Q23	$V_{\text{DDQ}}$	$V_{\text{DD}}$	$V_{\text{SS}}$	$V_{\text{DD}}$	$V_{\text{DDQ}}$	Q12	D3	Q3
<b>L</b>	Q33	Q24	D24	$V_{\text{DDQ}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{DDQ}}$	D11	Q11	Q2
<b>M</b>	D33	Q34	D25	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	$V_{\text{SS}}$	D10	Q1	D2
<b>N</b>	D34	D26	Q25	$V_{\text{SS}}$	A	A	A	$V_{\text{SS}}$	Q10	D9	D1
<b>P</b>	Q35	D35	Q26	A	A	C	A	A	Q9	D0	Q0
<b>R</b>	TDO	TCK	A	A	A	$\overline{\text{C}}$	A	A	A	TMS	TDI

#### Note

1. NC/36M, NC/72M, NC/144M, and NC/288M are not connected to the die and can be tied to any voltage level.

## Pin Definitions

Pin Name	IO	Pin Description
D <sub>[x:0]</sub>	Input-Synchronous	<b>Data Input Signals.</b> Sampled on the rising edge of K and $\bar{K}$ clocks during valid write operations. CY7C1393JV18 - D <sub>[17:0]</sub> CY7C1394JV18 - D <sub>[35:0]</sub>
$\bar{LD}$	Input-Synchronous	<b>Synchronous Load.</b> This input is brought LOW when a bus cycle sequence is defined. This definition includes address and read/write direction. All transactions operate on a burst of 2 data (one clock period of bus activity).
$\overline{BWS}_0$ , $\overline{BWS}_1$ , $\overline{BWS}_2$ , $\overline{BWS}_3$	Input-Synchronous	<b>Byte Write Select 0, 1, 2 and 3 – Active LOW.</b> Sampled on the rising edge of the K and $\bar{K}$ clocks during write operations. Used to select which byte is written into the device during the current portion of the write operations. Bytes <b>not</b> written remain <b>unaltered</b> . CY7C1393JV18 – $\overline{BWS}_0$ controls D <sub>[8:0]</sub> , $\overline{BWS}_1$ controls D <sub>[17:9]</sub> . CY7C1394JV18 – $\overline{BWS}_0$ controls D <sub>[8:0]</sub> , $\overline{BWS}_1$ controls D <sub>[17:9]</sub> , $\overline{BWS}_2$ controls D <sub>[26:18]</sub> and $\overline{BWS}_3$ controls D <sub>[35:27]</sub> . All the Byte Write Selects are sampled on the same edge as the data. Deselecting a Byte Write Select ignores the corresponding byte of data and is not written into the device.
A	Input-Synchronous	<b>Address Inputs.</b> Sampled on the rising edge of the K clock during active read and write operations. These address inputs are multiplexed for both read and write operations. Internally, the device is organized as 1M x 18 (2 arrays each of 512K x 18) for CY7C1393JV18, and 512K x 36 (2 arrays each of 256K x 36) for CY7C1394JV18. Therefore, only 19 address inputs are needed to access the entire memory array of CY7C1393JV18 and 18 address inputs for CY7C1394JV18. These inputs are ignored when the appropriate port is deselected.
Q <sub>[x:0]</sub>	Outputs-Synchronous	<b>Data Output Signals.</b> These pins drive out the requested data during a read operation. Valid data is driven out on the rising edge of both the C and $\bar{C}$ clocks during read operations, or K and $\bar{K}$ when in single clock mode. When the read port is deselected, Q <sub>[x:0]</sub> are automatically tri-stated. CY7C1393JV18 – Q <sub>[17:0]</sub> CY7C1394JV18 – Q <sub>[35:0]</sub>
R/ $\bar{W}$	Input-Synchronous	<b>Synchronous Read/Write Input.</b> When $\bar{LD}$ is LOW, this input designates the access type (read when R/ $\bar{W}$ is HIGH, write when R/ $\bar{W}$ is LOW) for the loaded address. R/ $\bar{W}$ must meet the setup and hold times around the edge of K.
C	Input Clock	<b>Positive Input Clock for Output Data.</b> C is used in conjunction with $\bar{C}$ to clock out the read data from the device. C and $\bar{C}$ are used together to deskew the flight times of various devices on the board back to the controller. See <a href="#">Application Example</a> on page 7 for further details.
$\bar{C}$	Input Clock	<b>Negative Input Clock for Output Data.</b> $\bar{C}$ is used in conjunction with C to clock out the read data from the device. C and $\bar{C}$ are used together to deskew the flight times of various devices on the board back to the controller. See <a href="#">Application Example</a> on page 7 for further details.
K	Input Clock	<b>Positive Input Clock Input.</b> The rising edge of K is used to capture synchronous inputs to the device and to drive out data through Q <sub>[x:0]</sub> when in single clock mode. All accesses are initiated on the rising edge of K.
$\bar{K}$	Input Clock	<b>Negative Input Clock Input.</b> $\bar{K}$ is used to capture synchronous inputs being presented to the device and to drive out data through Q <sub>[x:0]</sub> when in single clock mode.
CQ	Echo Clock	<b>CQ Referenced with Respect to C.</b> This is a free running clock and is synchronized to the input clock for output data (C) of the DDR II. In the single clock mode, CQ is generated with respect to K. The timings for the echo clocks are shown in the table <a href="#">Switching Characteristics</a> on page 20.
$\bar{CQ}$	Echo Clock	<b><math>\bar{CQ}</math> Referenced with Respect to <math>\bar{C}</math>.</b> This is a free running clock and is synchronized to the input clock for output data ( $\bar{C}$ ) of the DDR II. In the single clock mode, $\bar{CQ}$ is generated with respect to $\bar{K}$ . The timings for the echo clocks are shown in the table <a href="#">Switching Characteristics</a> on page 20.
ZQ	Input	<b>Output Impedance Matching Input.</b> This input is used to tune the device outputs to the system data bus impedance. CQ, $\bar{CQ}$ , and Q <sub>[x:0]</sub> output impedance are set to 0.2 x RQ, where RQ is a resistor connected between ZQ and ground. Alternatively, this pin is connected directly to V <sub>DDQ</sub> , which enables the minimum impedance mode. This pin cannot be connected directly to GND or left unconnected.

**Pin Definitions** (continued)

Pin Name	IO	Pin Description
$\overline{\text{DOFF}}$	Input	<b>DLL Turn Off – Active Low.</b> Connecting this pin to ground turns off the DLL inside the device. The timing in the DLL turned off operation differs from those listed in this data sheet. For normal operation, this pin is connected to a pull up through a 10 Kohm or less pull up resistor. The device behaves in DDR I mode when the DLL is turned off. In this mode, the device can be operated at a frequency of up to 167 MHz with DDR I timing.
TDO	Output	<b>TDO for JTAG.</b>
TCK	Input	<b>TCK Pin for JTAG.</b>
TDI	Input	<b>TDI Pin for JTAG.</b>
TMS	Input	<b>TMS Pin for JTAG.</b>
NC	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
NC/36M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
NC/72M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
NC/144M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
NC/288M	N/A	<b>Not Connected to the Die.</b> Can be tied to any voltage level.
$V_{\text{REF}}$	Input-Reference	<b>Reference Voltage Input.</b> Static input used to set the reference level for HSTL inputs, Outputs, and AC measurement points.
$V_{\text{DD}}$	Power Supply	<b>Power Supply Inputs to the Core of the Device.</b>
$V_{\text{SS}}$	Ground	<b>Ground for the Device.</b>
$V_{\text{DDQ}}$	Power Supply	<b>Power Supply Inputs for the Outputs of the Device.</b>

## Functional Overview

The CY7C1393JV18, and CY7C1394JV18 are synchronous pipelined Burst SRAMs equipped with a DDR II Separate IO interface, which operates with a read latency of one and half cycles when DOFF pin is tied HIGH. When DOFF pin is set LOW or connected to  $V_{SS}$  the device behaves in DDR I mode with a read latency of one clock cycle.

Accesses are initiated on the rising edge of the positive input clock (K). All synchronous input timing is referenced from the rising edge of the input clocks (K and  $\bar{K}$ ) and all output timing is referenced to the rising edge of the output clocks (C/ $\bar{C}$ , or K/K when in single clock mode).

All synchronous data inputs ( $D_{[x:0]}$ ) pass through input registers controlled by the rising edge of the input clocks (K and  $\bar{K}$ ). All synchronous data outputs ( $Q_{[x:0]}$ ) pass through output registers controlled by the rising edge of the output clocks (C/ $\bar{C}$  or K/K when in single-clock mode).

All synchronous control ( $R/\bar{W}$ ,  $\bar{LD}$ ,  $\overline{BWS}_{[0:x]}$ ) inputs pass through input registers controlled by the rising edge of the input clock (K).

CY7C1393JV18 is described in the following sections. The same basic descriptions apply to CY7C1394JV18.

### Read Operations

The CY7C1393JV18 is organized internally as two arrays of 512K x 18. Accesses are completed in a burst of two sequential 18-bit data words. Read operations are initiated by asserting  $R/\bar{W}$  HIGH and  $\bar{LD}$  LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the read address register. Following the next K clock rise, the corresponding lowest order 18-bit word of data is driven onto the  $Q_{[17:0]}$  using  $\bar{C}$  as the output timing reference. On the subsequent rising edge of C, the next 18-bit data word is driven onto the  $Q_{[17:0]}$ . The requested data is valid 0.45 ns from the rising edge of the output clock (C/ $\bar{C}$ , or K/K when in single clock mode). Read accesses are initiated on every rising edge of the positive input clock (K). This pipelines the data flow such that data is transferred out of the device on every rising edge of the output clocks, C/ $\bar{C}$  (or K/K when in single clock mode).

The CY7C1393JV18 first completes the pending read transactions, when read access is deselected. Synchronous internal circuitry automatically tri-states the output following the next rising edge of the positive output clock (C).

### Write Operations

Write operations are initiated by asserting  $R/\bar{W}$  LOW and  $\bar{LD}$  LOW at the rising edge of the positive input clock (K). The address presented to address inputs is stored in the write address register. On the following K clock rise the data presented to  $D_{[17:0]}$  is latched and stored into the 18-bit write data register, provided  $BWS_{[1:0]}$  are both asserted active. On the subsequent rising edge of the negative input clock ( $\bar{K}$ ) the information presented to  $D_{[17:0]}$  is also stored into the write data register, provided  $BWS_{[1:0]}$  are both asserted active. The 36 bits of data are then written into the memory array at the specified location. Write accesses are initiated on every rising edge of the positive

input clock (K). This pipelines the data flow such that 18 bits of data can be transferred into the device on every rising edge of the input clocks (K and  $\bar{K}$ ).

When Write access is deselected, the device ignores all inputs after the pending write operations are completed.

### Byte Write Operations

Byte write operations are supported by the CY7C1393JV18. A write operation is initiated as described in the section [Write Operations](#) on page 6. The bytes that are written are determined by  $BWS_0$  and  $BWS_1$ , which are sampled with each set of 18-bit data words. Asserting the appropriate Byte Write Select input during the data portion of a write latches the data being presented and writes it into the device. Deasserting the Byte Write Select input during the data portion of a write enables the data stored in the device for that byte to remain unaltered. This feature is used to simplify read, modify, and write operations to a byte write operation.

### Single Clock Mode

The CY7C1393JV18 is used with a single clock that controls both the input and output registers. In this mode the device recognizes only a single pair of input clocks (K and  $\bar{K}$ ) that control both the input and output registers. This operation is identical to the operation if the device had zero skew between the K/ $\bar{K}$  and C/ $\bar{C}$  clocks. All timing parameters remain the same in this mode. To use this mode of operation, tie C and  $\bar{C}$  HIGH at power on. This function is a strap option and not alterable during device operation.

### DDR Operation

The CY7C1393JV18 enables high performance operation through high clock frequencies (achieved through pipelining) and double data rate mode of operation.

If a read occurs after a write cycle, address and data for the write are stored in registers. Store the write information because the SRAM cannot perform the last word write to the array without conflicting with the read. The data stays in this register until the next write cycle occurs. On the first write cycle after the reads, the stored data from the earlier write is written into the SRAM array. This is called a posted write.

### Depth Expansion

Depth expansion requires replicating the  $\bar{LD}$  control signal for each bank. All other control signals are common between banks as appropriate.

### Programmable Impedance

Connect an external resistor,  $R_Q$ , between the ZQ pin on the SRAM and  $V_{SS}$  to enable the SRAM to adjust its output driver impedance. The value of  $R_Q$  is five times the value of the intended line impedance driven by the SRAM. The allowable range of  $R_Q$  to guarantee impedance matching with a tolerance of  $\pm 15$  percent is between 175 $\Omega$  and 350 $\Omega$ , with  $V_{DDQ} = 1.5V$ . The output impedance is adjusted every 1024 cycles at power up to account for drifts in supply voltage and temperature.

### Echo Clocks

Echo clocks are provided on the DDR II to simplify data capture on high speed systems. Two echo clocks are generated by the DDR II. CQ is referenced with respect to C and CQ is referenced with respect to C. These are free running clocks and are synchronized to the output clock of the DDR II. In the single clock mode, CQ is generated with respect to K and CQ is generated with respect to K. The timing for the echo clocks is shown in [Switching Characteristics](#) on page 20.

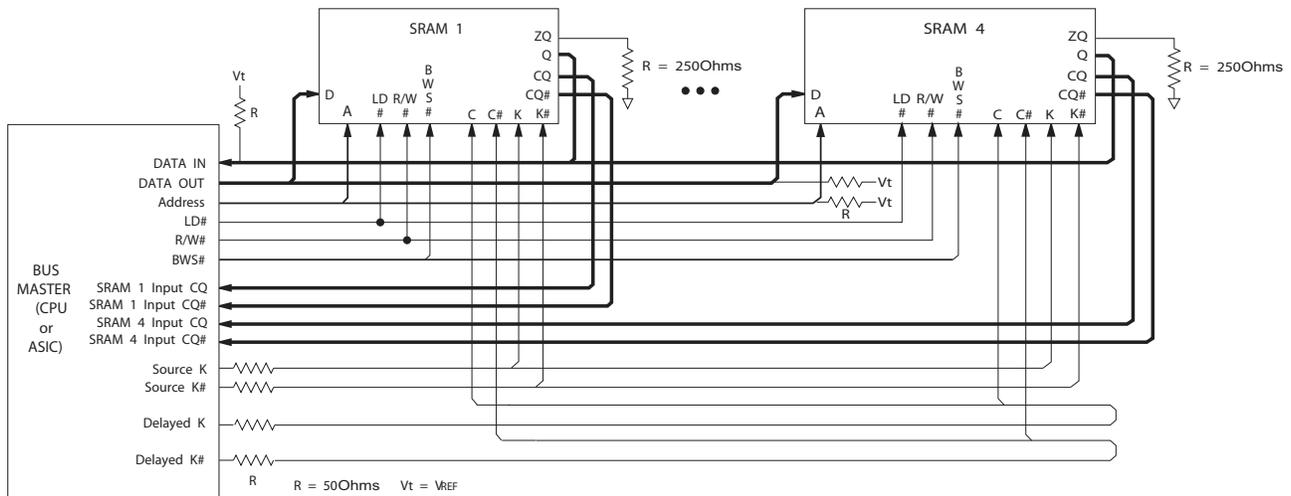
### DLL

These chips use a Delay Lock Loop (DLL) that is designed to function between 120 MHz and the specified maximum clock frequency. During power up, when the DOFF is tied HIGH, the DLL is locked after 1024 cycles of stable clock. The DLL is also reset by slowing or stopping the input clocks K and K for a minimum of 30 ns. However, it is not necessary to reset the DLL to lock it to the desired frequency. The DLL automatically locks 1024 clock cycles after a stable clock is presented. Disable the DLL by applying ground to the DOFF pin. When the DLL is turned off, the device behaves in DDR I mode (with one cycle latency and a longer access time). For information refer to the application note [AN5062](#) 'DLL Considerations in QDRII/DDRII/QDRII+/DDRII+'.

### Application Example

Figure 1 shows four DDR II SIO used in an application.

**Figure 1. Application Example**



## Truth Table

The truth table for CY7C1393JV18, and CY7C1394JV18 follows. [2, 3, 4, 5, 6, 7]

Operation	K	$\overline{\text{LD}}$	R/ $\overline{\text{W}}$	DQ	DQ
Write Cycle: Load address; wait one cycle; input write data on consecutive K and $\overline{\text{K}}$ rising edges.	L-H	L	L	D(A + 0) at K(t + 1) $\uparrow$	D(A + 1) at $\overline{\text{K}}$ (t + 1) $\uparrow$
Read Cycle: Load address; wait one and a half cycle; read data on consecutive $\overline{\text{C}}$ and C rising edges.	L-H	L	H	Q(A + 0) at $\overline{\text{C}}$ (t + 1) $\uparrow$	Q(A + 1) at C(t + 2) $\uparrow$
NOP: No Operation	L-H	H	X	High Z	High Z
Standby: Clock Stopped	Stopped	X	X	Previous State	Previous State

## Write Cycle Descriptions

The write cycle description table for CY7C1393JV18 follows. [2, 8]

$\overline{\text{BWS}}_0$	$\overline{\text{BWS}}_1$	K	$\overline{\text{K}}$	Comments
L	L	L-H	-	During the data portion of a write sequence: Both bytes (D <sub>[17:0]</sub> ) are written into the device.
L	L	-	L-H	During the data portion of a write sequence: Both bytes (D <sub>[17:0]</sub> ) are written into the device.
L	H	L-H	-	During the data portion of a write sequence: Only the lower byte (D <sub>[8:0]</sub> ) is written into the device, D <sub>[17:9]</sub> remains unaltered.
L	H	-	L-H	During the data portion of a write sequence: Only the lower byte (D <sub>[8:0]</sub> ) is written into the device, D <sub>[17:9]</sub> remains unaltered.
H	L	L-H	-	During the data portion of a write sequence: Only the upper byte (D <sub>[17:9]</sub> ) is written into the device, D <sub>[8:0]</sub> remains unaltered.
H	L	-	L-H	During the data portion of a write sequence: Only the upper byte (D <sub>[17:9]</sub> ) is written into the device, D <sub>[8:0]</sub> remains unaltered.
H	H	L-H	-	No data is written into the devices during this portion of a write operation.
H	H	-	L-H	No data is written into the devices during this portion of a write operation.

### Notes

- X = "Don't Care," H = Logic HIGH, L = Logic LOW,  $\uparrow$  represents rising edge.
- Device powers up deselected with the outputs in a tri-state condition.
- "A" represents address location latched by the devices when transaction was initiated. A + 0, A + 1 represents the internal address sequence in the burst.
- "t" represents the cycle at which a Read/Write operation is started. t + 1, and t + 2 are the first, and second clock cycles respectively succeeding the "t" clock cycle.
- Data inputs are registered at K and  $\overline{\text{K}}$  rising edges. Data outputs are delivered on C and  $\overline{\text{C}}$  rising edges, except when in single clock mode.
- It is recommended that K = K and C =  $\overline{\text{C}}$  = HIGH when clock is stopped. This is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.
- Is based on a write cycle that was initiated in accordance with the [Write Cycle Descriptions](#) table.  $\overline{\text{BWS}}_0$ ,  $\overline{\text{BWS}}_1$ ,  $\overline{\text{BWS}}_2$  and  $\overline{\text{BWS}}_3$  can be altered on different portions of a write cycle, as long as the setup and hold requirements are achieved.

## Write Cycle Descriptions

The write cycle description table for CY7C1394JV18 follows. [2, 8]

$\overline{BWS}_0$	$\overline{BWS}_1$	$\overline{BWS}_2$	$\overline{BWS}_3$	K	$\overline{K}$	Comments
L	L	L	L	L-H	-	During the data portion of a write sequence, all four bytes ( $D_{[35:0]}$ ) are written into the device.
L	L	L	L	-	L-H	During the data portion of a write sequence, all four bytes ( $D_{[35:0]}$ ) are written into the device.
L	H	H	H	L-H	-	During the data portion of a write sequence, only the lower byte ( $D_{[8:0]}$ ) is written into the device. $D_{[35:9]}$ remains unaltered.
L	H	H	H	-	L-H	During the data portion of a write sequence, only the lower byte ( $D_{[8:0]}$ ) is written into the device. $D_{[35:9]}$ remains unaltered.
H	L	H	H	L-H	-	During the data portion of a write sequence, only the byte ( $D_{[17:9]}$ ) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	L	H	H	-	L-H	During the data portion of a write sequence, only the byte ( $D_{[17:9]}$ ) is written into the device. $D_{[8:0]}$ and $D_{[35:18]}$ remains unaltered.
H	H	L	H	L-H	-	During the data portion of a write sequence, only the byte ( $D_{[26:18]}$ ) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	L	H	-	L-H	During the data portion of a write sequence, only the byte ( $D_{[26:18]}$ ) is written into the device. $D_{[17:0]}$ and $D_{[35:27]}$ remains unaltered.
H	H	H	L	L-H	-	During the data portion of a write sequence, only the byte ( $D_{[35:27]}$ ) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	L	-	L-H	During the data portion of a write sequence, only the byte ( $D_{[35:27]}$ ) is written into the device. $D_{[26:0]}$ remains unaltered.
H	H	H	H	L-H	-	No data is written into the device during this portion of a write operation.
H	H	H	H	-	L-H	No data is written into the device during this portion of a write operation.

## IEEE 1149.1 Serial Boundary Scan (JTAG)

These SRAMs incorporate a serial boundary scan Test Access Port (TAP) in the FBGA package. This part is fully compliant with IEEE Standard 1149.1-2001. The TAP operates using JEDEC standard 1.8V IO logic levels.

### Disabling the JTAG Feature

It is possible to operate the SRAM without using the JTAG feature. To disable the TAP controller, tie TCK LOW ( $V_{SS}$ ) to prevent clocking of the device. TDI and TMS are internally pulled up and may be unconnected. They may alternatively be connected to  $V_{DD}$  through a pull up resistor. Leave TDO unconnected. Upon power up, the device comes up in a reset state, which does not interfere with the operation of the device.

### Test Access Port—Test Clock

The test clock is used only with the TAP controller. All inputs are captured on the rising edge of TCK. All outputs are driven from the falling edge of TCK.

### Test Mode Select (TMS)

The TMS input is used to give commands to the TAP controller and is sampled on the rising edge of TCK. Leave this pin unconnected if the TAP is not used. The pin is pulled up internally, resulting in a logic HIGH level.

### Test Data-In (TDI)

The TDI pin is used to serially input information into the registers and is connected to the input of any of the registers. The register between TDI and TDO is chosen by the instruction that is loaded into the TAP instruction register. For information on loading the instruction register, see the [TAP Controller State Diagram](#) on page 12. TDI is internally pulled up and is unconnected if the TAP is unused in an application. TDI is connected to the most significant bit (MSB) on any register.

### Test Data-Out (TDO)

The TDO output pin is used to serially clock data out from the registers. The output is active, depending upon the current state of the TAP state machine (see [Instruction Codes](#) on page 15). The output changes on the falling edge of TCK. TDO is connected to the least significant bit (LSB) of any register.

### Performing a TAP Reset

A reset is performed by forcing TMS HIGH ( $V_{DD}$ ) for five rising edges of TCK. This reset does not affect the operation of the SRAM and is performed while the SRAM is operating. At power up, the TAP is reset internally to ensure that TDO comes up in a High Z state.

### TAP Registers

Registers are connected between the TDI and TDO pins to scan the data in and out of the SRAM test circuitry. Only one register can be selected at a time through the instruction registers. Data is serially loaded into the TDI pin on the rising edge of TCK. Data is output on the TDO pin on the falling edge of TCK.

#### *Instruction Register*

Three-bit instructions are serially loaded into the instruction register. This register is loaded when it is placed between the TDI and TDO pins, as shown in [on page 13](#). Upon power up, the instruction register is loaded with the IDCODE instruction. It is also loaded with the IDCODE instruction if the controller is placed in a reset state, as described in the previous section.

When the TAP controller is in the Capture-IR state, the two least significant bits are loaded with a binary '01' pattern to enable the fault isolation of the board level serial test path.

#### *Bypass Register*

To save time when serially shifting data through registers, it is sometimes advantageous to skip certain chips. The bypass register is a single-bit register that can be placed between TDI and TDO pins. This enables shifting of data through the SRAM with minimal delay. The bypass register is set LOW ( $V_{SS}$ ) when the BYPASS instruction is executed.

#### *Boundary Scan Register*

The boundary scan register is connected to all of the input and output pins on the SRAM. Several No Connect (NC) pins are also included in the scan register to reserve pins for higher density devices.

The boundary scan register is loaded with the contents of the RAM input and output ring when the TAP controller is in the Capture-DR state and is then placed between the TDI and TDO pins when the controller is moved to the Shift-DR state. The EXTEST, SAMPLE/PRELOAD, and SAMPLE Z instructions are used to capture the contents of the input and output ring.

The [Boundary Scan Order](#) on page 16 shows the order in which the bits are connected. Each bit corresponds to one of the bumps on the SRAM package. The MSB of the register is connected to TDI, and the LSB is connected to TDO.

#### *Identification (ID) Register*

The ID register is loaded with a vendor-specific, 32-bit code during the Capture-DR state when the IDCODE command is loaded in the instruction register. The IDCODE is hardwired into the SRAM and is shifted out when the TAP controller is in the Shift-DR state. The ID register has a vendor code and other information described in [Identification Register Definitions](#) on page 15.

### TAP Instruction Set

Eight different instructions are possible with the three-bit instruction register. All combinations are listed in [Instruction Codes](#) on page 15. Do not use three of these instructions that are listed as RESERVED. The other five instructions are described in this section in detail.

Instructions are loaded into the TAP controller during the Shift-IR state when the instruction register is placed between TDI and TDO. During this state, instructions are shifted through the instruction register through the TDI and TDO pins. To execute the instruction after it is shifted in, move the TAP controller into the Update-IR state.

#### *IDCODE*

The IDCODE instruction loads a vendor-specific, 32-bit code into the instruction register. It also places the instruction register

between the TDI and TDO pins and shifts the IDCODE out of the device when the TAP controller enters the Shift-DR state. The IDCODE instruction is loaded into the instruction register at power up or whenever the TAP controller is supplied a Test-Logic-Reset state.

#### *SAMPLE Z*

The SAMPLE Z instruction connects the boundary scan register between the TDI and TDO pins when the TAP controller is in a Shift-DR state. The SAMPLE Z command puts the output bus into a High Z state until the next command is supplied during the Update IR state.

#### *SAMPLE/PRELOAD*

SAMPLE/PRELOAD is a 1149.1 mandatory instruction. When the SAMPLE/PRELOAD instructions are loaded into the instruction register and the TAP controller is in the Capture-DR state, a snapshot of data on the input and output pins is captured in the boundary scan register.

The TAP controller clock only operates at a frequency up to 20 MHz, while the SRAM clock operates more than an order of magnitude faster. Because there is a large difference in the clock frequencies, it is possible that during the Capture-DR state, an input or output undergoes a transition. The TAP then tries to capture a signal while in transition (metastable state). This does not harm the device, but there is no guarantee as to the value that is captured. Repeatable results may not be possible.

To guarantee that the boundary scan register captures the correct value of a signal, stabilize the SRAM signal long enough to meet the TAP controller's capture setup plus hold times ( $t_{CS}$  and  $t_{CH}$ ). The SRAM clock input might not be captured correctly if there is no way in a design to stop (or slow) the clock during a SAMPLE/PRELOAD instruction. If this is an issue, it is still possible to capture all other signals and simply ignore the value of the CK and CK captured in the boundary scan register.

After the data is captured, it is possible to shift out the data by putting the TAP into the Shift-DR state. This places the boundary scan register between the TDI and TDO pins.

PRELOAD places an initial data pattern at the latched parallel outputs of the boundary scan register cells before the selection of another boundary scan test operation.

The shifting of data for the SAMPLE and PRELOAD phases occurs concurrently when required, that is, while the data captured is shifted out, the preloaded data is shifted in.

#### *BYPASS*

When the BYPASS instruction is loaded in the instruction register and the TAP is placed in a Shift-DR state, the bypass register is placed between the TDI and TDO pins. The advantage of the BYPASS instruction is that it shortens the boundary scan path when multiple devices are connected together on a board.

#### *EXTEST*

The EXTEST instruction drives the preloaded data out through the system output pins. This instruction also connects the boundary scan register for serial access between the TDI and TDO in the Shift-DR controller state.

#### *EXTEST OUTPUT BUS TRI-STATE*

IEEE Standard 1149.1 mandates that the TAP controller be able to put the output bus into a tri-state mode.

The boundary scan register has a special bit located at bit 47. When this scan cell, called the 'extest output bus tri-state', is latched into the preload register during the Update-DR state in the TAP controller, it directly controls the state of the output (Q-bus) pins, when the EXTEST is entered as the current instruction. When HIGH, it enables the output buffers to drive the output bus. When LOW, this bit places the output bus into a High Z condition.

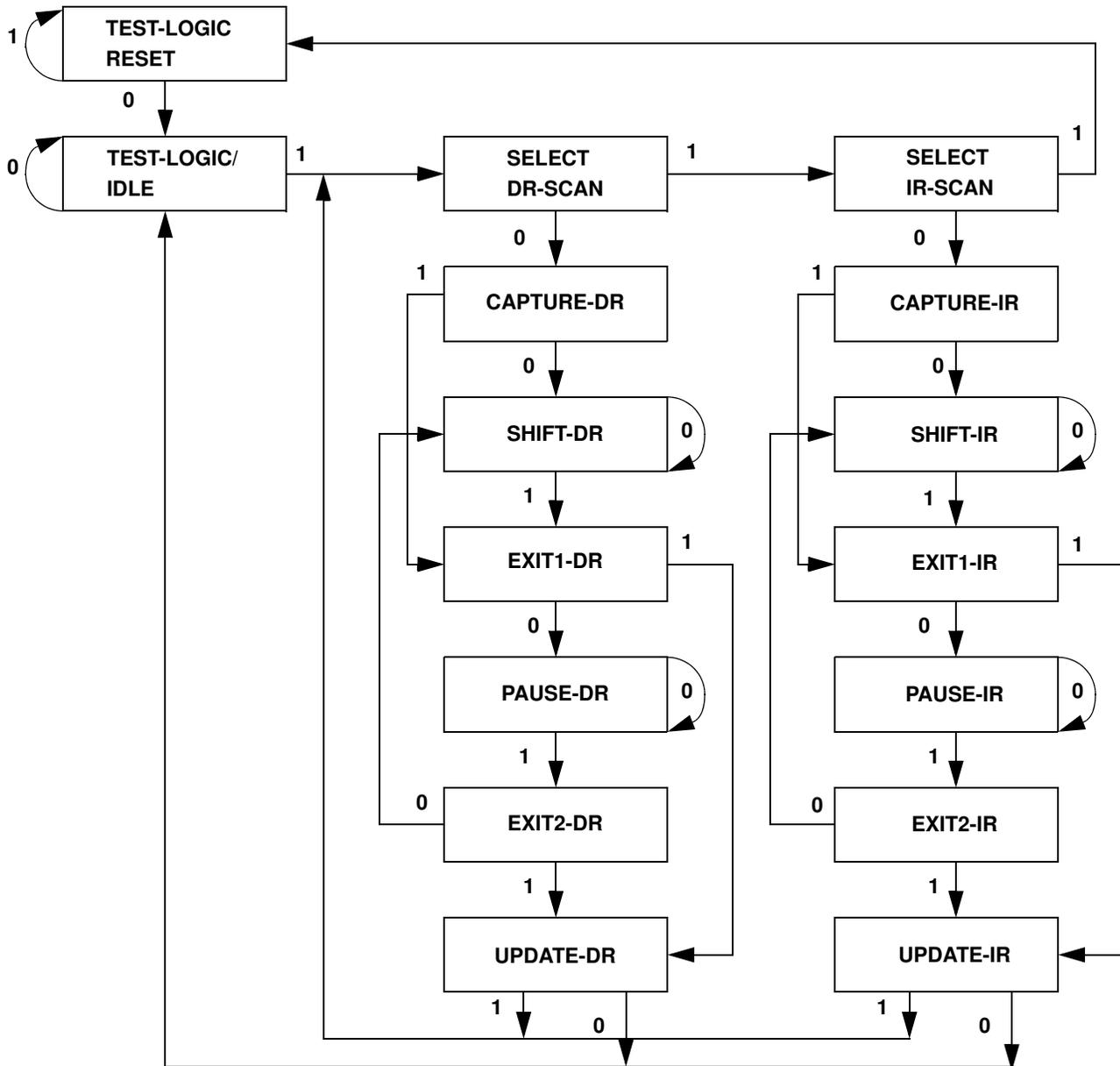
This bit is set by entering the SAMPLE/PRELOAD or EXTEST command, and then shifting the desired bit into that cell, during the Shift-DR state. During Update-DR, the value loaded into that shift-register cell latches into the preload register. When the EXTEST instruction is entered, this bit directly controls the output Q-bus pins. Note that this bit is pre-set LOW to enable the output when the device is powered up, and also when the TAP controller is in the Test-Logic-Reset state.

#### *Reserved*

These instructions are not implemented but are reserved for future use. Do not use these instructions.

## TAP Controller State Diagram

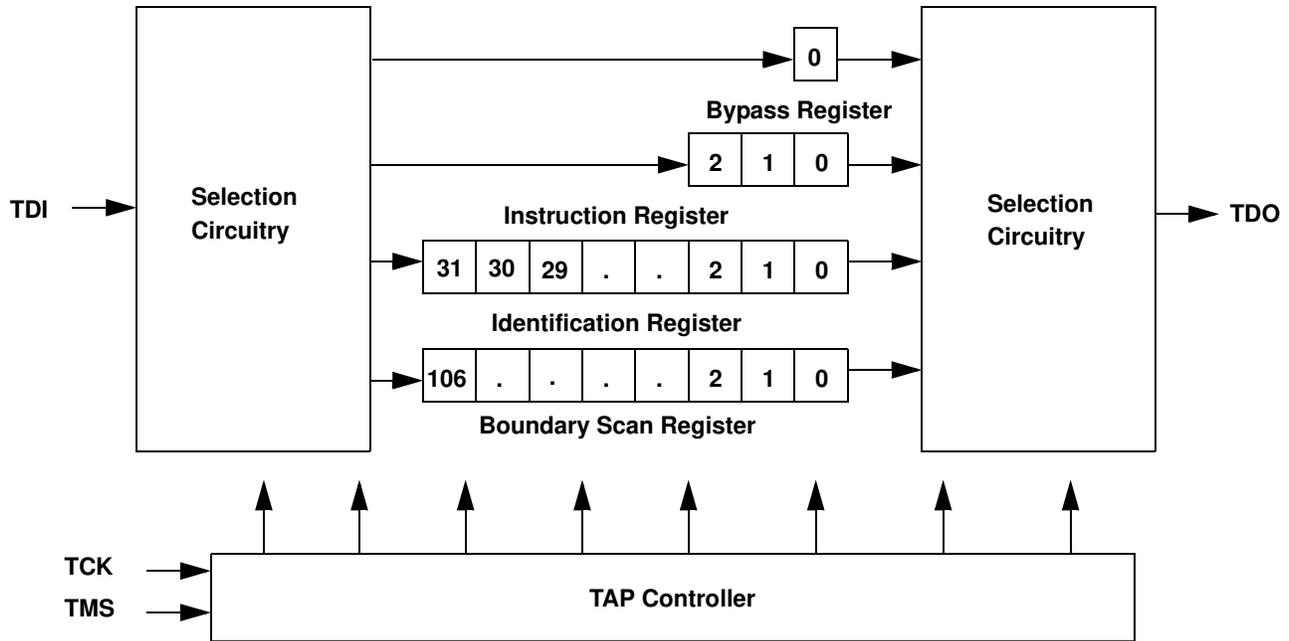
The state diagram for the TAP controller follows. <sup>[9]</sup>



**Note**

9. The 0/1 next to each state represents the value at TMS at the rising edge of TCK.

### TAP Controller Block Diagram



### TAP Electrical Characteristics

Over the Operating Range [10, 11, 12]

Parameter	Description	Test Conditions	Min	Max	Unit
V <sub>OH1</sub>	Output HIGH Voltage	I <sub>OH</sub> = -2.0 mA	1.4		V
V <sub>OH2</sub>	Output HIGH Voltage	I <sub>OH</sub> = -100 μA	1.6		V
V <sub>OL1</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.0 mA		0.4	V
V <sub>OL2</sub>	Output LOW Voltage	I <sub>OL</sub> = 100 μA		0.2	V
V <sub>IH</sub>	Input HIGH Voltage		0.65V <sub>DD</sub>	V <sub>DD</sub> + 0.3	V
V <sub>IL</sub>	Input LOW Voltage		-0.3	0.35V <sub>DD</sub>	V
I <sub>X</sub>	Input and Output Load Current	GND ≤ V <sub>I</sub> ≤ V <sub>DD</sub>	-5	5	μA

#### Notes

10. These characteristics pertain to the TAP inputs (TMS, TCK, TDI and TDO). Parallel load levels are specified in the [Electrical Characteristics](#) table.
11. Overshoot: V<sub>IH(AC)</sub> < V<sub>DDQ</sub> + 0.85V (Pulse width less than t<sub>CYC/2</sub>), Undershoot: V<sub>IL(AC)</sub> > -1.5V (Pulse width less than t<sub>CYC/2</sub>).
12. All Voltage referenced to Ground.

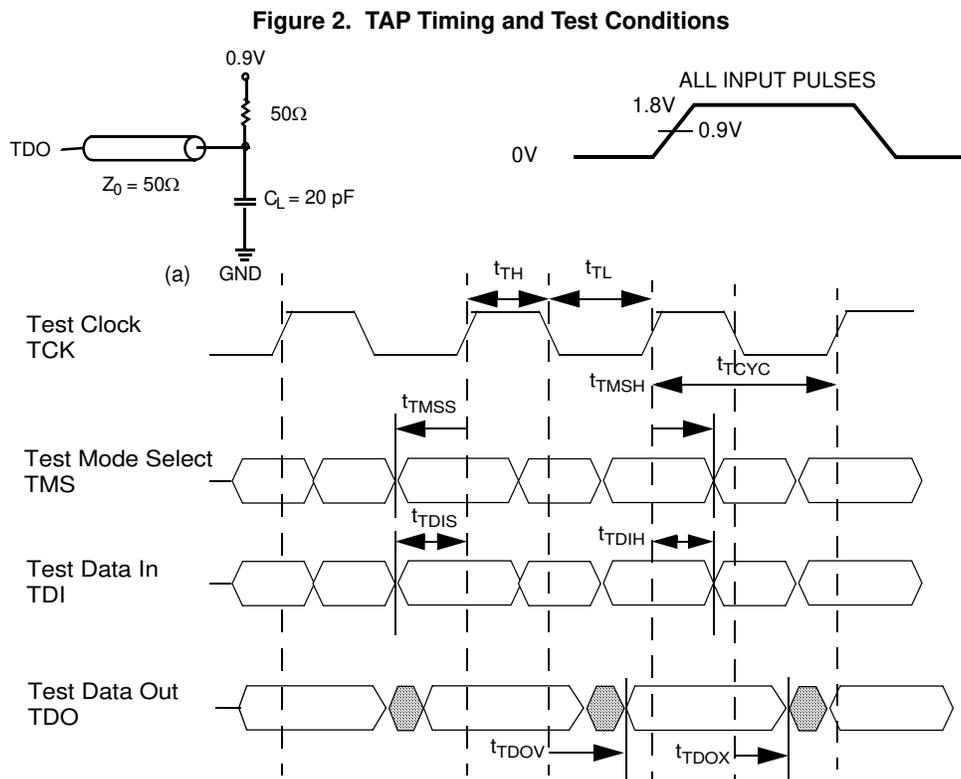
## TAP AC Switching Characteristics

Over the Operating Range [13, 14]

Parameter	Description	Min	Max	Unit
$t_{TCYC}$	TCK Clock Cycle Time	50		ns
$t_{TF}$	TCK Clock Frequency		20	MHz
$t_{TH}$	TCK Clock HIGH	20		ns
$t_{TL}$	TCK Clock LOW	20		ns
<b>Setup Times</b>				
$t_{TMSS}$	TMS Setup to TCK Clock Rise	5		ns
$t_{TDIS}$	TDI Setup to TCK Clock Rise	5		ns
$t_{CS}$	Capture Setup to TCK Rise	5		ns
<b>Hold Times</b>				
$t_{TMSH}$	TMS Hold after TCK Clock Rise	5		ns
$t_{TDIH}$	TDI Hold after Clock Rise	5		ns
$t_{CH}$	Capture Hold after Clock Rise	5		ns
<b>Output Times</b>				
$t_{TDOV}$	TCK Clock LOW to TDO Valid		10	ns
$t_{TDOX}$	TCK Clock LOW to TDO Invalid	0		ns

## TAP Timing and Test Conditions

Figure 2 shows the TAP timing and test conditions. [14]



### Notes

13.  $t_{CS}$  and  $t_{CH}$  refer to the setup and hold time requirements of latching data from the boundary scan register.
14. Test conditions are specified using the load in TAP AC Test Conditions.  $t_R/t_F = 1\text{ ns}$ .

### Identification Register Definitions

Instruction Field	Value		Description
	CY7C1393JV18	CY7C1394JV18	
Revision Number (31:29)	000	000	Version number.
Cypress Device ID (28:12)	11010100010010101	11010100010100101	Defines the type of SRAM.
Cypress JEDEC ID (11:1)	00000110100	00000110100	Allows unique identification of SRAM vendor.
ID Register Presence (0)	1	1	Indicates the presence of an ID register.

### Scan Register Sizes

Register Name	Bit Size
Instruction	3
Bypass	1
ID	32
Boundary Scan	107

### Instruction Codes

Instruction	Code	Description
EXTEST	000	Captures the input and output ring contents.
IDCODE	001	Loads the ID register with the vendor ID code and places the register between TDI and TDO. This operation does not affect SRAM operation.
SAMPLE Z	010	Captures the input and output contents. Places the boundary scan register between TDI and TDO. Forces all SRAM output drivers to a High Z state.
RESERVED	011	Do Not Use: This instruction is reserved for future use.
SAMPLE/PRELOAD	100	Captures the input and output ring contents. Places the boundary scan register between TDI and TDO. Does not affect the SRAM operation.
RESERVED	101	Do Not Use: This instruction is reserved for future use.
RESERVED	110	Do Not Use: This instruction is reserved for future use.
BYPASS	111	Places the bypass register between TDI and TDO. This operation does not affect SRAM operation.

**Boundary Scan Order**

Bit #	Bump ID
0	6R
1	6P
2	6N
3	7P
4	7N
5	7R
6	8R
7	8P
8	9R
9	11P
10	10P
11	10N
12	9P
13	10M
14	11N
15	9M
16	9N
17	11L
18	11M
19	9L
20	10L
21	11K
22	10K
23	9J
24	9K
25	10J
26	11J
27	11H

Bit #	Bump ID
28	10G
29	9G
30	11F
31	11G
32	9F
33	10F
34	11E
35	10E
36	10D
37	9E
38	10C
39	11D
40	9C
41	9D
42	11B
43	11C
44	9B
45	10B
46	11A
47	Internal
48	9A
49	8B
50	7C
51	6C
52	8A
53	7A
54	7B
55	6B

Bit #	Bump ID
56	6A
57	5B
58	5A
59	4A
60	5C
61	4B
62	3A
63	1H
64	1A
65	2B
66	3B
67	1C
68	1B
69	3D
70	3C
71	1D
72	2C
73	3E
74	2D
75	2E
76	1E
77	2F
78	3F
79	1G
80	1F
81	3G
82	2G
83	1J

Bit #	Bump ID
84	2J
85	3K
86	3J
87	2K
88	1K
89	2L
90	3L
91	1M
92	1L
93	3N
94	3M
95	1N
96	2M
97	3P
98	2N
99	2P
100	1P
101	3R
102	4R
103	4P
104	5P
105	5N
106	5R

## Power Up Sequence in DDR II SRAM

Power up and initialize DDR II SRAMs in a predefined manner to prevent undefined operations.

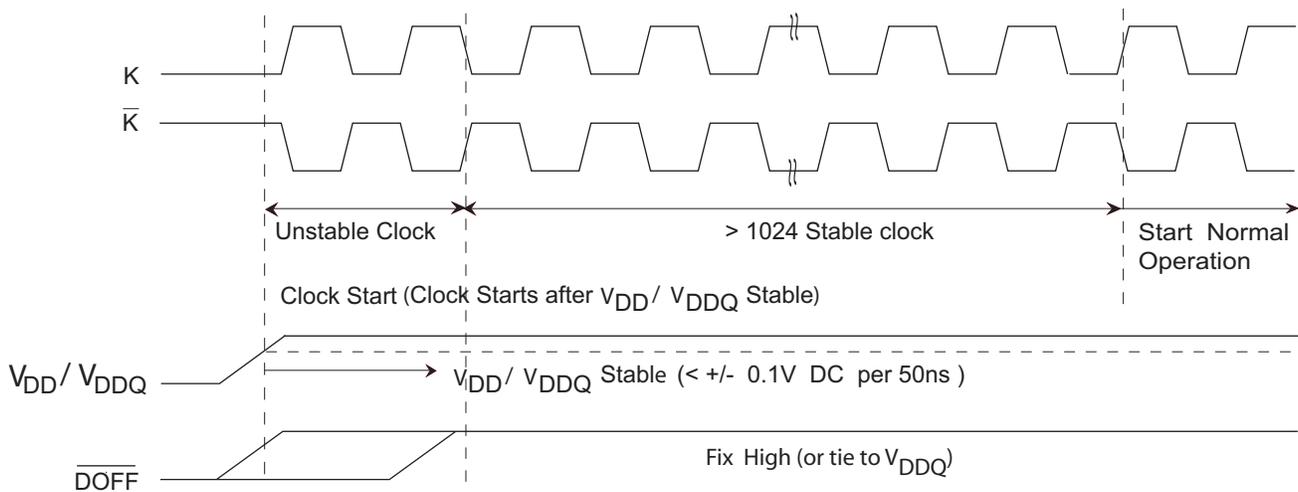
### Power Up Sequence

- Apply power and drive  $\overline{\text{DOFF}}$  either HIGH or LOW (All other inputs are HIGH or LOW).
  - Apply  $V_{\text{DD}}$  before  $V_{\text{DDQ}}$ .
  - Apply  $V_{\text{DDQ}}$  before  $V_{\text{REF}}$  or at the same time as  $V_{\text{REF}}$ .
  - Drive  $\overline{\text{DOFF}}$  HIGH.
- Provide stable  $\overline{\text{DOFF}}$  (HIGH), power and clock ( $K, \bar{K}$ ) for 1024 cycles to lock the DLL.

### DLL Constraints

- DLL uses K clock as its synchronizing input. The input has low phase jitter, which is specified as  $t_{\text{KC var}}$ .
- The DLL functions at frequencies down to 120 MHz.
- If the input clock is unstable and the DLL is enabled, then the DLL may lock onto an incorrect frequency, causing unstable SRAM behavior. To avoid this, provide 1024 cycles stable clock to relock to the desired clock frequency.

**Figure 3. Power Up Waveforms**



## Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... -65°C to +150°C  
 Ambient Temperature with Power Applied.. -55°C to +125°C  
 Supply Voltage on V<sub>DD</sub> Relative to GND.....-0.5V to +2.9V  
 Supply Voltage on V<sub>DDQ</sub> Relative to GND.....-0.5V to +V<sub>DD</sub>  
 DC Applied to Outputs in High Z ..... -0.5V to V<sub>DDQ</sub> + 0.3V  
 DC Input Voltage <sup>[11]</sup>..... -0.5V to V<sub>DD</sub> + 0.3V  
 Current into Outputs (LOW)..... 20 mA  
 Static Discharge Voltage (MIL-STD-883, M. 3015).. > 2001V  
 Latch-up Current..... > 200 mA

## Operating Range

Range	Ambient Temperature (T <sub>A</sub> )	V <sub>DD</sub> <sup>[15]</sup>	V <sub>DDQ</sub> <sup>[15]</sup>
Commercial	0°C to +70°C	1.8 ± 0.1V	1.4V to V <sub>DD</sub>
Industrial	-40°C to +85°C		

## Electrical Characteristics

### DC Electrical Characteristics

Over the Operating Range <sup>[12]</sup>

Parameter	Description	Test Conditions	Min	Typ	Max	Unit	
V <sub>DD</sub>	Power Supply Voltage		1.7	1.8	1.9	V	
V <sub>DDQ</sub>	IO Supply Voltage		1.4	1.5	V <sub>DD</sub>	V	
V <sub>OH</sub>	Output HIGH Voltage	Note 16	V <sub>DDQ</sub> /2 - 0.12		V <sub>DDQ</sub> /2 + 0.12	V	
V <sub>OL</sub>	Output LOW Voltage	Note 17	V <sub>DDQ</sub> /2 - 0.12		V <sub>DDQ</sub> /2 + 0.12	V	
V <sub>OH(LOW)</sub>	Output HIGH Voltage	I <sub>OH</sub> = -0.1 mA, Nominal Impedance	V <sub>DDQ</sub> - 0.2		V <sub>DDQ</sub>	V	
V <sub>OL(LOW)</sub>	Output LOW Voltage	I <sub>OL</sub> = 0.1 mA, Nominal Impedance	V <sub>SS</sub>		0.2	V	
V <sub>IH</sub>	Input HIGH Voltage		V <sub>REF</sub> + 0.1		V <sub>DDQ</sub> + 0.3	V	
V <sub>IL</sub>	Input LOW Voltage		-0.3		V <sub>REF</sub> - 0.1	V	
I <sub>X</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub>	-5		5	μA	
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>DDQ</sub> , Output Disabled	-5		5	μA	
V <sub>REF</sub>	Input Reference Voltage <sup>[18]</sup>	Typical Value = 0.75V	0.68	0.75	0.95	V	
I <sub>DD</sub> <sup>[19]</sup>	V <sub>DD</sub> Operating Supply	V <sub>DD</sub> = Max, I <sub>OUT</sub> = 0 mA, f = f <sub>MAX</sub> = 1/t <sub>CYC</sub>	300 MHz	(x18)		865	mA
				(x36)		935	
			250 MHz	(x18)		725	
				(x36)		770	
I <sub>SB1</sub>	Automatic Power down Current	Max V <sub>DD</sub> , Both Ports Deselected, V <sub>IN</sub> ≥ V <sub>IH</sub> or V <sub>IN</sub> ≤ V <sub>IL</sub> f = f <sub>MAX</sub> = 1/t <sub>CYC</sub> , Inputs Static	300 MHz	(x18)		285	mA
				(x36)		300	
			250 MHz	(x18)		260	
				(x36)		275	

### Notes

15. Power up: assumes a linear ramp from 0V to V<sub>DD</sub>(min) within 200 ms. During this time V<sub>IH</sub> < V<sub>DD</sub> and V<sub>DDQ</sub> ≤ V<sub>DD</sub>.
16. Outputs are impedance controlled. I<sub>OH</sub> = -(V<sub>DDQ</sub>/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
17. Outputs are impedance controlled. I<sub>OL</sub> = (V<sub>DDQ</sub>/2)/(RQ/5) for values of 175Ω ≤ RQ ≤ 350Ω.
18. V<sub>REF</sub>(min) = 0.68V or 0.46V<sub>DDQ</sub>, whichever is larger, V<sub>REF</sub>(max) = 0.95V or 0.54V<sub>DDQ</sub>, whichever is smaller.
19. The operation current is calculated with 50% read cycle and 50% write cycle.

## Neutron Soft Error Immunity

Parameter	Description	Test Conditions	Typ	Max*	Unit
LSBU	Logical Single-Bit Upsets	25°C	320	368	FIT/Mb
LMBU	Logical Multi-Bit Upsets	25°C	0	0.01	FIT/Mb
SEL	Single Event Latchup	85°C	0	0.1	FIT/Dev

\* No LMBU or SEL events occurred during testing; this column represents a statistical  $\chi^2$ , 95% confidence limit calculation. For more details refer to Application Note AN 54908 "Accelerated Neutron SER Testing and Calculation of Terrestrial Failure Rates"

### AC Electrical Characteristics

Over the Operating Range <sup>[11]</sup>

Parameter	Description	Test Conditions	Min	Typ	Max	Unit
V <sub>IH</sub>	Input HIGH Voltage		V <sub>REF</sub> + 0.2	–	–	V
V <sub>IL</sub>	Input LOW Voltage		–	–	V <sub>REF</sub> – 0.2	V

### Capacitance

Tested initially and after any design or process change that may affect these parameters.

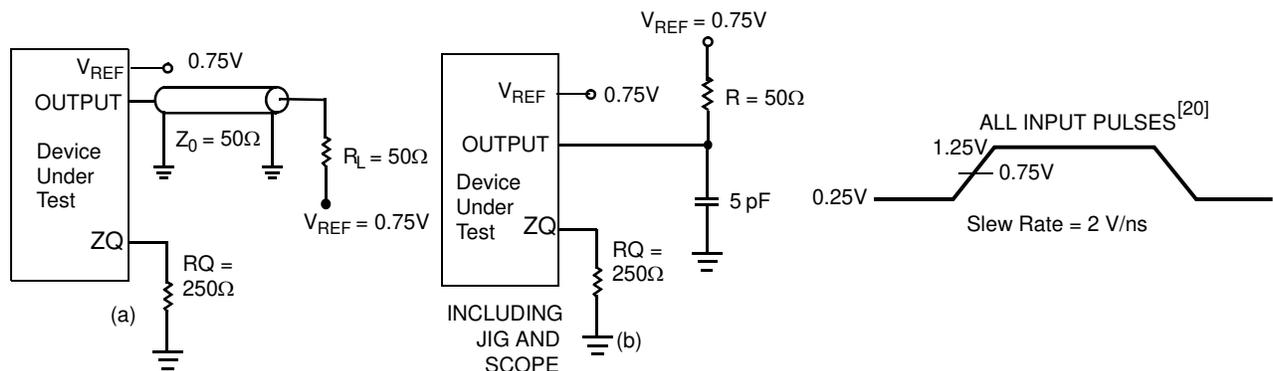
Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>DD</sub> = 1.8V, V <sub>DDQ</sub> = 1.5V	5	pF
C <sub>CLK</sub>	Clock Input Capacitance		6	pF
C <sub>O</sub>	Output Capacitance		7	pF

### Thermal Resistance

Tested initially and after any design or process change that may affect these parameters.

Parameter	Description	Test Conditions	165 FBGA Package	Unit
θ <sub>JA</sub>	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	18.7	°C/W
θ <sub>JC</sub>	Thermal Resistance (Junction to Case)		4.5	°C/W

**Figure 4. AC Test Loads and Waveforms**



**Note**

20. Unless otherwise noted, test conditions are based on signal transition time of 2V/ns, timing reference levels of 0.75V, V<sub>ref</sub> = 0.75V, R<sub>Q</sub> = 250Ω, V<sub>DDQ</sub> = 1.5V, input pulse levels of 0.25V to 1.25V, and output loading of the specified I<sub>OL</sub>/I<sub>OH</sub> and load capacitance shown in (a) of AC Test Loads and Waveforms.

## Switching Characteristics

Over the Operating Range [20, 21]

Cypress Parameter	Consortium Parameter	Description	300 MHz		250 MHz		Unit
			Min	Max	Min	Max	
t <sub>POWER</sub>		V <sub>DD</sub> (Typical) to the First Access [22]	1		1		ms
t <sub>CYC</sub>	t <sub>KHKH</sub>	K Clock and C Clock Cycle Time	3.3	8.4	4.0	8.4	ns
t <sub>KH</sub>	t <sub>KHKL</sub>	Input Clock (K/ $\bar{K}$ ; C/ $\bar{C}$ ) HIGH	1.32	–	1.6	–	ns
t <sub>KL</sub>	t <sub>KLKH</sub>	Input Clock (K/ $\bar{K}$ ; C/ $\bar{C}$ ) LOW	1.32	–	1.6	–	ns
t <sub>KH<math>\bar{K}</math>H</sub>	t <sub>KH<math>\bar{K}</math>H</sub>	K Clock Rise to $\bar{K}$ Clock Rise and C to $\bar{C}$ Rise (rising edge to rising edge)	1.49	–	1.8	–	ns
t <sub>KHCH</sub>	t <sub>KHCH</sub>	K/ $\bar{K}$ Clock Rise to C/ $\bar{C}$ Clock Rise (rising edge to rising edge)	0	1.45	0	1.8	ns
<b>Setup Times</b>							
t <sub>SA</sub>	t <sub>AVKH</sub>	Address Setup to K Clock Rise	0.4	–	0.5	–	ns
t <sub>SC</sub>	t <sub>IVKH</sub>	Control Setup to K Clock Rise ( $\bar{LD}$ , R/ $\bar{W}$ )	0.4	–	0.5	–	ns
t <sub>SCDDR</sub>	t <sub>IVKH</sub>	Double Data Rate Control Setup to Clock (K/ $\bar{K}$ ) Rise ( $\bar{BWS}_0$ , $\bar{BWS}_1$ , $\bar{BWS}_2$ , $\bar{BWS}_3$ )	0.3	–	0.35	–	ns
t <sub>SD</sub>	t <sub>DVKH</sub>	D <sub>[X:0]</sub> Setup to Clock (K/ $\bar{K}$ ) Rise	0.3	–	0.35	–	ns
<b>Hold Times</b>							
t <sub>HA</sub>	t <sub>KHAX</sub>	Address Hold after K Clock Rise	0.4	–	0.5	–	ns
t <sub>HC</sub>	t <sub>KHIX</sub>	Control Hold after K Clock Rise ( $\bar{LD}$ , R/ $\bar{W}$ )	0.4	–	0.5	–	ns
t <sub>HCDDR</sub>	t <sub>KHIX</sub>	Double Data Rate Control Hold after Clock (K/ $\bar{K}$ ) Rise ( $\bar{BWS}_0$ , $\bar{BWS}_1$ , $\bar{BWS}_2$ , $\bar{BWS}_3$ )	0.3	–	0.35	–	ns
t <sub>HD</sub>	t <sub>KHDX</sub>	D <sub>[X:0]</sub> Hold after Clock (K/ $\bar{K}$ ) Rise	0.3	–	0.35	–	ns
<b>Output Times</b>							
t <sub>CO</sub>	t <sub>CHQV</sub>	C/ $\bar{C}$ Clock Rise (or K/ $\bar{K}$ in single clock mode) to Data Valid	–	0.45	–	0.45	ns
t <sub>DOH</sub>	t <sub>CHQX</sub>	Data Output Hold after Output C/ $\bar{C}$ Clock Rise (Active to Active)	–0.45	–	–0.45	–	ns
t <sub>CCQO</sub>	t <sub>CHCQV</sub>	C/ $\bar{C}$ Clock Rise to Echo Clock Valid	–	0.45	–	0.45	ns
t <sub>CQOH</sub>	t <sub>CHCQX</sub>	Echo Clock Hold after C/ $\bar{C}$ Clock Rise	–0.45	–	–0.45	–	ns
t <sub>CQD</sub>	t <sub>CQHCV</sub>	Echo Clock High to Data Valid		0.27		0.30	ns
t <sub>CQDOH</sub>	t <sub>CQHCV</sub>	Echo Clock High to Data Invalid	–0.27	–	–0.30	–	ns
t <sub>CQH</sub>	t <sub>CQHCQL</sub>	Output Clock (CQ/ $\bar{CQ}$ ) HIGH [23]	1.24	–	1.55	–	ns
t <sub>CQH<math>\bar{CQ}</math>H</sub>	t <sub>CQH<math>\bar{CQ}</math>H</sub>	CQ Clock Rise to $\bar{CQ}$ Clock Rise (rising edge to rising edge) [23]	1.24	–	1.55	–	ns
t <sub>CHZ</sub>	t <sub>CHQZ</sub>	Clock (C/ $\bar{C}$ ) Rise to High Z (Active to High Z) [24, 25]	–	0.45	–	0.45	ns
t <sub>CLZ</sub>	t <sub>CHQX1</sub>	Clock (C/ $\bar{C}$ ) Rise to Low Z [24, 25]	–0.45	–	–0.45	–	ns
<b>DLL Timing</b>							
t <sub>KC Var</sub>	t <sub>KC Var</sub>	Clock Phase Jitter	–	0.20	–	0.20	ns
t <sub>KC lock</sub>	t <sub>KC lock</sub>	DLL Lock Time (K, C)	1024	–	1024	–	Cycles
t <sub>KC Reset</sub>	t <sub>KC Reset</sub>	K Static to DLL Reset	30		30		ns

### Notes

21. When a part with a maximum frequency above 250 MHz is operating at a lower clock frequency, it requires the input timing of the frequency range in which it is being operated and outputs data with the output timings of that frequency range.
22. This part has a voltage regulator internally; t<sub>POWER</sub> is the time that the power must be supplied above V<sub>DD</sub> minimum initially before a read or write operation can be initiated.
23. These parameters are extrapolated from the input timing parameters (t<sub>KH $\bar{K}$ H</sub> - 250 ps, where 250 ps is the internal jitter. An input jitter of 200 ps (t<sub>KC Var</sub>) is already included in the t<sub>KH $\bar{K}$ H</sub>). These parameters are only guaranteed by design and are not tested in production
24. t<sub>CHZ</sub>, t<sub>CLZ</sub>, are specified with a load capacitance of 5 pF as in (b) of [AC Test Loads and Waveforms](#) on page 19. Transition is measured ± 100 mV from steady-state voltage.
25. At any voltage and temperature t<sub>CHZ</sub> is less than t<sub>CLZ</sub> and t<sub>CHZ</sub> less than t<sub>CO</sub>.



## Ordering Information

The table below contains only the parts that are currently available. If you don't see what you are looking for, please contact your local sales representative. For more information, visit the Cypress website at [www.cypress.com](http://www.cypress.com) and refer to the product summary page at <http://www.cypress.com/products>

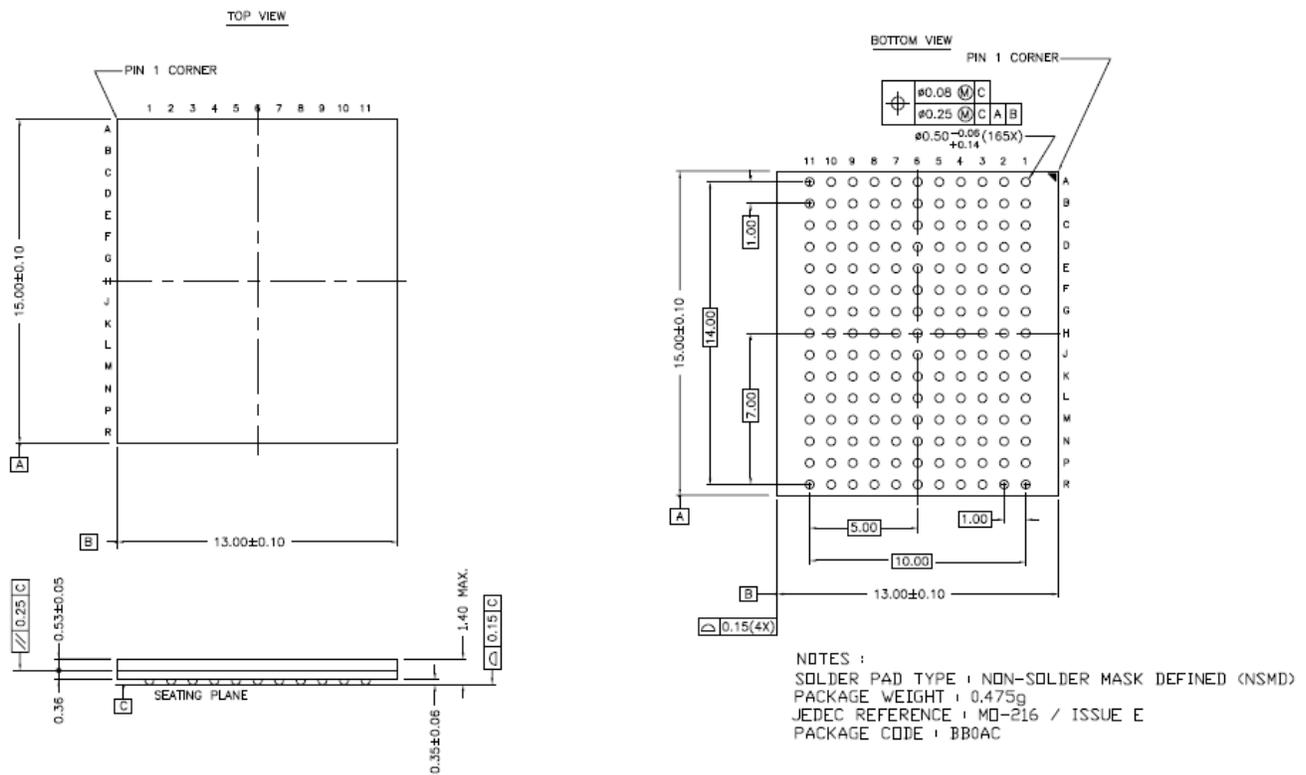
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**Table 1. Ordering Information**

Speed (MHz)	Ordering Code	Package Diagram	Package Type	Operating Range
300	CY7C1393JV18-300BZXC	51-85180	165-Ball Fine Pitch Ball Grid Array (13 x 15 x 1.4 mm) Pb-Free	Commercial

## Package Diagram

**Figure 6. 165-Ball FBGA (13 x 15 x 1.4 mm)**



51-85180 \*B

## Document History Page

Document Title: CY7C1393JV18/CY7C1394JV18, 18 Mbit DDR II SIO SRAM Two Word Burst Architecture				
Document Number: 001-44698				
Revision	ECN	Orig. of Change	Submission Date	Description of Change
**	2192568	VKN/PYRS	See ECN	New datasheet
*A	2561974	VKN/PYRS	09/04/08	Converted from preliminary to final, Added 250 MHz speed bin, Changed JTAG ID [31:29] from 001 to 000, Updated power up sequence waveform and its description, Changed Ambient Temperature with Power Applied from “-10°C to +85°C” to “-55°C to +125°C” in the “Maximum Ratings “ on page 20, Changed $\Theta_{JA}$ and $\Theta_{JC}$ from 28.51 and 5.91 °C/W to 18.7 and 4.5 °C/W respectively.
*B	2748221	NJY	08/04/09	Updated package diagram Post to external web
*C	2755901	VKN	08/25/09	Removed x8 and x9 part number details Included Soft Error Immunity Data Modified Ordering Information table by including parts that are available and modified the disclaimer for the Ordering information. Updated Package Diagram.

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