Product Document

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Datasheet

DS001021

Mira030

0.3MP Global Shutter CMOS Image Sensor

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Abstract

This datasheet document describes the specification and functionalities of Mira030, a VGA (0.3 MP) global shutter CMOS image sensor.

Content Guide

1 General Description

Mira030 is a monochrome global shutter CMOS image sensor with a resolution of 640H × 480V. The sensor supports complex on-chip operations such as external trigger, windowing and horizontal or vertical mirroring. Its maximum frame rate is 180fps at a resolution of 640H × 480V. Registers of this chip are accessible via the standard I²C interface. External triggering is possible via the TRIG pin.

1.1 Key Benefits & Features

Figure 1:
Mira030 Key Benefits and Associated Features

Benefits	Features
High speed applications	180 fps at 10b full resolution
Motion blur robustness & low PLS	Global shutter pixel
Standard data interfaces	MIPI and LVDS
Standard control interface	I²C interface
Low power consumption	Max 120 mW at max frame rate

1.2 Applications

- Machine vision
- Barcode scanner
- Automotive
- Motion monitoring
- Miniature cameras

1.3 Block Diagram

The functional blocks of this device are shown in Figure 2. Mira030 supports the Mobile Industry Processor Interface (MIPI) and the Low Voltage Differential Signaling (LVDS) interface. Also a typical configuration is depicted in Figure 3.

Figure 2:
Functional Blocks of Mira030

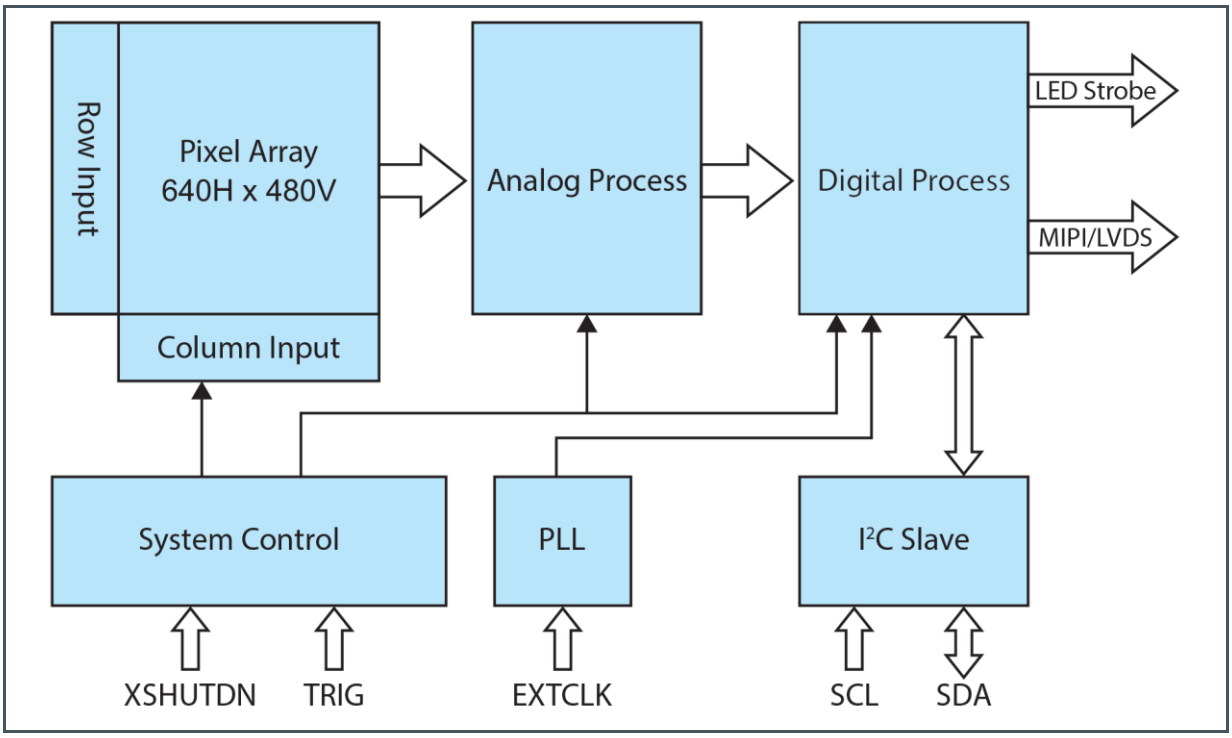
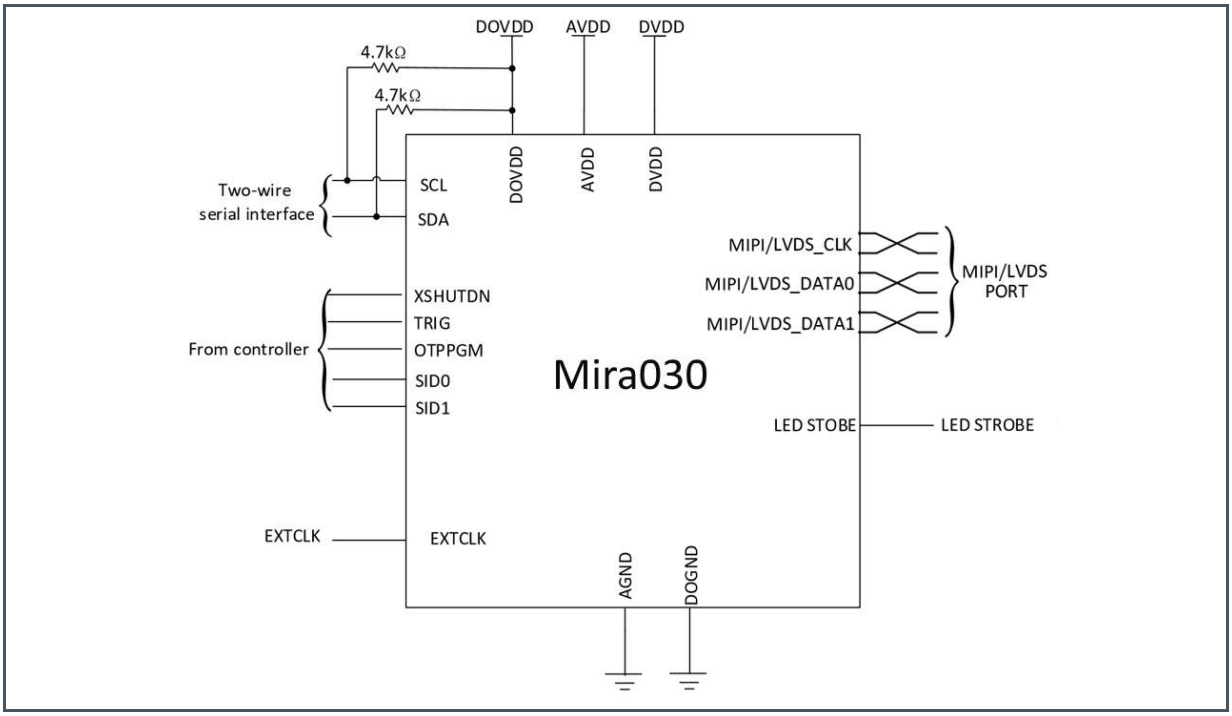


Figure 3:
Typical Configuration



2 Ordering Information

Figure 4:
Ordering Code

Ordering Code	Package	Delivery Form	Delivery Quantity
MIRA030-1RM2D0	RW	Cassette	10000
MIRA030-1RM2WP	CSP	Tray	10000

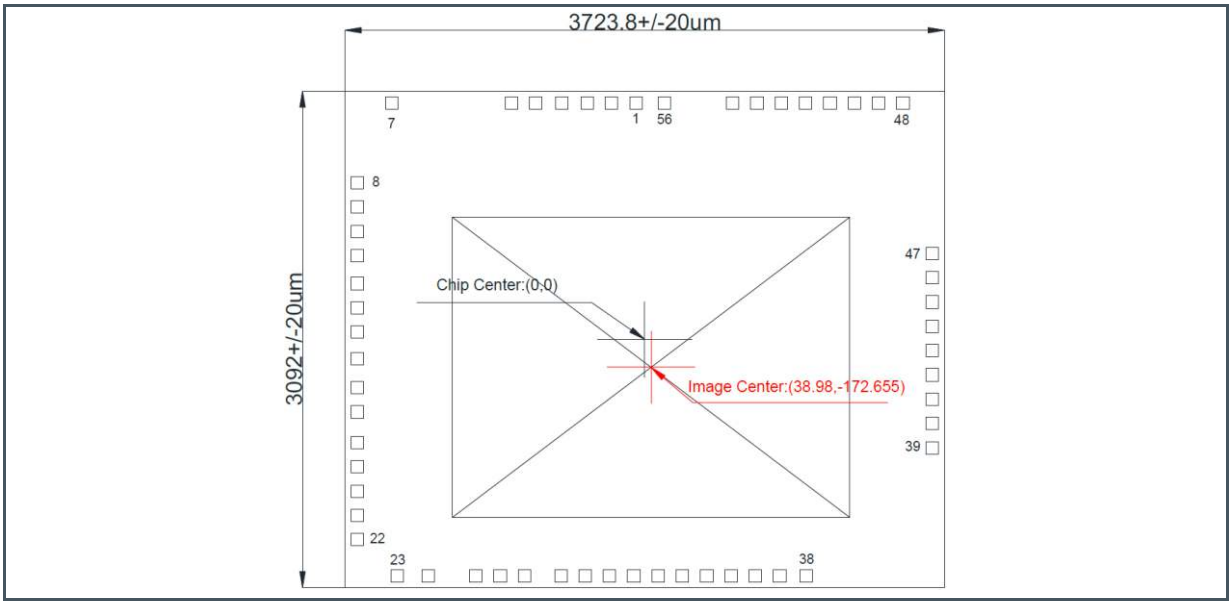
3 Pin Assignment

3.1 Reconstructed Wafer

3.1.1 Pin Diagram

The pin assignment is shown below.

Figure 5:
Mira030 RW Package Pin Assignment



3.1.2 Pin Description

The bonding area size of each pin in Figure 6 is 70.2 x 70.2.

Figure 6:
Mira030 Pin Description RW

Pad #	Pad Name	X-axis	Y-axis	Pin Type	Description
1	TRIG	-54.9	1462.05	Input	Trigger Signal, External Exposure Control
2	DOGND	-205.2	1462.05	GND	I/O GND
3	DVDD	-355.5	1462.05	Power	1.5V Digital Power
4	AVDD	-511.2	1462.05	Power	2.8V Analog Power

Pad #	Pad Name	X-axis	Y-axis	Pin Type	Description
5	AGND	-672.75	1462.05	GND	Analog Ground
6	FSYNC	-823.05	1462.05	Input	DVP Frame SYNC
7	OTPPGM	-1564.2	1462.05	Input	OTP burning voltage control pin (connect a 4.7kΩ resistor to the DGND pin)
8	DVDD	-1777.95	969.3	Power	1.5V Digital Power
9	DOGND	-1777.95	819	GND	I/O GND
10	LEDSTROBE	-1777.95	668.7	Output	LED STROBE Signal
11	SDA	-1777.95	518.4	Input/output	I^2C Data Line (open drain)
12	SCL	-1777.95	346.5	Input	I^2C Clock Line
13	EXTCLK	-1777.95	196.2	Input	Clock Input
14	LREF	-1777.95	45.9	Input	DVP Row SYNC
15	PCLK	-1777.95	-120.6	Input	DVP Clock
16	DOGND	-1777.95	-298.8	GND	I/O GND
17	DVDD	-1777.95	-449.1	Power	1.5V Digital power
18	D<0>	-1777.95	-637.65	Output	DVP Output bit[0]
19	D<1>	-1777.95	-787.95	Output	DVP Output bit[1]
20	DOVDD	-1777.95	-938.25	Power	1.8V I/O Power
21	D<2>	-1777.95	-1088.55	Output	DVP Output bit[2]
22	D<3>	-1777.95	-1238.85	Output	DVP Output bit[3]
23	DOVDD	-1528.2	-1462.05	Power	1.8V I/O Power
24	DOGND	-1339.2	-1462.05	GND	I/O GND
25	D<4>/MD0N	-1044	-1462.05	Output	DVP Output bit[4]/MIPI DATA 0 Negative
26	D<5>/MD0P	-893.7	-1462.05	Output	DVP Output bit[5]/MIPI DATA 0 Positive
27	DVDD	-743.4	-1462.05	Power	1.5V Digital Power
28	D<6>/MCN	-518.4	-1462.05	Output	DVP Output bit[6]/MIPI Clock Negative
29	D<7>/MCP	-368.1	-1462.05	Output	DVP Output bit[7]/MIPI Clock Positive
30	DOGND	-217.8	-1462.05	GND	I/O GND
31	D<8>/MD1N	-67.5	-1462.05	Output	DVP Output bit[8]/MIPI DATA 1 Negative
32	D<9>/MD1P	82.8	-1462.05	Output	DVP Output bit[9]/MIPI DATA 1 Positive
33	DOVDD	233.1	-1462.05	Power	1.8V I/O Power
34	D<10>	383.4	-1462.05	Output	DVP Output bit[10]
35	D<11>	533.7	-1462.05	Output	DVP Output bit[11]
36	DOGND	684	-1462.05	GND	I/O GND
37	AGND	834.3	-1462.05	GND	Analog Ground
38	AVDD	997.2	-1462.05	Power	2.8V Analog Power
39	TXVDD	1777.95	-670.5	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
40	VREFH	1777.95	-520.2	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
41	VREFN	1777.95	-369.9	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)

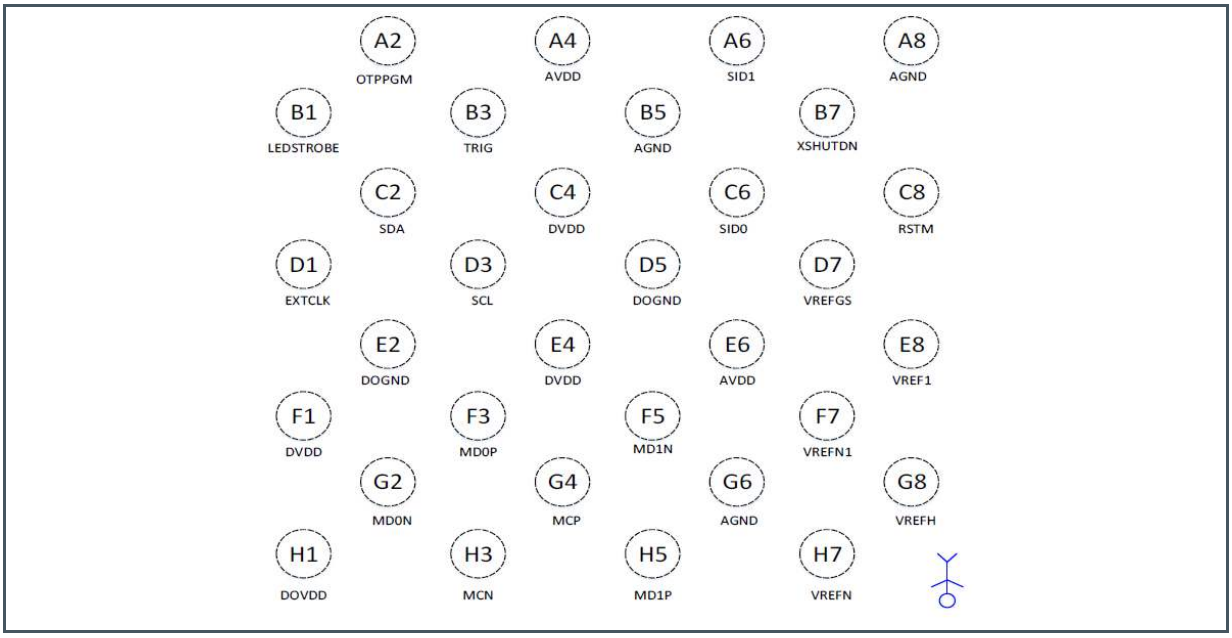
Pad #	Pad Name	X-axis	Y-axis	Pin Type	Description
42	VREFN1	1777.95	-219.6	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
43	VREF1	1777.95	-69.3	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
44	AVDD	1777.95	81	Power	2.8V Analog Power
45	GS_VREF	1777.95	231.3	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
46	RST_M	1777.95	381.6	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
47	AGND	1777.95	531.9	GND	Analog Ground
48	AGND	1595.7	1462.05	GND	Analog Ground
49	AVDD	1445.4	1462.05	Power	2.8V Analog Power
50	ATM	1295.1	1462.05	NC	Test
51	XSHUTDN	1144.8	1462.05	Input	XSHUTDN Signal Input (internal pull-up, active low)
52	DOGND	994.5	1462.05	GND	I/O GND
53	SID0	844.2	1462.05	Input	I^2C Device ID 0
54	SID1	693.9	1462.05	Input	I^2C Device ID 1
55	DVDD	543.6	1462.05	Power	1.5V Digital Power
56	TRIGS	119.7	1462.05	Input	Reserved

3.2 CSP Package

3.2.1 Pin Diagram

Figure 7 shows the top view of Mira030 package pin assignment for MIPI.

Figure 7:
Top View of Mira030 CSP Package Pin Assignment for MIPI



3.2.2 Pin Description

Figure 8:
Mira030 Pin Description CSP

No.	Pin No.	Pin Name	Pin Type	Description
1	A2	OTPPGM	Input	OTP burning voltage (connect a 4.7kΩ resistor to the DOGND pin)
2	A4	AVDD	Power	2.8V Analog Power Supply
3	A6	SID1	Input	I²C Device ID 1 (internal pull-down)
4	A8	AGND	GND	Analog Ground
5	B1	LEDSTROBE	Output	LED Strobe Signal
6	B3	TRIG	Input	External Trigger of Exposure
7	B5	AGND	GND	Analog Ground

No.	Pin No.	Pin Name	Pin Type	Description
8	B7	XSHUTDN	Input	Shutdown (internal pull-up, active low)
9	C2	SDA	Input/output	I²C Data Line (open drain)
10	C4	DVDD	Power	1.5V Digital Power Supply
11	C6	SID0	Input	I²C Device ID 0 (internal pull-down)
12	C8	RSTM	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
13	D1	EXTCLK	Input	Clock Input
14	D3	SCL	Input	I²C Clock
15	D5	DOGND	GND	I/O GND
16	D7	VREFGS	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
17	E2	DOGND	GND	I/O GND
18	E4	DVDD	Power	1.5V Digital Power Supply
19	E6	AVDD	Power	2.8V Analog Power Supply
20	E8	VREF1	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
21	F1	DVDD	Power	1.5V Digital Power Supply
22	F3	MD0P	Output	MIPI Data 0 Positive
23	F5	MD1N	Output	MIPI Data 1 Negative
24	F7	VREFN1	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
25	G2	MD0N	Output	MIPI Data 0 Negative
26	G4	MCP	Output	MIPI Clock Positive
27	G6	AGND	GND	Analog Ground
28	G8	VREFH	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)
29	H1	DOVDD	Power	1.8V I/O Power Supply
30	H3	MCN	Output	MIPI Clock Negative
31	H5	MD1P	Output	MIPI Data 1 Positive
32	H7	VREFN	Output	Internal Reference Voltage (connect an external capacitor to the AGND pin)

4 Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 9:
Absolute Maximum Ratings of Mira030

Symbol	Parameter	Min	Max	Unit	Comments
Electrical Parameters					
V_{AVDD}	Analog Supply Voltage	-0.3	3.4	V	
V_{DVDD}	Digital Supply Voltage	-0.3	1.8	V	
V_{DOVDD}	I/O Supply Voltage	-0.3	2.2	V	
	I/O Input Voltage	-0.3	V_{DOVDD} + 0.3	V	
	I/O Output Voltage	-0.3	V_{DOVDD} + 0.3	V	
I_{SCR}	Input Current (latch-up immunity)	± 100		mA	JEDEC JESD78D Nov 2011
Continuous Power Dissipation (T_A = 70 °C)					
P_T	Continuous Power Dissipation	120		mW	
Electrostatic Discharge					
ESD_{HBM}	Electrostatic Discharge HBM	± V>2		kV	MIL-STD-883J Method 3015.9
ESD_{CDM}	Electrostatic Discharge CDM	± V>250		V	ANSI/ESDA/JEDEC JS-002-2014
Temperature Ranges and Storage Conditions					
R_{THJA}	Junction to Ambient Thermal Resistance		40	°C/W	Reference Package Thermal Resistance value
T_A	Operating Ambient Temperature	-30	80	°C	
T_J	Operating Junction Temperature	-25	85	°C	
T_{SPEC}	Operating Temperature Spec	-20	60	°C	Best performance(1)
T_{STRG_CSP}	Storage Temperature CSP	-40	85	°C	
T_{STRG_WAF}	Storage Temperature Wafer	20	30	°C	
t_{STRG_CSP}	Storage Time CSP		12	months	
t_{STRG_WAF}	Storage Time Wafer		6	months	
RH_{NC_CSP}	Relative Humidity (non-condensing)	5	85	%	
RH_{NC_WAF}	Relative Humidity (non-condensing) Wafer		30	%	N2 Wafer Stocker condition(2)
MSL	Moisture Sensitivity Level		3		JESD22-A113F IPC-JEDEC_J-STD-020D

(1) Ideal temperature range for best performance.
(2) Die and wafers, when in storage, should be stored at temperature between 20°C and 30°C, relative humidity of less than 30%, and in clean, dry, inert atmosphere (e.g. Nitrogen) or in a vacuum sealed bag.

5 Electrical Characteristics

All limits are guaranteed. The parameters with Min and Max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

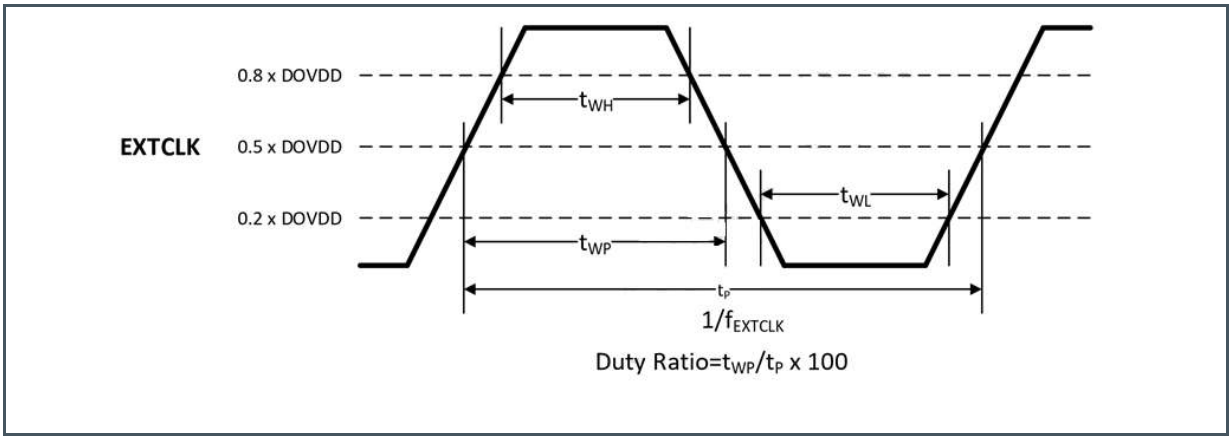
Figure 10:
DC Electrical Characteristics (MIPI mode: V_{AVDD} = 2.8V, V_{DOVDD} = 1.8V)

Symbol	Parameter	Min	Typ	Max	Unit
Power Supply					
V_{AVDD}	Analog supply voltage	2.7	2.8	2.9	V
V_{DVDD}	Digital supply voltage	1.4	1.5	1.6	V
V_{DOVDD}	I/O supply voltage	1.7	1.8	1.9	V
I_{AVDD}	Analog supply current	-	-	-	mA
I_{DVDD}	Digital supply current	-	-	-	mA
I_{DOVDD}	I/O supply current	-	-	-	mA
P_{tot}	Total power consumption (MIPI 2-lane, 180fps)	-	-	-	mW
Digital Input (Reference: AVDD = 2.8V, DOVDD = 1.8V)					
V_{IL}	Input low level	-	-	0.3 × V_{DOVDD}	V
V_{HL}	Input high level	0.7 × V_{DOVDD}	-	-	V
C_{IN}	Input capacitor	-	-	10	pF
Digital Output (25 pF standard load)					
V_{OH}	Output high level	0.9 × V_{DOVDD}	-	-	V
V_{OL}	Output low level	-	-	0.1 × V_{DOVDD}	V
Serial Interface Input (SCL and SDA)					
V_{IL}	Input low level	-0.5	0	0.3 × V_{DOVDD}	V
V_{HL}	Input high level	0.7 × V_{DOVDD}	V_{DOVDD}	V_{DOVDD} + 0.5	V

Figure 11:
AC Characteristics (T = 25°C, V_{AVDD} = 2.8V, V_{DOVDD} = 1.8V)

Symbol	Parameter	Min	Typ	Max	Unit
AC Parameters					
DLE	DC differential linearity deviation	-	< 1	-	LSB
ILE	DC integral linearity deviation	-	< 2	-	LSB
-	Soft reset settling time	-	-	1	ms
-	Resolution change settling time	-	-	1	ms
-	Register initialization time	-	-	300	ms
Crystal and Clock Input					
F_{EXTCLK}	Input clock frequency	6	-	27	MHz
t_{wh}	Input clock high pulse width	5	-	-	ns
t_{wl}	Input clock low pulse width	5	-	-	ns
-	Input clock duty cycle	45	50	55	%

Figure 12:
Input Clock Waveform



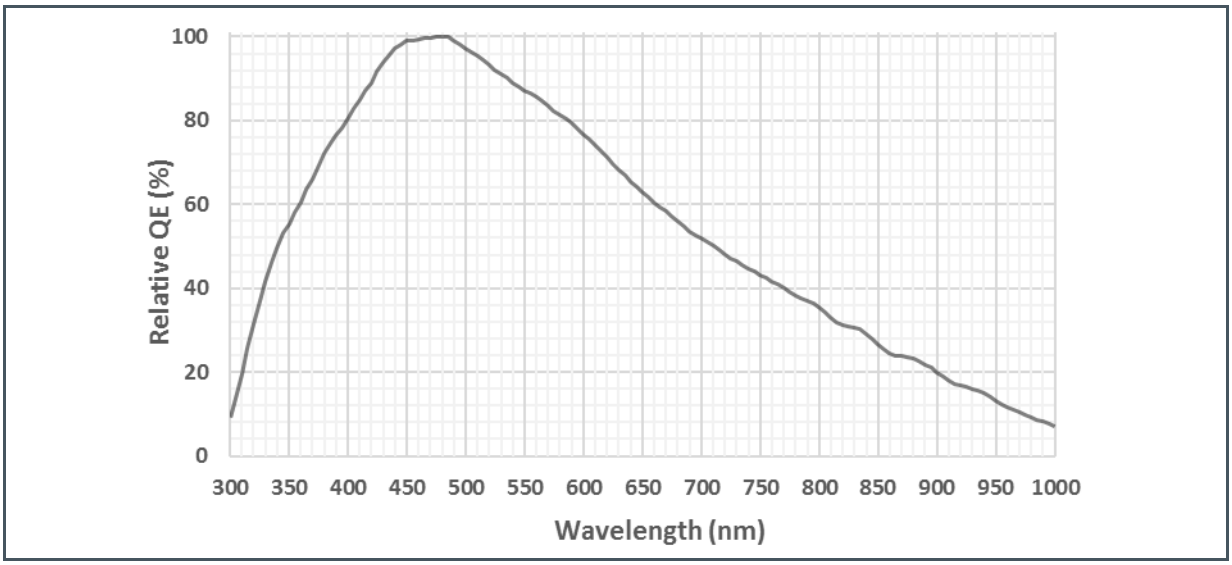
6 Electro-Optical Characteristics

Below are the typical electro-optical specifications of the Mira030, measured in typical conditions.

Figure 13:
Electro-Optical Characteristics of Mira030

Parameter	Value	Remark
Active pixels	640H × 480V	
Pixel size	3.744 x 3.744 µm² BSI	
Pixel type	Global Shutter	
Optical format	1/6”	
Full well charge	7 ke-	
Temporal noise	11 e-	
Dynamic range	56 dB	Normal mode
SNR	38 dB	SNR
Max Responsivity	6500 mV/lux*s	
Maximum frame rate	180 fps	640H × 480V @10-bit
Output interface	12/10/8-bit 1/2-lane MIPI 12/10/8-bit 1/2-lane LVDS	Output interface
Output format	RAW / MONO	
CRA	33°	
Package	32-pin CSP	
Package size	3.704 mm × 3.072 mm	

Figure 14:
Relative QE Measurement Curve of Mira030



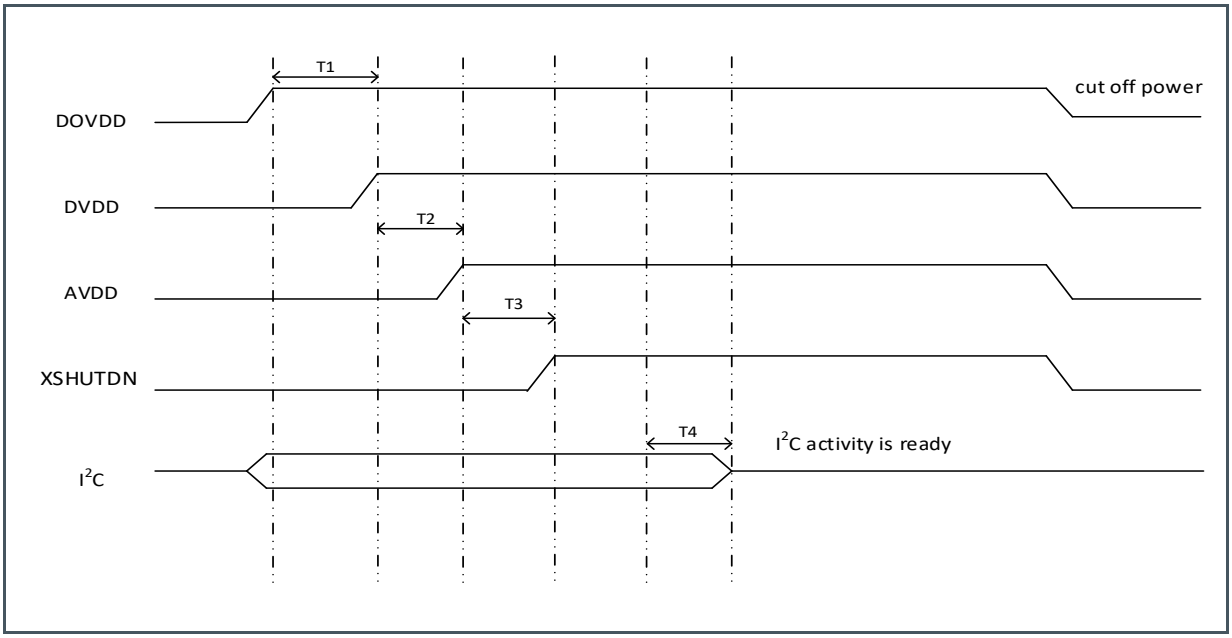
7 Functional Description

7.1 Chip Description

7.1.1 Power-On Sequence

With an external supply of 1.5V to DVDD, the following power-on sequence is required.

Figure 15:
Power-On Sequence



(1) T1 > 0 ms, T2 > 1 ms, T3 > 2 ms, T4 > 2 ms

7.1.2 Sleep Mode

Under sleep mode, this chip keeps registers unchanged. This chip offers two approaches to enter sleep mode:

1. Hardware approach: pull the XSHUTDN pin low, registers access through I²C is not supported.
2. Software approach: write 0 to register 16'h0100 [0], registers access through I²C access remains active.

Figure 16:
Sleep Mode Control Register

Address	Function	Default Value	Read/Write	Description
16'h0100	Manual sleep mode	1'b0	Read/Write	Bit [0]: manual sleep mode control 0: sleep mode enable 1: sleep mode disable

7.1.3 Reset Mode

During reset, this chip resets its registers to their default values. This chip enters reset mode by writing 1 to register 16'h0103[0].

Figure 17:
Soft Reset Control Register

Address	Function	Default Value	Read/Write	Description
16'h0103	Soft Reset	1'b0	Write	Bit [0]: soft reset

7.2 Configuration Interface

Registers of this chip can be read and written via the standard I²C interface. The device address of the I²C interface is determined by the SID0 and SID1 pins as shown in Figure 18.

Figure 18:
I²C Bus Device Address Control

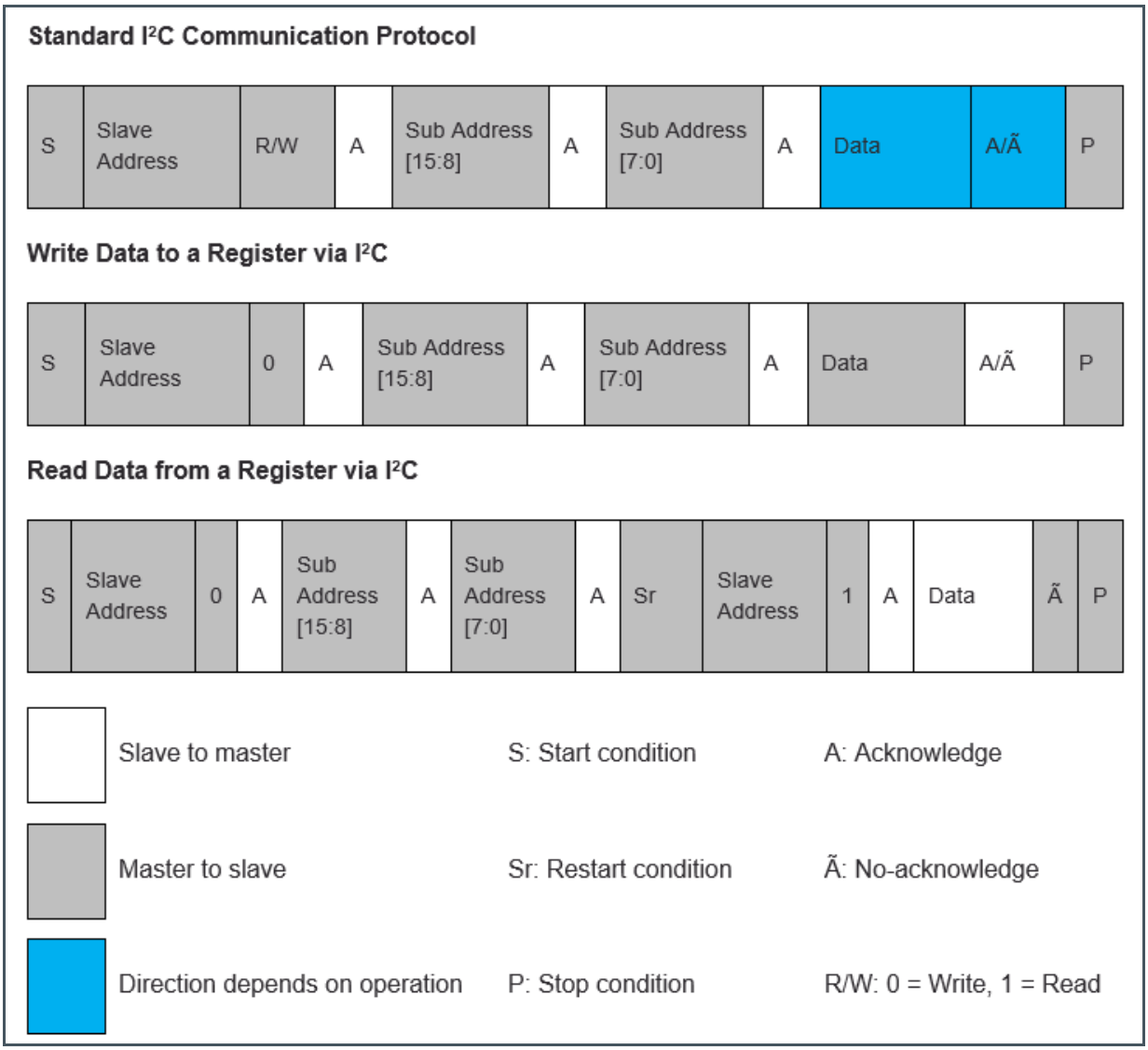
7-bit I²C Bus Device Address	SID0	SID1
7'h30	Low	Low
7'h31	High	Low
7'h32	Low	High
7'h33	High	High

In the example below, the first line below shows a standard I²C communication protocol for 7-bit slave address, 16-bit sub address and 8-bit data. The slave address is the I²C bus device address, which is 7-bit. The R/W bit is either 1 for read or 0 for write. The two sub address bytes are the high byte and low byte of the 16-bit address of the register to be accessed.

The second line shows a write operation.

The third line shows a read operation. A dummy write operation is required to set the sub address (i.e. register address) before the read operation.

Figure 19:
I²C Bus Device Address Control Example

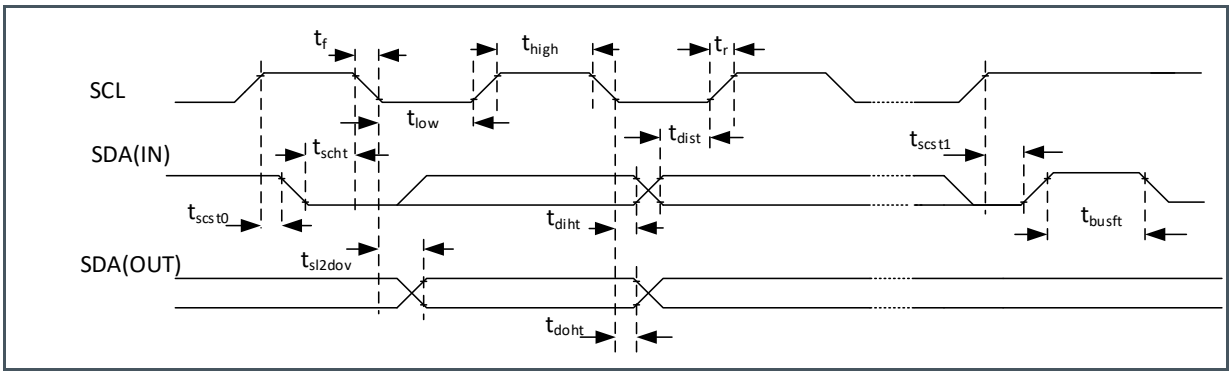


Information

16-bit register address, 8-bit data and 7-bit device address

Figure 20 shows the I²C interface timing diagram

Figure 20:
I²C Interface Timing



(1) I²C interface timing is based on a 400 kHz mode.
(2) The beginning of a rising edge and the end of a falling edge are at 10% of the amplitude of the signal. The end of a rising edge and the beginning of a falling edge are at 90% of the amplitude of the signal.

Figure 21:
I²C Interface Timing Parameter

Symbol	Parameter	Min	Typical	Max	Unit
f_{I^2C}	Clock frequency	-	-	400	kHz
t_{low}	Clock low period	1.3	-	-	µs
t_{high}	Clock high period	0.6	-	-	µs
t_{sl2dov}	SCL low to data out valid	0.1	-	0.9	µs
t_{busft}	Bus free time before new start	1.3	-	-	µs
t_{scht}	Start condition hold time	0.6	-	-	µs
t_{scst0}	Start condition setup time	0.6	-	-	µs
t_{diht}	Data in hold time	0	-	-	µs
t_{dist}	Data in setup time	0.1	-	-	µs
t_{scst1}	Stop condition setup time	0.6	-	-	µs
t_f / t_r	Ratio of fall time to rise time	-	-	1	
t_{doht}	Data out hold time	0.05	-	-	µs

7.3 Sensor ID

Figure 22:
Sensor ID Registers

Function	Address	Default Value
Sensor ID high byte	16'h3107	8'h00
Sensor ID low byte	16'h3108	8'h31

7.4 Data Interface

There are three types of data interfaces in this chip: the Mobile Industry Processor Interface (MIPI) and the Low Voltage Differential Signaling (LVDS).

7.4.1 Mobile Industry Processor Interface (MIPI)

This chip provides a Mobile Industry Processor Interface (MIPI) which supports 8/10/12-bit, 1/2-lane data serial output. Figure 23 shows the MIPI/LVDS interface.

Figure 23:
MIPI/LVDS Interface

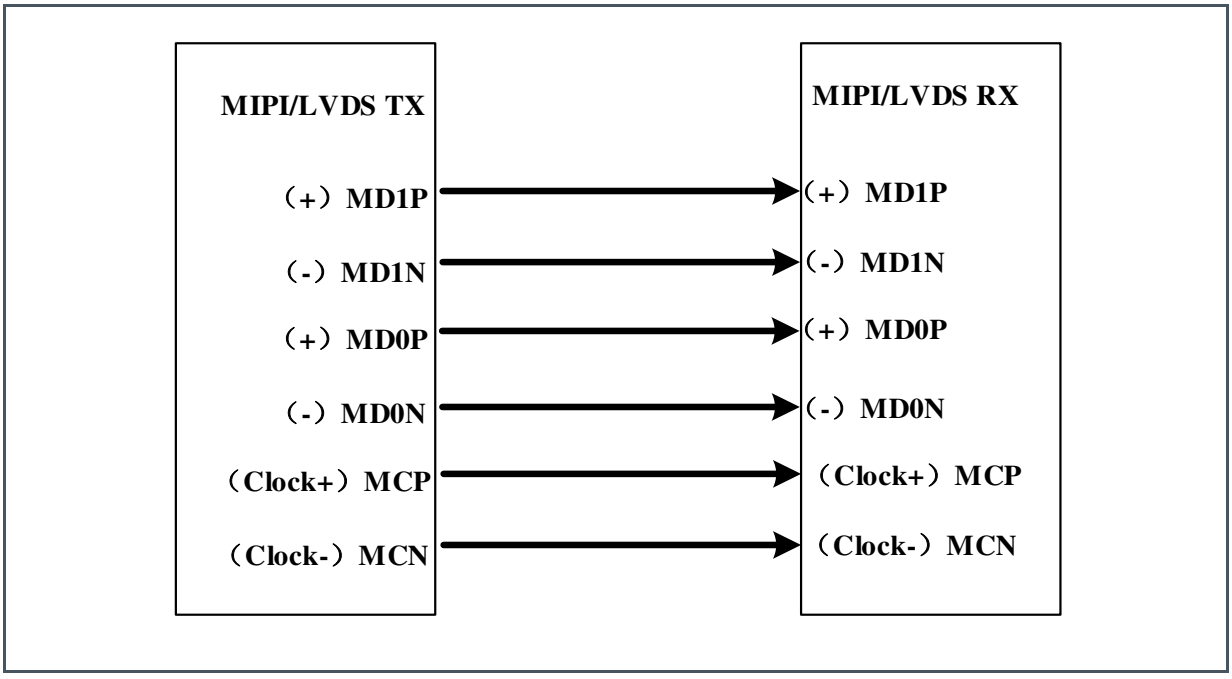


Figure 24 shows an example of low-level MIPI data packet, and more specifically the transmission sequence of a short packet followed by a long packet.

Figure 24:
MIPI Low Level Data Packet

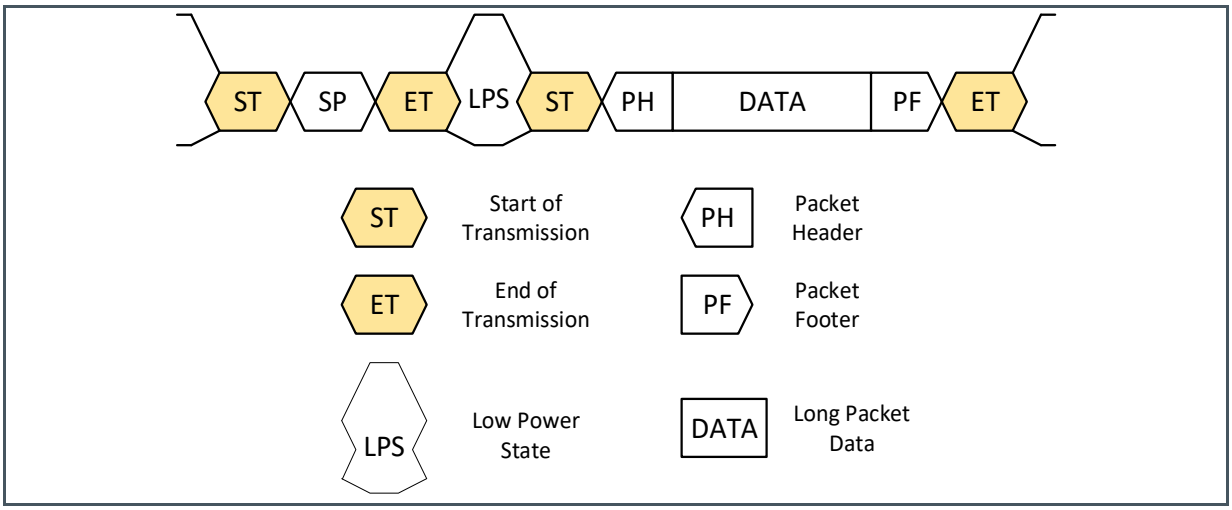


Figure 25 shows the MIPI long/short packet structure. The Data Identifier (DI) is used to distinguish different packet types.

Figure 25:
MIPI Long & Short Packet Structure

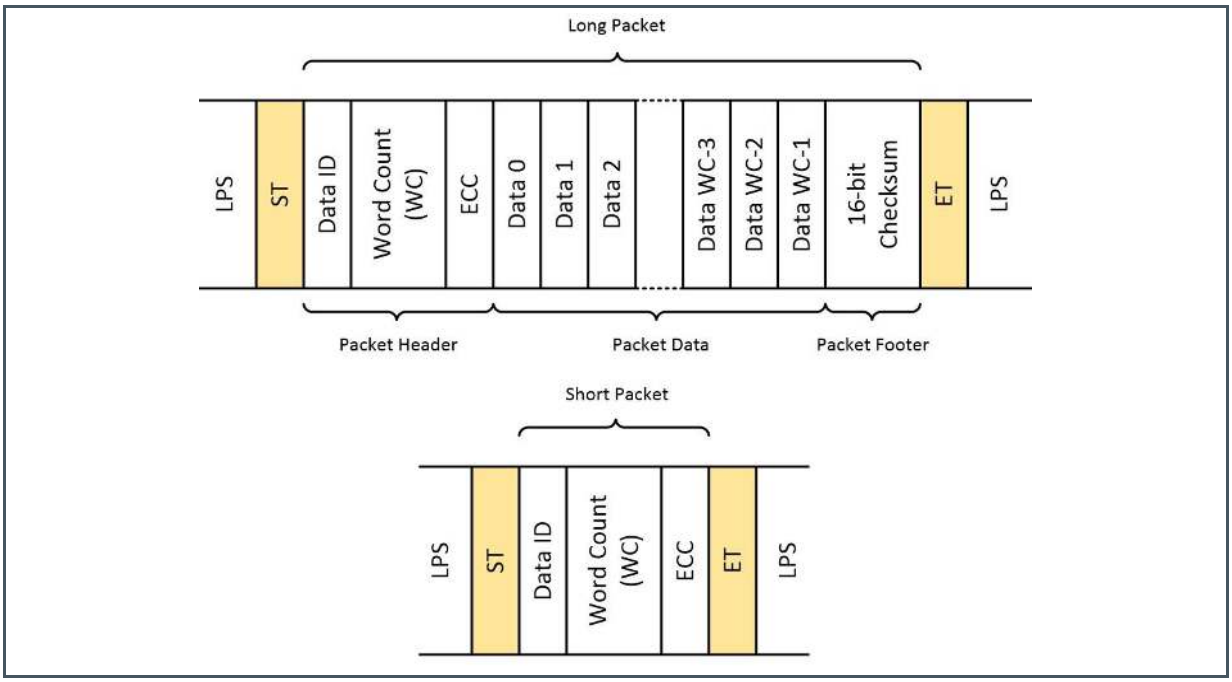
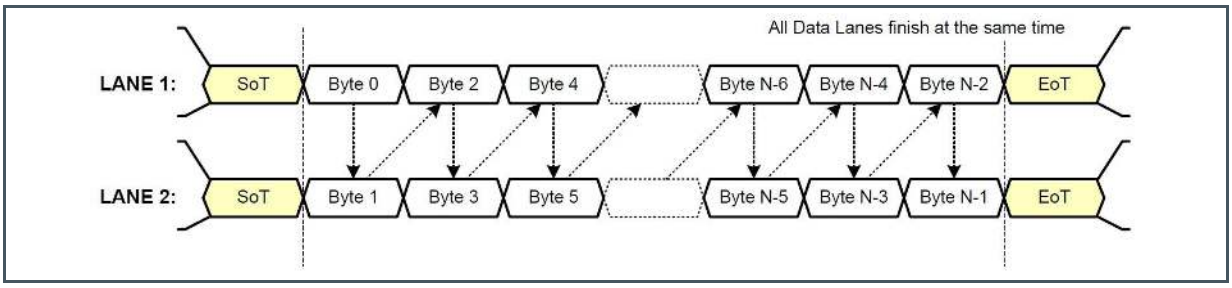


Figure 26 shows the data packet transmission diagram of the MIPI working in 2-lane. It should be noted that the number of data packages transmitting in 2-lane must be an even number.

Figure 26:
MIPI 2-Lane Data Package Transmission



In Figure 27, DI consists of two parts, Virtual Channel (VC) and Data Type (DT). By default, the MIPI data VC value given by this chip is 0, and values of DT are shown in Figure 28.

Figure 27:
MIPI Data Packet DI Structure

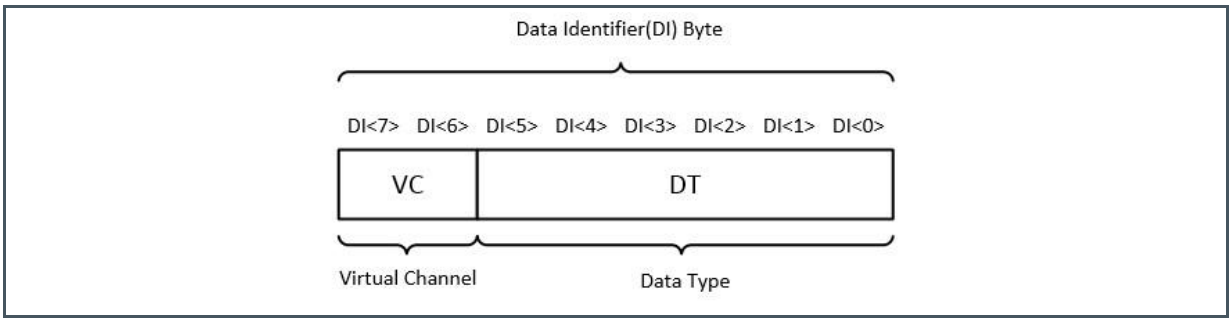


Figure 28:
MIPI Data Types

DT	Description
6'h00	Frame start short packet
6'h01	Frame end short packet
6'h2a	8-bit data long packet
6'h2b	10-bit data long packet
6'h2c	12-bit data long packet

Other useful MIPI control register can be found below.

Figure 29:
MIPI Control Registers

Function	Address	Description
LVDS/MIPI selection	16'h3022	Bit [3]: MIPI/LVDS mode 1'b1: LVDS 1'b0: MIPI
MIPI FIFO read disable	16'h4603	Bit [0]: MIPI read from FIFO 0: enable 1: disable
MIPI lane number	16'h3018	Bit [7:5]: MIPI lane number 3'h0: 1-lane mode 3'h1: 2-lane mode
MIPI output data mode	16'h3031	Bit [3:0]: MIPI bit mode 4'h8: raw8 mode 4'ha: raw10 mode 4'hc: raw12 mode
MIPI clock setting	16'h303f	Bit [7]: Data clock 1'h0: T_{PCLK} (the period of pixel clock, divided from PLL with a division ratio given by FAEs) 1'h1: divided from the system clock (refer to PLL below) with a division ration given by FAEs
MIPI FIFO setting	16'h3c00	Bit [2]: FIFO mode 1'b0: FIFO data for MIPI
Low power (LP) driving	16'h3650	Bit [1:0]: LP mode driving capability, the default value is 2'b10
HIGH speed (HS) driving	16'h3651	Bit [2:0]: HS mode driving capability, the default value is 3'b101
MIPI lane 0 & 1 delay	16'h3652	Bit [7]: lane 0 invert, the default value is 0 Bit [6:4]: delay of lane 0 equals to the value of bit [6:4] × 100 ps, the default value is 3'b100 Bit [3]: lane 1 invert, the default value is 0 Bit [2:0]: delay of lane 1 equals to the value of bit [2:0] × 100 ps, the default value is 3'b100
MIPI clock delay	16'h3654	Bit [3]: clock invert, the default value is 0 Bit [2:0]: delay of MIPI clock equals to the value of bit [2:0] × 100 ps, the default value is 3'b100

7.4.2 Low Voltage Differential Signaling (LVDS)

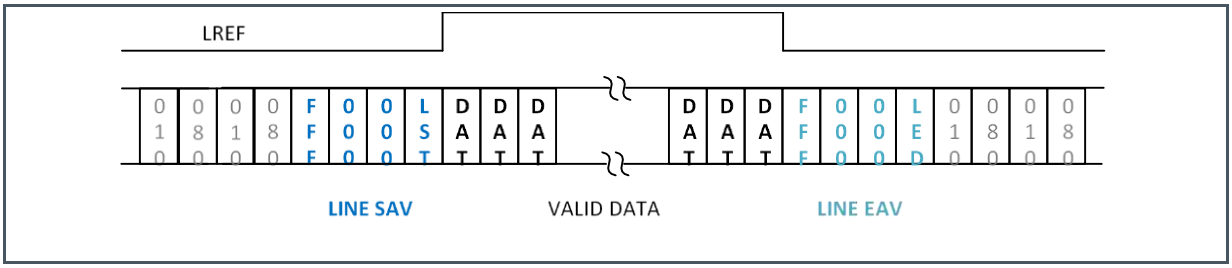
This chip provides a Low Voltage Differential Signaling (LVDS) interface. The LVDS interface is multiplexed with the MIPI, and is selected by a register. The LVDS in this chip supports 1 or 2 data lanes for transmitting 8/10/12-bit data, the MSB of which is sent first by default. Figure 23 shows the MIPI/LVDS interface.

In this chip, the transmission sequence of LVDS is:

1. Power-up reset;
2. First active line, second active line, …, last active line;
3. Only one dummy line;
4. Next frame first active line, second active line, …, and so on.

Figure 30 shows a LVDS data structure of a lane. A LINE SAV synchronization code is inserted at the beginning, a LINE EAV synchronization code is inserted at the end. Dummy lines are used to indicate the end of a frame. The data of LVDS are 8/10/12-bit, while the LVDS synchronization code is 8-bit. The LVDS synchronization code always locates at the 8 MSBs of the data of LVDS. Figure 31 lists all LVDS synchronization codes.

Figure 30:
LVDS Data Structure of 1-Lane (10-Bit Example)



(1) Data 10'h010 and 10'h080 are Dummy0 and Dummy1 data, which can be controlled by registers.
(2) The lane data structure of ½-lane is the same as shown in Figure 26.

Figure 31:
LVDS Synchronization Codes

Default Value	Description
8'hab	Dummy line SAV
8'hb6	Dummy line EAV
8'h80	Active Line SAV
8'h9d	Active Line EAV

(1) Take 10-bit as an example, active line SAV is 10'h200.

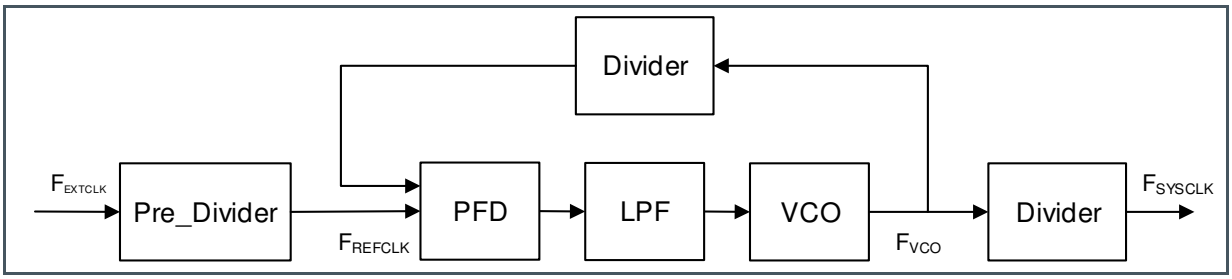
Figure 32:
LVDS Control Registers

Function	Address	Description
LVDS/MIPI selection	16'h3022	Bit [3]: MIPI/LVDS mode 1'b1: LVDS 1'b0: MIPI
MIPI FIFO read disable	16'h4603	Bit [0]: MIPI read from FIFO 0: enable 1: disable
LVDS lane number	16'h3018	Bit [7:5]: MIPI lane number 3'h0: 1-lane mode 3'h1: 2-lane mode
LVDS output data mode	16'h302b	Bit [6:5]: LVDS bit mode 2'b00: raw8 mode 2'b01: raw10 mode 2'b10: raw12 mode
LVDS clock setting	16'h303f	Bit [7]: Data clock 1'h0: T_{PCLK} (the period of pixel clock, divided from PLL with a division ratio given by FAEs) 1'h1: divided from the system clock (refer to PLL below) with a division ration given by FAEs
LVDS bit setting	16'h4b00	Bit [3]: r_bit_flip_i 1'b1: MSB first 1'b0: LSB first
DUMMY0 data	{16'h4b02[3:0], 16'h4b03}	Dummy0 data
DUMMY1 data	{16'h4b04[3:0], 16'h4b05}	Dummy1 data
LVDS lane 0 & 1 delay	16'h3652	Bit [7]: lane 0 invert Bit [6:4]: delay of lane 0 equals to the value of bit [6:4] × 100 ps Bit [3]: lane 1 invert Bit [2:0]: delay of lane 1 equals to the value of bit [2:0] × 100 ps
LVDS clock delay	16'h3654	Bit [3]: clock invert Bit [2:0]: delay of MIPI clock equals to the value of bit [2:0] × 100 ps

7.5 On-Chip PLL

The input clock frequency F_{EXTCLK} of the phase locked loop (PLL) module ranges from 6 MHz to 27 MHz, while the VCO output frequency F_{VCO} ranges from 400 MHz to 1200 MHz. The system clock frequency F_{SYSCLK} is obtained by dividing F_{VCO}. The PLL block diagram is shown in Figure 33.

Figure 33:
PLL Block Diagram



8 Sensor Operation

8.1 Illumination Trigger

Mira030 supports an illumination strobe feature and can be used to control a light source (LED or VCSEL). During exposure, the LEDSTROBE pin outputs a logic level ‘high’ to enable an external illumination.

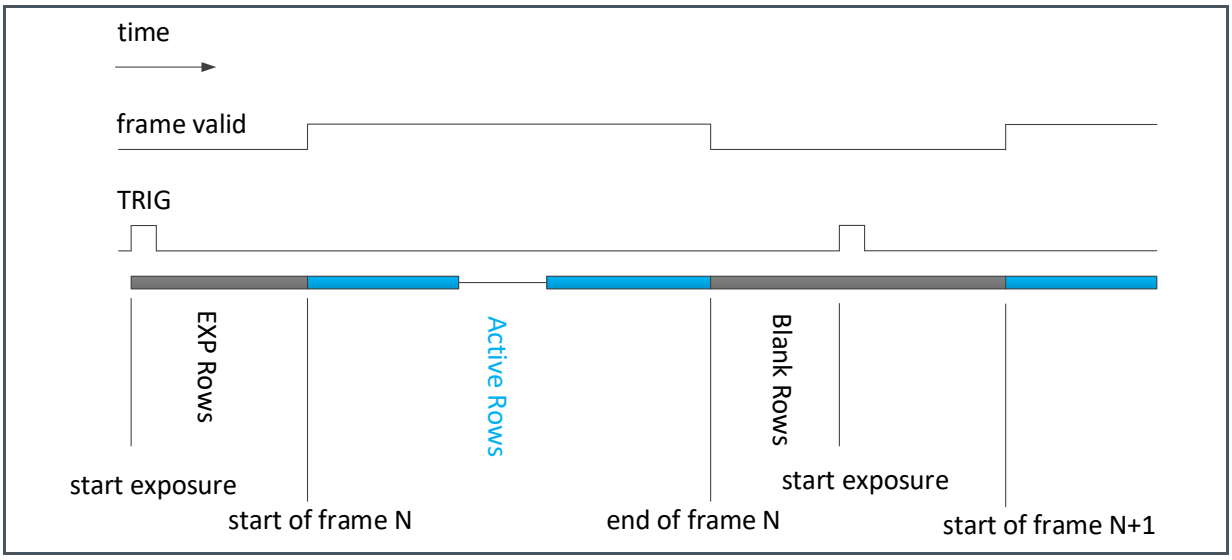
Figure 34:
Illumination Strobe Control Register

Function	Address	Description
Illumination strobe enable	16’h3361	Bit [7:6]: LED strobe enable 2’b11: LED strobe disable 2’b00: LED strobe enable

8.2 External Triggering Mode

In external triggering mode, the exposure and data output of multiple sensors are synchronized by an external triggering signal applied on the TRIG pin. When the rising edge of the signal is detected, the chip starts exposure after a short delay, and outputs data after completing exposure. The short delay is determined by register 16’h3226, and the exposure time is determined by registers {16’h3e01, 16’h3e02}. The frame rate is determined by the signal. Figure 35 shows the timing diagram of external triggering mode, which consists of the following time intervals: EXP Rows, Active Rows, and Blank Rows.

Figure 35:
External Triggering Global Shutter Mode Timing Diagram



(1) EXP Rows = {16'h3e01, 16'h3e02[7:4]} + 16'h3226, in the unit of line.
(2) When the rising edge of the TRIG is detected, the chip starts exposure after a short delay which is determined by the value of the register 16'h3226, in the unit of line. As multiple pixel reset operations are carried out during the delay to achieve a high image quality, the value of the register 16'h3226 is recommended to keep unchanged.
(3) Start of frame N indicates the end of the exposure and the start of outputting data.
(4) During Active Rows, image data can be read. The duration of Active Rows is controlled by registers, in the unit of line.
(5) Blank Rows is the blanking time after reading image data. The duration of Blank Rows is controlled by registers, in the unit of line.

Figure 36:
External Triggering Mode Control Registers

Function	Address	Description
External triggering mode enable	16'h3222	Bit [1]: External triggering mode enable 1: enable 0: disable
Active Rows	{16'h3202,16'h3203}, {16'h3206,16'h3207}, 16'h3248, 16'h3249, {16'h324a, 16'h324b}, {16'h324c, 16'h324d}	Active Rows = {16'h3206,16'h3207} – {16'h3202,16'h3203} + 1 + 16'h3249 – 16'h3248 + 1 + {16'h324c, 16'h324d} – {16'h324a, 16'h324b} + 1
Blank Rows	{16'h3218, 16'h3219}	Blank Rows = {16'h3228, 16'h3229} × 2

8.3 AEC & AGC

The AEC/AGC adjustment is based on the image brightness. AEC adjusts the exposure time while AGC adjusts the gain value so that the image brightness can fall within a range bounded by pre-set brightness thresholds.

8.3.1 AEC & AGC Control Strategy

Mira030 does not have the AEC function, so a back-end platform is needed in order to achieve AEC/AGC.

During the AEC/AGC adjustment process, the exposure time and gain are interrelated and should be considered as a whole. A recommended adjustment strategy is as follows: maximize the exposure time first, and then apply gain if the exposure time has reached its maximum.

Consider a dark scene, the sequence of adjustment is: increase the exposure time with no gain until the exposure time reaches its maximum. When the exposure time reaches its maximum but the image is still too dark, adjust the gain. It should be noted that when the gain is increased, the average image noise also increases. However, when the exposure time increases, the signal-to-noise ratio will improve.

On the other hand, when the image is too bright, the gain should be reduced first. If all gains are reduced to their minimum but the image is still too bright, then the exposure time should be reduced.

8.3.2 AEC Control Registers

Figure 37:
Exposure (manual) Control Registers

Function	Address	Description
Exposure time	{16'h3e01, 16'h3e02}	Exposure time in the unit of 1/16 line

For AEC control, please refer to the following instructions:

1. The AEC adjustment step is 1/16 line of exposure time. One line of exposure time equals to line length × T_{PCLK}, where T_{PCLK} is the period of pixel clock, and line length equals to the value of registers {16'h320c, 16'h320d}.
2. If the exposure time and gain are written to registers in the N^{th} frame, they are effective on the $(N+2)^{th}$ frame.
3. The upper limit of the exposure time is frame length - 6 lines, where frame length equals to the value of registers {16'h320e, 16'h320f}. Hence, the maximum value written to registers {16'h3e01, 16'h3e02[7:4]} is the value of registers {16'h320e, 16'h320f} - 6. If the exposure time is larger than or equal to the frame length, in order to avoid flickering owing to timing errors, the actual frame length will be automatically increased, with a decrease in the frame rate as a drawback.

8.3.3 AGC Control Registers

For AGC control, please refer to the following two methods:

1. When register 16'h3e03 is set to 8'h03, the gain equals to the value of registers {16'h3e08, 16'h3e09} ÷ 8'h10.
2. When register 16'h3e03 is set to 8'h0b, the values of analog gain and digital gain are shown in Figure 39 and Figure 40 respectively. The accuracy of the digital fine gain of this chip is 1/128. The values of digital gain listed in Figure 40 are based on a digital fine gain with a precision of 1/16 as an example.

When the analog coarse gain is changed, the following registers need to be updated:

Figure 38:
Analog Gain Related Settings

Address	Value	Condition
16'h3314	8'h1e	Analog Gain < 2
	8'h4f	Analog Gain >= 2
16'h3317	8'h10	Analog Gain < 2
	8'h0f	Analog Gain >= 2

Figure 39:
Analog Gain Settings

Items	Course Gain 16'h3e08[4:2]	Fine Gain 16'h3e09[7:0]		Total Gain
		Register Value	Gain	
Analog Gain Control	Gain = 1 Register Value: 0	10	1	1
		11	1.0625	1.0625
		12	1.125	1.125
		13	1.1875	1.1875
		14	1.25	1.25
		15	1.3125	1.3125
		16	1.375	1.375
		17	1.4375	1.4375
		18	1.5	1.5
		19	1.5625	1.5625
		1a	1.625	1.625
		1b	1.6875	1.6875
		1c	1.75	1.75
		1d	1.8125	1.8125
		1e	1.875	1.875
		1f	1.9375	1.9375
	Gain = 2 Register Value: 1	10	1	2
		11	1.0625	2.125
		12	1.125	2.25
		13	1.1875	2.375
		14	1.25	2.5

Items	Course Gain 16'h3e08[4:2]	Fine Gain 16'h3e09[7:0]		Total Gain
		Register Value	Gain	
		15	1.3125	2.625
		16	1.375	2.75
		17	1.4375	2.875
		18	1.5	3
		19	1.5625	3.125
		1a	1.625	3.25
		1b	1.6875	3.375
		1c	1.75	3.5
		1d	1.8125	3.625
		1e	1.875	3.75
		1f	1.9375	3.875
	Gain = 4 Register Value: 3	10	1	4
		11	1.0625	4.25
		12	1.125	4.5
		13	1.1875	4.75
		14	1.25	5
		15	1.3125	5.25
		16	1.375	5.5
		17	1.4375	5.75
		18	1.5	6
		19	1.5625	6.25
		1a	1.625	6.5
		1b	1.6875	6.75
		1c	1.75	7
		1d	1.8125	7.25
		1e	1.875	7.5
		1f	1.9375	7.75
	Gain = 8 Register Value: 7	10	1	8
		11	1.0625	8.5
		12	1.125	9
		13	1.1875	9.5
		14	1.25	10
		15	1.3125	10.5

Items	Course Gain 16'h3e08[4:2]	Fine Gain 16'h3e09[7:0]		Total Gain
		Register Value	Gain	
		16	1.375	11
		17	1.4375	11.5
		18	1.5	12
		19	1.5625	12.5
		1a	1.625	13
		1b	1.6875	13.5
		1c	1.75	14
		1d	1.8125	14.5
		1e	1.875	15
		1f	1.9375	15.5

Figure 40:
Digital Gain Settings

Items	Course Gain 16'h3e06[1:0]	Fine Gain 16'h3e07[7:0]		Total gain
		Register Value	Gain	
Digital Gain Control	Gain = 1 Register Value: 0	80	1	1
		88	1.0625	1.0625
		90	1.125	1.125
		98	1.1875	1.1875
		a0	1.25	1.25
		a8	1.3125	1.3125
		b0	1.375	1.375
		b8	1.4375	1.4375
		c0	1.5	1.5
		c8	1.5625	1.5625
		d0	1.625	1.625
		d8	1.6875	1.6875
		e0	1.75	1.75
		e8	1.8125	1.8125
		f0	1.875	1.875
		f8	1.9375	1.9375

Items	Course Gain 16'h3e06[1:0]	Fine Gain 16'h3e07[7:0]		Total gain
		Register Value	Gain	
	Gain = 2 Register Value: 1	80	1	2
		88	1.0625	2.125
		90	1.125	2.25
		98	1.1875	2.375
		a0	1.25	2.5
		a8	1.3125	2.625
		b0	1.375	2.75
		b8	1.4375	2.875
		c0	1.5	3
		c8	1.5625	3.125
		d0	1.625	3.25
		d8	1.6875	3.375
		e0	1.75	3.5
		e8	1.8125	3.625
		f0	1.875	3.75
		f8	1.9375	3.875
	Gain = 4 Register Value: 3	80	1	4
		88	1.0625	4.25
		90	1.125	4.5
		98	1.1875	4.75
		a0	1.25	5
		a8	1.3125	5.25
		b0	1.375	5.5
		b8	1.4375	5.75
		c0	1.5	6
		c8	1.5625	6.25
		d0	1.625	6.5
		d8	1.6875	6.75
		e0	1.75	7
		e8	1.8125	7.25
		f0	1.875	7.5
		f8	1.9375	7.75

8.4 Group Hold

Group hold refers to the packing of a group of registers to be effective at a specific time within a frame. The procedure of packing a group is as follows:

- First, set register 16'h3812 to 8'h00 to start packing the group. Then write the required values to registers of the group. Finally set register 16'h3812 to 8'h30 to end packing the group.
- The maximum number of registers within a group is 10.
- If register 16'h3812 is set to 8'h30 within the M^{th} frame, the group of registers is effective in the $(M + 1 + N)^{th}$ frame, where N is the value of register 16'h3802. N = 0 means the $(M + 1)^{th}$ frame (the following frame without frame delay). N = 1 means delaying one frame and so on.
- The actual effective time of the group of registers is delayed P lines from the start of the $(M + 1 + N)^{th}$ frame, where P is the value of registers {16'h3235,16'h3236}. If P = 0, the group of registers is effective from the start of frame without delay.

Figure 41:
Group Hold Control Registers

Function	Address	Description
Intra-frame effective time	{16'h3235, 16'h3236}	Delay effective time from the start of frame, in the unit of line. If set to 0, the group of registers is effective from the start of frame without delay.
Frame delay control	16'h3802	Bit [7:0]: Determine the number of frames to be delayed before the group of registers is effective. Setting to 0 implies the following frame. Setting to N implies a delay of N frames

8.5 Black Level Control (BLC)

The pixel array of this chip contains 12 black lines, which can provide data for the offset cancellation algorithm. Digital image processing must subtract the black level data first. The BLC algorithm can estimate the black level compensation value from the black row data, and will subtract the black level compensation value from the pixel value. If the subtraction is negative at some specific pixels, the result is set to zero.

By default, changing the gain value will re-trigger the BLC operation.

Black level has two calculation modes: the manual BLC mode and the automatic BLC mode. In the manual BLC mode, the compensation value is specified by registers. In the automatic BLC mode, the compensation value is calculated by the black lines. The BLC target value is a threshold for the BLC algorithm to calibrate.

Figure 42:
BLC Control Registers

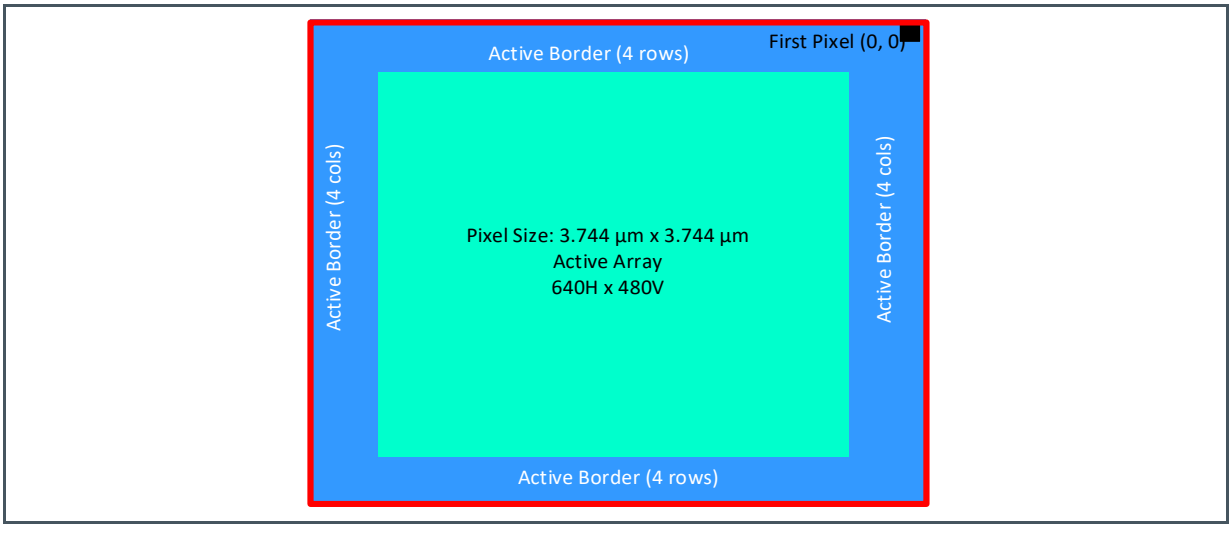
Function	Register	Description
BLC enable	16'h3900	Bit [0]: BLC enable 0: bypass BLC 1: enable BLC
Auto BLC enable	16'h3902	Bit [6]: BLC auto mode 0: manual mode 1: auto mode
BLC channel select	{16'h3928[0], 16'h3905[6]}	16'h3928[0]: 0: use 8 channel offset mode 1: use 4 channel offset mode 16'h3905[6]: one channel enable 0: use 8 or 4 channel offset 1: use one channel mode
BLC target	{16'h3907[4:0], 16'h3908}	BLC target

8.6 Video Output Mode

8.6.1 Read Order

Figure 43 provides the first read pixel location as well as the entire array structure diagram. It shows the top view when the A2 pin indicator is placed in the upper left corner.

Figure 43:
Mira030 Pixel Array



Mira030 supports mirror mode and flip mode. Mirror mode reverses the sensor data readout order, and flip mode vertically reverses the sensor readout order as shown in Figure 44. The register that control these operation are shown in Figure 45.

Figure 44:
Mirror & Flip Examples

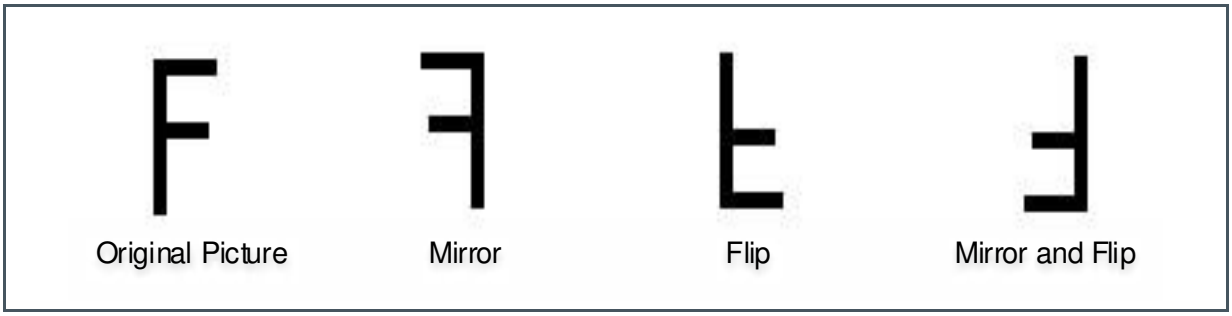


Figure 45:
Mirror & Flip Control Registers

Function	Address	Default Value	Description
Mirror	16'h3221	2'h3	Bit [2:1]: Mirror control 2'b00: mirror off 2'b11: mirror on
Flip	16'h3221	2'h3	Bit [6:5]: Flip control 2'b00: flip off 2'b11: flip on

8.6.2 Output Window

Figure 46:
Output Window Registers

Function	Address	Description
Window width	{16'h3208, 16'h3209}	Output window width
Window height	{16'h320a, 16'h320b}	Output window height
Column start	{16'h3210, 16'h3211}	Output window column start
Row start	{16'h3212, 16'h3213}	Output window row start

8.7 Frame Rate Calculator

Figure 47 shows an effective output diagram. The frame rate can be calculated using the following formula:

Equation 1:

$$frame\ rate = \frac{1}{T_{PCLK} \times line\ length \times frame\ length}$$

$$line\ time = T_{PCLK} \times line\ length$$

Where, T_{PCLK} is the period of the pixel clock, line length is the sum of the width of the active pixel area and the line blanking area (horizontal), frame length is the sum of height of the active pixel area and the frame blanking area (vertical).

Figure 47:
Video Effective Output

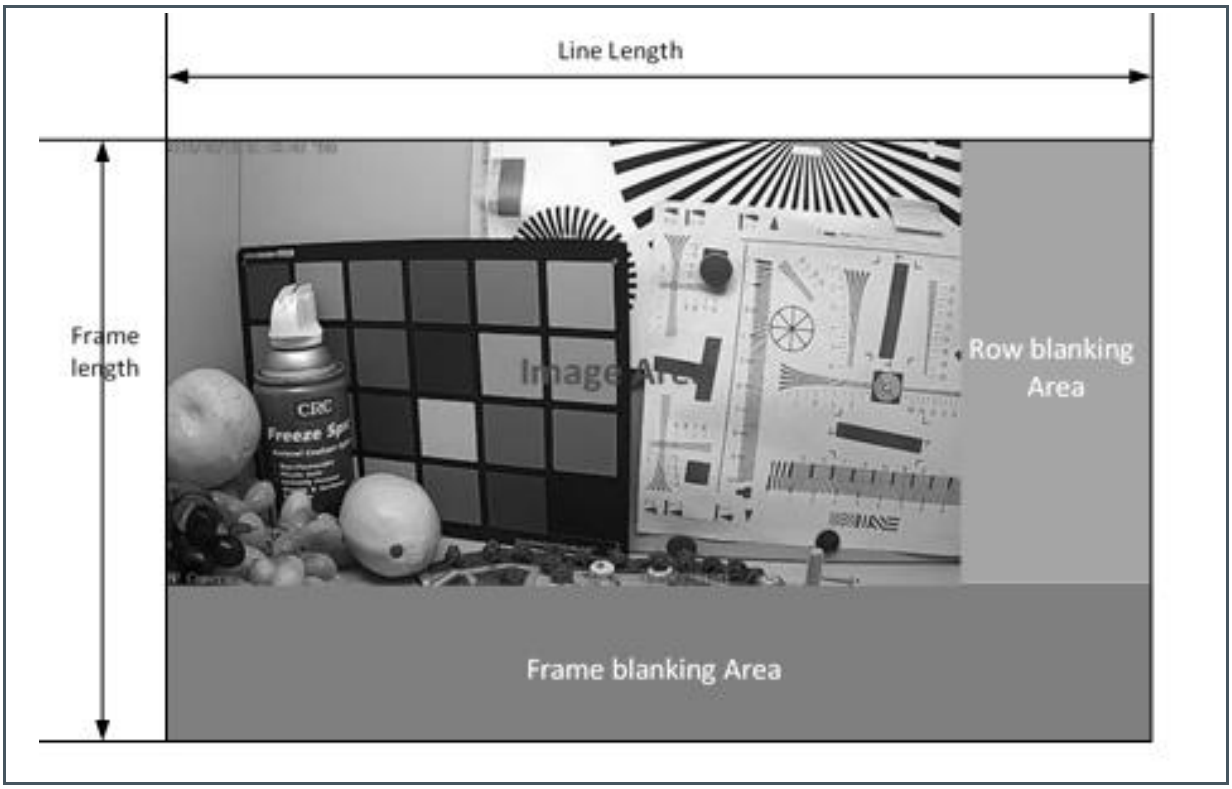


Figure 50:
Frame Rate Related Registers

Function	Address	Description
Line length	{16'h320c, 16'h320d}	Line length
Frame length	{16'h320e, 16'h320f}	Frame length, in the unit of line

8.8 Test Mode

For the ease of testing, Mira030 provides a grey ramp test mode as shown below.

Figure 48:
Test Mode Image

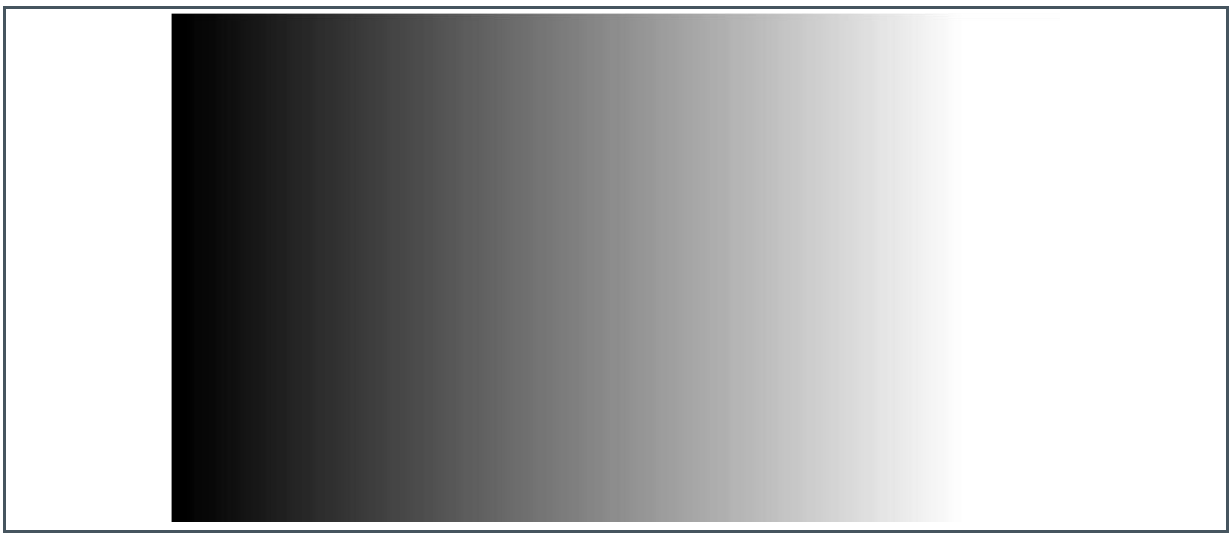


Figure 49:
Test Mode Control Registers

Function	Address	Description
Grey ramp mode	16'h4501	Bit [3]: incremental pattern enable 0: Normal image 1: Incremental pattern

9 Application Information

A typical application circuit is depicted in Figure 50, where the capacitor connections are shown in Figure 51.

Figure 50:
Schematic

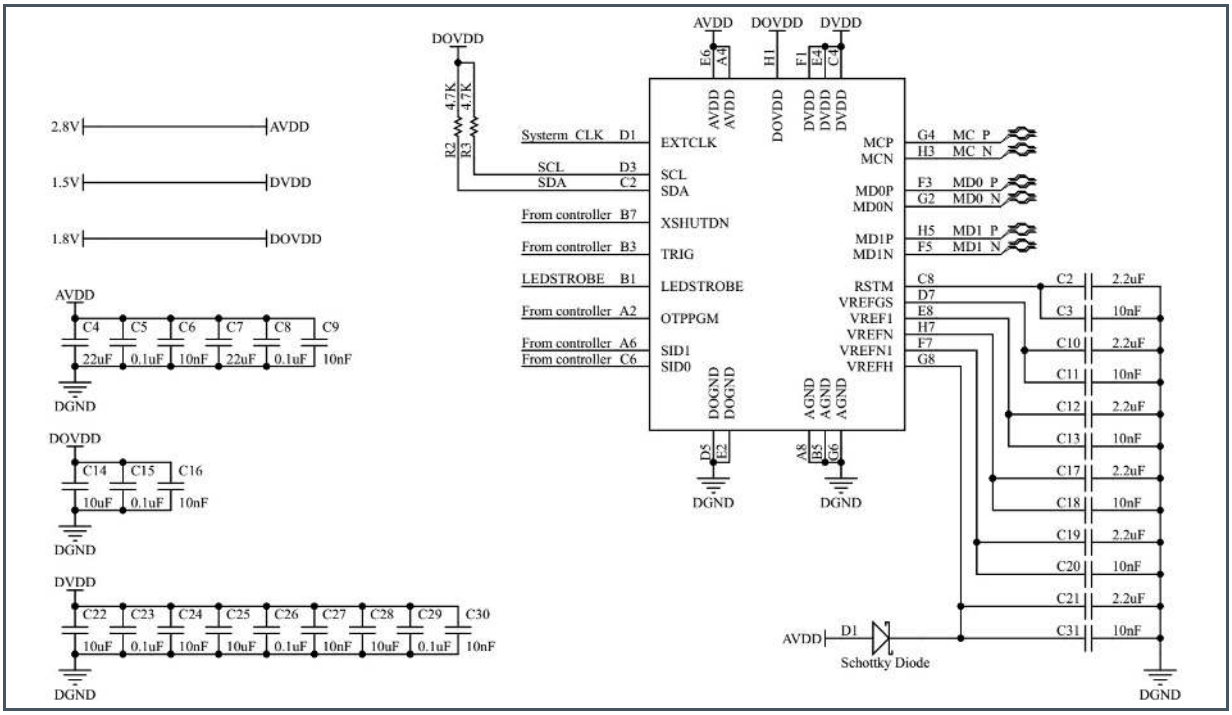
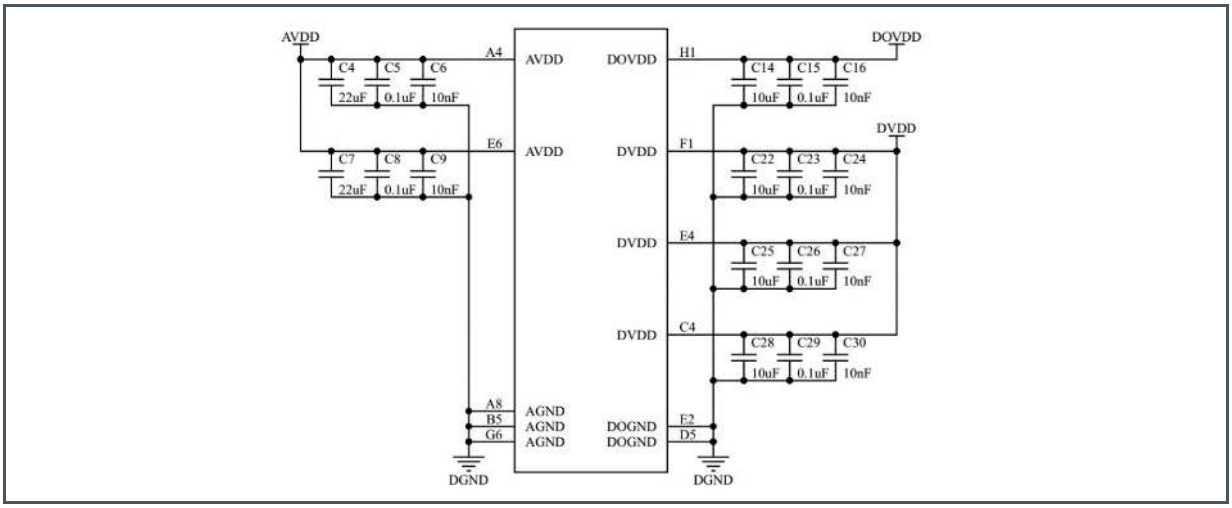


Figure 51:
Power Supply and Filter Connection



A reduction of the capacitors in the above schematic to reduce the cost are given in Figure 52 and Figure 53.

Figure 52:
Schematic Cost Optimized

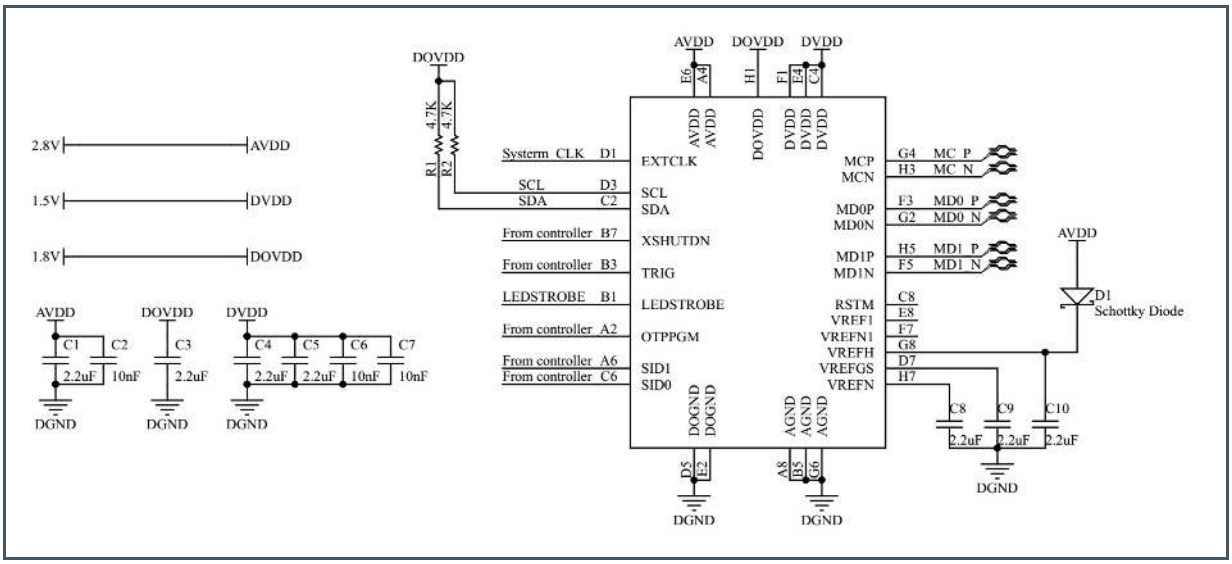
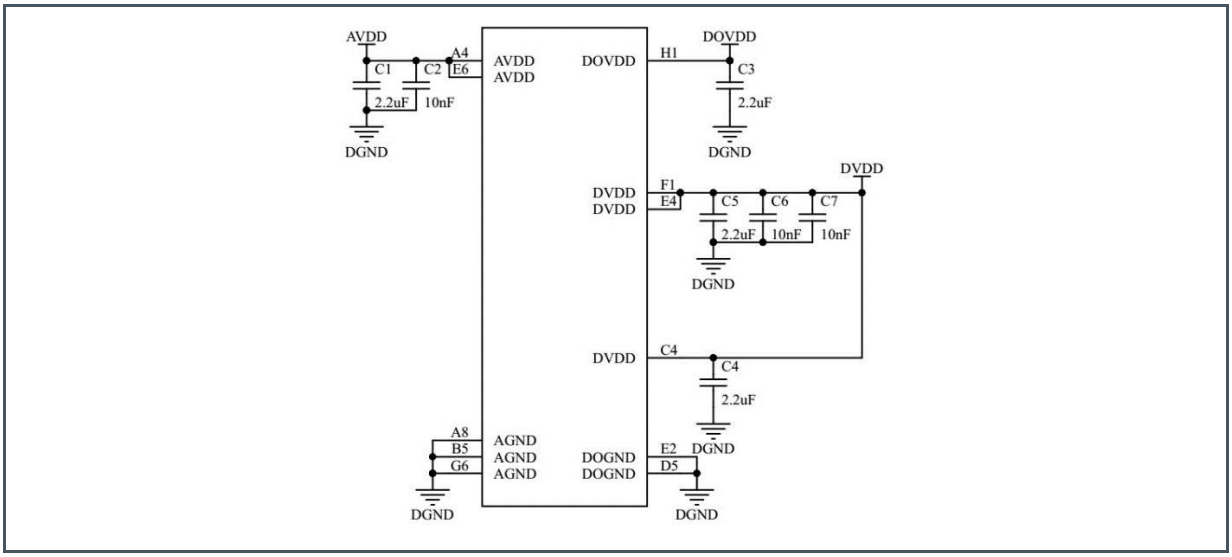
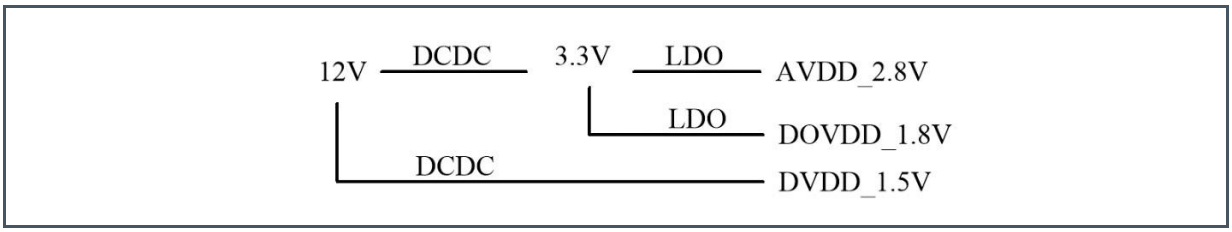


Figure 53:
Power Supply and Filter Connection Cost Optimized



It is recommended to generate the external power supplies using the power tree illustrated in Figure 54.

Figure 54:
Power Tree Recommendation



The following remarks give more advice on the above schematics:

- Mira030 requires three power supplies: the DOVDD pin must be externally connected to a 1.8V power supply, the AVDD pin is externally connected to a 2.8V power supply, and the DVDD pin is externally connected to a 1.5V power supply.
    - For optimized performance: the capacitors need to be placed separately close to the pin for each power supply. For AVDD, they are 22µF + 0.1µF + 10nF. If wiring is difficult, the combination of 22µF + 10nF may be used. For DOVDD, they are 10µF + 0.1µF + 10nF. If wiring is difficult, the combination of 10µF + 10nF may be used. For DVDD, they are 10µF + 0.1µF + 10nF. If wiring is difficult, the combination of 10µF + 10nF may be used. The low-frequency and high-frequency power ripples are filtered respectively. The capacitor values can be found in Figure 51.
    - For cost optimization: for AVDD, A4 and A6 pins share two filter capacitors 2.2µF + 10nF. For DOVDD, a 2.2µF capacitor is connected closed to the pin. For DVDD, a 10nF capacitor is connected to E4 and F1 pins sharing one 2.2µF. The C4 pin is separately connected to a 2.2µF capacitor. The capacitor values can be found in Figure 53.
- The same two approaches can be applied to the capacitors for the reference voltages.
    - For optimized performance: the RSTM, VREFGS, VREF1, VREFN, VREFN1 and VREFH pins must be externally connected to two capacitors 2.2µF + 10nF to ground to filter out the low-frequency and high-frequency supply ripples. The capacitor needs to be close to the chip pin and keeps as far as possible from the I/O signals such as EXTCLK, TRIG and MIPI differential pairs. Connect a Schottky diode to the VREFH and AVDD pin, the forward conductive voltage of the diode should not exceed 200mV@1mA (RB521CS-30 is recommended).
    - For cost optimization: the VREFGS, VREFN and VREFH pins must be externally connected to a 2.2µF capacitor to ground. The capacitor needs to be close to the chip pin and keeps as far as possible from the I/O signals such as EXTCLK, TRIG and MIPI differential pairs. Connect a Schottky diode to the VREFH and AVDD pin, the forward conductive voltage of the diode should not exceed 200mV@1mA (RB521CS-30 is recommended).
- An external main control chip controls the active low XSHUTDN pin.
- A crystal connecting to the EXTCLK pin generates the system clock signal. Alternatively, a system can apply the system clock signal directly to the EXTCLK pin with a signal frequency ranged from 6 to 27 MHz.
- The requirements of routing MIPI differential pairs are as follows:

- The control standard of the impedance of MIPI differential pairs is 100Ω, and the tolerance is limited to ±10%.
- The differential pairs should not be right-angled in order to avoid reflections, and as a result affect high speed transmission performance.
- Reference layer: there must be a reference layer below the MIPI differential pairs (a ground plane is recommended). The continuity of the layer must be guaranteed, that is the layer below the MIPI differential pairs cannot be fragmented, cannot consist of gaps, and cannot be cut by other lines. A whole layer of ground is preferred. If not possible, the minimum requirement is to ensure that the reference layer below the MIPI differential pairs is 4W wider than each side of the MIPI signal wire, where W is the width of MIPI differential pairs.
- Equal length: the difference in length between the two wires of a MIPI differential pair should be limited to 10 mils, and the difference in length among MIPI differential pairs should be controlled within 100 mils. These requirements ensure that the differential signals can reach the receiving end at the same time. When implementing the requirement of equal length, the symmetry should be considered. The distance between snake-shaped wires should be 4W to avoid being too dense. The wires should be wound near the bonding pad as much as possible to keep equal length, and the wire width and distance cannot be changed arbitrarily.
- Symmetry: MIPI differential pairs should be kept equal length and distance. The purpose of symmetry is to ensure the consistency of trace impedance in order to reduce reflection. Poor symmetry may result in signal distortion, instability or no image.
- Keep clear of interference: the clearance between MIPI differential pairs should be larger than 2W. The clearance between MIPI differential pairs and other high-speed signals (parallel data lines, clock lines, etc.) should be larger than 3W, and they should not be routed in parallel. A larger clearance should be considered to avoid interference generated from circuits such as switching power supplies.
- Through holes: through holes should be avoided for MIPI differential pairs. If unavoidable, through holes should be on both wires of the differential pair in order to maintain symmetry. If a differential pair is routed to another layer by means of through holes, the reference layer should also follow by means of through holes near the through holes of the differential pair.

10 Package Drawings & Markings

10.1 Reconstructed Wafer

- Max total die count: 2126 ea
- Film frame: compact disco stainless SUS420
- Carrier tape: UV tape

Figure 55:
RW Physical Dimensions

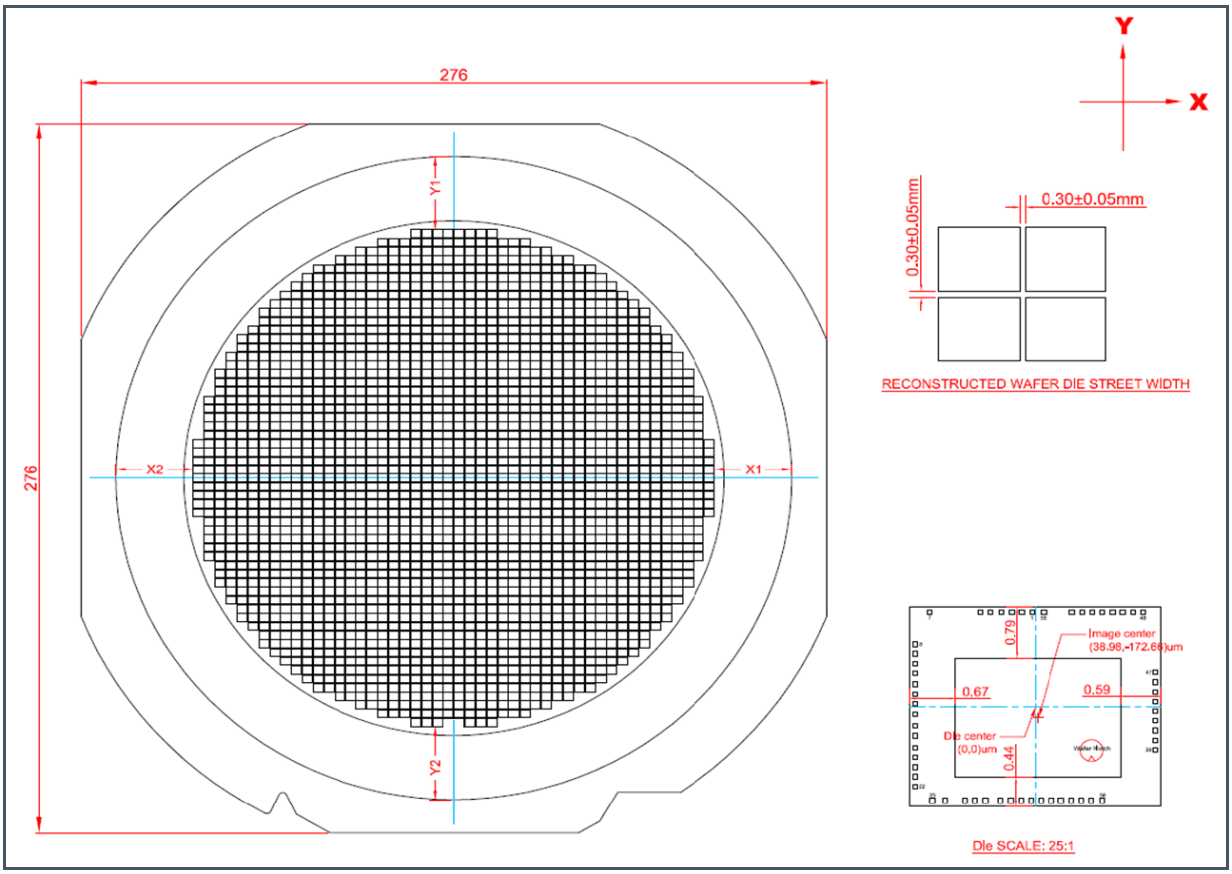


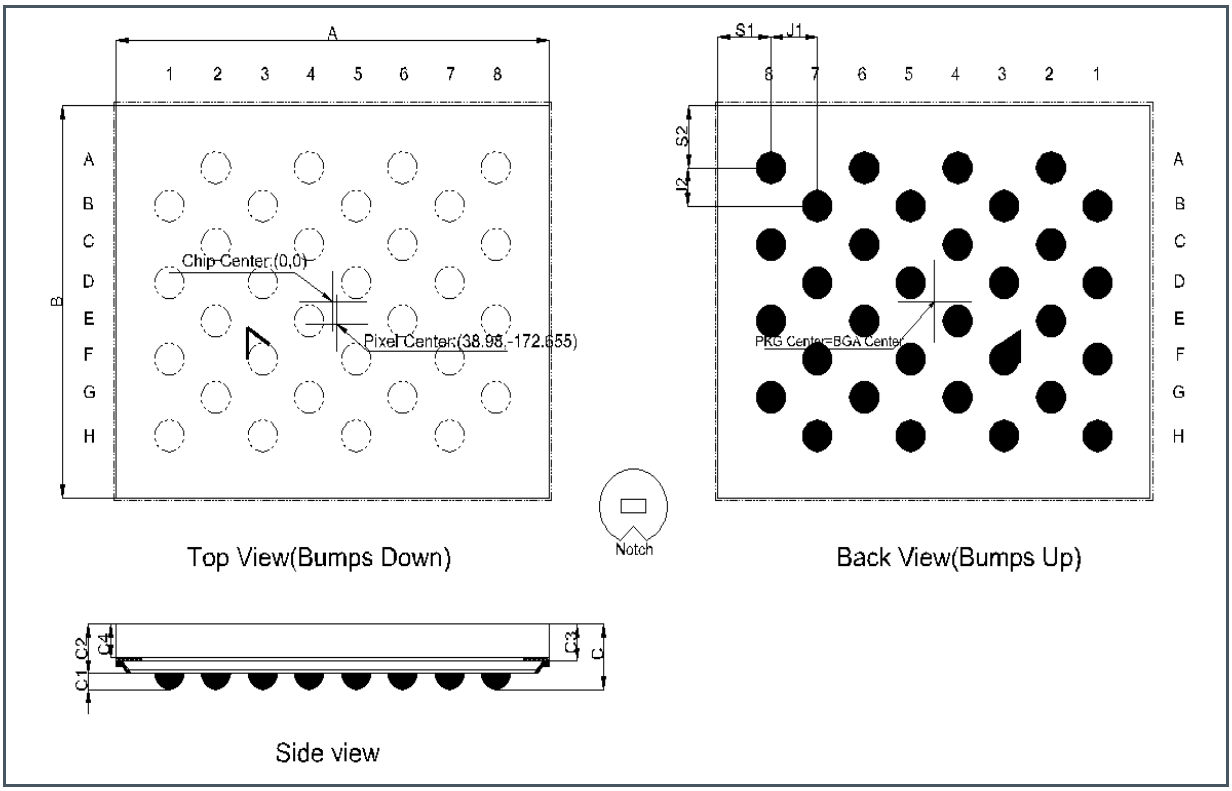
Figure 56:
RW Physical Size

Parameter	Description
Wafer Diameter	200 mm (8”)
Grinding Thickness	150 µm ± 10 µm

Parameter	Description
Singulated Die Size	X = 3723.8 µm ± 20 µm, Y = 3092 µm ± 20 µm
Bond Pad Size	X = 77.4 µm, Y = 77.4 µm
Bond Pad Opening	X = 70.2 µm, Y = 70.2 µm
Minimum Bond Pad Pitch	150.3 µm
Optical Array (Optical center from die center)	X = 38.98 µm, Y = -172.66 µm
RW Offset	(X1 - X2) ÷ 2 = 0 ± 5 mm; (Y1 - Y2) ÷ 2 = 0 ± 5 mm;
Placement Accuracy X,Y,Theta	X, Y (±50 µm), Theta < 1°
Maximum Total Die Count	2126 ea
RW Layout	X = 48, Y = 57

10.2 CSP Package

Figure 57:
Package Drawing



Information

- The pin identification is on F3.
- The center of the CSP does not coincide with the optical center. Pixel Center (38.98, -172.655) is the same as the optical center. The unit is in µm.

Figure 58:
Package Dimensions

Parameter	Symbol	Nominal Millimeters	Min	Max	Nominal Inches	Min	Max
Package Body Dimension X	A	3.7038	3.6788	3.7288	0.1458	0.1448	0.1468
Package Body Dimension Y	B	3.0720	3.0470	3.0970	0.1209	0.1200	0.1219
Package Height	C	0.7600	0.7000	0.8200	0.0299	0.0276	0.0323
Ball Height	C1	0.1300	0.1000	0.1600	0.0051	0.0040	0.0063
Package Body Thickness	C2	0.6300	0.5950	0.6650	0.0248	0.0234	0.0262
Thickness from top glass surface to wafer	C3	0.4450	0.4250	0.4650	0.0175	0.0167	0.0183
Glass Thickness	C4	0.4000	0.3900	0.4100	0.0157	0.0154	0.0161
Ball Diameter	D	0.2500	0.2200	0.2800	0.0098	0.0087	0.0110
Total Ball Count	N	32	—	—	—	—	—
Pins Pitch X axis	J1	0.4000	—	—	—	—	—
Pins Pitch Y axis	J2	0.3000	—	—	—	—	—
Edge to Pin Center Distance along X1	S1	0.4519	0.4219	0.4819	0.0178	0.0166	0.0190
Edge to Pin Center Distance along Y1	S2	0.4860	0.4560	0.5160	0.0191	0.0180	0.0203

11 Revision Information

Document Status	Product Status	Definition
Product Preview	Pre-Development	Information in this datasheet is based on product ideas in the planning phase of development. All specifications are design goals without any warranty and are subject to change without notice
Preliminary Datasheet	Pre-Production	Information in this datasheet is based on products in the design, validation or qualification phase of development. The performance and parameters shown in this document are preliminary without any warranty and are subject to change without notice
Datasheet	Production	Information in this datasheet is based on products in ramp-up to full production or full production which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade
Datasheet (discontinued)	Discontinued	Information in this datasheet is based on products which conform to specifications in accordance with the terms of ams AG standard warranty as given in the General Terms of Trade, but these products have been superseded and should not be used for new designs

Changes from previous version to current revision v2-00	Page
Removed “Confidential” from footer	

- Page and figure numbers for the previous version may differ from page and figure numbers in the current revision.
- Correction of typographical errors is not explicitly mentioned.

12 Legal Information

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