Panasonic

AN32058A

http://www.semicon.panasonic.co.jp/en/

7 x 7 Dots Matrix LED Driver LSI

FEATURES

- 7 x 7 LED Matrix Driver
  (Total LED that can be driven = 49)
- Built-in memory (ROM and RAM)
- LDO : 2-ch
- SPI Interface : 1-ch
- Driver for RGB color unit : 1-ch
- 44 pin Plastic Quad Flat Non-leaded package (QFN Type)

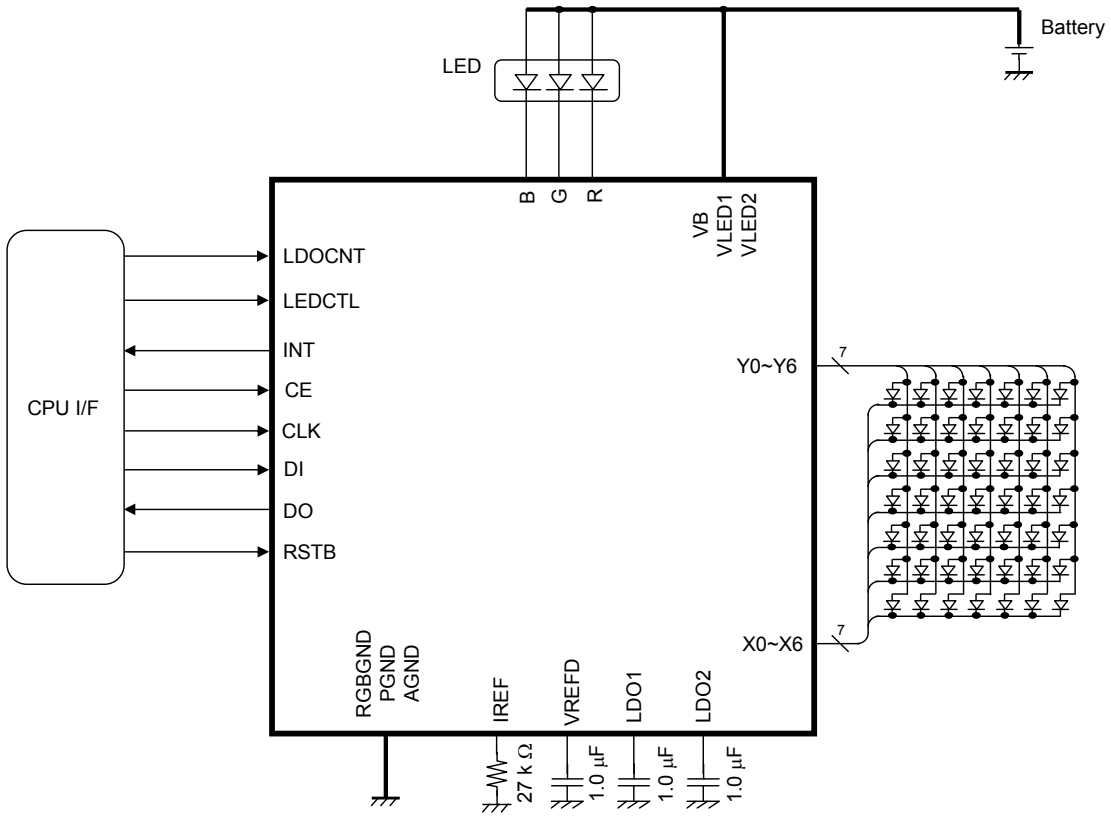
DESCRIPTION

AN32058A is 49 Dots Matrix LED Driver. It can drive up to 16 RGB LEDs.

APPLICATIONS

- Mobile Phone
- Smart Phone
- PCs
- Game Consoles
- Home Appliances etc.

TYPICAL APPLICATION



Note)
The application circuit is an example. The operation of the mass production set is not guaranteed. Sufficient evaluation and verification is required in the design of the mass production set. The Customer is fully responsible for the incorporation of the above illustrated application circuit in the design of the equipment.

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ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit	Note
Supply voltage	VB_{MAX}	6.0	V	*1
	$VLED_{MAX}$	6.5	V	*1
Operating ambience temperature	T_{opr}	– 30 to + 85	°C	*2
Operating junction temperature	T_j	– 30 to + 125	°C	*2
Storage temperature	T_{stg}	– 55 to + 125	°C	*2
Input Voltage Range	LEDCTL, RSTB, CE, CLK, DI	– 0.3 to 3.4	V	—
	LDOCNT	– 0.3 to 6.0	V	—
Output Voltage Range	INT, DO	– 0.3 to 3.4	V	—
	R, G, B, LDO1, LDO2, X0, X1, X2, X3, X4, X5, X6, Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3 to 6.5	V	—
ESD	HBM (Human Body Model)	2.0	kV	—

Note) This product may sustain permanent damage if subjected to conditions higher than the above stated absolute maximum rating. This rating is the maximum rating and device operating at this range is not guaranteeable as it is higher than our stated recommended operating range.
When subjected under the absolute maximum rating for a long time, the reliability of the product may be affected.
*1 VB_{MAX} = VB, $VLED_{MAX}$ = VLED1 = VLED2.
The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
*2 Except for the power dissipation, operating ambient temperature, and storage temperature, all ratings are for Ta = 25°C.

POWER DISSIPATION RATING

PACKAGE	θ_{JA}	P_D (Ta=25 °C)	P_D (Ta=85 °C)
44 pin Plastic Quad Flat Non-leaded package (QFN Type)	71.8 °C /W	1.392 W	0.557 W

Note) For the actual usage, please refer to the P_D-Ta characteristics diagram in the package specification, follow the power supply voltage, load and ambient temperature conditions to ensure that there is enough margin and the thermal design does not exceed the allowable value.

CAUTION

Although this IC has built-in ESD protection circuit, it may still sustain permanent damage if not handled properly. Therefore, proper ESD precautions are recommended to avoid electrostatic damage to the MOS gates

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RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage range	VB	3.1	3.7	4.6	V	*1
	VLED	3.1	5.0	5.6	V	*1
Input Voltage Range	LEDCTL, RSTB, CE, CLK, DI	– 0.3	—	3.0	V	—
	LDOCNT	– 0.3	—	VB + 0.3	V	*2
Output Voltage Range	INT, DO	– 0.3	—	3.0	V	—
	R, G, B, LDO1, LDO2, X0, X1, X2, X3, X4, X5, X6, Y0, Y1, Y2, Y3, Y4, Y5, Y6	– 0.3	—	VLED + 0.3	V	*2

Note) *1: The values under the condition not exceeding the above absolute maximum ratings and the power dissipation.
Do not apply external currents and voltages to any pin not specifically mentioned.
Voltage values, unless otherwise specified, are with respect to GND. GND is voltage for AGND, RGBGND and PGND.
VB is voltage for VB. VLED is voltage for VLED1 and VLED2.
*2: (VB + 0.3) V must not exceed 6 V. (VLED + 0.3) V must not exceed 6.5 V.

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ELECTRICAL CHARACTERISTICS

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current consumption							
Current consumption (1)	ICC1	At OFF mode LDOCNT = Low	—	0	1	μA	—
Current consumption (2)	ICC2	At Standby mode LDOCNT = Low LDO2 is active.	—	8	12	μA	—
Current consumption (3)	ICC3	LDOCNT = High LDO1 and LDO2 are active.	—	18	24	μA	—
Reference voltage							
Output voltage	VREF	I_{VREF} = 0 μA	1.21	1.24	1.27	V	—
Reference current							
Output voltage	VIREF	I_{IREF} = 0 μA	0.44	0.54	0.64	V	—
Voltage regulator (LDO1)							
Output voltage	VL1	I_{LDO1} = – 30 mA	1.79	1.85	1.91	V	—
Short circuit protection current	IPT1	LDOCNT = High REG18 = High V_{LDO1} = 0 V, IPT1 = I_{LDO1}	50	100	200	mA	—
Ripple rejection (1)	PSL11	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO1} = – 15 mA PSL11 = 20log (acV_{LDO1} / 0.2)	—	– 45	– 40	dB	—
Ripple rejection (2)	PSL12	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO1} = – 15 mA PSL12 = 20log (acV_{LDO1} / 0.2)	—	– 35	– 25	dB	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Voltage regulator (LDO2)							
Output voltage	VL2	I_{LDO2} = – 30 mA	2.76	2.85	2.94	V	—
Short circuit protection current	IPT2	LDOCNT = High V_{LDO2} = 0V IPT2 = I_{LDO2}	50	100	300	mA	—
Ripple rejection (1)	PSL21	VB = 3.6 V + 0.2 V[p-p] f = 1 kHz I_{LDO2} = – 15 mA PSL21 = 20log (acV_{LDO2} / 0.2)	—	– 35	– 30	dB	—
Ripple rejection (2)	PSL22	VB = 3.6 V + 0.2 V[p-p] f = 10 kHz I_{LDO2} = – 15 mA PSL22 = 20log (acV_{LDO2} / 0.2)	—	– 25	– 15	dB	—
Oscillator							
Oscillation frequency	FDC	—	0.96	1.20	1.44	MHz	—
SCAN Switch							
Resistance at the Switch ON	RSCAN	$I_{Y0, Y1, Y2, Y3, Y4, Y5, Y6}$ = 5 mA RSCAN = $V_{Y0, Y1, Y2, Y3, Y4, Y5, Y6}$ / 5 mA	—	2	4.8	Ω	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current generator (For 7 × 7 dots matrix LED)							
Output current (1)	IMX1	At 1mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX1 = $I_{X0, X1, X2, X3, X4, X5, X6}$	0.950	1.033	1.116	mA	*1
Output current (2)	IMX2	At 2 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX2 = $I_{X0, X1, X2, X3, X4, X5, X6}$	1.907	2.073	2.239	mA	*1
Output current (3)	IMX4	At 4 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX4 = $I_{X0, X1, X2, X3, X4, X5, X6}$	3.824	4.157	4.490	mA	*1
Output current (4)	IMX8	At 8 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX8 = $I_{X0, X1, X2, X3, X4, X5, X6}$	7.660	8.326	8.992	mA	*1
Output current (5)	IMX15	At 15 mA setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 1 V IMX15 = $I_{X0, X1, X2, X3, X4, X5, X6}$	14.408	15.661	16.914	mA	*1
Leakage Current when matrix LED turns off	IMXOFF	Current OFF setup $V_{X0, X1, X2, X3, X4, X5, X6}$ = 4.75 V IMXOFF = $I_{X0, X1, X2, X3, X4, X5, X6}$	—	—	1	μA	—
The error between channels	IMXCH	The average value of all channels, and the current error of each channel	– 5	—	5	%	—

*1 : Values when recommended parts (ERJ2RHD273X) are used for IREF terminal.
The other current settings are combination of above items.

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Current generator (For RGB color unit)							
Output current (1)	IRGB1	At 1mA setup $V_{R, G, B}$ = 1 V	0.949	1.031	1.113	mA	*1
Output current (2)	IRGB2	At 2 mA setup $V_{R, G, B}$ = 1 V	1.892	2.056	2.220	mA	*1
Output current (3)	IRGB4	At 4 mA setup $V_{R, G, B}$ = 1 V	3.764	4.091	4.418	mA	*1
Output current (4)	IRGB8	At 8 mA setup $V_{R, G, B}$ = 1 V	7.510	8.163	8.816	mA	*1
Leakage Current when RGB turn off	IRGBOFF	Current OFF setup $V_{R, G, B}$ = 4.75 V IRGBOFF = $I_{R, G, B}$	—	—	1	μA	—
The error between channels	IRGBCH	The average value of all channels, and the current error of each channel	– 5	—	5	%	—

*1 : Values when recommended parts (ERJ2RHD273X) are used for IREF terminal.
The other current settings are combination of above items.

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
SPI I/F, LEDCTL, RSTB							
Input voltage range of High-level	VIH	High-level recognition voltage	LDO1 × 0.8	—	LDO2 + 0.3	V	—
Input voltage range of Low-level	VIL	Low-level recognition voltage	– 0.3	—	0.4	V	—
Input current of High-level	IIH	$V_{LEDCTL, RSTB, CE, CLK, DI}$ = 1.85 V IIH = $I_{LEDCTL, RSTB, CE, CLK, DI}$	—	0	1	µA	—
Input current of Low-level	IIL	$V_{LEDCTL, RSTB, CSB, CLK, DI}$ = 0 V IIL = $I_{LEDCTL, RSTB, CE, CLK, DI}$	—	0	1	µA	—
INT							
Output voltage of High-level (1)	VOH1	I_{INT} = – 2 mA VDDSEL = LDO2	LDO2 × 0.8	—	—	V	—
Output voltage of Low-level (1)	VOL1	I_{INT} = 2 mA VDDSEL = LDO2 (I_{INT} = 0.5 mA)	—	—	LDO2 ×0.2 (0.15)	V	—
Output voltage of High-level (2)	VOH2	I_{INT} = – 2 mA VDDSEL = LDO1	LDO1 × 0.8	—	—	V	—
Output voltage of Low-level (2)	VOL2	I_{INT} = 2 mA VDDSEL = LDO1 (I_{INT} = 0.5 mA)	—	—	LDO1 ×0.3 (0.15)	V	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
LDOCNT							
Input voltage range of High-level	VIH	High-level recognition voltage	VB × 0.7	—	VB + 0.3	V	—
Input voltage range of Low-level	VIL	Low-level recognition voltage	– 0.3	—	0.4	V	—
Input current of High-level	IIH	V_{LDOCNT} = 3.6 V IIH = I_{LDOCNT}	—	0	1	µA	—
Input current of Low-level	IIL	V_{LDOCNT} = 0 V IIL = I_{LDOCNT}	—	0	1	µA	—
DO							
Output voltage of High-level	VOH	I_{DO} = – 2 mA	LDO1 × 0.8	—	—	V	—
Output voltage of Low-level	VOL	I_{DO} = 2 mA	—	—	LDO1 × 0.2	V	—

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ELECTRICAL CHARACTERISTICS (continued)

VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Voltage regulator (LDO1) Output capacitor 1 µF, Output capacitor's ESR less than 0.1 Ω							
Rise time	Tsu1	Time until output voltage reaches to 0 V to 90%	—	0.25	—	ms	*2 *3
Fall time	Tsd1	Time until output voltage reaches to 10%	—	5	—	ms	*2 *3
Maximum load current	IOMAX1	—	—	15	—	mA	*3
Load transient response (1)	Vtr11	I_{LDO1} = – 50 µA → – 15 mA (1 µs)	—	70	—	mV	*3
Load transient response (2)	Vtr12	I_{LDO1} = – 15 mA → – 50 µA (1 µs)	—	70	—	mV	*3
Voltage regulator (LDO2) Output capacitor 1 µF, Output capacitor's ESR less than 0.1 Ω							
Rise time	Tsu2	Time until output voltage reaches to 0 V to 90%	—	0.25	—	ms	*2 *3
Fall time	Tsd2	Time until output voltage reaches to 10%	—	5	—	ms	*2 *3
Maximum load current	IOMAX2	—	—	15	—	mA	*3
Load transient response (1)	Vtr21	I_{LDO2} = – 50 µA → – 15 mA (1 µs)	—	70	—	mV	*3
Load transient response (2)	Vtr22	I_{LDO2} = – 15 mA → – 50 µA (1 µs)	—	70	—	mV	*3
TSD (Thermal shutdown circuit)							
Detection temperature	Tdet	Temperature which LDO1, LDO2, Constant current circuit, Matrix SW and RGB turns off.	—	160	—	°C	*3 *4
Return temperature	Tsd11	Returning temperature	—	110	—	°C	*3 *5

Note) *2 : Rise time and Fall time are defined as below.

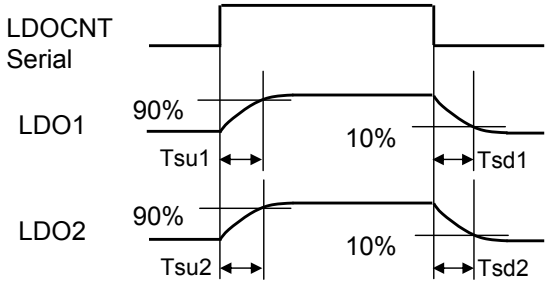
Actual evaluation result of rise time : LDO1 : 290 to 400 µs, LDO2 : 220 to 310 µs

Actual evaluation result of fall time : LDO1 : 6.2 to 8.5 ms, LDO2 : 5.8 to 7.9 ms

*3 : Typical Design Value

*4 : LDO1, LDO2, Constant current circuit, and Matrix SW and RGB are turned off when TSD is High. When TSD is High, the register is set as 14hD1 = 1. However, data can be read only when the register is read immediately after INT occurs since internal regulator is turned off.

*5 : Only LDO1 and LDO2 return after ON state of TSD. A logic part will be in Reset state.



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ELECTRICAL CHARACTERISTICS (continued)

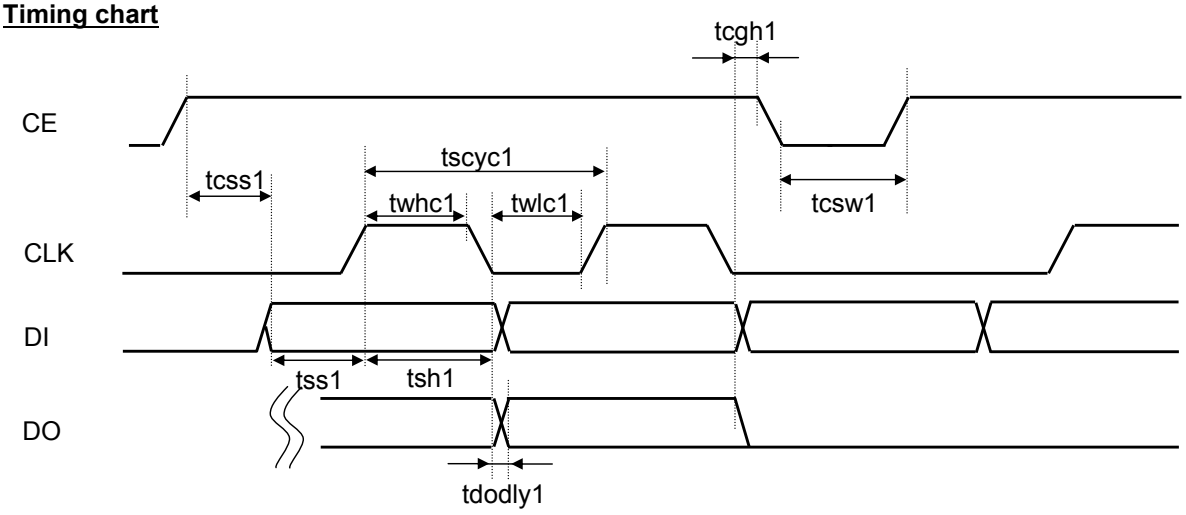
VB = 3.6 V, VLED1 = VLED2 = 4.9 V

Note) T_a = 25 °C ± 2 °C unless otherwise specified.

Parameter	Symbol	Condition	Limits			Unit	Note
			Min	Typ	Max		
Microcomputer interface characteristic (Vdd = 1.85 V ± 3 %) Write access Timing							
CLK cycle time	tscyc1	—	—	125	—	ns	*3
CLK cycle time High period	twhc1	—	—	60	—	ns	*3
CLK cycle time Low period	twlc1	—	—	60	—	ns	*3
Serial-data setup time	tss1	—	—	62	—	ns	*3
Serial-data hold time	tsh1	—	—	62	—	ns	*3
Transceiver interval	tcsw1	—	—	62	—	ns	*3
Chip enable setup time	tcss1	—	—	5	—	ns	*3
Chip enable hold time	tcgh1	—	—	5	—	ns	*3
Microcomputer interface characteristic (Vdd = 1.85 V ± 3 %) Read access Timing							
CLK cycle time	tscyc1	—	—	125	—	ns	*3
CLK cycle time High period	twhc1	—	—	60	—	ns	*3
CLK cycle time Low period	twlc1	—	—	60	—	ns	*3
Serial-data setup time	tss1	—	—	62	—	ns	*3
Serial-data hold time	tsh1	—	—	62	—	ns	*3
Transceiver interval	tcsw1	—	—	62	—	ns	*3
Chip enable setup time	tcss1	—	—	5	—	ns	*3
Chip enable hold time	tcgh1	—	—	5	—	ns	*3
DC delay time	tdodly1	Only read mode	—	25	—	ns	*3

Note) *3 : Typical Design Value

Timing chart



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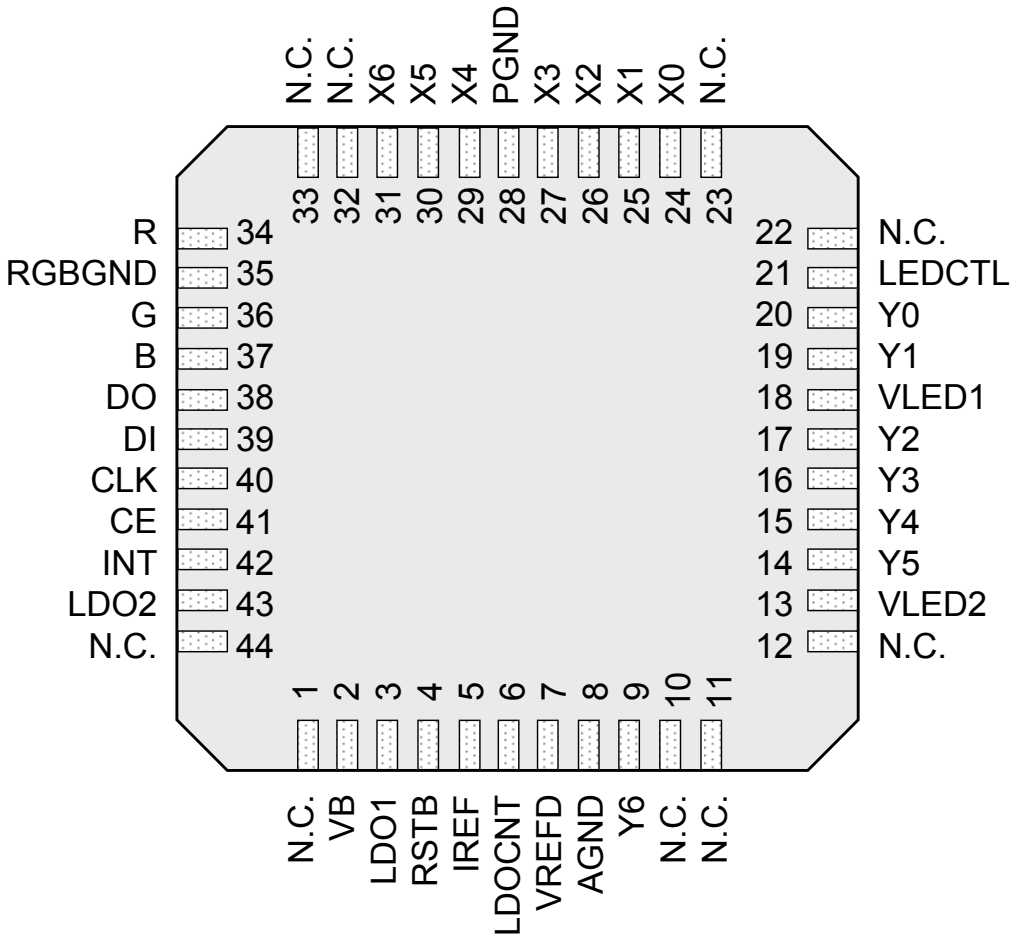
PIN CONFIGURATION

Top View



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PIN FUNCTIONS

Pin No.	Pin name	Type	Description
1 10 11 12 22 23 32 33 44	N.C.	—	No Connection
2	VB	Power supply	The power supply's connect terminal for BGR circuit and LDO circuit.
3	LDO1	Output	LDO1 (1.85 V) output terminal.
4	RSTB	Input	Reset input terminal ("L" active)
5	IREF	Output	The resistance connect terminal for constant current value setup.
6	LDOCNT	Input	ON/OFF control terminal of LDO1 and LDO2.
7	VREFD	Output	BGR circuit output terminal.
8	AGND	Ground	The GND terminal for Analog circuitry.
9	Y6	Output	The output terminal of matrix switching control. It connects with the G Column of matrix LED.
13 18	VLED2 VLED1	Power supply	The power supply's connect terminal for matrix LED. Connect with the output of battery or step-up DC/DC converter
14	Y5	Output	The output terminal of matrix switching control. It connects with the F Column of matrix LED.
15	Y4	Output	The output terminal of matrix switching control. It connects with the E Column of matrix LED.
16	Y3	Output	The output terminal of matrix switching control. It connects with the D Column of matrix LED.
17	Y2	Output	The output terminal of matrix switching control. It connects with the C Column of matrix LED.
19	Y1	Output	The output terminal of matrix switching control. It connects with the B Column of matrix LED.
20	Y0	Output	The output terminal of matrix switching control. It connects with the A Column of matrix LED.
21	LEDCTL	Input	LED's lighting ON/OFF control terminal. (It is based on register 0Ah.)

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PIN FUNCTIONS (continued)

Pin No.	Pin name	Type	Description
24	X0	Output	Constant current circuit. The output terminal of PWM control. It connects with the 1st Row of matrix LED.
25	X1	Output	Constant current circuit. The output terminal of PWM control. It connects with the 2nd Row of matrix LED.
26	X2	Output	Constant current circuit. The output terminal of PWM control. It connects with the 3rd Row of matrix LED.
27	X3	Output	Constant current circuit. The output terminal of PWM control. It connects with the 4th Row of matrix LED.
28	PGND	Ground	The GND terminal for matrix LED
29	X4	Output	Constant current circuit. The output terminal of PWM control. It connects with the 5th Row of matrix LED.
30	X5	Output	Constant current circuit. The output terminal of PWM control. It connects with the 6th Row of matrix LED.
31	X6	Output	Constant current circuit. The output terminal of PWM control. It connects with the 7th Row of matrix LED.
34	R	Output	LED contact terminal.
35	RGBGND	Ground	The GND terminal for RGB terminal.
36	G	Output	LED contact terminal.
37	B	Output	LED contact terminal.
38	DO	Output	Data output terminal for SPI interface.
39	DI	Input	Data input terminal for SPI interface.
40	CLK	Input	Clock input terminal for SPI interface.
41	CE	Input	Chip-enable terminal for SPI1 interface. ("H" active)
42	INT	Output	Interrupt output terminal.
43	LDO2	Output	LDO2 (2.85 V) output terminal.

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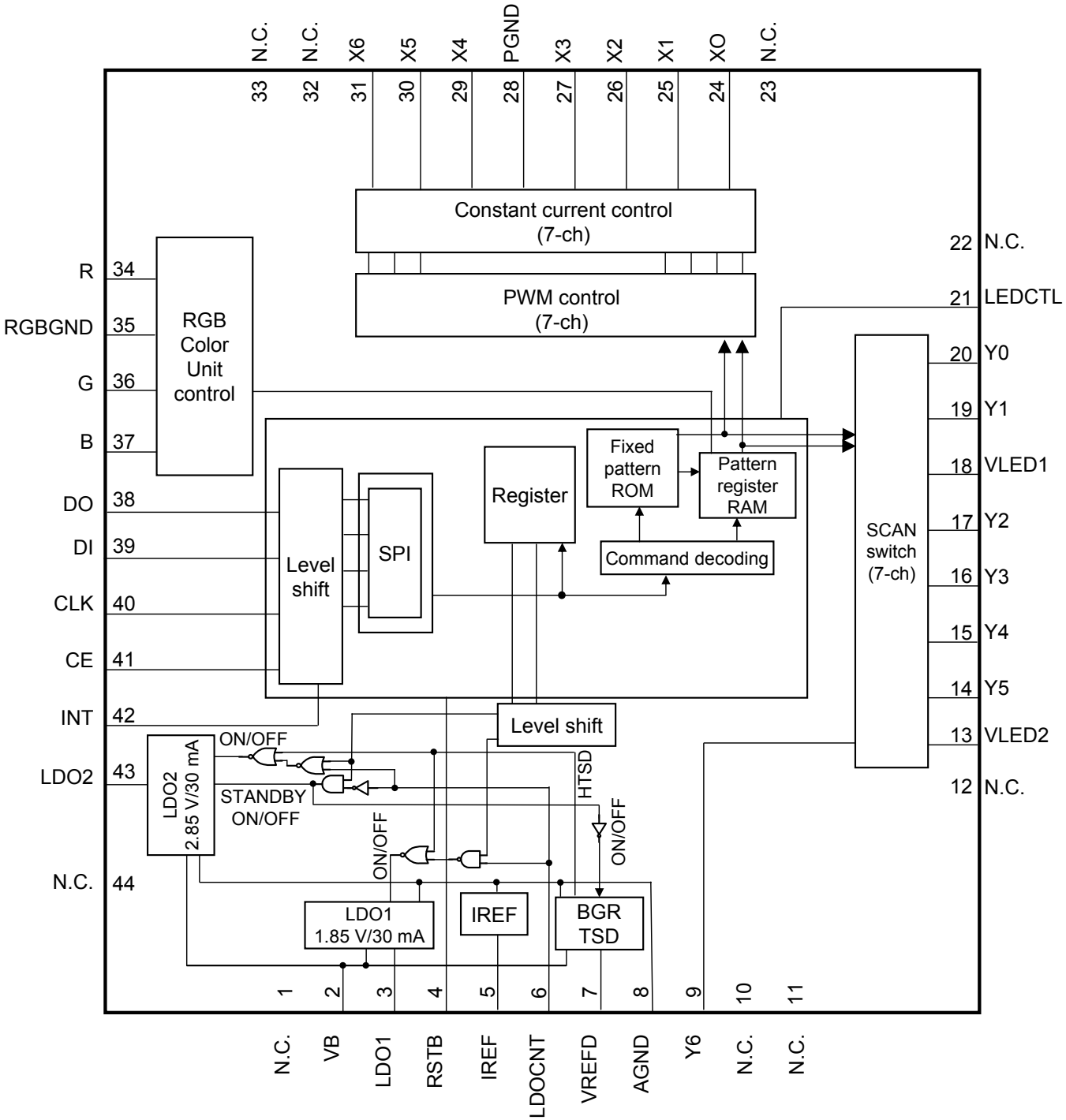
FUNCTIONAL BLOCK DIAGRAM



Notes: This block diagram is for explaining functions. Part of the block diagram may be omitted, or it may be simplified.

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OPERATION

1. Explanation in each mode (Power supply starting sequence)

Mode	LDOCNT	REG18	REG28	Note
OFF	Low	0	0	• It is necessary to make it LDOCNT = High for the return from OFF-mode.
OFF → Normal mode	"L" → "H"	0/1	0/1	• The signal from serial interface is not received in LDOCNT = Low and the state of REG28 = Low or REG18 = Low. • It shifts to standby mode with LDOCNT = Low and REG28 = High. • The signal from serial interface is not received at Standby-mode. (Power supply for Logic is LDO1 and LDO2.) Therefore, standby release by the signal from serial interface cannot be performed. • In Standby-mode, if LDOCNT is switched to High from Low, it will return to the normal mode. • It cannot shift to OFF-mode from Standby-mode. Once returning to the normal mode, please shift to OFF-mode.
	"H"	0/1	0/1	
Normal mode → OFF	"H" → "L"	0	0	• Regardless of the value of REG18, LDO1 turns on at LDOCNT = High. • Regardless of the value of REG28, LDO2 turns on at LDOCNT = High. • Serial interface signal is not received at RSTB = Low • 5 ms after being set to LDOCNT = High, the receptionist of serial interface signal is attained. • RSTB terminal prohibits the input signal of those other than a rectangle wave. • All register setting become default setting if RSTB = Low • (The default setting of REG18 and REG28 are [1] • If RSTB = Low before LDOCNT = Low, LDO1 and LDO2 can't turn off.) • All register setting become default setting when LDO2 turn off. • The setting order to change off mode is as following. • REG18, 28 = [0] → LDOCNT = "L" → RSTB = "L"
Normal mode → Standby mode		0	1	

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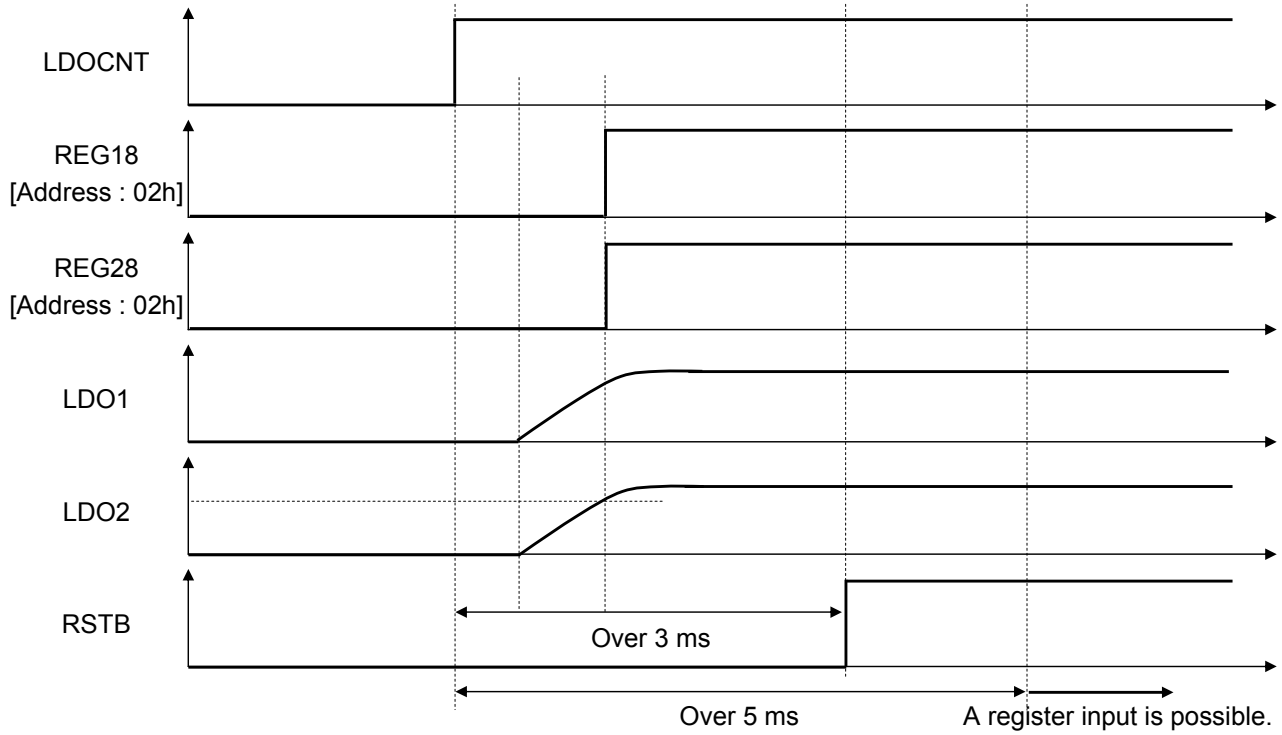
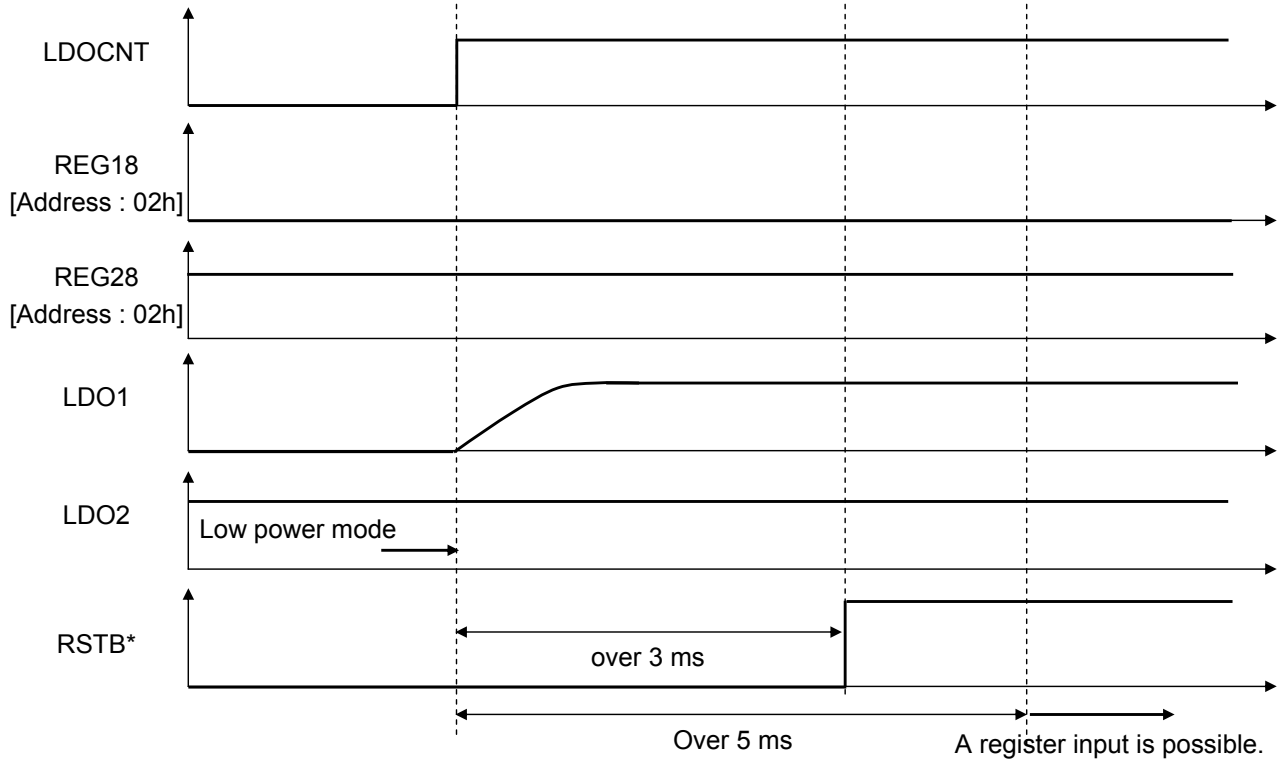
OPERATION (continued)

1. Explanation in each mode (Power supply starting sequence) (continued)

- Shift to the Normal mode from OFF-mode



- Shift to the Normal mode from Standby mode



* It is a waveform in the case of applying reset to register setup at Standby mode.
* Maintain the state of RSTB = High to hold the register setup.

Established : 2007-05-24
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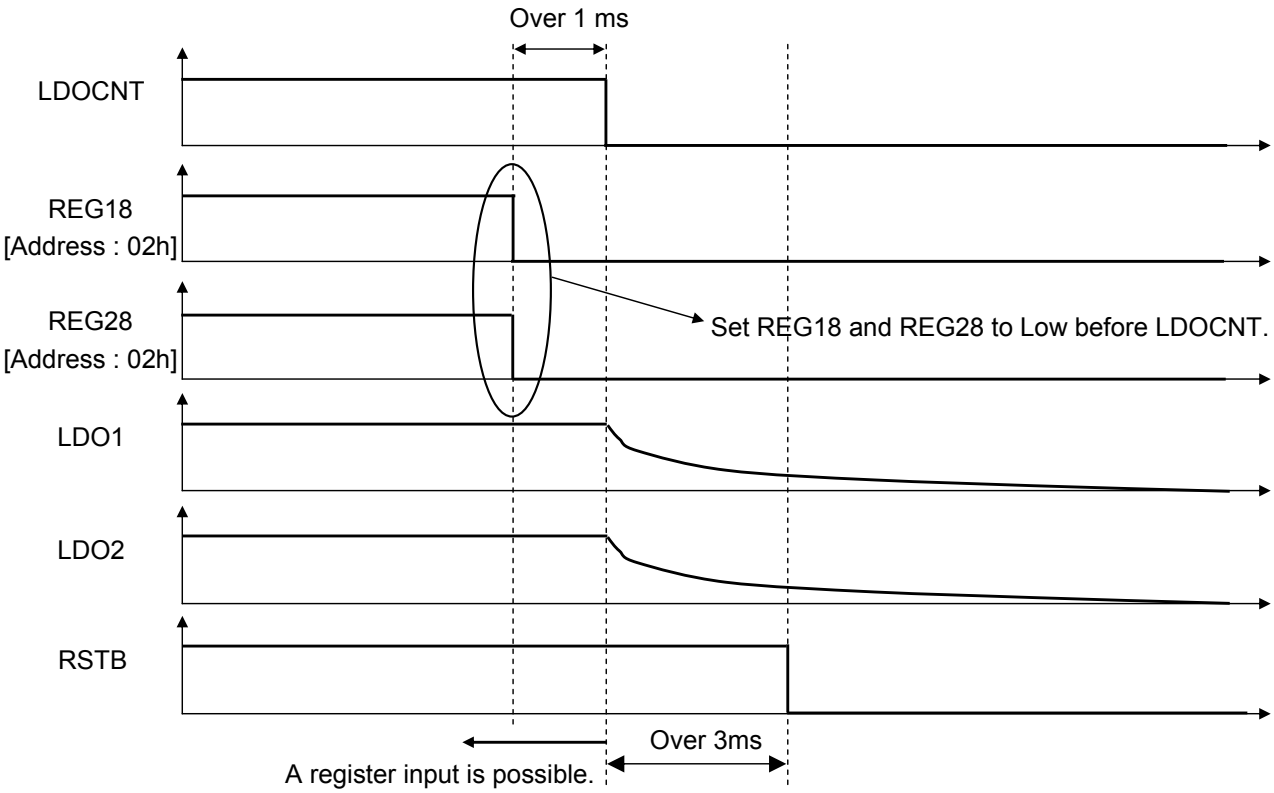
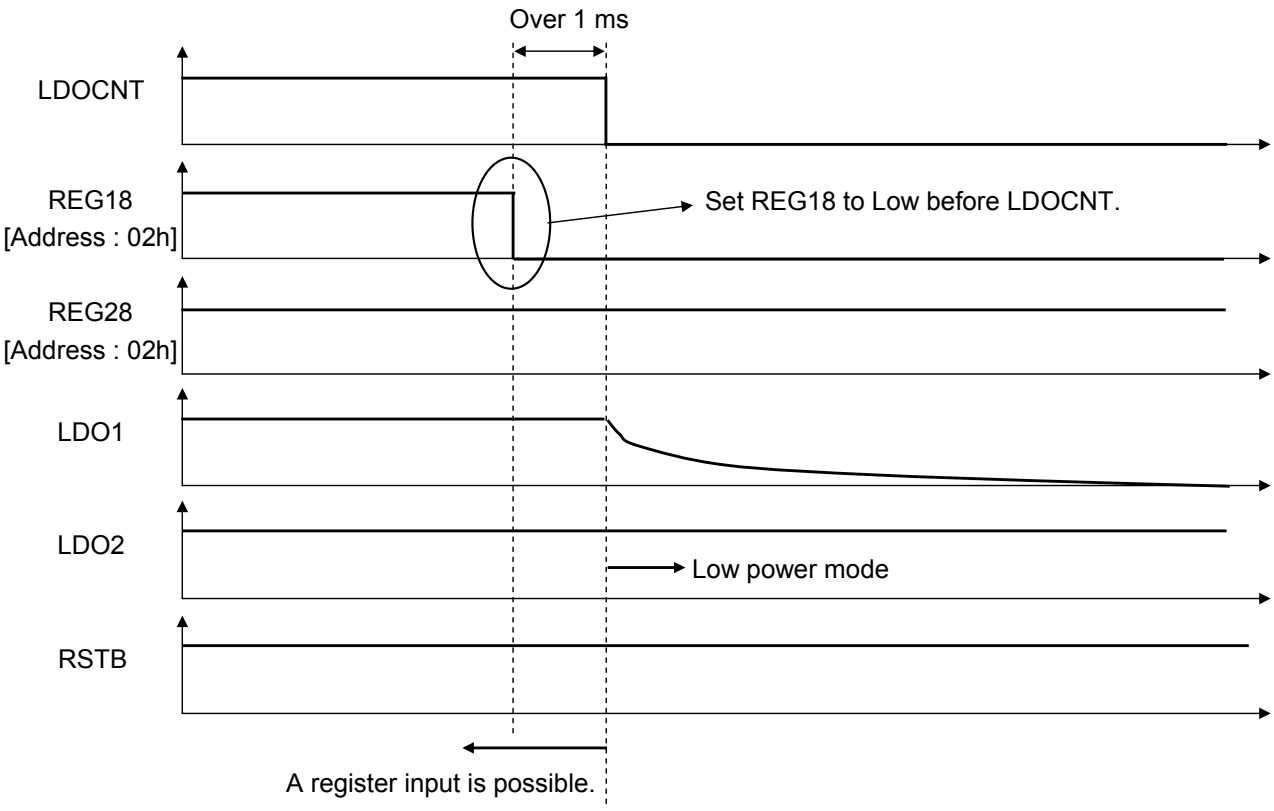
OPERATION (continued)

1. Explanation in each mode (Power supply starting sequence) (continued)

- Shift to the OFF-mode from Normal mode



- Shift to the Standby mode from Normal mode



Established : 2007-05-24
Revised : 2013-04-15

OPERATION (continued)

1. Explanation in each mode (Power supply starting sequence) (continued)

- Shift to the OFF-mode from Normal mode

VBAT	LDOCNT	MODE
"L"	"L"	OFF
"L"	"H"	Prohibition
"H"	"L"	OFF
"H"	"H"	ON

Note) "L" in column of VBAT and LDOCNT means 0 V, "H" means 3.1 to 4.6 V (operating supply voltage range).

- Logic pin condition

The following setting is common for OFF, Standby and Normal mode.
The pin setting when RSTB = Low, under Normal mode is as follows.

Pin name	Pin state	Logic*
INT	Output	"L"
CE	Input	"L"
CLK	Input	"L"
DI	Input	"L"
DO	Output	"L"
LEDCTL	Input	"L"
LDOCNT	Input	Depends on each mode

Note)*: Logic state for pins indicated as “Output” under Pin state shows the output level.
Logic state for pins indicated as “Input” under Pin state shows the input level to be set to the pins.

Established : 2007-05-24
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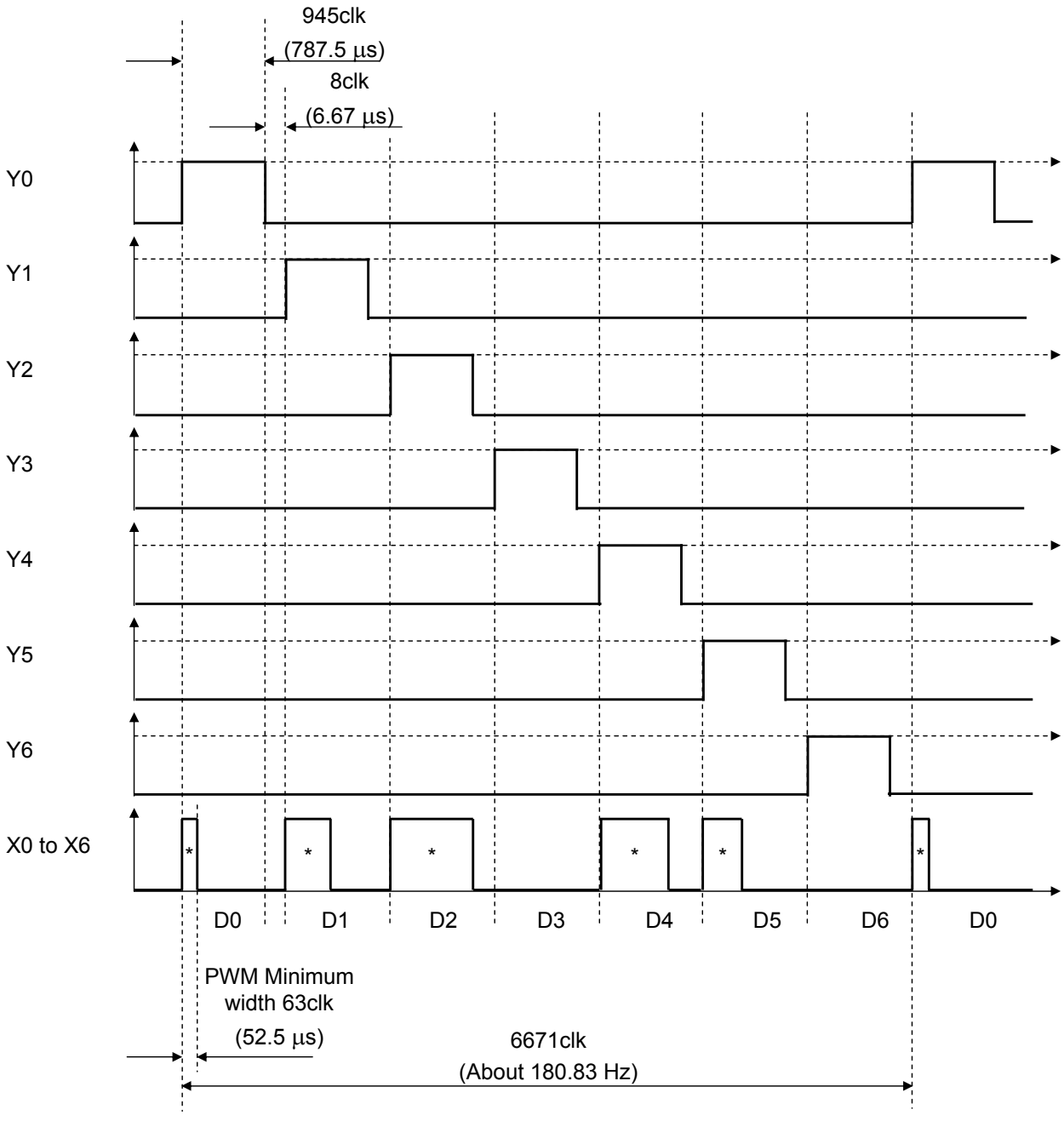
OPERATION (continued)

2. Explanation of operation

- Matrix part operation waveform

- The following waveform is an internal signal. In following Yx = Xx = Low, the waveform of actual Yx terminal is set to Hi-Z.
- It is controlled by internal 1.2 MHz clock in default condition.
- Y side switches from Y0 to Y6 in that order. The turning on term of each pin is constant 945clock (787.5 µs) and each turning on term includes 8clock (6.67 µs) interval.
- "*" mark shows the turning on term and D3, D6 is the turning off term in the following figure.
- 7×7 matrix display is controlled by X0 to X6 with Yx switching timing.



Established : 2007-05-24
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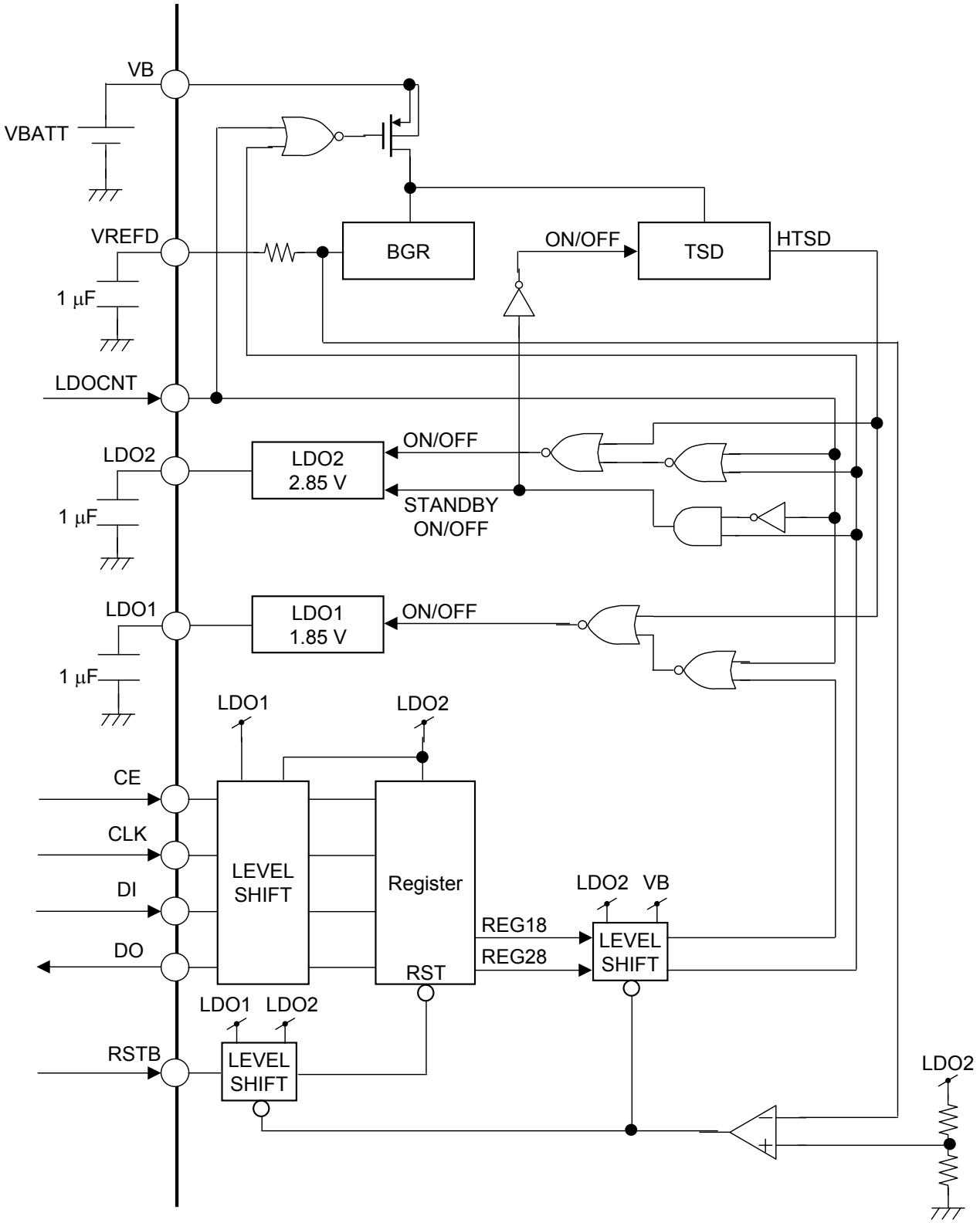
OPERATION (continued)

3. Block configuration

- RESET part block configuration



All the logic portions to which the power supply is not connected are connected to VB as power supplies.

Established : 2007-05-24
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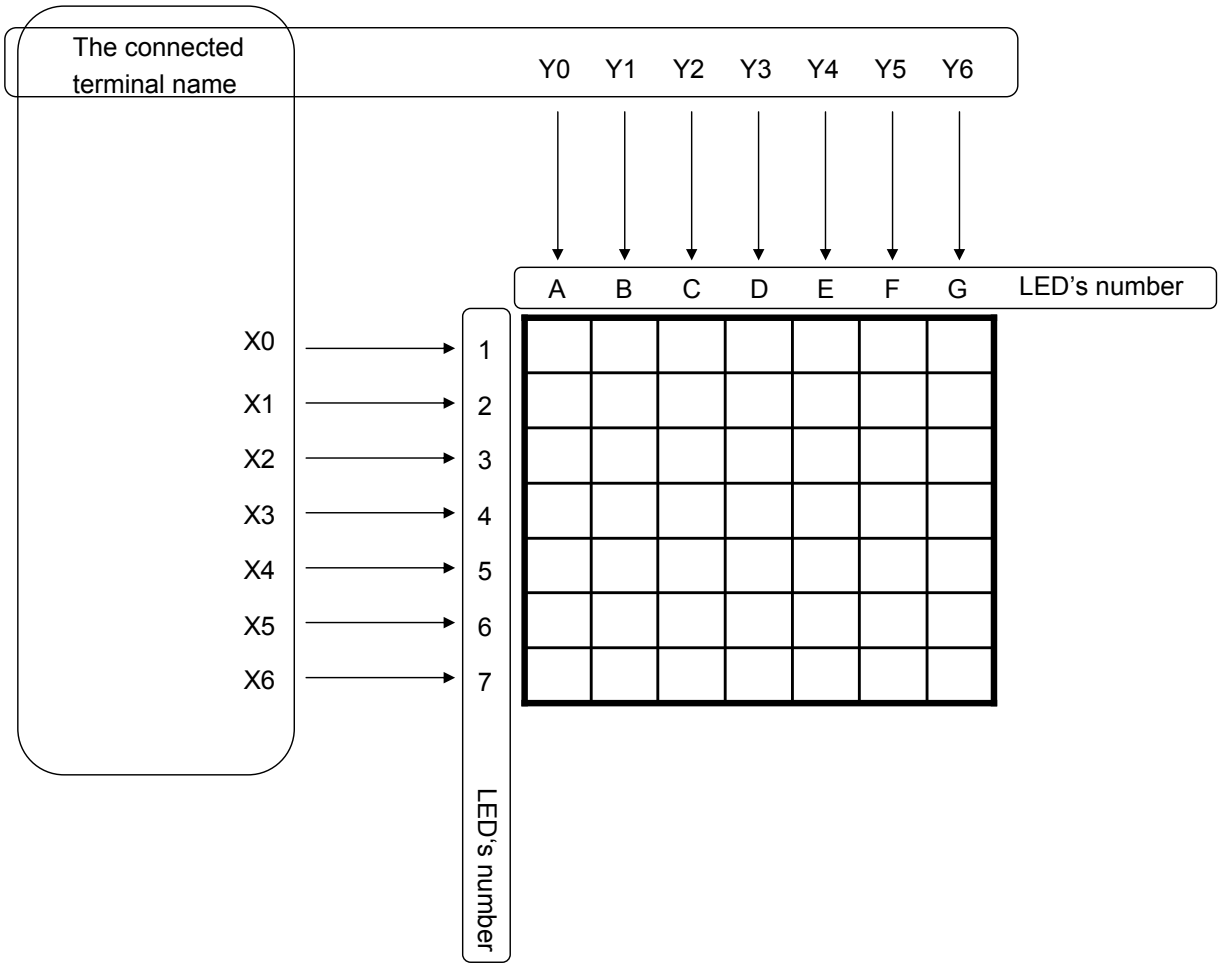
OPERATION (continued)

3. Block configuration (continued)

- Explanation of matrix LED part, matrix LED's number

- LED matrix driver circuit can display character and pattern by controlling the 7×7 matrix LED individually.
- In this specification, LED's number controlled by each terminal can be matched off against the following figure.
- It is controlled by internal 1.2 MHz clock in default condition.
- In the scroll mode, LED matrix can move the display of character from right to left as the following arrangement.



Established : 2007-05-24
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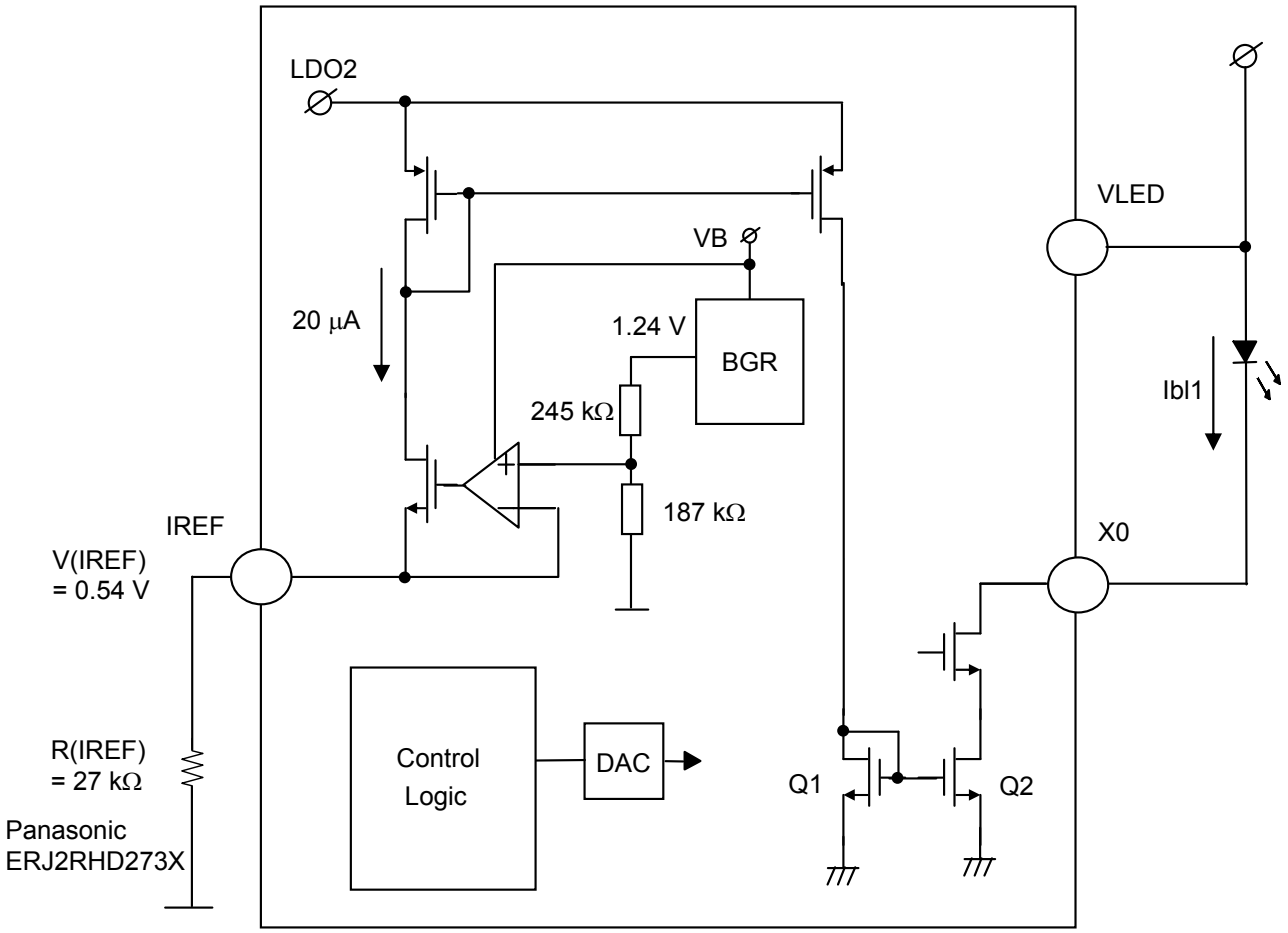
OPERATION (continued)

3. Block configuration (continued)

- Equivalent circuit of matrix LED driver

X0 terminal case



- The reference current for constant current driver is calculated by the following formula.
  V(IREF) / R(IREF) = 0.54 V / 27 kΩ = 20 μA
- The LED driver current can be set from 0 mA to 30 mA by register setting via serial interface.
- The constant current value can be changed by the external resistor value of IREF terminal, but the accuracy in case of that setting is not guaranteed.
- ERJ2RHD273X is recommended for the external resistor of IREF terminal to keep the constant current accuracy.

Established : 2007-05-24
Revised : 2013-04-15

OPERATION (continued)

4. Register and Address

- Register Map

Sub address	R/W	Data name	Data							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	W	POWERCNT	—	—	—	—	—	OSCEN	—	—
02h	W	LDOCNT	—	—	—	—	—	—	REG18	REG28
03h	For test									
04h	For test									
05h	For test									
06h	For test									
07h	For test									
08h	For test									
09h	For test									
0Ah	W	LEDCTL	LEDACT	—	—	—	—	DISMTX	DISRGB	—
10h	For test									
11h	For test									
12h	For test									
13h	For test									
14h	R	IOFACTOR	FACGD1	—	—	—	RAM ACT	FRMINT	CPUWRER	TSD
15h	For test									
16h	For test									
17h	For test									
18h	For test									
19h	For test									
1Ah	W/R	VDDSEL	INTVSEL	—	—	—	—	—	—	—

Established : 2007-05-24
Revised : 2013-04-15

OPERATION (continued)

4. Register and Address (continued)

- Register Map (continued)

Sub Address	R/W	Data Name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
20h	R/W	MTXON	—	—	—	—	—	—	—	MTXON
21h	R/W	MTXDATA	MTXDATA[7:0]							
22h	R/W	FFROM	—	—	—	—	—	—	ROM77[1:0]	
23h	R/W	ROMSEL	SELROM[7:0]							
24h	R/W	RAMCOPY	—	—	—	—	—	—	SELRAM	COPYSTART
25h	R/W	SETFROM	SETFROM[7:0]							
26h	R/W	SETTO	SETTO[7:0]							
27h	R/W	REPON	—	—	—	—	—	—	—	REPON
28h	R/W	SETTIME	—	—	—	—	—	—	SETTIME[1:0]	
29h	R/W	RAMRST	—	—	—	—	—	—	RAM1	RAM2
2Ah	R/W	SCROLL	—	—	—	—	—	—	—	SCLON
2Bh	For test									
2Ch	R/W	RGBON	—	—	—	—	—	—	—	RGBON
2Dh	R/W	RGBDATA	—	—	RGBDATA[5:0]					
2Eh	For test									
30h	R/W	RAMNUM	—	—	—	—	—	—	—	RAMNUM
⋮										
6Bh	For test									
6Dh	For test									
6Fh	For test									
70h	For test									
71h	For test									
72h	For test									
73h	For test									
74h	For test									
75h	For test									
76h	For test									
77h	For test									

* Access the address from 6Bh to 77h is prohibited.

Established : 2007-05-24
Revised : 2013-04-15

OPERATION (continued)

4. Register and Address (continued)

RAM address map

Sub Address	Data Name	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
31h	A1	BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
32h	A2	BLA2[3:0]				FRA2[1:0]		DLA2[1:0]	
33h	A3	BLA3[3:0]				FRA3[1:0]		DLA3[1:0]	
34h	A4	BLA4[3:0]				FRA4[1:0]		DLA4[1:0]	
35h	A5	BLA5[3:0]				FRA5[1:0]		DLA5[1:0]	
36h	A6	BLA6[3:0]				FRA6[1:0]		DLA6[1:0]	
37h	A7	BLA7[3:0]				FRA7[1:0]		DLA7[1:0]	
38h	B1	BLB1[3:0]				FRB1[1:0]		DLB1[1:0]	
39h	B2	BLB2[3:0]				FRB2[1:0]		DLB2[1:0]	
3Ah	B3	BLB3[3:0]				FRB3[1:0]		DLB3[1:0]	
3Bh	B4	BLB4[3:0]				FRB4[1:0]		DLB4[1:0]	
3Ch	B5	BLB5[3:0]				FRB5[1:0]		DLB5[1:0]	
3Dh	B6	BLB6[3:0]				FRB6[1:0]		DLB6[1:0]	
3Eh	B7	BLB7[3:0]				FRB7[1:0]		DLB7[1:0]	
3Fh	C1	BLC1[3:0]				FRC1[1:0]		DLC1[1:0]	
40h	C2	BLC2[3:0]				FRC2[1:0]		DLC2[1:0]	
41h	C3	BLC3[3:0]				FRC3[1:0]		DLC3[1:0]	
42h	C4	BLC4[3:0]				FRC4[1:0]		DLC4[1:0]	
43h	C5	BLC5[3:0]				FRC5[1:0]		DLC5[1:0]	
44h	C6	BLC6[3:0]				FRC6[1:0]		DLC6[1:0]	
45h	C7	BLC7[3:0]				FRC7[1:0]		DLC7[1:0]	
46h	D1	BLD1[3:0]				FRD1[1:0]		DLD1[1:0]	
47h	D2	BLD2[3:0]				FRD2[1:0]		DLD2[1:0]	
48h	D3	BLD3[3:0]				FRD3[1:0]		DLD3[1:0]	
49h	D4	BLD4[3:0]				FRD4[1:0]		DLD4[1:0]	
4Ah	D5	BLD5[3:0]				FRD5[1:0]		DLD5[1:0]	
4Bh	D6	BLD6[3:0]				FRD6[1:0]		DLD6[1:0]	
4Ch	D7	BLD7[3:0]				FRD7[1:0]		DLD7[1:0]	

OPERATION (continued)

4. Register and Address (continued)

RAM address map (continued)

Sub Address	Data Name	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
4Dh	E1	BLE1[3:0]				FRE1[1:0]		DLE1[1:0]	
4Eh	E2	BLE2[3:0]				FRE2[1:0]		DLE2[1:0]	
4Fh	E3	BLE3[3:0]				FRE3[1:0]		DLE3[1:0]	
50h	E4	BLE4[3:0]				FRE4[1:0]		DLE4[1:0]	
51h	E5	BLE5[3:0]				FRE5[1:0]		DLE5[1:0]	
52h	E6	BLE6[3:0]				FRE6[1:0]		DLE6[1:0]	
53h	E7	BLE7[3:0]				FRE7[1:0]		DLE7[1:0]	
54h	F1	BLF1[3:0]				FRF1[1:0]		DLF1[1:0]	
55h	F2	BLF2[3:0]				FRF2[1:0]		DLF2[1:0]	
56h	F3	BLF3[3:0]				FRF3[1:0]		DLF3[1:0]	
57h	F4	BLF4[3:0]				FRF4[1:0]		DLF4[1:0]	
58h	F5	BLF5[3:0]				FRF5[1:0]		DLF5[1:0]	
59h	F6	BLF6[3:0]				FRF6[1:0]		DLF6[1:0]	
5Ah	F7	BLF7[3:0]				FRF7[1:0]		DLF7[1:0]	
5Bh	G1	BLG1[3:0]				FRG1[1:0]		DLG1[1:0]	
5Ch	G2	BLG2[3:0]				FRG2[1:0]		DLG2[1:0]	
5Dh	G3	BLG3[3:0]				FRG3[1:0]		DLG3[1:0]	
5Eh	G4	BLG4[3:0]				FRG4[1:0]		DLG4[1:0]	
5Fh	G5	BLG5[3:0]				FRG5[1:0]		DLG5[1:0]	
60h	G6	BLG6[3:0]				FRG6[1:0]		DLG6[1:0]	
61h	G7	BLG7[3:0]				FRG7[1:0]		DLG7[1:0]	
62h	LEDR	BLLEDR[3:0]				FRLEDR[1:0]		DLLEDR[1:0]	
63h	LEDG	BLLEDG[3:0]				FRLEDG[1:0]		DLLEDG[1:0]	
64h	LEDB	BLLEDB[3:0]				FRLEDB[1:0]		DLLEDB[1:0]	

Established : 2007-05-24
Revised : 2013-04-15

OPERATION (continued)

4. Register and Address (continued)

- ROM Address Map

[00000000] - [10010101] : ROM(Only luminosity) 7 × 7 Pattern No.0 (default) to Pattern No.149

Pattern No.	Contents of the pattern	Display
0	All putting out lights	Nothing
1	Number	0
2	Number	1
3	Number	2
4	Number	3
5	Number	4
6	Number	5
7	Number	6
8	Number	7
9	Number	8
10	Number	9
11	Alphabetic character	A
12	Alphabetic character	B
13	Alphabetic character	C
14	Alphabetic character	D
15	Alphabetic character	E
16	Alphabetic character	F
17	Alphabetic character	G
18	Alphabetic character	H
19	Alphabetic character	I
20	Alphabetic character	J
21	Alphabetic character	K
22	Alphabetic character	L
23	Alphabetic character	M
24	Alphabetic character	N
25	Alphabetic character	O
26	Alphabetic character	P
27	Alphabetic character	Q
28	Alphabetic character	R
29	Alphabetic character	S
30	Alphabetic character	T

Pattern No.	Contents of the pattern	Display
31	Alphabetic character	U
32	Alphabetic character	V
33	Alphabetic character	W
34	Alphabetic character	X
35	Alphabetic character	Y
36	Alphabetic character	Z
37	Alphabetic character	a
38	Alphabetic character	b
39	Alphabetic character	c
40	Alphabetic character	d
41	Alphabetic character	e
42	Alphabetic character	f
43	Alphabetic character	g
44	Alphabetic character	h
45	Alphabetic character	i
46	Alphabetic character	j
47	Alphabetic character	k
48	Alphabetic character	l
49	Alphabetic character	m
50	Alphabetic character	n
51	Alphabetic character	o
52	Alphabetic character	p
53	Alphabetic character	q
54	Alphabetic character	r
55	Alphabetic character	s
56	Alphabetic character	t
57	Alphabetic character	u
58	Alphabetic character	v
59	Alphabetic character	w
60	Alphabetic character	x
61	Alphabetic character	y

Established : 2007-05-24
Revised : 2013-04-15

OPERATION (continued)

4. Register and Address (continued)

• ROM Address Map (continued)

[00000000] - [10010101] : ROM(Only luminosity) 7×7 Pattern No.0 (default) to Pattern No.149

Pattern No.	Contents of the pattern	Display
62	Alphabetic character	z
63	Number	00
64	Number	01
65	Number	02
66	Number	03
67	Number	04
68	Number	05
69	Number	06
70	Number	07
71	Number	08
72	Number	09
73	Number	10
74	Number	11
75	Number	12
76	Number	13
77	Number	14
78	Number	15
79	Number	16
80	Number	17
81	Number	18
82	Number	19
83	Number	20
84	Number	21
85	Number	22
86	Number	23
87	Number	24
88	Number	25
89	Number	26
90	Number	27
91	Number	28
92	Number	29

Pattern No.	Contents of the pattern	Display
93	Number	30
94	Number	31
95	Number	32
96	Number	33
97	Number	34
98	Number	35
99	Number	36
100	Number	37
101	Number	38
102	Number	39
103	Number	40
104	Number	41
105	Number	42
106	Number	43
107	Number	44
108	Number	45
109	Number	46
110	Number	47
111	Number	48
112	Number	49
113	Number	50
114	Number	51
115	Number	52
116	Number	53
117	Number	54
118	Number	55
119	Number	56
120	Number	57
121	Number	58
122	Number	59
123	Number	60

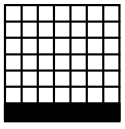
Established : 2007-05-24
Revised : 2013-04-15

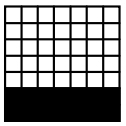
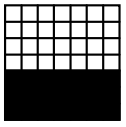
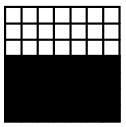
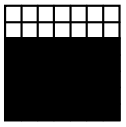
OPERATION (continued)

4. Register and Address (continued)

• ROM Address Map (continued)

[00000000] - [10010101] : ROM(Only luminosity) 7×7 Pattern No.0 (default) to Pattern No.149

Pattern No.	Contents of the pattern	Display
124	Symbol	Zero antenna
125	Symbol	One antenna
126	Symbol	Two antenna
127	Symbol	Three antenna
128	Symbol	▶
129	Symbol	■
130	Symbol	‖
131	Symbol	>>
132	Symbol	<<
133	Symbol	:
134	Symbol	!
135	Symbol	?
136	Symbol	▲
137	Symbol	▼
138	Symbol	←
139	Symbol	→
140	Symbol	+
141	Symbol	-
142	Symbol	/
143	Symbol	

Pattern No.	Contents of the pattern	Display
144	Symbol	
145	Symbol	
146	Symbol	
147	Symbol	
148	Symbol	
149	Symbol	

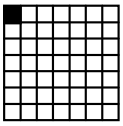
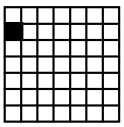
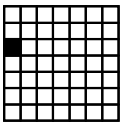
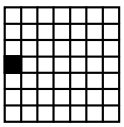
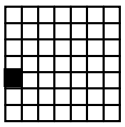
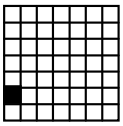
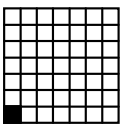
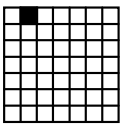
Established : 2007-05-24
Revised : 2013-04-15

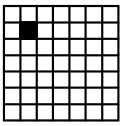
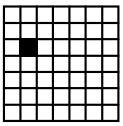
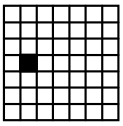
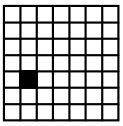
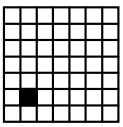
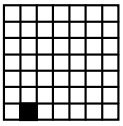
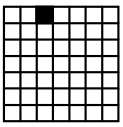
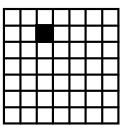
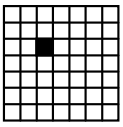
OPERATION (continued)

4. Register and Address (continued)

- ROM Address Map (continued)

[10010110] - [11010000] : ROM(Luminosity + Cycle + Delay) 7 × 7 Pattern No.150 to Pattern No.208

Pattern No.	Contents of the pattern	Display
150	Gradation	
151	Gradation	
152	Gradation	
153	Gradation	
154	Gradation	
155	Gradation	
156	Gradation	
157	Gradation	
158	Gradation	

Pattern No.	Contents of the pattern	Display
159	Gradation	
160	Gradation	
161	Gradation	
162	Gradation	
163	Gradation	
164	Gradation	
165	Gradation	
166	Gradation	
167	Gradation	

Established : 2007-05-24
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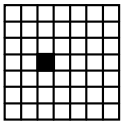
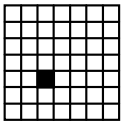
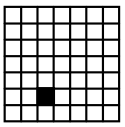
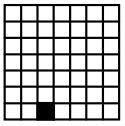
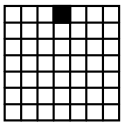
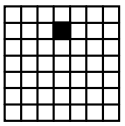
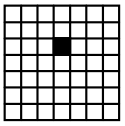
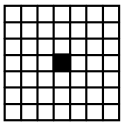
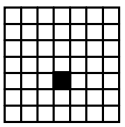
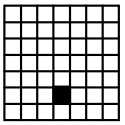
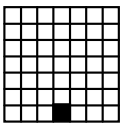
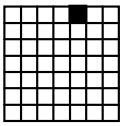
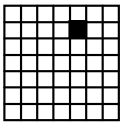
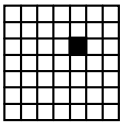
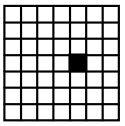
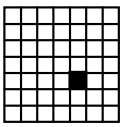
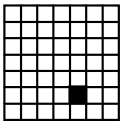
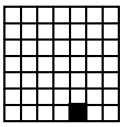
OPERATION (continued)

4. Register and Address (continued)

- ROM Address Map (continued)

[10010110] - [11010000] : ROM(Luminosity + Cycle + Delay) 7 × 7 Pattern No.150 to Pattern No.208

Pattern No.	Contents of the pattern	Display
168	Gradation	
169	Gradation	
170	Gradation	
171	Gradation	
172	Gradation	
173	Gradation	
174	Gradation	
175	Gradation	
176	Gradation	

Pattern No.	Contents of the pattern	Display
177	Gradation	
178	Gradation	
179	Gradation	
180	Gradation	
181	Gradation	
182	Gradation	
183	Gradation	
184	Gradation	
185	Gradation	

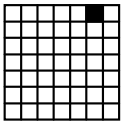
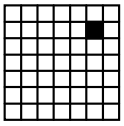
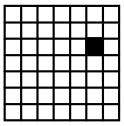
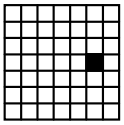
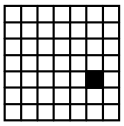
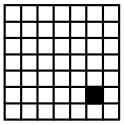
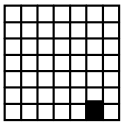
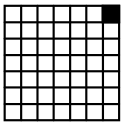
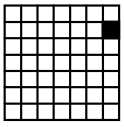
Established : 2007-05-24
Revised : 2013-04-15

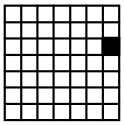
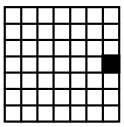
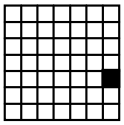
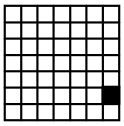
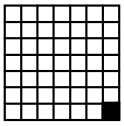
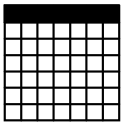
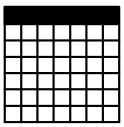
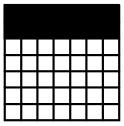
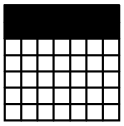
OPERATION (continued)

4. Register and Address (continued)

- ROM Address Map (continued)

[10010110] - [11010000] : ROM(Luminosity + Cycle + Delay) 7 × 7 Pattern No.150 to Pattern No.208

Pattern No.	Contents of the pattern	Display
186	Gradation	
187	Gradation	
188	Gradation	
189	Gradation	
190	Gradation	
191	Gradation	
192	Gradation	
193	Gradation	
194	Gradation	

Pattern No.	Contents of the pattern	Display
195	Gradation	
196	Gradation	
197	Gradation	
198	Gradation	
199	Gradation	
200	Gradation	
201	Gradation	
202	Gradation	
203	Gradation	

Established : 2007-05-24
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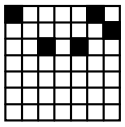
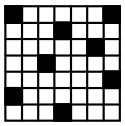
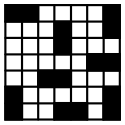
OPERATION (continued)

4. Register and Address (continued)

- ROM Address Map (continued)

[10010110] - [11010000] : ROM(Luminosity + Cycle + Delay) 7 × 7 Pattern No.150 to Pattern No.208

Pattern No.	Contents of the pattern	Display
204	Gradation	
205	Gradation	
206	Gradation	
207	Gradation	
208	Gradation	

Established : 2007-05-24
Revised : 2013-04-15

OPERATION (continued)

4. Register and Address (continued)

- Register table which needs a clock

About the following addresses, even if an internal clock or an external clock does not exist,
Read / Write is possible in the data to register. However, it cannot be given to operation finally needed.

Sub Address	R/W	Data Name	DATA							
			D7	D6	D5	D4	D3	D2	D1	D0
01h	W	POWERCNT	—	—	—	—	—	OSCEN	—	—
14h	R	IOFACTOR	FACG D1	—	—	—	RAM ACT	FRMINT	CPU WRER	TSD
20h	R/W	MTXON	—	—	—	—	—	—	—	MTXON
21h	R/W	MTXDATA	MTXDATA[7:0]							
22h	R/W	FFROM	—	—	—	—	—	—	ROM77[1:0]	
23h	R/W	ROMSEL	SELROM[7:0]							
24h	R/W	RAMCOPY	—	—	—	—	—	—	SELRAM	COPY START
25h	R/W	SETFROM	SETFROM[7:0]							
26h	R/W	SETTO	SETTO[7:0]							
27h	R/W	REPON	—	—	—	—	—	—	—	REPON
28h	R/W	SETTIME	—	—	—	—	—	—	SETTIME[1:0]	
29h	R/W	RAMRST	—	—	—	—	—	—	RAM1	RAM2
2Ah	R/W	SCROLL	—	—	—	—	—	—	—	SCLON
2Bh	R/W	SCLTIME	—	—	—	—	—	—	SCLTIME[1:0]	
2Ch	R/W	RGBON	—	—	—	—	—	—	—	RGBON
2Dh	R/W	RGBDATA	—	—	RGBDATA[5:0]					
30h	R/W	RAMNUM	—	—	—	—	—	—	—	RAMNUM

Established : 2007-05-24
Revised : 2013-04-15

OPERATION (continued)

4. Register and Address (continued)

- Register table which needs a clock (continued)

About the following addresses, when an internal clock or an external clock does not exist, data cannot be Read / Write in at register.

Sub Address	Data Name	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
31h	A1	BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
32h	A2	BLA2[3:0]				FRA2[1:0]		DLA2[1:0]	
33h	A3	BLA3[3:0]				FRA3[1:0]		DLA3[1:0]	
34h	A4	BLA4[3:0]				FRA4[1:0]		DLA4[1:0]	
35h	A5	BLA5[3:0]				FRA5[1:0]		DLA5[1:0]	
36h	A6	BLA6[3:0]				FRA6[1:0]		DLA6[1:0]	
37h	A7	BLA7[3:0]				FRA7[1:0]		DLA7[1:0]	
38h	B1	BLB1[3:0]				FRB1[1:0]		DLB1[1:0]	
39h	B2	BLB2[3:0]				FRB2[1:0]		DLB2[1:0]	
3Ah	B3	BLB3[3:0]				FRB3[1:0]		DLB3[1:0]	
3Bh	B4	BLB4[3:0]				FRB4[1:0]		DLB4[1:0]	
3Ch	B5	BLB5[3:0]				FRB5[1:0]		DLB5[1:0]	
3Dh	B6	BLB6[3:0]				FRB6[1:0]		DLB6[1:0]	
3Eh	B7	BLB7[3:0]				FRB7[1:0]		DLB7[1:0]	
3Fh	C1	BLC1[3:0]				FRC1[1:0]		DLC1[1:0]	
40h	C2	BLC2[3:0]				FRC2[1:0]		DLC2[1:0]	
41h	C3	BLC3[3:0]				FRC3[1:0]		DLC3[1:0]	
42h	C4	BLC4[3:0]				FRC4[1:0]		DLC4[1:0]	
43h	C5	BLC5[3:0]				FRC5[1:0]		DLC5[1:0]	
44h	C6	BLC6[3:0]				FRC6[1:0]		DLC6[1:0]	
45h	C7	BLC7[3:0]				FRC7[1:0]		DLC7[1:0]	
46h	D1	BLD1[3:0]				FRD1[1:0]		DLD1[1:0]	
47h	D2	BLD2[3:0]				FRD2[1:0]		DLD2[1:0]	
48h	D3	BLD3[3:0]				FRD3[1:0]		DLD3[1:0]	
49h	D4	BLD4[3:0]				FRD4[1:0]		DLD4[1:0]	
4Ah	D5	BLD5[3:0]				FRD5[1:0]		DLD5[1:0]	
4Bh	D6	BLD6[3:0]				FRD6[1:0]		DLD6[1:0]	
4Ch	D7	BLD7[3:0]				FRD7[1:0]		DLD7[1:0]	

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OPERATION (continued)

4. Register and Address (continued)

- Register table which needs a clock (continued)

About the following addresses, when an internal clock or an external clock does not exist, data cannot be Read / Write in at register.

Sub Address	Data Name	DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
4Dh	E1	BLE1[3:0]				FRE1[1:0]		DLE1[1:0]	
4Eh	E2	BLE2[3:0]				FRE2[1:0]		DLE2[1:0]	
4Fh	E3	BLE3[3:0]				FRE3[1:0]		DLE3[1:0]	
50h	E4	BLE4[3:0]				FRE4[1:0]		DLE4[1:0]	
51h	E5	BLE5[3:0]				FRE5[1:0]		DLE5[1:0]	
52h	E6	BLE6[3:0]				FRE6[1:0]		DLE6[1:0]	
53h	E7	BLE7[3:0]				FRE7[1:0]		DLE7[1:0]	
54h	F1	BLF1[3:0]				FRF1[1:0]		DLF1[1:0]	
55h	F2	BLF2[3:0]				FRF2[1:0]		DLF2[1:0]	
56h	F3	BLF3[3:0]				FRF3[1:0]		DLF3[1:0]	
57h	F4	BLF4[3:0]				FRF4[1:0]		DLF4[1:0]	
58h	F5	BLF5[3:0]				FRF5[1:0]		DLF5[1:0]	
59h	F6	BLF6[3:0]				FRF6[1:0]		DLF6[1:0]	
5Ah	F7	BLF7[3:0]				FRF7[1:0]		DLF7[1:0]	
5Bh	G1	BLG1[3:0]				FRG1[1:0]		DLG1[1:0]	
5Ch	G2	BLG2[3:0]				FRG2[1:0]		DLG2[1:0]	
5Dh	G3	BLG3[3:0]				FRG3[1:0]		DLG3[1:0]	
5Eh	G4	BLG4[3:0]				FRG4[1:0]		DLG4[1:0]	
5Fh	G5	BLG5[3:0]				FRG5[1:0]		DLG5[1:0]	
60h	G6	BLG6[3:0]				FRG6[1:0]		DLG6[1:0]	
61h	G7	BLG7[3:0]				FRG7[1:0]		DLG7[1:0]	
62h	LEDR	BLLEDR[3:0]				FRLEDR[1:0]		DLLEDR[1:0]	
63h	LEDG	BLLEDG[3:0]				FRLEDG[1:0]		DLLEDG[1:0]	
64h	LEDB	BLLEDB[3:0]				FRLEDB[1:0]		DLLEDB[1:0]	

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OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
01h	Data Name	—	—	—	—	—	OSCEN	—	—
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

D2 : OSCEN ON/OFF bit for internal oscillators
[0] : Internal oscillating circuit is OFF (default)
[1] : Internal oscillating circuit is ON

- The variation width of an internal oscillator is set to 0.96MHz - 1.44 MHz.
- The variation width of an internal clock is set to 694.4 ns - 1042 ns.

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
02h	Data Name	—	—	—	—	—	—	REG18	REG28
	Default	0	0	0	0	0	0	1	1
	mode	W	W	W	W	W	W	W	W

D1 : REG18 The ON/OFF control for LDO1(When LDOCNT terminal is Low)
[0] : LDO1 OFF
[1] : LDO1 ON (default)

D0 : REG28 The ON/OFF control for LDO2(When LDOCNT terminal is Low)
[0] : LDO2 OFF
[1] : LDO2 ON (default)

- When LDOCNT terminal is High, regardless of the state of REG18, LDO1 will be activated.
- When LDOCNT terminal is High, regardless of the state of REG28, LDO2 will be activated.
- Set LDOCNT to Low after setting REG28 to Low to put into OFF mode.

OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
03h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
04h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	R	R	R	R	R	R	R	R

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
05h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
06h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
07h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

*Don't access to address from 03h to 07h.

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OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
08h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
09h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

*Don't access to address from 08h to 09h.

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
0Ah	Data Name	LEDACT	—	—	—	—	DISMTX	DISRGB	—
	Default	0	0	0	0	0	0	0	0
	mode	W	W	W	W	W	W	W	W

D7 : LEDACT A putting-out-lights setup of LED by LEDCTL terminal.
[0] : The light is switched on at LEDCTL = Low(default)
[1] : The light is switched on at LEDCTL = High

D2 : DISMTX A putting-out-lights ON/OFF setup of 7 × 7 dots matrix LED by LEDCTL terminal.
[0] : Putting-out-lights control OFF by LEDCTL terminal. (default)
[1] : Putting-out-lights control ON by LEDCTL terminal.

D1 : DISRGB A putting-out-lights ON/OFF setup of R, G and B terminal by LEDCTL terminal.
[0] : Putting-out-lights control OFF by LEDCTL terminal. (default)
[1] : Putting-out-lights control ON by LEDCTL terminal.

OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
10h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
11h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
12h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
13h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

*Don't access to address from 10h to 13h.

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OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
14h	Data Name	FACGD1	—	—	—	RAMACT	FRMINT	CPUWRER	TSD
	Default	0	0	0	0	0	0	0	0
	mode	R	R	R	R	R	R	R	R

D7 : FACGD1
[0] : Normal operation (default)
[1] : No read clearance

D3 : RAMACT Internal RAM access judgment
[0] : RAM is not accessed. (default)
[1] : RAM is accessed.

D2 : FRMINT Frame display end judgment during scroll display
[0] : Under frame display (default)
[1] : Frame display end

D1 : CPUWRER CPU access error judgment
[0] : CPU access error does not occur. (default)
[1] : CPU access error occurs.

D0 : TSD Abnormal detection of TSD error
[0] : TSD abnormal detection does not occur. (default)
[1] : TSD abnormal detection occurs.

- CPUWRER indicates the error when CPU writes the data to 31h to 64h during copying from ROM to RAM1 or RAM2.
- The WRITE contents from CPU are not reflected in this LSI at CPUWRER = High. Write from CPU again.
- The interval of FACGD1 = "1" is maximum 1.93 μs (at the internal clock operation) from the renewal time of data.
- At FACGD1 = "1", if address 14h data is read, data of D0 to D6 are cleared.
- RAM access from CPU cannot be performed at RAMACT = "1" .
- When each address 14h register is set to High, the pulse in a cycle of 4 ms is output from INT.
- The pulse output from INT continues an output until address 14h is read.
- RSTB terminal = Low can reset to stop the INT pulse signal in case of that the serial read function is not used.
- The states for RAMACT = "1" are shown below.
  1. While copying to RAM from ROM.
  2. While clearing RAM

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OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
15h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	R	R	R	R	R	R	R	R

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
16h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
17h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
18h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
19h	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

*Don't access to address from 15h to 19h.

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OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
1Ah	Data Name	INTVSEL	—	—	—	—	—	—	—
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7 : INTVSEL The voltage setup of INT terminal
[0] : 1.85 V (default)
[1] : 2.85 V

OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
20h	Data Name	—	—	—	—	—	—	—	MTXON
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : MTXON ON/OFF setup of matrix LED
[0] : OFF (default)
[1] : ON

- During MTXON = "1", subsequent ROM, RAM, and the control contents to a register are sequentially processed and lit up.
- Wait 5 ms when MTXON is set to "1" after address 01h OSCEN is set to "1".
- Set MTXON to "1", and then set up other addresses to display the matrix part.

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
21h	Data Name	MTXDATA[7:0]							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : MTXDATA[7:0] Address setup of ROM/RAM of the data to read
[00000000] - [10010101] : ROM (Only luminosity)
7×7 pattern No.0 (default) to No.149
[10010110] - [11010000] : ROM (Luminosity + Cycle + Delay)
7×7 pattern No. 150 to No.208
[11010001] : RAM (Luminosity + Cycle + Delay)
7×7 pattern RAM No.1
[11010010] : RAM (Luminosity + Cycle + Delay)
7×7 pattern RAM No.2

- The pattern No.0 of ROM is all "0" data of matrix LED.
- Accessing to 21h is disabled while copying from ROM to RAM (COPYSTART 24h = "1").

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OPERATION (continued)

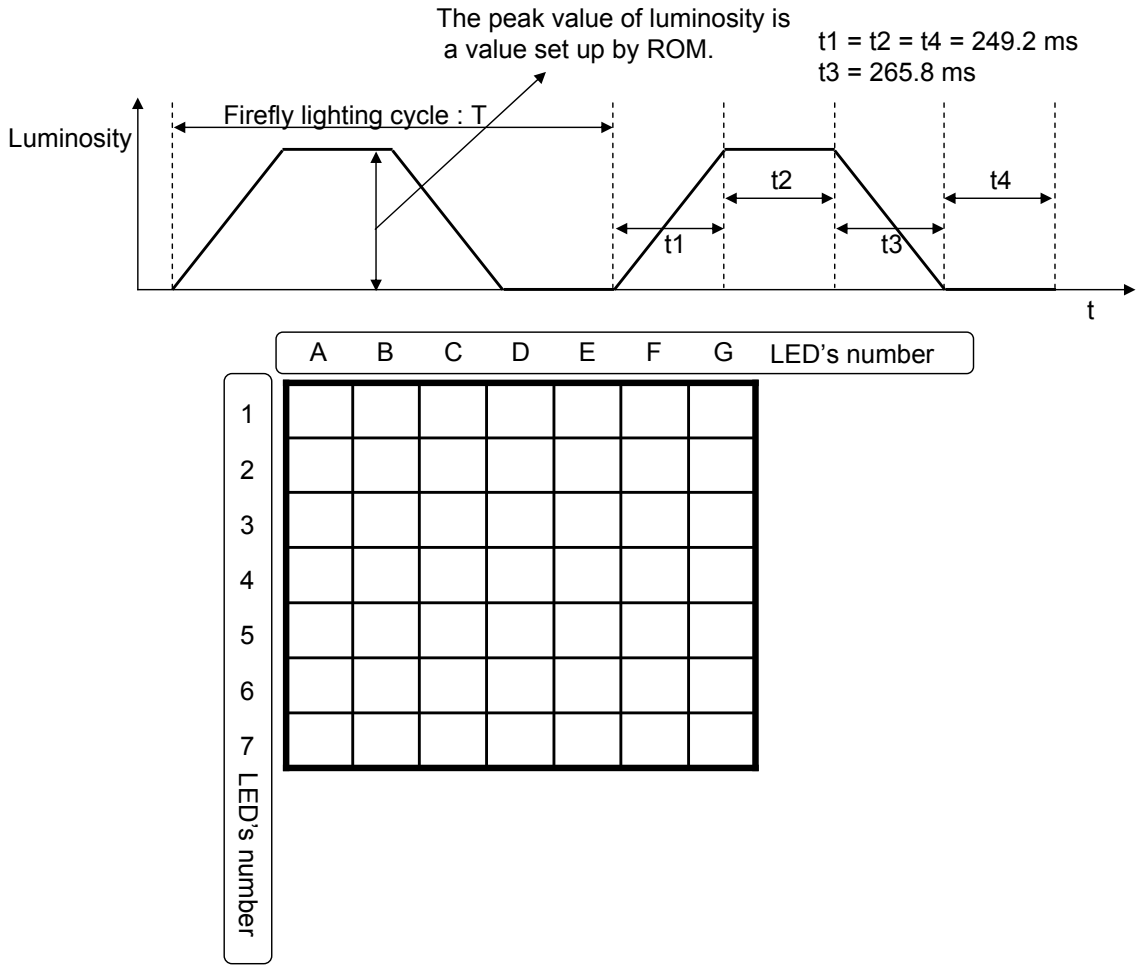
4. Register and Address (continued)

• Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
22h	Data Name	—	—	—	—	—	—	ROM77[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1-0 : ROM77[1:0] Lighting control of the 7×7 (LED No.A1-G7) fixed pattern of ROM
[00] : ROM data is displayed.
[01] : ROM data is displayed by firefly lighting in 1 s.
[10] : ROM data is displayed by firefly lighting in 2 s.
[11] : ROM data is displayed by firefly lighting in 3 s

• During display of repetition (REPON = "1"), ROM77 must not be changed.



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OPERATION (continued)

4. Register and Address (continued)

• Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
23h	Data Name	SELROM[7:0]							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : SELROM[7:0] Address setup of ROM copied to RAM
[00000000] - [10010101] : ROM (Only luminosity) 7×7 pattern No.0 (default) to No.149
[10010110] - [11010000] : ROM (Luminosity + Cycle + Delay) 7×7 pattern No.150 to No.208

・Accessing to 23h is disabled while copying from ROM to RAM (COPYSTART 24h = "1").

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
24h	Data Name	—	—	—	—	—	—	SELRAM	COPYSTART
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1 : SELRAM RAM number setup of a copy place.
[0] : RAM No.1
[1] : RAM No.2

D0 : COPYSTART Copy start ON/OFF control to RAM from ROM
[0] : OFF
[1] : The copy set up by SELROM and SELRAM is started. (It returns to 0 by internal 51 CLK.)

・Address 24h is only for copying data to RAM and never start LED display.
(However, if this RAM is copied when LED display is showing, LED display is updated.)
・Writing in address 21h-MTXDATA, 2Ah-SCLON, and 27h-REPON is disabled while copying.
(RAMACT flag is raised.)
・Accessing to SELRAM is disabled while copying from ROM to RAM (COPYSTART 24h = "1")
・Don't write address 29h (RAM-clear) while copying.
(The waiting time for over 1 ms is required after COPYSTART.)

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OPERATION (continued)

4. Register and Address (continued)

• Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
25h	Data Name	SETFROM[7:0]							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : SETFROM[7:0] An address setup of the ROM frame data at the repetition display start.
[00000000] - [10010101] : ROM (Only luminosity) 7×7 pattern No.0 (default) to No.149
[10010110] - [11010000] : ROM (Luminosity + Cycle + Delay) 7×7 pattern No.150 to No.208

・During display of repetition (REPON = "1"), Don't change the setting of SETFROM.

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
26h	Data Name	SETTO[7:0]							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : SETTO[7:0] Address setup of the ROM frame data at the repetition display end
[00000000] - [10010101] : ROM (Only luminosity) 7×7 pattern No.0 (default) to No.149
[10010110] - [11010000] : ROM (Luminosity + Cycle + Delay) 7×7 pattern No.150 to No.208

・During display of repetition (REPON = "1"), don't change the setting of SETTO.

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OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
27h	Data Name	—	—	—	—	—	—	—	REPON
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : REPON Repetition display ON/OFF control
[0] : Repetition display OFF (default)
[1] : Repetition display ON

- During display of repetition, display of set-up ROM is continued.
- A repetition display is started in the state of MTXON = "1" and REPON = "1".
- Accessing to 27h is disabled while copying from ROM to RAM (COPYSTART 24h = "1").
- When the setting of SCLON is changed from Low to High while REPON = "1", REPON becomes "0" and it shifts to scroll function.
- During display of repetition (REPON = "1"), don't change the setting of SETFROM and SETTO.

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
28h	Data Name	—	—	—	—	—	—	SETTIME[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1-0 : SETTIME[1:0] A frame display time setup of repetition display
[00] : 1 s (default)
[01] : 2 s
[10] : 3 s
[11] : 4 s

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OPERATION (continued)

4. Register and Address (continued)

• Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
29h	Data Name	—	—	—	—	—	—	RAM1	RAM2
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1 : RAM1 The data in 7×7 RAM1 is cleared.
0 : Overwrite is possible. (default)
1 : The data in 7×7 RAM1 is cleared. (It returns to 0 by internal 2 CLK.)

D0 : RAM2 The data in 7×7 RAM2 is cleared.
0 : Overwrite is possible. (default)
1 : The data in 7×7 RAM2 is cleared. (It returns to 0 by internal 2 CLK.)

- Don’t set the RAM-clear operation for RAM1 or RAM2 during display of repetition (SCLON = "1").
- Don’t set the RAM-clear operation (29h) during the COPY operation (24h).
  (The waiting time for over 1 ms is required after COPYSTART.)

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OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
2Ah	Data Name	—	—	—	—	—	—	—	SCLON
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : SCLON ON/OFF setup of scroll display
[0] : OFF (default)
[1] : ON

- The scroll display displays the data which exists in the RAM No.1-2 of 7×7 in order of A-G column. The display travel time of a column is the preset value of SCLTIME.
- During display of scroll, data can be written to RAM without specifying RAM number.
  (Writing is performed to empty RAM.)
- The scroll display is started in the state of MTXON = "1" and SCLON.
- Accessing to 2Ah is disabled while copying from ROM to RAM (COPYSTART 24h = "1").
- When the setting of REPON is changed from "0" to "1" while SCLON = "1", SCLON becomes "0" and it shifts to repetition display function.
- During display of scroll (SCLON = "1"), don't change the setting of RAM1 and RAM2.
- Once the scroll function was set, then the SCLON = "0" or MTXON = "0", RSTB terminal must be "L" to reset before the scroll function is set again.

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
2Bh	Data Name	—	—	—	—	—	—	SCLTIME[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1-0 : SCLTIME[1:0] Frame display time setup of scroll display
[00] : 0.1 s (default)
[01] : 0.2 s
[10] : 0.4 s
[11] : 0.8 s

- The display travel time of the column is the preset value of SCLTIME.

Established : 2007-05-24
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OPERATION (continued)

4. Register and Address (continued)

• Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
2Ch	Data Name	—	—	—	—	—	—	—	RGBON
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D0 : RGBON ON/OFF setup of RGB lighting
[0] : OFF (default)
[1] : ON

• Wait 5 ms when RGBON is set to "1" after address 01h OSCEN is set to "1".

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
2Dh	Data Name	—	—	RGBDATA[5:0]					
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-0 : RGBDATA[5:0] Address setup of ROM and register which read RGB data
[000000] : Register is displayed.
[000001] - [101010] : ROM (RGB pattern, Luminosity + Cycle + Delay) pattern No.1 to No.42

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
2Eh	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	R	R	R	R	R	R	R	R

*Don't access to address 2Eh.

Established : 2007-05-24
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OPERATION (continued)

4. Register and Address (continued)

• Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
30h	Data Name	—	—	—	—	—	—	—	RAMNUM
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D1-0 : RAMNUM[1:0] RAM number setup at the CPU access (READ and WRITE).
[0] : RAM No.1
[1] : RAM No.2

• Accessing to 30h is disabled during display of scroll (2Ah SCLON = "1").

Established : 2007-05-24
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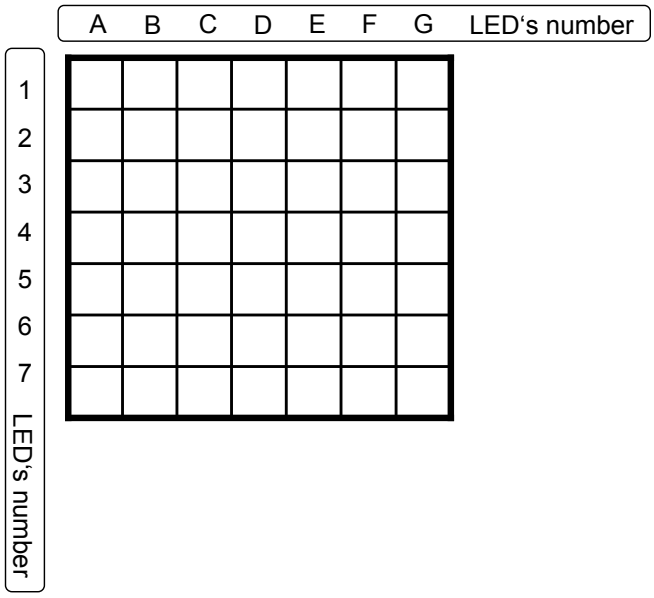
OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
31h	Data Name	BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-4 : BLA1[1:0] Luminosity setup of LED No.A1
[0000] : 0 mA (default)
[0001] : 1 mA
[0010] : 2 mA
[0011] : 3 mA
[0100] : 4 mA
[0101] : 5 mA
[0110] : 8 mA
[0111] : 11 mA
[1000] : 15 mA
[1001] : 17 mA
[1010] : 19 mA
[1011] : 21 mA
[1100] : 24 mA
[1101] : 26 mA
[1110] : 28 mA
[1111] : 30 mA



D3-2 : FRA1[1:0] Firefly operation and cycle setup of the LED No.A1
[00] : Lighting mode (default)
[01] : Firefly lighting cycle 1 s
[10] : Firefly lighting cycle 2 s
[11] : Firefly lighting cycle 3 s

D1-0 : DLA1[1:0] Firefly operation delay setup of the LED No.A1
[00] : No delay (default)
[01] : Delay 25%
[10] : Delay 50%
[11] : Delay 75%

- The operation is the same as above for the addresses to 61h corresponding to each LED number.
- The waiting time for 2 or more internal clocks (2 μs or more) is required after the data from address 31h to 61h is written in. Please input other serial commands after that.

Established : 2007-05-24
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OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
62h	Data Name	BLLEDR[3:0]				FRLEDR[1:0]		DLLEDR[1:0]	
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

D7-4 : BLLEDR1[1:0] Luminosity setup of R1 terminal
[0000] : 0 mA (default)
[0001] : 1 mA
[0010] : 2 mA
:
:
[1110] : 14 mA
[1111] : 15 mA

D3-2 : FRLEDR1[1:0] Firefly operation and cycle setup of R1 terminal
[00] : Lighting mode (default)
[01] : Firefly lighting cycle 1 s
[10] : Firefly lighting cycle 2 s
[11] : Firefly lighting cycle 3 s

D1-0 : DLLEDR1[1:0] Firefly operation delay setup of R1 terminal
[00] : No delay (default)
[01] : Delay 25%
[10] : Delay 50%
[11] : Delay 75%

- The operation is the same as above for the addresses to 64h corresponding to G and B terminal.
- The waiting time for 2 or more internal clocks (2 μs or more) is required after the data from address 62h to 64h is written in. Please input other serial commands after that.

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OPERATION (continued)

4. Register and Address (continued)

- Register map detailed explanation (continued)

Sub Address		DATA							
		D7	D6	D5	D4	D3	D2	D1	D0
6Bh	Data Name	For test							
	Default	0	0	0	0	0	0	0	0
	mode	W/R	W/R	W/R	W/R	W/R	W/R	W/R	W/R

*Address from 6Bh onwards are registers for test. Don't write into these addresses.

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OPERATION (continued)

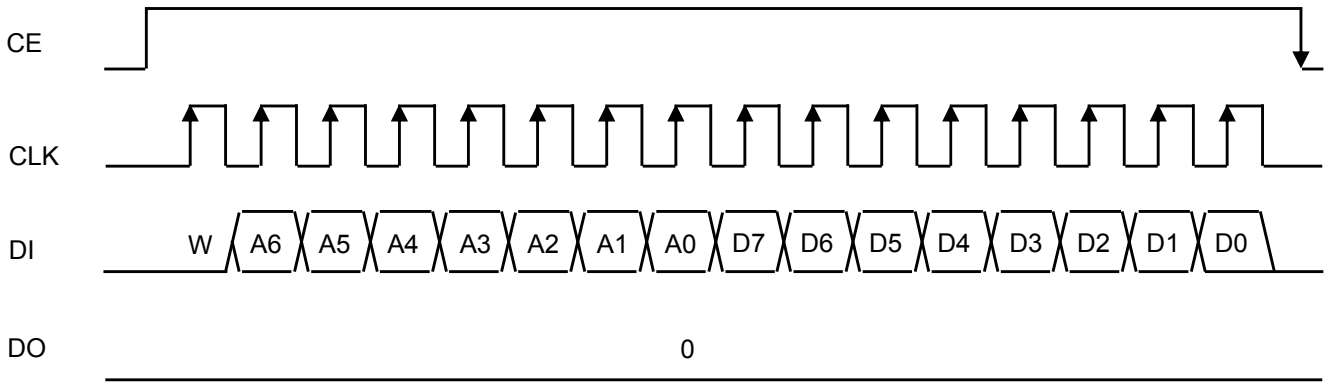
5. Serial interface format

- SPI format
- The interface with microcomputer consists of 16 bit-serial register (8-bit of command, 8-bit of address), and address decoder and transmitting register (8-bit).
- Serial interface consists of four terminals of serial clock terminal (CLK), serial-data input terminal (DI), serial-data output terminal (DO), and chip enable input terminal (CE).

(1) Write operation

- Data is taken into internal shift register by the rising edge of CLK. (Maximum 13 MHz of frequency of CLK can be used)
- Serial interface consists of four terminals of serial clock terminal (CLK), serial-data input terminal (DI), serial-data output terminal (DO), and chip enable input terminal (CE).
- Data is transmitted at MSB first in order of a control register address (8-bit) and control command (8-bit).

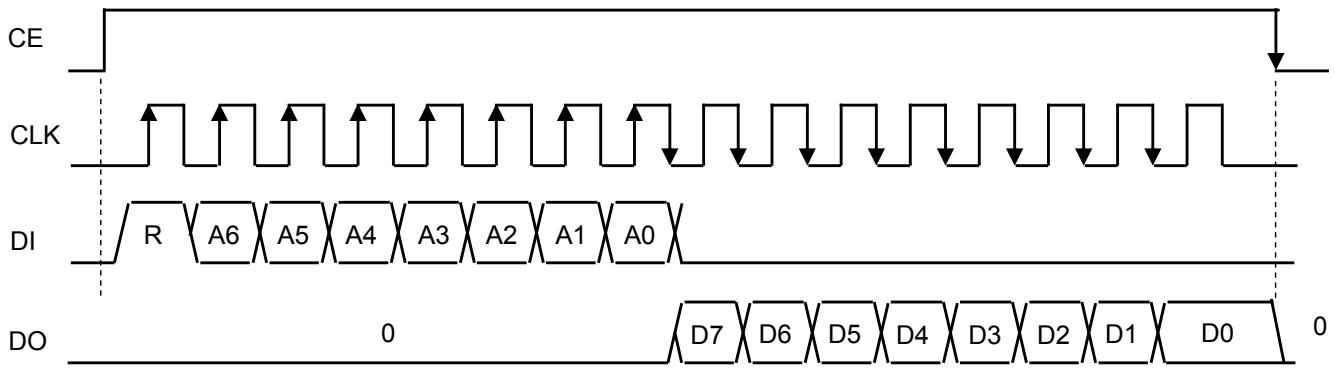
Write access Timing



(2) Transmission operation

- Data is taken into internal shift register by the rising edge of CLK. (A maximum of 6 MHz of frequency of CLK can be used)
- It is not possible to read RAM data.
- In High interval of CE, reception of data becomes ENABLE. (active : High)
- Data is transmitted at MSB first in order of a control register address (8-bit) and control command (max 8-bit).

Read access Timing



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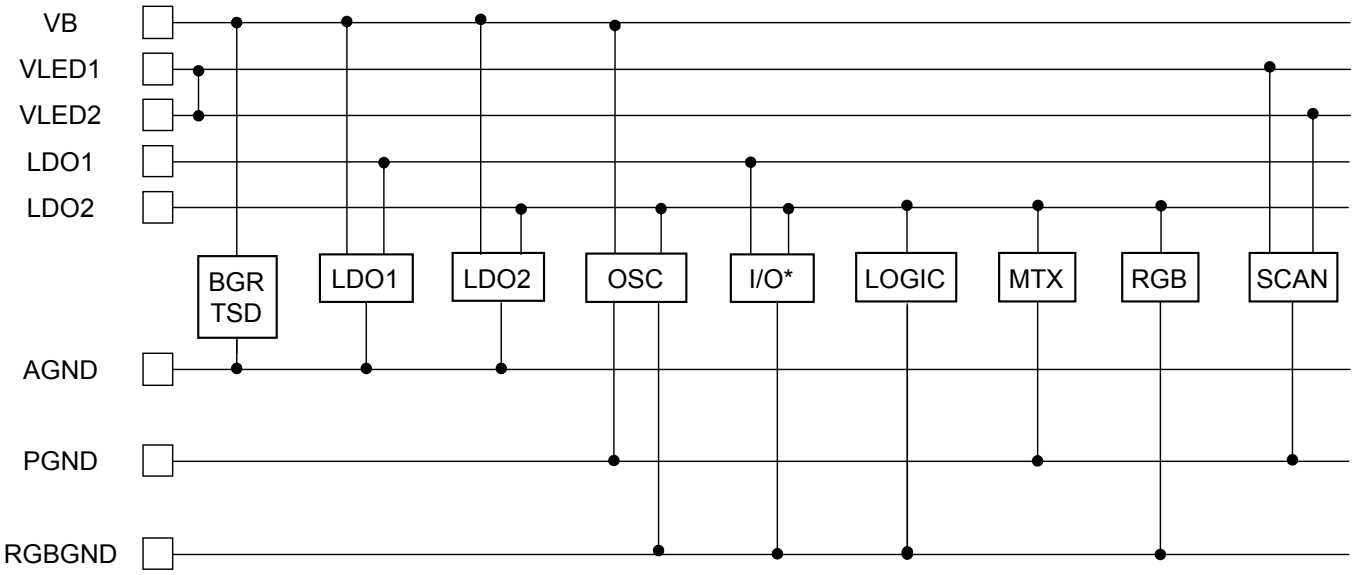
OPERATION (continued)

6. Signal distribution diagram

- Power supply distribution diagram



*CLK, CE, DI, DO, LEDCTL

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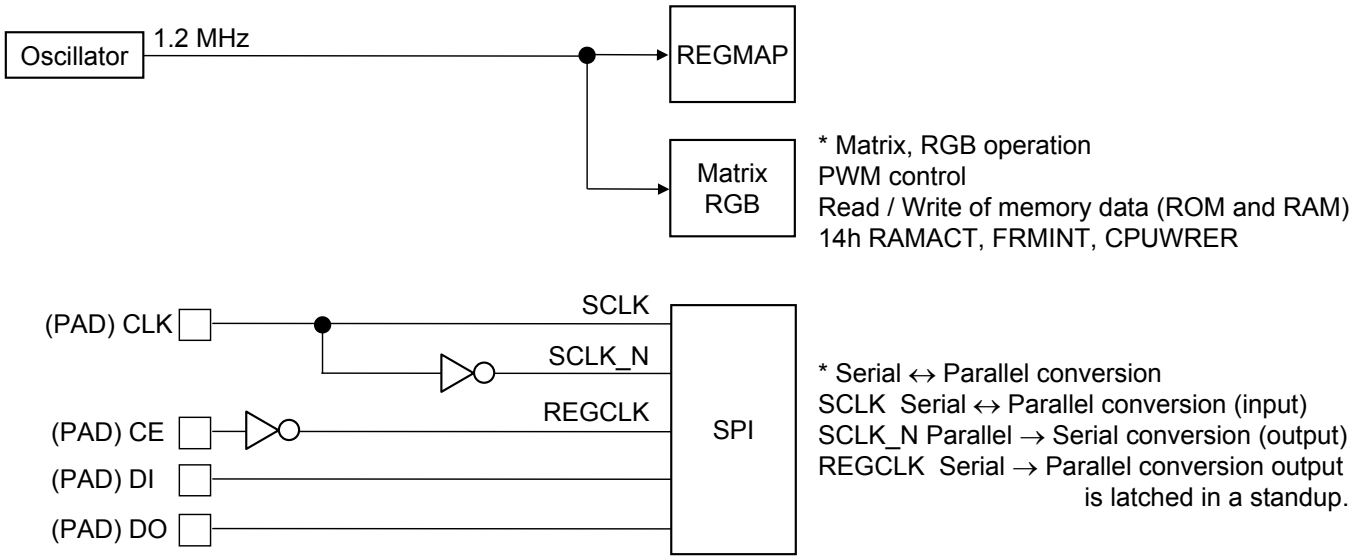
OPERATION (continued)

6. Signal distribution diagram (continued)

- Control / Clock distribution diagram



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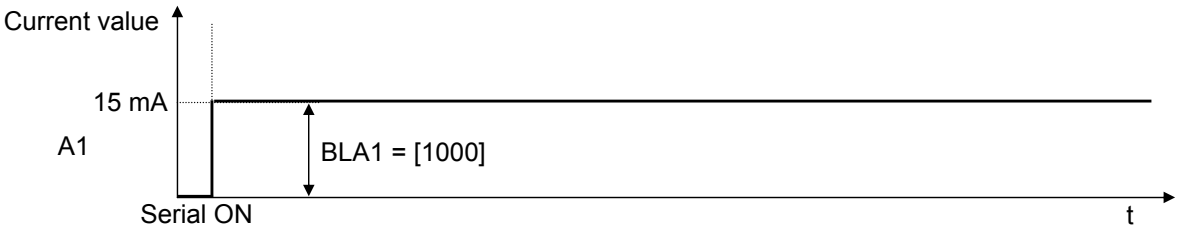
OPERATION (continued)

7. Example of firefly lighting

- Example of firefly lighting 1

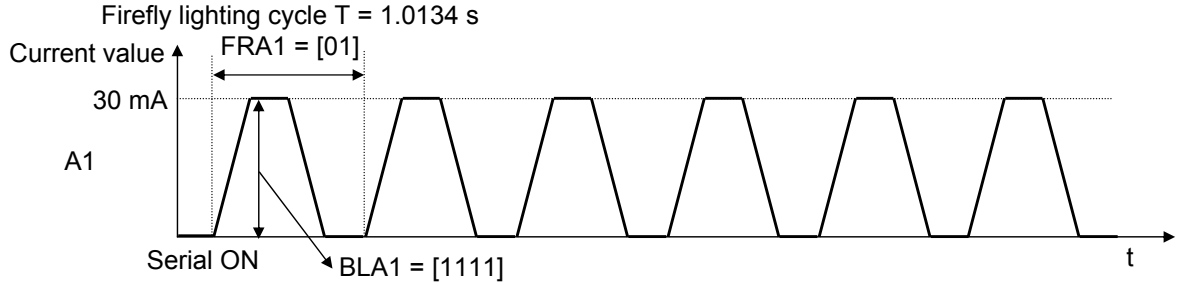
Example of initial setting for lighting

BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
1	0	0	0	0	0	0	0



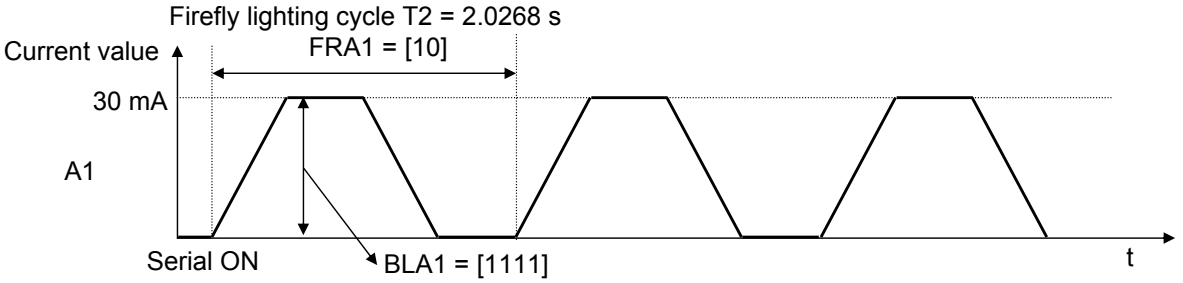
Firefly lighting setup 1 s

BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
1	1	1	1	0	1	0	0



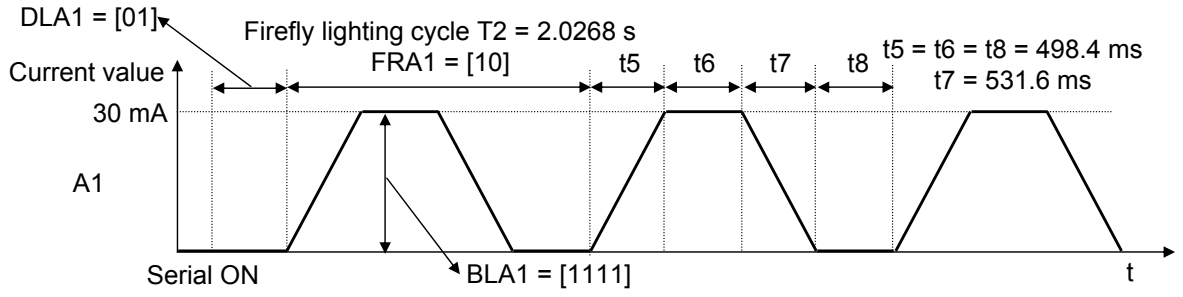
Change to cycle 1 s to 2 s

BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
1	1	1	1	1	0	0	0



Change to delay 0 → 25 %

BLA1[3:0]				FRA1[1:0]		DLA1[1:0]	
1	1	1	1	1	0	0	1



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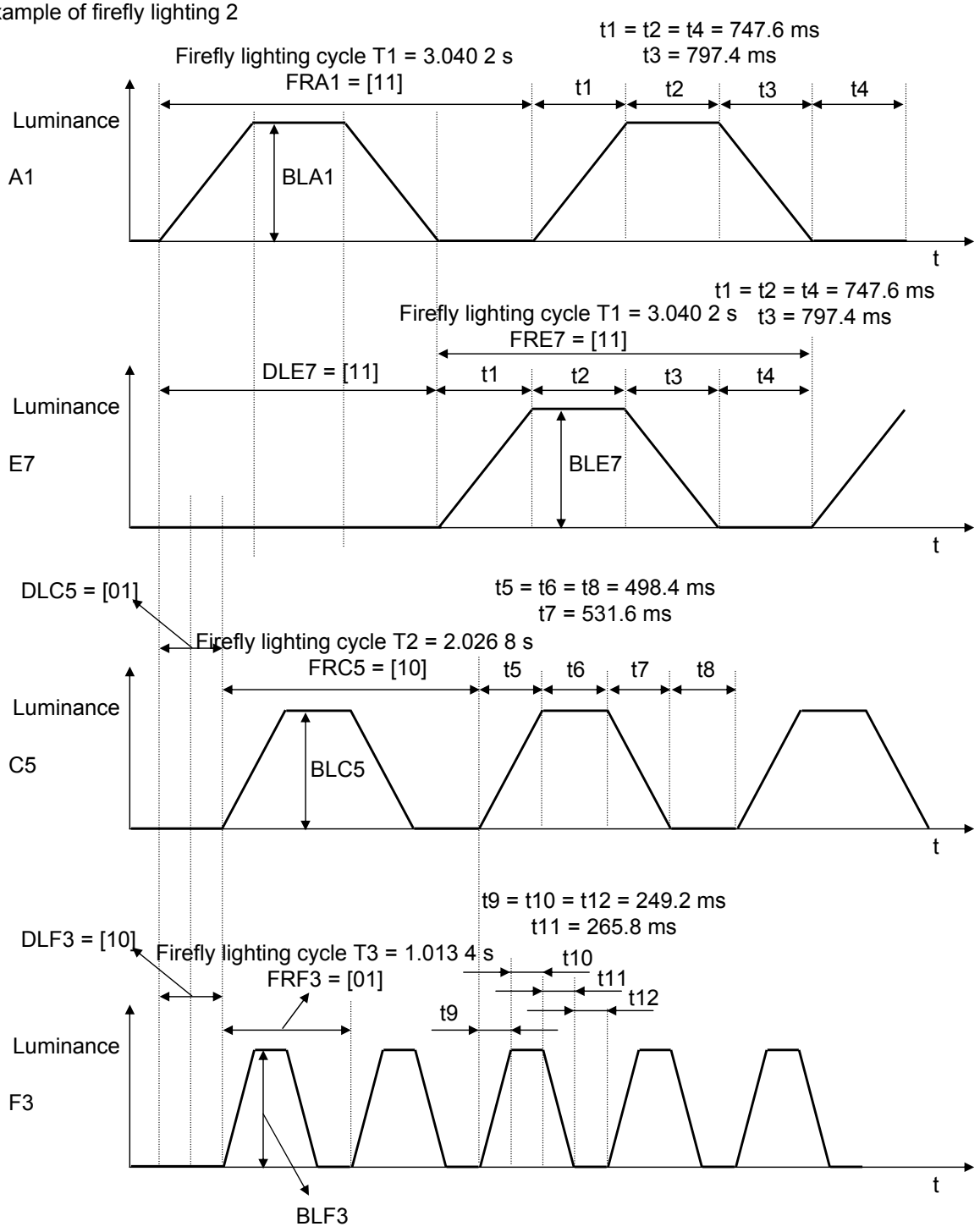
OPERATION (continued)

7. Example of firefly lighting (continued)

- Example of firefly lighting 2



1. Normally, it is not possible to control data when RGBGND pin voltage is undefined. Therefore, please keep the RGBGND pin voltage at the lowest voltage.
2. Please check the input waveform to the CLK pin. When inputting clock into the CLK pin, if the input clock is ringing with input voltage between 0.4 V to LDO1 × 0.8 V (input voltage indefinite range), it will result in serial data not able to be written to or be read out from a register. (It is recommended to smooth the rising and falling edge of the input clock by connecting input capacitance (a capacitor, etc.) to the CLK pin.)

Established : 2007-05-24
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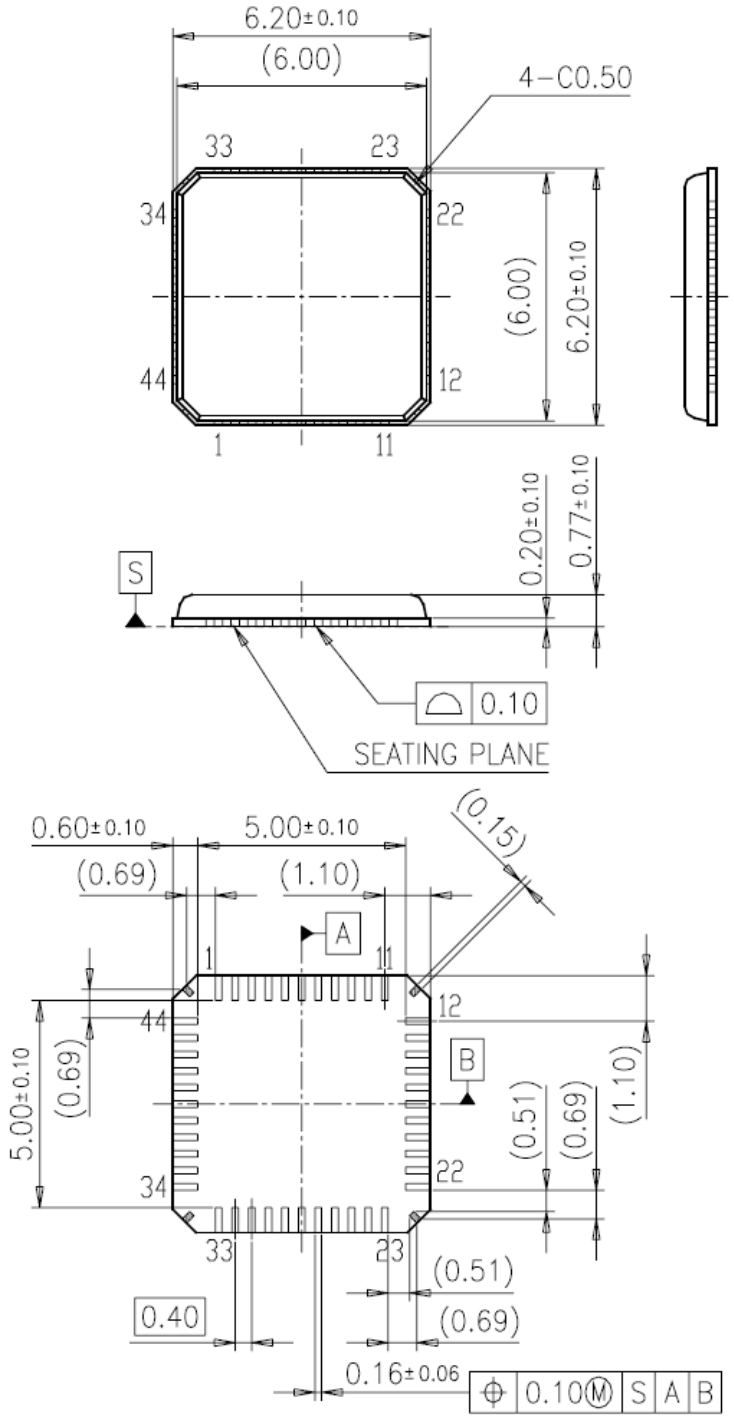
PACKAGE INFORMATION (Reference Data)

Package Code : ∗QFN044-P-0606C

Unit:mm



Body Material	:	Epoxy Resin
Lead Material	:	Cu Alloy
Lead Finish Method	:	Pd Plating

Established : 2007-05-24
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IMPORTANT NOTICE

1. When using the LSI for new models, verify the safety including the long-term reliability for each product.
2. When the application system is designed by using this LSI, please confirm the notes in this book.
   Please read the notes to descriptions and the usage notes in the book.
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   Consult our sales staff in advance for information on the following applications: Special applications in which exceptional quality and reliability are required, or if the failure or malfunction of this LSI may directly jeopardize life or harm the human body.
   Any applications other than the standard applications intended.
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   (2) Traffic control equipment (such as for automobile, airplane, train, and ship)
   (3) Medical equipment for life support
   (4) Submarine transponder
   (5) Control equipment for power plant
   (6) Disaster prevention and security device
   (7) Weapon
   (8) Others : Applications of which reliability equivalent to (1) to (7) is required
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7. Pay attention in the PCB (printed-circuit-board) pattern layout in order to prevent damage due to short circuit between pins. In addition, refer to the Pin Description for the pin configuration.
8. Perform visual inspection on the PCB before applying power, otherwise damage might happen due to problems such as solder-bridge between the pins of the semiconductor device. Also, perform full technical verification on the assembly quality, because the same damage possibly can happen due to conductive substances, such as solder ball, that adhere to the LSI during transportation.
9. Take notice in the use of this product that it might be damaged or occasionally emit smoke when an abnormal state occurs such as output pin-VCC short (Power supply fault), output pin-GND short (Ground fault), or output-to-output-pin short (load short). Safety measures such as installation of fuses are recommended because the extent of the above-mentioned damage and smoke emission will depend on the current capability of the power supply.
10. The protection circuit is for maintaining safety against abnormal operation. Therefore, the protection circuit should not work during normal operation.
    Especially for the thermal protection circuit, if the area of safe operation or the absolute maximum rating is momentarily exceeded due to output pin to VCC short (Power supply fault), or output pin to GND short (Ground fault), the LSI might be damaged before the thermal protection circuit could operate.
11. Unless specified in the product specifications, make sure that negative voltage or excessive voltage are not applied to the pins because the device might be damaged, which could happen due to negative voltage or excessive voltage generated during the ON and OFF timing when the inductive load of a motor coil or actuator coils of optical pick-up is being driven.
12. Verify the risks which might be caused by the malfunctions of external components.

Established : 2007-05-24
Revised : 2013-04-15

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