

NB3L14S

2.5 V 1:4 LVDS Fanout Buffer

The NB3L14S is a differential 1:4 LVDS Clock fanout buffer. The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT pin. The NB3L14S LVDS signals will be buffered and replicated to identical LVDS copies of the Input operating up to 300 MHz. As such, the NB3L14S is ideal for Clock distribution applications that require low skew.

The NB3L14S is offered in a small 3 mm x 3 mm 16-QFN package. Application notes, models, and support documentation are available at www.onsemi.com.

Features

- Maximum Input Clock Frequency; 300 MHz
- Low Output-to-Output Skew; 20 ps
- 450 ps Typical Propagation Delay
- 250 ps Typical Rise and Fall Times
- Single Power Supply; $V_{CC} = 2.5 \pm 5\%$
- These are Pb-Free Devices



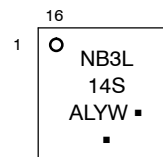
ON Semiconductor®

<http://onsemi.com>

MARKING DIAGRAM*



QFN-16
MN SUFFIX
CASE 485G



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

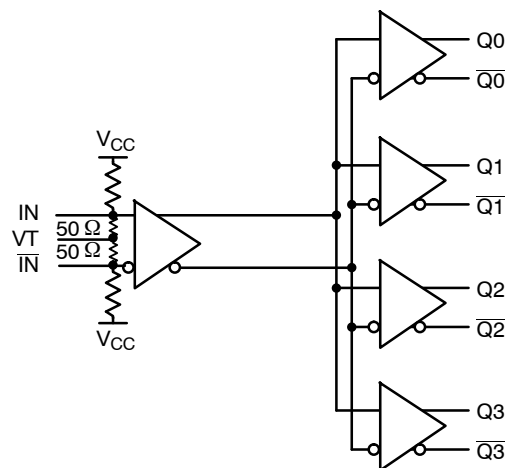


Figure 1. Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 7 of this data sheet.

NB3L14S

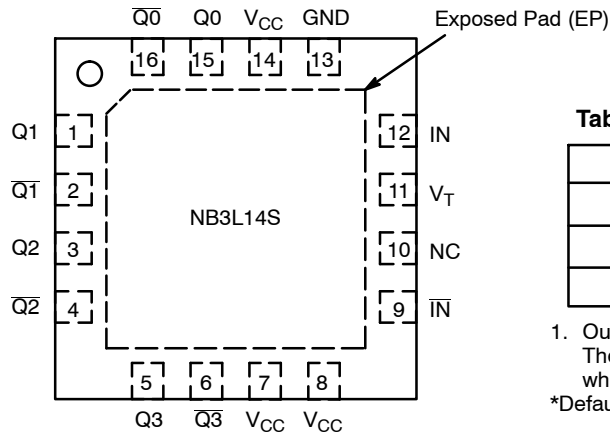


Figure 2. NB3L14S Pinout, 16-pin QFN (Top View)

Table 1. TRUTH TABLE

IN*	IN̄*	Q	Q̄
0	1	0	1
1	0	1	0
x	x	0 (Note 1)	1 (Note 1)

1. Outputs will be at the known state in this table at initial power up. The outputs will also be at the known state during normal operation when inputs are left open.

*Defaults high when left open

Table 2. PIN DESCRIPTION

Pin	Name	I/O	Description
1	Q1	LVDS Output	Non-inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
2	Q1̄	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
3	Q2	LVDS Output	Non-inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
4	Q2̄	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
5	Q3	LVDS Output	Non-inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
6	Q3̄	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
7	V _{CC}	-	Positive Supply Voltage.
8	V _{CC}	-	Positive Supply Voltage.
9	IN̄	LVDS	Inverted Differential Input; pin will default HIGH when left open
10	NC	No Connect	This is not connected.
11	V _T	Input Termination	Internal 100 Ω Center-tapped Termination Pin for IN and IN̄, leave open for LVDS.
12	IN	LVDS	Non-inverted Differential Input; pin will default HIGH when left open.
13	GND	-	Negative Supply Voltage.
14	V _{CC}	-	Positive Supply Voltage.
15	Q0	LVDS Output	Non-inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
16	Q0̄	LVDS Output	Inverted IN output. Typically loaded with 100 Ω receiver termination resistor across differential pair.
-	EP	-	The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and is required to be electrically and thermally connected to GND on the PC board.

NB3L14S

Table 3. ATTRIBUTES

Characteristics	Value
Moisture Sensitivity (Note 2)	Level 1
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Input Pull-up Resistors to V_{CC} on Inputs	200 k Ω
ESD Protection Human Body Model Machine Model	> 4 kV > 200 V
Transistor Count	440
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

2. For additional information, see Application Note AND8003/D.

Table 4. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{CC}	Positive Power Supply	GND = 0 V		4.6	V
V_{IN}	Positive Input	GND = 0 V	$V_{IN} \leq V_{CC}$	4.6	V
I_{IN}	Input Current Through R_T (50 Ω Resistor)	Static Surge		35 70	mA mA
I_{OSC}	Output Short Circuit Current Line-to-Line (Q to \bar{Q}) Line-to-GND (Q or \bar{Q} to GND)	Q or \bar{Q} Q to \bar{Q} to GND	Continuous Continuous	12 24	mA
T_A	Operating Temperature Range	QFN-16		-40 to +85	$^{\circ}$ C
T_{stg}	Storage Temperature Range			-65 to +150	$^{\circ}$ C
θ_{JA}	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	QFN-16 QFN-16	41.6 35.2	$^{\circ}$ C/W $^{\circ}$ C/W
θ_{JC}	Thermal Resistance (Junction-to-Case)	1S2P (Note 3)	QFN-16	4.0	$^{\circ}$ C/W
T_{sol}	Wave Solder Pb-Free			265	$^{\circ}$ C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard multilayer board – 1S2P (1 signal, 2 power) with 8 filled thermal vias under exposed pad.

NB3L14S

Table 5. DC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }2.625\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

Symbol	Characteristic	Min	Typ	Max	Unit
I_{CC}	Power Supply Current (Note 4)		45	65	mA

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 4, 8, and 9) (Note 5)

V_{IHD}	Differential Input HIGH Voltage	1150		1800	mV
V_{ILD}	Differential Input LOW Voltage	GND		$V_{IHD} - 150$	mV
V_{CMR}	Input Common Mode Range (Differential Configuration) (Note 6)	75		1725	mV
V_{ID}	Differential Input Voltage ($V_{IHD} - V_{ILD}$)	150		1800	mV
R_{TIN}	Internal Input Termination Resistor	40	50	60	Ω

LVDS OUTPUTS (Note 7)

V_{OD}	Differential Output Voltage (Single-Ended Measurement)	250	350	450	mV
ΔV_{OD}	Change in Magnitude of V_{OD} for Complementary Output States (Note 8)	0	1	25	mV
V_{OS}	Offset Voltage (Figure 7)	1125	1250	1375	mV
ΔV_{OS}	Change in Magnitude of V_{OS} for Complementary Output States (Note 8)	0	1	25	mV
V_{OH}	Output HIGH Voltage (Note 9)		1425	1600	mV
V_{OL}	Output LOW Voltage (Note 10)	900	1075		mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

4. Input pins, $I_N = 300\text{ mV}$, $\overline{I_N} = 1\text{ V}$. Output pins loaded with $R_L = 100\ \Omega$ across the outputs.
5. V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
6. V_{CMR} min varies 1:1 with GND, V_{CMR} max varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.
7. LVDS outputs require $100\ \Omega$ receiver termination resistor between differential pair. See Figure 6.
8. Parameter guaranteed by design verification not tested in production.
9. $V_{OHmax} = V_{OSmax} + \frac{1}{2} V_{ODmax}$.
10. $V_{OLmax} = V_{OSmin} - \frac{1}{2} V_{ODmax}$.

NB3L14S

Table 6. AC CHARACTERISTICS ($V_{CC} = 2.375\text{ V to }2.625\text{ V}$, $GND = 0\text{ V}$)

Symbol	Characteristic	-40°C to +85°C			Unit
		Min	Typ	Max	
f_{inMax}	Maximum Input Clock Frequency	300			MHz
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) $f_{in} \leq 300\text{ MHz}$	250	350	450	mV
t_{PLH} , t_{PHL}	Differential Input to Differential Output, IN to Q Propagation Delay @ 50 MHz	300	450	600	ps
t_{SKEW}	Within Device Output-to-Output Skew (Note 12) Device-to-Device Skew (Note 12)		5 30	20 200	ps
V_{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 11)	150		1800	mV
t_r , t_f	Output Rise/Fall Times @ 50 MHz Q, \bar{Q} (20% – 80%)		250	350	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- 11. Input voltage swing is a single-ended measurement operating in differential mode.
- 12. Skew is measured between outputs under identical transition @ 50 MHz.

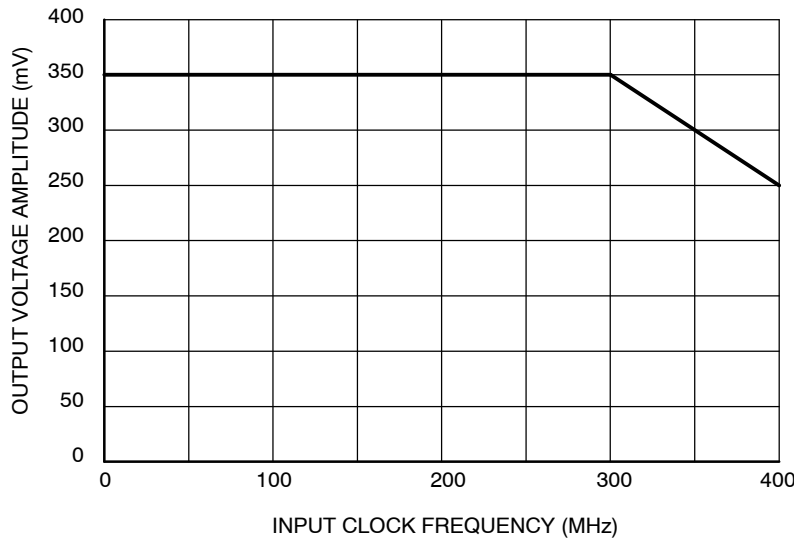


Figure 3. Output Voltage Amplitude (V_{OUTPP}) versus Input Clock Frequency (f_{in}) and Temperature (@ $V_{CC} = 2.5\text{ V}$)

NB3L14S

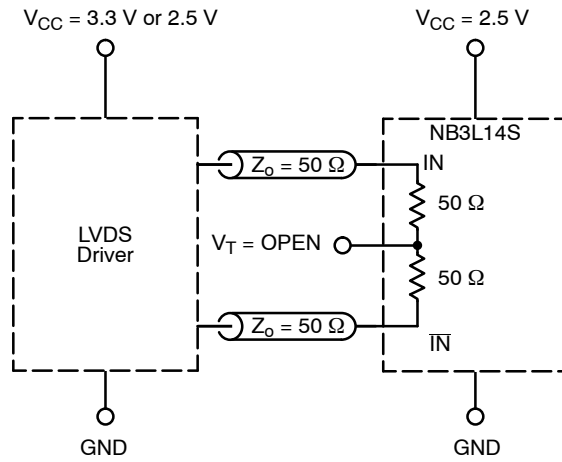


Figure 4. LVDS Interface

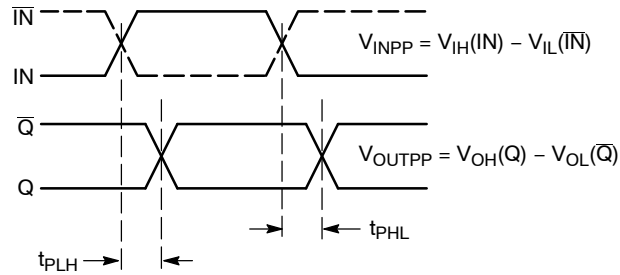


Figure 5. AC Reference Measurement

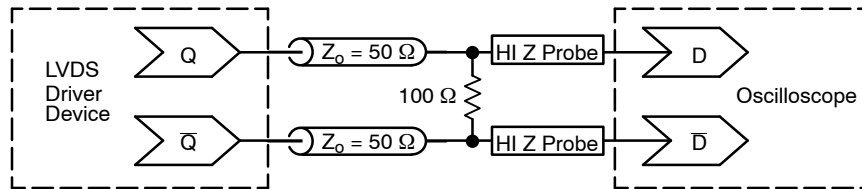


Figure 6. Typical LVDS Termination for Output Driver and Device Evaluation

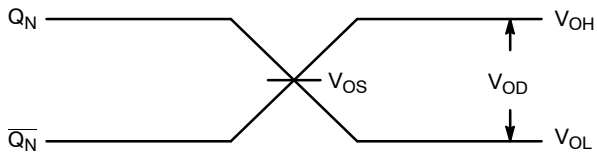


Figure 7. LVDS Output

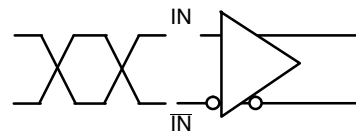


Figure 8. Differential Inputs Driven Differentially

NB3L14S

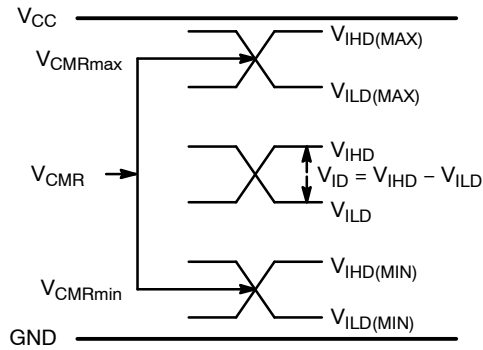


Figure 9. V_{CMR} Diagram

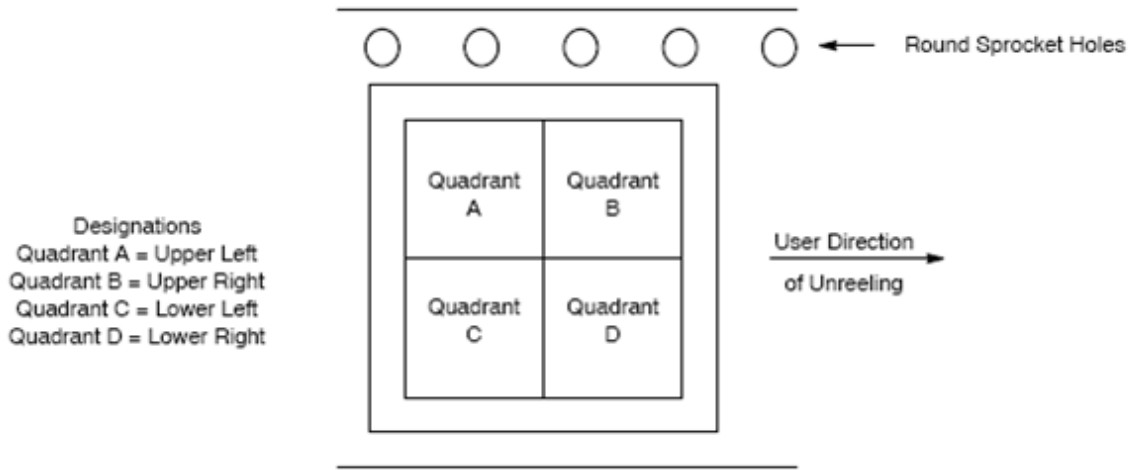


Figure 10. Tape and Reel Pin 1 Quadrant Orientation

ORDERING INFORMATION

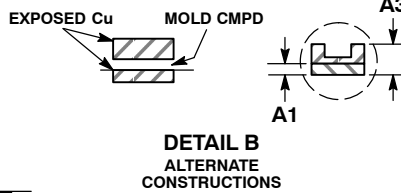
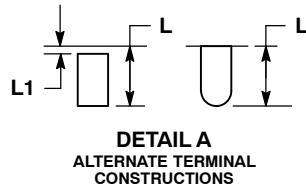
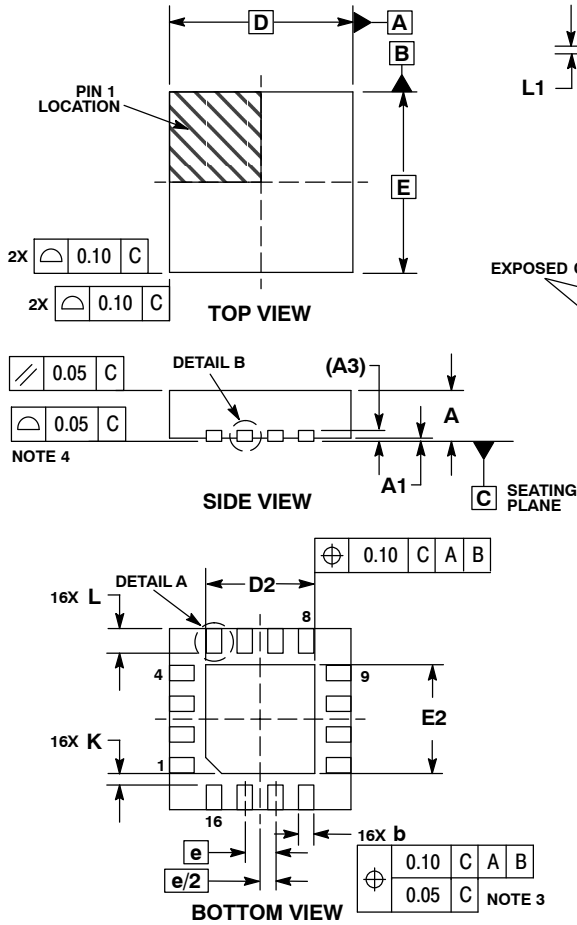
Device	Package	Shipping [†]
NB3L14SMNG	QFN-16, 3 X 3 mm (Pb-Free)	123 Units / Rail
NB3L14SMNTXG	QFN-16, 3 X 3 mm (Pb-Free)	3000 / Tape & Reel (Pin 1 Orientation in Quadrant B, Figure 10)

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NB3L14S

PACKAGE DIMENSIONS

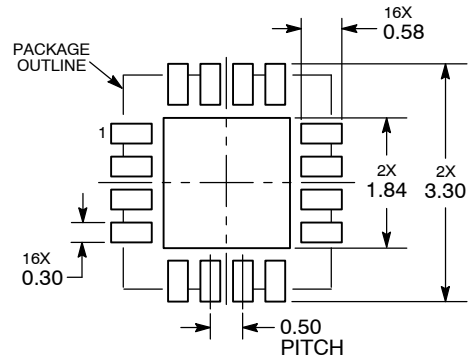
QFN16 3x3, 0.5P
CASE 485G
ISSUE F



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
K	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

AnyLevel and ECLinPS MAX are trademarks of Semiconductor Components Industries, LLC (SCILLC).

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of SCILLC's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marketing.pdf. SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative