EMC1702

High-Side Current-Sense and Dual 1°C Temperature Monitor

PRODUCT FEATURES

Datasheet

General Description

The EMC1702 is a combination high-side current sensing device with precision temperature measurement. It measures the voltage developed across an external sense resistor to represent the high-side current of a battery or voltage regulator. It also measures the source voltage and uses these measured values to present a proportional power calculation. The EMC1702 contains additional bi-directional peak detection circuitry to flag instantaneous current spikes with programmable time duration and magnitude threshold. Finally, the EMC1702 includes an external diode channel for temperature measurement as well as an internal diode for ambient temperature measurements.

The temperature measurement includes advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model including 45nm and 65nm processors), and automatic diode type detection.

Both current sensing and temperature monitoring include two tiers of protection: one that can be masked and causes the ALERT pin to be asserted, and the other that cannot be masked and causes the THERM pin to be asserted.

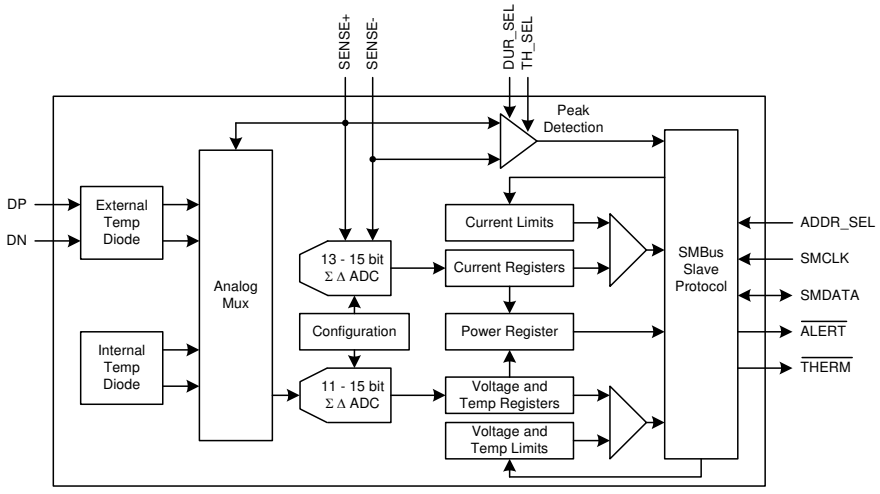
Applications

- Notebook and Desktop Computers
- Industrial
- Power Management Systems
- Embedded Applications

Features

- High-side current sensor
  - Bi-directional current measurement
  - Measures source voltage and indicates power ratio
  - 1% current measurement accuracy
  - Integrated over 82ms to 2.6sec with 11-bit resolution
  - 3V to 24V bus voltage range
- Independent hardware set instantaneous current peak detector
  - Software controls to program time duration and magnitude threshold
- Power supply options
  - Bus or separately powered for low voltage operation
- Wide temperature operating range: -40°C to +85°C
- One external temperature monitor
  - 1°C accuracy (20°C < T_{DIODE} < 110°C) with 0.125°C resolution
  - Ideality factor setting
  - Support for 45nm and 65nm CPU diodes requiring the BJT/transistor model w/ beta compensation
  - Determines external diode type and optimal settings
  - Resistance Error Correction
- Internal temperature monitor
  - ±1°C accuracy (-5°C < T_A < 85°C)
- ALERT and THERM outputs for temperature, voltage, and out-of-current limit reporting
- SMBus 2.0 interface
  - Pin-selectable SMBus Address
  - Block Read and Write
- Available in a 12-pin 4mm x 4mm QFN RoHS Compliant Package

Block Diagram



Ordering Information:

ORDERING NUMBER	PACKAGE	FEATURES
EMC1702-1-KP-TR	12-pin 4mm x 4mm QFN (Lead-free ROHS compliant)	External Diode, current sensor, hardware set peak detector

REEL SIZE IS 4,000 PIECES

This product meets the halogen maximum concentration values per IEC61249-2-21

For RoHS compliance and environmental information, please visit www.smsc.com/rohs

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Chapter 1 Pin Description

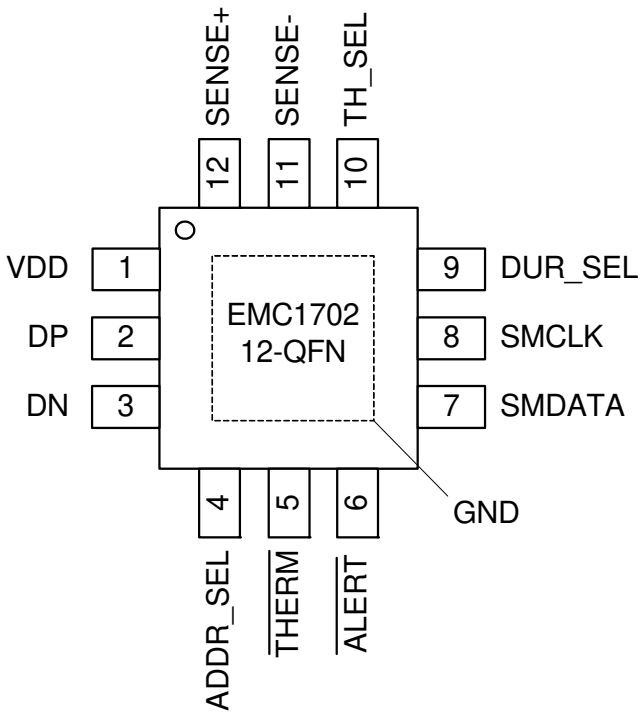


Figure 1.1 EMC1702 Pin Diagram 12-Pin QFN 4mm x 4mm

Table 1.1 Pin Description for EMC1702

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE
1	VDD	Positive power supply voltage	Power (24V)
2	DP	External Diode positive (anode) connection	AIO (2V)
3	DN	External Diode negative (cathode) connection	AIO (2V)
4	ADDR_SEL	Selects SMBus Address	AI
5	$\overline{\text{THERM}}$	Active low output - requires pull-up resistor	OD (5V)
6	$\overline{\text{ALERT}}$	Active low output - requires pull-up resistor	OD (5V)
7	SMDATA	SMBus data input/output - requires external pull-up resistor	DIOD (5V)
8	SMCLK	SMBus clock input - requires external pull-up resistor	DI (5V)
9	DUR_SEL	Selects peak detector duration	AI

Table 1.1 Pin Description for EMC1702 (continued)

PIN NUMBER	PIN NAME	PIN FUNCTION	PIN TYPE
10	TH_SEL	Selects peak detector threshold	AI
11	SENSE-	Negative current sense measurement point	AI (24V)
12	SENSE+	Positive current sense measurement point	AI (24V)
Bottom Pad	GND	Ground	Power

The pin types are described in Table 1.2. All pins labeled with (5V) are 5V tolerant. All pins labeled with (24V) are 24V tolerant.

Table 1.2 Pin Types

PIN TYPE	DESCRIPTION
Power	This pin is used to supply power or ground to the device.
AI	Analog Input - this pin is used as an input for analog signals.
AIO	Analog Input / Output - this pin is used as an I/O for analog signals.
OD	Open Drain Digital Output - this pin is used as a digital output. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.
DI	Digital Input - this pin is used for digital inputs. This pin is 5V tolerant.
DIOD	Open Drain Digital Input / Output - this pin is bi-directional. It is open drain and requires a pull-up resistor. This pin is 5V tolerant.

Chapter 2 Electrical Characteristics

Table 2.1 Absolute Maximum Ratings

Voltage on 5V tolerant pins	-0.3 to 5.5	V
Voltage on 2V tolerant pins	-0.3 to 2	V
Voltage on VDD, SENSE- and SENSE+ pins	-0.3 to 26	V
Voltage on any other pin to GND	-0.3 to 4	V
Voltage between Sense pins (|(SENSE+ - SENSE-)|)	< 6	V
Package Power Dissipation	0.5W up to T_A = 85°C	W
Junction to Ambient (θ_{JA}) (QFN12 package)	58	°C/W
Operating Ambient Temperature Range	-40 to 85	°C
Storage Temperature Range	-55 to 150	°C
ESD Rating - SMCLK, SMDATA, $\overline{\text{ALERT}}$, $\overline{\text{THERM}}$ pins - HBM	4000	V
ESD Rating - All other pins - HBM	2000	V

Note 2.1 Stresses at or above those values listed could cause permanent damage to the device. This is a stress rating only, and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied. Prolonged stresses above the stated operating levels and below the Absolute Maximum Ratings may degrade device performance and lead to permanent damage.

Note 2.2 All voltages are relative to ground.

Note 2.3 The Package Power Dissipation specification assumes a thermal via design with the thermal landing be soldered to the PCB ground plane with four 12 mil vias.

Note 2.4 Junction to Ambient (θ_{JA}) is dependent on the design of the thermal vias. Without thermal vias and a thermal landing, the θ_{JA} is approximately 60°C/W including localized PCB temperature increase.

2.1 Electrical Specifications

Table 2.2 Electrical Specifications

V_{DD} = V_{BUS} = 3V TO 24V, V_{PULLUP} = 3V TO 5.5V, T_A = -40°C TO 85°C, ALL TYPICAL VALUES AT V_{DD} = V_{PULLUP} = 3.3V, V_{BUS} = 12V, AND T_A = 27°C UNLESS OTHERWISE NOTED.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
DC POWER						
Supply Voltage	V_{DD}	3		24	V	
VDD Pin Supply Current	I_{DD}		610	750	uA	Temp conversions at 0.0625 conversions / second, dynamic averaging disabled current sense active
			650	950	uA	Temp conversions at 4 conversions / second, dynamic averaging disabled current sense active
			950	1100	uA	Temp conversions at 8 conversions / second, dynamic averaging enabled current sense active
VDD Pin Supply Current	$I_{DD\_T\_STANDBY}$			750	uA	Temp conversions disabled (TMEAS / STOP = '1') current sense active
VDD Pin Supply Current	$I_{DD\_ALL\_STANDBY}$			300	uA	Temp conversions disabled (TMEAS / STOP = '1') Current sense disabled (IMEAS / STOP = '1')
SENSE+ Pin Bias Current	I_{SENSE+}		90		uA	V_{SENSE} = 0V, V_{DD} = 3V to 24V, Current sense active
			15		uA	V_{SENSE} = 0V, V_{DD} = 3V to 24V, current sense disabled
			10	20	uA	V_{DD} = 0V
SENSE- Pin Bias Current	I_{SENSE-}		10		uA	V_{SENSE} = 0V, V_{DD} = 3V to 24V, Current sense active
			10		uA	V_{SENSE} = 0V, VDD = 3V to 24V, current sense disabled
			0		uA	V_{DD} = 0V
Pull-up Voltage	V_{PULLUP}	3		5.5	V	Pull-up voltage for SMBus, $\overline{\text{ALERT}}$, and $\overline{\text{THERM}}$ pins
Leakage Current (±)	I_{LEAK}			5	uA	$\overline{\text{ALERT}}$ and $\overline{\text{THERM}}$ pins, SMDATA and SMCLK pins powered or unpowered, T_A < 85°C

Table 2.2 Electrical Specifications (continued)

V_{DD} = V_{BUS} = 3V TO 24V, V_{PULLUP} = 3V TO 5.5V, T_A = -40°C TO 85°C, ALL TYPICAL VALUES AT V_{DD} = V_{PULLUP} = 3.3V, V_{BUS} = 12V, AND T_A = 27°C UNLESS OTHERWISE NOTED.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
CURRENT SENSE						
Common Mode Voltage	V_{CM}	3		24	V	Voltage on SENSE+ and/or SENSE- pins, referenced to Ground
Differential Mode Voltage	V_{DIFF}	-6		+6	V	Voltage between SENSE+ and SENSE- pins
Full Scale Range (±) (see Section 5.20)	FSR	0		10	mV	1 LSB = 4.885uV
		0		20	mV	1 LSB = 9.77uV
		0		40	mV	1 LSB = 19.54uV
		0		80	mV	1 LSB = 39.08uV
Total Measurement Error (±)	V_{SENSE_ERR}		0.5	1	%	Total Error, FSR = 80mV
				3	%	Total Error, FSR = 10mV to 40mV
Offset Error (±)	V_{SENSE_OFF}			3	LSB	Offset Error, FSR = 80mV
Power Supply Rejection	V_{SENSE_PSR}		-120		dB	FSR = 10mV to 80mV, 3V < V_{DD} < 24V
Common Mode Rejection	V_{SENSE_CMR}		-110		dB	FSR = 10mV to 80mV, 3V < V_{BUS} < 24V
SOURCE VOLTAGE						
Full Scale Voltage	FSV	3		23.9883	V	Voltage on SENSE+ pin
Total Measurement Error (±) (see Section 4.1.2)	V_{SOURCE_ERR}		0.2	0.5	%	
POWER RATIO						
Full Scale Range		0		100	%	1 LSB = 1.53m%
Total Measurement Error (±)	P_{RATIO_ERR}			1.6	%	FSR = 80mV
				3	%	FSR = 10mV to 40mV
CURRENT SENSE PEAK DETECTION						
Peak Detector Threshold Range	V_{TH}	10		85	mV	Programmable via TH_SEL pin
Peak Detector Duration Range	T_{DUR}	1		4096	ms	Programmable via DUR_SEL pin
V_{SENSE} Peak Detection	t_{FILTER}		5		us	

Table 2.2 Electrical Specifications (continued)

V_{DD} = V_{BUS} = 3V TO 24V, V_{PULLUP} = 3V TO 5.5V, T_A = -40°C TO 85°C, ALL TYPICAL VALUES AT V_{DD} = V_{PULLUP} = 3.3V, V_{BUS} = 12V, AND T_A = 27°C UNLESS OTHERWISE NOTED.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNIT**	**CONDITIONS**
Threshold Accuracy (±)	V_{TH_ERR}		2	5	%	V_{TH} = 80mV
EXTERNAL TEMPERATURE MONITORS						
Temperature Accuracy (±)			0.25	1	°C	+20°C < T_{DIODE} < +110°C 0°C < T_A < 85°C
			0.5	2	°C	-40°C < T_{DIODE} < 127°C
Temperature Resolution			0.125		°C	
Diode Decoupling Capacitor	C_{FILTER}		2200	2700	pF	Connected across external diode, CPU, GPU, or AMD diode
Series Resistance Canceled	R_{SERIES}			100	Ohm	Sum of series resistance in both DP and DN lines
INTERNAL TEMPERATURE MONITOR						
Temperature Accuracy (±)			0.25	1	°C	-5°C < T_A < 85°C
				2	°C	-40°C < T_A < 85°C
Temperature Resolution			0.125		°C	
CONVERSION TIMES						
First Conversion Ready	t_{CONV_T}		180	300	ms	Time after power up before temperature and voltage measurements updated and P_{RATIO} updated
SMBus Delay	t_{SMB_D}			25	ms	Time before SMBus communications should be sent by host
DIGITAL I/O PINS (SMCLK, SMDATA, $\overline{\text{THERM}}$, $\overline{\text{ALERT}}$)						
Input High Voltage	V_{IH}	2.0			V	SMCLK, SMDATA OD pins pulled up to V_{PULLUP}
Input Low Voltage	V_{IL}			0.8	V	
Output Low Voltage	V_{OL}			0.4	V	OD pin pulled to V_{PULLUP} 4 mA current sink

APPLICATION NOTE: The EMC1702 is trimmed at the 80mV range for best accuracy.

2.2 SMBus Electrical Specifications

Table 2.3 SMBus Electrical Specifications

V_{DD}= V_{BUS} = 3V to 24V, V_{PULLUP} = 3V to 5.5V, T_A = -40°C to 85°C Typical values are at T_A = 27°C unless otherwise noted.						
CHARACTERISTIC	**SYMBOL**	**MIN**	**TYP**	**MAX**	**UNITS**	**CONDITIONS**
SMBUS INTERFACE						
Input Capacitance	C_{IN}		4	10	pF	
SMBUS TIMING						
Clock Frequency	f_{SMB}	10		400	kHz	
Spike Suppression	t_{SP}			50	ns	
Bus Free Time Start to Stop	t_{BUF}	1.3			us	
Setup Time: Start	$t_{SU:STA}$	0.6			us	
Setup Time: Stop	$t_{SU:STO}$	0.6			us	
Data Hold Time	$t_{HD:DAT}$	0			us	
Data Setup Time	$t_{SU:DAT}$	0.6			us	
Clock Low Period	t_{LOW}	1.3			us	
Clock High Period	t_{HIGH}	0.6			us	
Clock/Data Fall time	t_{FALL}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Clock/Data Rise time	t_{RISE}			300	ns	Min = $20+0.1C_{LOAD}$ ns
Capacitive Load	C_{LOAD}			400	pF	Total per bus line

Chapter 3 Communications

3.1 System Management Bus Interface Protocol

The EMC1702 communicates with a host controller, such as an SMSC SIO, through the SMBus. The SMBus is a two-wire serial communication protocol between a computer host and its peripheral devices. A detailed timing diagram is shown in Figure 3.1. Stretching of the SMCLK signal is supported; however, the EMC1702 will not stretch the clock signal.

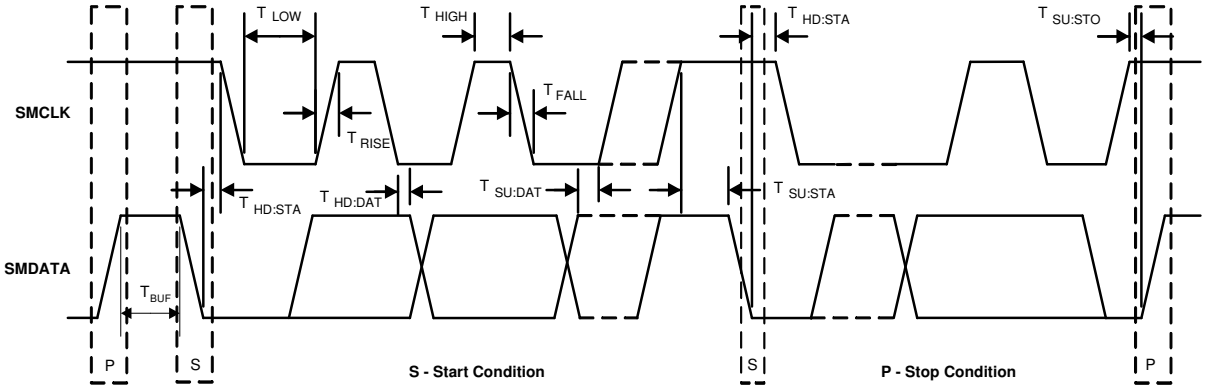


Figure 3.1 SMBus Timing Diagram

3.1.1 SMBus Start Bit

The SMBus Start bit is defined as a transition of the SMBus Data line from a logic '1' state to a logic '0' state while the SMBus Clock line is in a logic '1' state.

3.1.2 SMBus Address and RD / $\overline{WR}$ Bit

The SMBus Address Byte consists of the 7-bit client address followed by a 1-bit RD / $\overline{WR}$ indicator. If this RD / $\overline{WR}$ bit is a logic '0', the SMBus host is writing data to the client device. If this RD / $\overline{WR}$ bit is a logic '1', the SMBus host is reading data from the client device.

The EMC1702 SMBus address is determined by a single resistor connected between ground and the ADDR_SEL pin as shown in Table 3.1.

Table 3.1 ADDR_SEL Resistor Setting

RESISTOR (5%)	SMBUS ADDRESS	RESISTOR (5%)	SMBUS ADDRESS
0	1001_100(r/w)	1600	0101_000(r/w)
100	1001_101(r/w)	2000	0101_001(r/w)
180	1001_110(r/w)	2700	0101_010(r/w)
300	1001_111(r/w)	3600	0101_011(r/w)
430	1001_000(r/w)	5600	0101_100(r/w)

Table 3.1 ADDR_SEL Resistor Setting (continued)

RESISTOR (5%)	SMBUS ADDRESS	RESISTOR (5%)	SMBUS ADDRESS
560	1001_001(r/w)	9100	0101_100(r/w)
750	1001_010(r/w)	20000	0101_101(r/w)
1270	1001_011(r/w)	Open	0011_000(r/w)

All SMBus Data bytes are sent most significant bit first and composed of 8-bits of information.

3.1.3 SMBus ACK and NACK Bits

The SMBus client will acknowledge all data bytes that it receives (as well as the client address if it matches and the ARA address if the $\overline{\text{ALERT}}$ pin is asserted). This is done by the client device pulling the SMBus Data line low after the 8th bit of each byte that is transmitted.

The host will NACK (not acknowledge) the data received from the client by holding the SMBus data line high after the 8th data bit has been sent.

3.1.4 SMBus Stop Bit

The SMBus Stop bit is defined as a transition of the SMBus Data line from a logic ‘0’ state to a logic ‘1’ state while the SMBus clock line is in a logic ‘1’ state. When the EMC1702 detects an SMBus Stop bit, and it has been communicating with the SMBus protocol, it will reset its client interface and prepare to receive further communications.

3.1.5 SMBus Time-out

The EMC1702 includes an SMBus time-out feature. Following a 30ms period of inactivity on the SMBus, the device will time-out and reset the SMBus interface.

The time-out functionality defaults to disabled and can be enabled by writing to the TIMEOUT bit (see Section 5.12).

3.1.6 SMBus and I^2C Compliance

The major differences between SMBus and I^2C devices are highlighted here. For complete compliance information, refer to the SMBus 2.0 specification.

1. Minimum frequency for SMBus communications is 10kHz.
2. The client protocol will reset if the clock is held at a logic ‘0’ for longer than 30ms. This time-out functionality is disabled by default.
3. The client protocol will reset if both the clock and data lines are held at a logic ‘1’ for longer than 150us. This function is disabled by default.
4. I^2C devices do not support the Alert Response Address functionality (which is optional for SMBus).

3.2 SMBus Protocols

The EMC1702 is SMBus 2.0 compatible and supports Send Byte, Read Byte, Receive Byte, Write Byte, Block Read, and Block Write as valid protocols. It will respond to the Alert Response Address protocol but is not in full compliance.

All of the protocols listed below use the convention in Table 3.2.

Table 3.2 Protocol Format

DATA SENT TO DEVICE	DATA SENT TO THE HOST
# of bits sent	# of bits sent

3.2.1 Write Byte

The Write Byte is used to write one byte of data to the registers, as shown in Table 3.3:

Table 3.3 Write Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	XXh	0	0 -> 1

3.2.2 Read Byte

The Read Byte protocol is used to read one byte of data from the registers, as shown in Table 3.4.

Table 3.4 Read Byte Protocol

START	SLAVE ADDRESS	WR	ACK	Register Address	ACK	START	Slave Address	RD	ACK	Register Data	NACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	0 -> 1	YYYY_YYY	1	0	XXh	1	0 -> 1

3.2.3 Send Byte

The Send Byte protocol is used to set the internal address register pointer to the correct address location. No data is transferred during the Send Byte protocol, as shown in Table 3.5.

Table 3.5 Send Byte Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	STOP
1 -> 0	YYYY_YYY	0	0	XXh	0	0 -> 1

3.2.4 Receive Byte

The Receive Byte protocol is used to read data from a register when the internal register address pointer is known to be at the right location (e.g. set via Send Byte). This is used for consecutive reads of the same register, as shown in Table 3.6.

Table 3.6 Receive Byte Protocol

START	SLAVE ADDRESS	RD	ACK	REGISTER DATA	NACK	STOP
1 -> 0	YYYY_YYY	1	0	XXh	1	0 -> 1

3.2.5 Block Write

The Block Write is used to write multiple data bytes to a group of contiguous registers, as shown in Table 3.7. It is an extension of the Write Byte Protocol.

Table 3.7 Block Write Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	REGISTER DATA	ACK
1 ->0	YYYY_YYY	0	0	XXh	0	XXh	0
REGISTER DATA	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**ACK**	**STOP**
XXh	0	XXh	0	. . .	XXh	0	0 -> 1

3.2.6 Block Read

The Block Read is used to read multiple data bytes from a group of contiguous registers, as shown in Table 3.8. It is an extension of the Read Byte Protocol.

Table 3.8 Block Read Protocol

START	SLAVE ADDRESS	WR	ACK	REGISTER ADDRESS	ACK	START	SLAVE ADDRESS	RD	ACK	REGISTER DATA
1->0	YYYY_YYY	0	0	XXh	0	1 ->0	YYYY_YYY	1	0	XXh
ACK	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**REGISTER DATA**	**ACK**	**. . .**	**REGISTER DATA**	**NACK**	**STOP**
0	XXh	0	XXh	0	XXh	0	. . .	XXh	1	0 -> 1

3.2.7 Alert Response Address

The $\overline{\text{ALERT}}$ output can be used as a processor interrupt or as an SMBus Alert when configured to operate as an interrupt.

When it detects that the $\overline{\text{ALERT}}$ pin is asserted, the host will send the Alert Response Address (ARA) to the general address of 0001_100xb. All devices with active interrupts will respond with their client address, as shown in Table 3.9.

Table 3.9 Alert Response Address Protocol

START	ALERT RESPONSE ADDRESS	RD	ACK	DEVICE ADDRESS	NACK	STOP
1 -> 0	0001_100	1	0	YYYY_YYY	1	0 -> 1

The EMC1702 will respond to the ARA in the following way if the $\overline{\text{ALERT}}$ pin is asserted.

1. Send Slave Address and verify that full slave address was sent (i.e. the SMBus communication from the device was not prematurely stopped due to a bus contention event).
2. Set the MASK bit to clear the $\overline{\text{ALERT}}$ pin.

Chapter 4 General Description

The EMC1702 is a combination high-side current sensing device with precision voltage and temperature measurement capabilities. It measures the voltage developed across an external sense resistor to represent the high-side current of a battery or voltage regulator. The EMC1702 also measures the source voltage and uses these measured values to present a proportional power calculation. The EMC1702 contains additional bi-directional peak detection circuitry to flag instantaneous current spikes with programmable time duration and magnitude threshold. Finally, the EMC1702 includes an external diode channel for temperature measurement as well as an internal diode for ambient temperature measurements.

The EMC1702 current-sense measurement converts differential input voltage measured across an external sense resistor to a proportional output voltage. This voltage is digitized using a variable resolution (13-bit to 15-bit) Sigma-Delta ADC and transmitted via the SMBus or I^2C protocol. The current range allows for large variations in measured current with high accuracy and low voltage drop across the resistor.

The supply voltage is also measured and stored. When combined with the sense resistor voltage measurement the power provided from the source can be determined. Programmable limits on both voltage and current levels are used to generate an interrupt.

The EMC1702 has two levels of monitoring. The first provides a maskable $\overline{\text{ALERT}}$ signal to the host when the measured temperatures or voltages meet or exceed user programmable limits. This allows the EMC1702 to be used as an independent thermal watchdog to warn the host of temperature hot spots without direct control by the host. The second level of monitoring provides a non maskable interrupt on the $\overline{\text{THERM}}$ pin if the measured values meet or exceed a second programmable limit.

The temperature measurement includes advanced features such as Resistance Error Correction (REC), Beta Compensation (to support CPU diodes requiring the BJT/transistor model including 45nm and 65nm processors) and automatic diode type detection. These features combine to provide a robust solution for complex environmental monitoring applications.

A system diagram is shown in Figure 4.1.

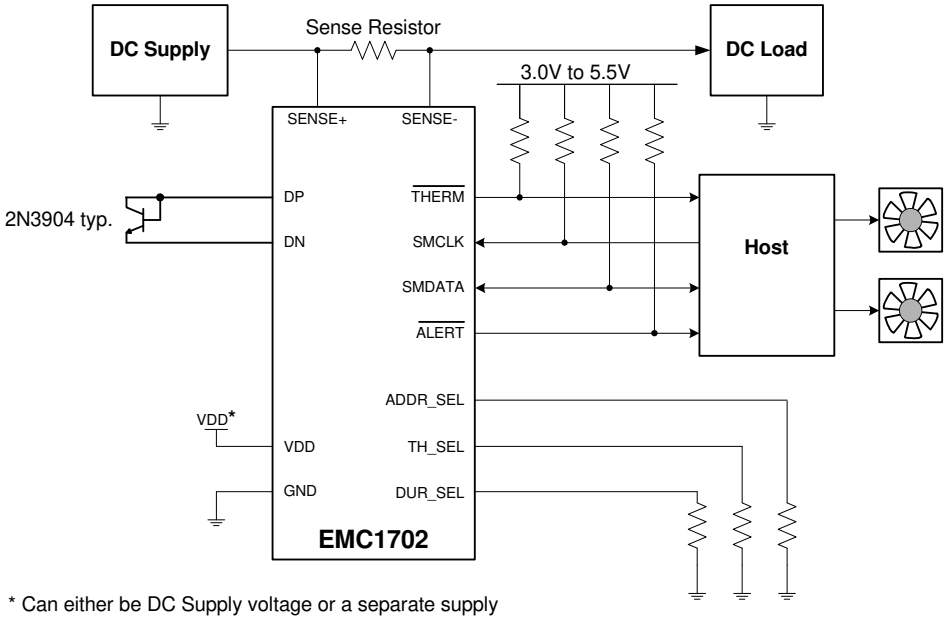


Figure 4.1 EMC1702 System Diagram

4.1 Source Monitoring

The EMC1702 includes circuitry for both source current sensing and source voltage measurement. From these measurements, a ratiometric value corresponding to the power delivered at the SENSE+ pin is provided.

4.1.1 Current Measurement

The EMC1702 includes a high-side current sensing circuit. This circuit measures the voltage, V_{SENSE}, induced across a fixed external current sense resistor, R_{SENSE}, and stores a representative voltage as a signed 11-bit number in the Sense Voltage Registers (see Section 5.22).

This circuitry is able to measure the direction of current flow (from SENSE+ to SENSE- or from SENSE- to SENSE+). Current flowing from SENSE+ to SENSE- is defined as positive current. Current flowing from SENSE- to SENSE+ is defined as negative.

The EMC1702 contains user programmable bipolar Full Scale Sense Ranges (FSSR) of ±10mV, ±20mV, ±40mV, or ±80mV (see Section 5.20). The default for this setting is ±80mV.

Each V_{SENSE} measurement is averaged over a user programmable time (see Section 5.20). It is compared against programmable high and low limits (see Section 5.25). If V_{SENSE} exceeds (or drops below) the respective limits, the $\overline{ALERT}$ pin may be asserted (the default operation is to enable current sense interrupts on the $\overline{ALERT}$ pin).

The EMC1702 also contains user programmable current peak detection circuitry (see Section 4.1.4) that will assert the $\overline{THERM}$ pin if a current spike is detected larger than the programmed threshold and of longer duration than the programmed time. This circuitry is independent of V_{SENSE}.

Full Scale Current (FSC) can be calculated from:

$FSC = \frac{FSR}{R_{SENSE}}$	where:	**[1]**
	FSC is the Full-Scale Current	
	FSR, the Full Scale Range, is either 10mV, 20mV, 40mV or 80mV (see Section 5.20)	
	R_{SENSE} is the external sense resistor value	

Actual source current through R_{SENSE} can then be calculated using:

$I_{SOURCE} = FSC \times \frac{V_{SENSE}}{2,047}$	where:	**[2]**
	I_{SOURCE} is the actual source current	
	FSC is the Full-Scale Current value (from Equation [1])	
	V_{SENSE} is the value read from the Sense Voltage Registers, ignoring the four lowest bits which are always zero (see Section 5.22)	

For example: Suppose the system is drawing 1.65A through a 10mΩ resistor and the FSR is set for 20mV. Therefore, by Equation [1], the FSC is 2A.

For a positive voltage the Sense Voltage Registers are read, ignoring the lower four bits since they are always zero, as 69_8h (0110_1001_1000b or 1688d) which is 82.5% of the full scale source current. This results in a calculated source current of 1.649A using Equation [2].

For a negative voltage the Sense Voltage Registers are read as 96_8h, also ignoring the lower four bits since they are always zero. To calculate source current the binary value is first converted from two's complement by inverting the bits and adding one:

96_8h = 1001_0110_1000b. Inverting equals 0110_1001_0111b (69_7h) and adding one gives 0110_1001_1000b (69_8h).

This results in the same calculated value as in the positive voltage case.

4.1.2 Voltage Measurement

Source voltage is measured on the supply side of the R_{SENSE} resistor (SENSE+) and stored as an unsigned 11-bit number in the Source Voltage Registers as V_{SOURCE} (see Section 5.23).

Each V_{SOURCE} measurement is averaged over a user programmable time (see Section 5.6 and Section 5.19). The measurement is delayed by the programmed conversion rate. V_{SOURCE} is compared against programmable high, low, and critical limits (see Section 5.15, Section 5.16, and Section 5.17). If the value meets or exceeds the high limits or drops below the low limits, the $\overline{ALERT}$ pin may be asserted (default is to enable this function). If the value meets or exceeds the critical limit, the $\overline{THERM}$ pin will be asserted (see Section 5.27).

Full Scale Voltage (FSV) is given by the maximum value of the Source Voltage Registers:

$FSV = 23.9883\,V$	where:	**[3]**
	FSV is the Full-Scale Voltage (a constant)	

Actual source voltage at the SENSE+ pin can be calculated using:

$Source\ Voltage = FSV \times \frac{V_{SOURCE}}{4,094}$	where:	**[4]**
	Source Voltage is the voltage at the SENSE+ pin	
	FSV is the Full-Scale Voltage (from Equation [3])	
	V_{SOURCE} is the digital value read from the Source Voltage Registers. Note that the lowest five bits are always zero (see Section 5.23)	

For example: Suppose that the actual source voltage is 10.65V. The Source Voltage Registers are read as V_{SOURCE} = 71_Ah (0111_0001_1010b or 1818d) which is 44.4% of the full scale source voltage. This results in a calculated source voltage of 10.65V using Equation [4].

Note that the actual source voltage may also be determined by scaling each bit set by the indicated bit weighting as described in Section 5.23.

4.1.3 Power Calculation

The EMC1702 may be used to determine the average power provided at the source side of R_{SENSE} (SENSE+) using the value, P_{RATIO}, contained in the Power Ratio Registers (see Section 5.24). The value represents the % of maximum calculable power.

P_{RATIO} is mathematically generated by multiplying the absolute values of V_{SENSE} and V_{SOURCE} (see Section 4.1.1 and Section 4.1.2) and stored as a shifted 16-bit unsigned number. P_{RATIO} is updated whenever either V_{SENSE} or V_{SOURCE} is updated.

Full Scale Power can be calculated from:

$FSP = FSC \times FSV$	where: FSP is the Full-Scale Power FSC is the Full-Scale Current (from Equation [1]) FSV is the Full-Scale Voltage (from Equation [3])	**[5]**

Actual power drawn from the source can be calculated using:

$P_{SOURCE} = FSP \times \frac{P_{RATIO}}{65,535}$	where: P_{SOURCE} is the actual power provided by the source measured at SENSE+ FSP is the Full-Scale Power (from Equation [5]) P_{RATIO} is the value read from the Power Ratio Registers (see Section 5.24)	**[6]**

For example: Suppose that the actual source voltage is 10.65V and the source current through a 10mΩ resistor is 1.65A. The FSC value is 2A per Equation [1]; thus, the expected power is 17.573W which is 36.6% of the FSP value.

Reading the Power Ratio Registers will report P_{RATIO} as 24,003d (0101_1101_1100_0011b or 5D_C3h), which is 36.6% of the full scale source power. This results in a calculated source power of 17.6W.

4.1.4 Current Peak Detection

The EMC1702 includes a hardware set instantaneous current peak detector. The peak detector threshold and duration values may also be set via the SMBus.

The peak detector supports detection of current spikes that occur faster than the minimum current sensing conversion time. This allows quick reaction to events requiring system-level response. The circuitry compares the measured current against a user-defined threshold value and user-defined time duration. If the measured current exceeds the threshold, an internal timer is started. If the timer reaches the programmed duration, the $\overline{\text{THERM}}$ pin is asserted (see Figure 4.2 for an example of peak current detection) and the PEAK status bit set.

The $\overline{\text{THERM}}$ pin will remain asserted until the Peak is no longer detected at which point it will be released. The PEAK status bit will likewise be cleared.

The Peak Detection circuitry may also assert the $\overline{\text{ALERT}}$ pin. In this case, the $\overline{\text{ALERT}}$ pin must be configured to operate in Comparator mode. If the $\overline{\text{ALERT}}$ pin is configured to operate in Interrupt mode, the Peak Detection circuitry will not cause the $\overline{\text{ALERT}}$ pin to be asserted.

The Peak Detection circuitry includes filtering (t_{FILTER}). When the instantaneous current exceeds the threshold, it must drop below the threshold for a period of time greater than t_{FILTER} before the timer is reset. The Peak Detection circuitry works for current flowing in either direction through the sense resistor (R_{SENSE}).

APPLICATION NOTE: The Peak Detector circuitry works independently of the current measurement integration.

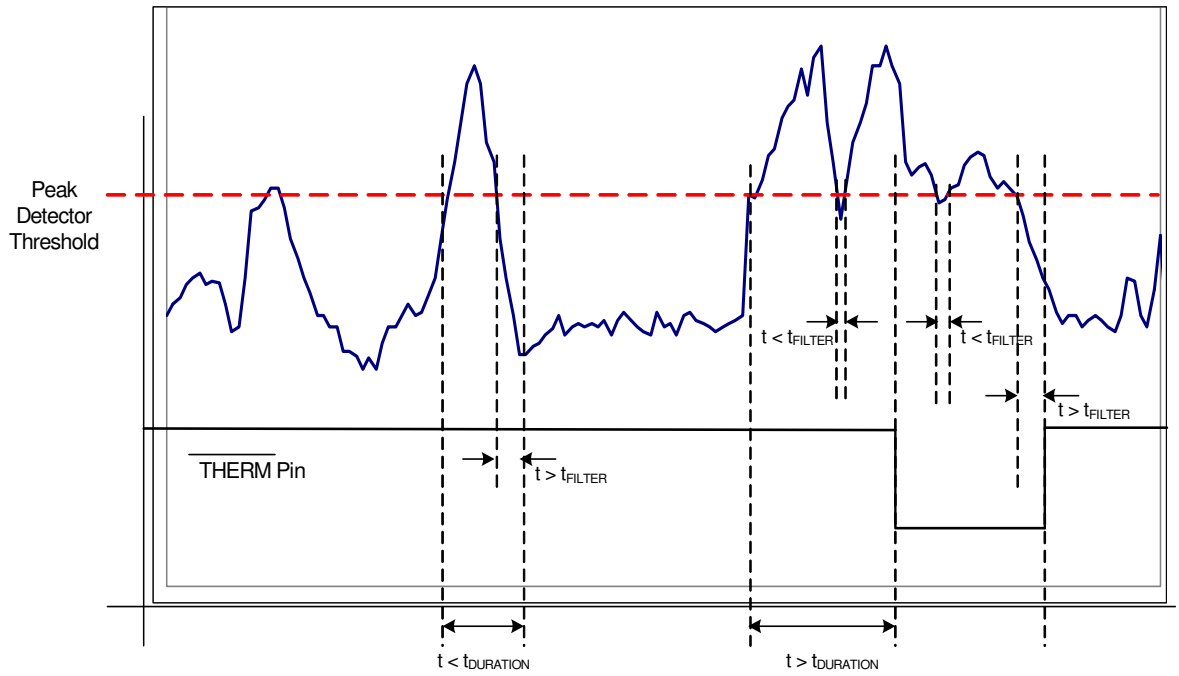


Figure 4.2 Peak Detection Example

The peak detector threshold is determined upon device power up by the value of the resistor connected between the TH_SEL pin and ground or via the SMBus (see Section 5.21). The resistor selects one of 16 different V_{SENSE} measurement limits (from 10mV to 85mV) as shown in Table 4.1.

Table 4.1 TH_SEL Resistor Setting

RESISTOR (5%)	PEAK DETECTION THRESHOLD	RESISTOR (5%)	PEAK DETECTION THRESHOLD
0	10mV	1600	50mV
100	15mV	2000	55mV
180	20mV	2700	60mV
300	25mV	3600	65mV
430	30mV	5600	70mV
560	35mV	9100	75mV
750	40mV	20000	80mV
1270	45mV	Open	85mV

The peak detector duration is determined upon device power up by the value of the resistor between the DUR_SEL pin and ground or via the SMBus (see Section 5.21). The resistor selects one of 16 different time durations from 1 ms to 4.096s as shown in Table 4.2.

Table 4.2 DUR_SEL Resistor Setting

RESISTOR (5%)	PEAK DETECTION MINIMUM DURATION ($T_{DURATION}$)	RESISTOR (5%)	PEAK DETECTION MINIMUM DURATION ($T_{DURATION}$)
0	1ms	1600	384ms
100	5ms	2000	512ms
180	26 ms	2700	768ms
300	51 ms	3600	1024ms
430	77 ms	5600	1536ms
560	102ms	9100	2048ms
750	128ms	20000	3072ms
1270	256ms	Open	4096ms

4.2 VDD Biasing Options

The wide device operating voltage range allows the EMC1702 to be powered from either the source voltage or an external supply. The EMC1702 contains circuitry to detect the voltage supply level on the VDD pin and enable an internal regulator as necessary.

4.3 Modes of Operation

The EMC1702 has multiple modes of operation as described here:

- Fully Active - In this mode of operation, the device is measuring all temperature channels, source voltage, and sense voltage. All data is updated at the end of the respective conversion and the limits are checked. Writing to the One-Shot register will have no effect.
- Current Sense only - In this mode of operation, the device is measuring source voltage and sense voltage only. The temperature data is not updated. V_{SOURCE} and V_{SENSE} data are updated at the end of the respective conversion and the limits are checked. Writing to the One-Shot register will update the temperature measurements. This one-shot measurement may cause the $\overline{ALERT}$ or $\overline{THERM}$ pins to be asserted if the measured temperature violates the respective limits.
- Temperature only - In this mode of operation, the device is measuring the temperature channels only. V_{SOURCE} and V_{SENSE} data are not updated. The temperature data is updated at the end of the conversion and the limits are checked. Writing to the One-Shot register will update V_{SOURCE} and V_{SENSE}. This one-shot measurement may cause the $\overline{ALERT}$ or $\overline{THERM}$ pins to be asserted if the measured voltage or current sense readings meet or exceed the respective limits.
- Standby (Stop) - In this mode of operation, the majority of circuitry is powered down to reduce supply current. The temperature, source voltage, and sense voltage measurements are not updated and the limits are not checked. In this mode of operation, the SMBus is fully active and the part will return requested data. Writing to the One-Shot register (see Section 5.8) will enable the device to update all measurement channels (temperature, V_{SOURCE}, and V_{SENSE}). This one-shot measurement may cause the $\overline{ALERT}$ or $\overline{THERM}$ pins to be asserted if any of the measured values violate their respective limits. Once all the channels are updated, the device will return to the Standby mode.

4.4 $\overline{\text{ALERT}}$ Output

The $\overline{\text{ALERT}}$ pin is an open drain output and requires a pull-up resistor to V_{PULLUP} and has two modes of operation: Interrupt mode and Comparator mode. The mode of the $\overline{\text{ALERT}}$ output is selected via the ALERT / COMP bit in the Configuration Register (see Section 5.5).

The $\overline{\text{ALERT}}$ pin modes apply to the High Limit only for all channels. The Low Limits and diode faults will always cause the $\overline{\text{ALERT}}$ pin to behave as if it were in Interrupt mode.

The $\overline{\text{ALERT}}$ pin is used as an interrupt signal or as an SMBus Alert signal that allows an SMBus slave to communicate an error condition to the master. One or more SMBus Alert outputs can be hard-wired together.

4.4.1 $\overline{\text{ALERT}}$ Pin Interrupt Mode

When configured to operate in Interrupt mode, the $\overline{\text{ALERT}}$ pin asserts low when an out-of-limit measurement ($\geq$ high limit or < low limit) is detected on any temperature measurement and the consecutive alert queue has been filled. The $\overline{\text{ALERT}}$ pin will also be asserted if a diode fault is detected.

Additionally, the $\overline{\text{ALERT}}$ pin may be asserted if the measured current or the source voltage are out of limit ($\geq$ high limit or < low limit).

The $\overline{\text{ALERT}}$ pin will remain asserted as long as an out-of-limit condition remains. Once the out-of-limit condition has been removed, the $\overline{\text{ALERT}}$ pin will remain asserted until the appropriate status bits are cleared. The pin can be masked by setting the MASK_ALL bit. Once the $\overline{\text{ALERT}}$ pin has been masked, it will be de-asserted and remain de-asserted until the MASK_ALL bit is cleared by the user. Any interrupt conditions that occur while the $\overline{\text{ALERT}}$ pin is masked will update the Status Register normally.

When the $\overline{\text{ALERT}}$ pin is configured to operate in Interrupt mode, the Peak Detector circuitry will not generate interrupts when a current peak is detected.

4.4.2 $\overline{\text{ALERT}}$ Pin Comparator Mode

When the $\overline{\text{ALERT}}$ pin is configured to operate in Comparator mode, it will be asserted if any of the measured temperatures meets or exceeds the respective high limit. The $\overline{\text{ALERT}}$ pin will remain asserted until all temperatures drop below the corresponding high limit minus the Tcrit Hysteresis value (see Section 5.9).

Additionally, the $\overline{\text{ALERT}}$ pin may be asserted if the measured current or the source voltage meet or exceed their respective high limit. The $\overline{\text{ALERT}}$ pin will remain asserted until the measured values drop below the corresponding high limit minus the Vcrit Hysteresis value (see Section 5.27).

When the $\overline{\text{ALERT}}$ pin is asserted in Comparator mode, the corresponding high limit status bits will be set. Reading these bits will not clear them until the $\overline{\text{ALERT}}$ pin is deasserted. Once the $\overline{\text{ALERT}}$ pin is deasserted, the status bits will be automatically cleared.

The MASK_ALL (see Section 5.5) bit will not block the $\overline{\text{ALERT}}$ pin in this mode; however, individual mask bits (see Section 5.11) will control the respective events that will assert the $\overline{\text{ALERT}}$ pin.

When the $\overline{\text{ALERT}}$ pin is configured to operate in Comparator mode and the Peak Detector circuitry is linked to the $\overline{\text{ALERT}}$ pin, an interrupt will be generated when a current peak is detected (see Section 5.19).

4.5 $\overline{\text{THERM}}$ Output

The $\overline{\text{THERM}}$ output is asserted independently of the $\overline{\text{ALERT}}$ output and cannot be masked. Whenever any of the measured temperatures meets or exceeds the user programmed Tcrit Limit values for the programmed number of consecutive measurements, the $\overline{\text{THERM}}$ output is asserted. Once it has been asserted, it will remain asserted until all measured temperatures drops below the Tcrit Limit minus the Tcrit Hysteresis (also programmable).

Additionally, the $\overline{\text{THERM}}$ pin will be asserted if the current sense Peak Detection circuitry has detected a current spike (see Section 4.1.4). The $\overline{\text{THERM}}$ pin will remain asserted so long as the Peak Detection circuitry continues to detect excessive instantaneous current (greater than the programmed threshold).

As well, the $\overline{\text{THERM}}$ pin will be asserted if the measured current or source voltage meet or exceed the user programmed Vcrit Limit values. In this case, the $\overline{\text{THERM}}$ pin will remain asserted until all measured voltages drop below the Vcrit Limit minus the Vcrit Hysteresis (see Section 5.27).

4.6 Temperature Measurement

The EMC1702 can monitor the temperature of one externally connected diode. The external diode channel is configured with Resistance Error Correction and Beta Compensation based on user settings and system requirements.

The EMC1702 also measures the internal or ambient temperature.

The device contains programmable High, Low, and Tcrit limits for all measured temperature channels. If the measured temperature drops below the Low limit or above the High limit, the $\overline{\text{ALERT}}$ pin can be asserted (based on user settings). If the measured temperature meets or exceeds the Tcrit limit, the $\overline{\text{THERM}}$ pin is asserted unconditionally, providing two tiers of temperature detection.

4.6.1 Resistance Error Correction

The EMC1702 includes active Resistance Error Correction to remove the effect of up to 100 ohms of series resistance. Without this automatic feature, voltage developed across the parasitic resistance in the remote diode path causes the temperature to read higher than what the true temperature is. The error induced by parasitic resistance is approximately +0.7°C per ohm. Sources of series resistance include bulk resistance in the remote temperature transistor junctions, series resistance in the CPU resistance due to off-board connections, and resistance in the printed circuit board traces and package leads. Resistance Error Correction in the EMC1702 eliminates the need to characterize and compensate for parasitic resistance in the remote diode path.

The Resistance Error Correction can be disabled for each channel.

APPLICATION NOTE: When measuring AMD diodes, disable REC.

4.6.2 Beta Compensation

The forward current gain, or beta, of a transistor is not constant as emitter currents change. The variation in beta causes an error in temperature reading. Compensating for this error is also known as implementing the BJT or transistor model for temperature measurement.

For discrete transistors configured with the collector and base shorted together, the beta is generally sufficiently high such that the percent change in beta variation is very small. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 50 would contribute approximately 0.25°C error at 100°C. However for substrate transistors where the base-emitter junction is used for temperature measurement and the collector is tied to the substrate, the proportional beta variation will cause large error. For example, a 10% variation in beta for two forced emitter currents with a transistor whose ideal beta is 0.5 would contribute approximately 8.25°C error at 100°C.

The Beta Compensation circuitry in the EMC1702 corrects for this beta variation to eliminate any error which would normally be induced. It automatically detects the appropriate beta setting to use and will properly recognize and measure a discrete diode.

4.6.3 Ideality Factor

The EMC1702 is designed for external diodes with an ideality factor of 1.008. Not all external diodes, processor or discrete, will have this exact value. This variation of the ideality factor introduces error in the temperature measurement which must be corrected for. This correction is typically done using programmable offset registers. Since an ideality factor mismatch introduces an error that is a function of temperature, this correction is only accurate within a small range of temperatures. To provide maximum flexibility to the user, the EMC1702 provides a register for each external diode where the ideality factor of the diode used may be programmed to eliminate errors across all temperatures.

APPLICATION NOTE: When monitoring a substrate transistor or CPU diode and beta compensation is enabled, the Ideality Factor should not be adjusted. Beta Compensation automatically corrects for most ideality errors.

4.6.4 Dynamic Averaging

The EMC1702 supports dynamic averaging. When enabled, this feature changes the conversion time for all channels based on the selected conversion rate. This essentially increases the averaging factor as shown in Table 4.3. The benefits of Dynamic Averaging are improved noise rejection due to the longer integration time as well as less random variation on the temperature measurement.

Table 4.3 Dynamic Averaging Behavior

CONVERSION RATE	AVERAGING FACTOR (RELATIVE TO 11-BIT CONVERSION)	
	DYNAMIC AVERAGING ENABLED	DYNAMIC AVERAGING DISABLED
≤ 1 / sec	16x	1x
2 / sec	8x	1x
4 / sec	4x	1x
8 / sec	1x	1x

4.7 Diode Connections

For the EMC1702, the external diode channel supports any of the diode connections shown in Figure 4.3.

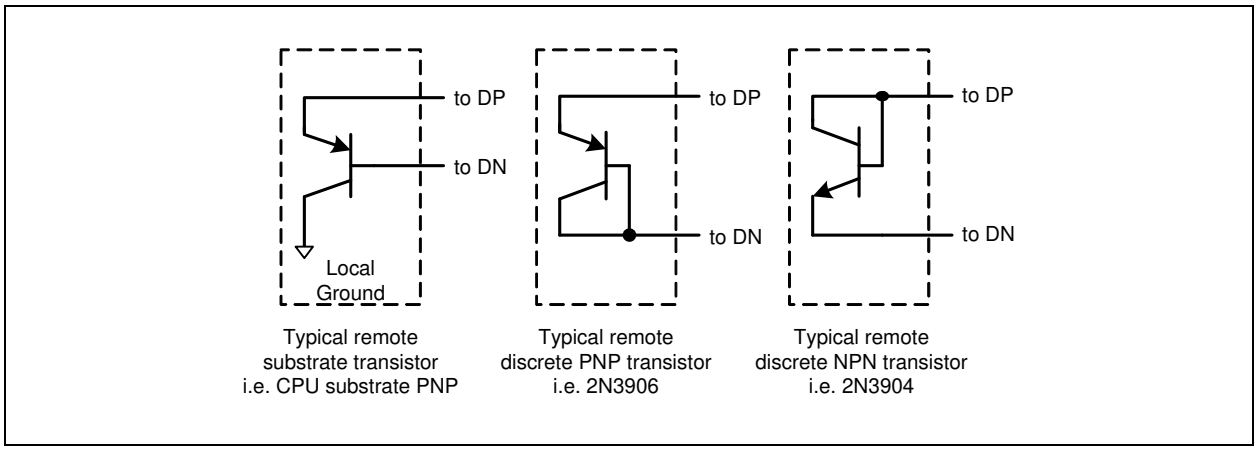


Figure 4.3 Diode Connections

4.7.1 Diode Faults

The EMC1702 actively detects an open and short condition on each measurement channel. When a diode fault is detected, the temperature data MSByte is forced to a value of 80h and the FAULT bit is set in the Status Register.

Chapter 5 Register Description

The registers shown in Table 5.1 are accessible through the SMBus. An entry of '-' indicates that the bit is not used and will always read '0'.

Table 5.1 Register Set in Hexadecimal Order

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
00h	R	Internal Diode Data High Byte	Stores the integer data for the Internal Diode (mirrored at address 38h)	00h	Page 32
01h	R	External Diode 1 Data High Byte	Stores the integer data for External Diode 1 (mirrored at address 3Ah)	00h	Page 32
02h	R	Status	Stores the status bits for the Internal Diode and External Diode (mirrored at address 34h)	00h	Page 33
03h	R/W	Configuration	Controls the general operation of the device (mirrored at address 09h)	00h	Page 34
04h	R/W	Conversion Rate	Controls the conversion rate for updating measurement data (mirrored at address 0Ah)	06h (4/sec)	Page 35
05h	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 0Bh)	55h (85°C)	Page 36
06h	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 0Ch)	80h (-128°C)	Page 36
07h	R/W	External Diode 1 High Limit High Byte	Stores the integer portion of the high limit for External Diode 1 (mirrored at register 0Dh)	55h (85°C)	Page 36
08h	R/W	External Diode 1 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 1 (mirrored at register 0Eh)	80h (-128°C)	Page 36
09h	R/W	Configuration	Controls the general operation of the device (mirrored at address 03h)	00h	Page 34
0Ah	R/W	Conversion Rate	Controls the conversion rate for updating measurement data (mirrored at address 04h)	06h (4/sec)	Page 35
0Bh	R/W	Internal Diode High Limit	Stores the 8-bit high limit for the Internal Diode (mirrored at address 05h)	55h (85°C)	Page 36
0Ch	R/W	Internal Diode Low Limit	Stores the 8-bit low limit for the Internal Diode (mirrored at address 06h)	80h (-128°C)	Page 36

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
0Dh	R/W	External Diode 1 High Limit High Byte	Stores the integer portion of the high limit for External Diode 1 (mirrored at register 07h)	55h (85°C)	Page 36
0Eh	R/W	External Diode 1 Low Limit High Byte	Stores the integer portion of the low limit for External Diode 1 (mirrored at register 08h)	80h (-128°C)	Page 36
0Fh	W	One-Shot	A write to this register initiates a one-shot update.	00h	Page 36
10h	R	External Diode 1 Data Low Byte	Stores the fractional data for External Diode 1 (mirrored at address 3Bh)	00h	Page 32
13h	R/W	External Diode 1 High Limit Low Byte	Stores the fractional portion of the high limit for External Diode 1	00h	Page 36
14h	R/W	External Diode 1 Low Limit Low Byte	Stores the fractional portion of the low limit for External Diode 1	00h	Page 36
19h	R/W	External Diode 1 Tcrit Limit	Stores the 8-bit critical temperature limit for External Diode 1	64h (100°C)	Page 37
1Bh	R-C	External Diode Fault	Stores status bits indicating which external diode detected a diode fault	00h	Page 37
1Fh	R/W	Channel Mask Register	Controls the masking of individual channels	00h	Page 37
20h	R/W	Internal Diode Tcrit Limit	Stores the 8-bit critical temperature limit for the Internal Diode	64h (100°C)	Page 37
21h	R/W	Tcrit Hysteresis	Stores the 8-bit hysteresis value that applies to all THERM limits	0Ah (10°C)	Page 37
22h	R/W	Consecutive Alert	Controls the number of out-of-limit conditions that must occur before an interrupt is asserted	70h	Page 38
25h	R/W	External Diode 1 Beta Configuration	Stores the Beta Compensation circuitry settings for External Diode 1	10h	Page 39
27h	R/W	External Diode 1 Ideality Factor	Stores the ideality factor for External Diode 1	12h (1.008)	Page 40
29h	R	Internal Diode Data Low Byte	Stores the fractional data for the Internal Diode (mirrored at register 39h)	00h	Page 32
34h	R-C	Status	Stores the status bits for the measured temperature channels, Current Sense circuitry, and Peak Detector circuitry.	00h	Page 33
35h	R-C	High Limit Status	Status bits for the High Limits	00h	Page 41
36h	R-C	Low Limit Status	Status bits for the Low Limits	00h	Page 42

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
37h	R-C	Crit Limit Status	Status bits for the Tcrit and Vcrit Limits	00h	Page 42
38h	R	Internal Diode High Byte	Stores the integer data for the Internal Diode	00h	Page 32
39h	R	Internal Diode Low Byte	Stores the fractional data for the Internal Diode	00h	Page 32
3Ah	R	External Diode 1 High Byte	Stores the integer data for External Diode 1	00h	Page 32
3Bh	R	External Diode 1 Low Byte	Stores the fractional data for External Diode 1	00h	Page 32
40h	R/W	Averaging Control	Controls the digital averaging setting for the all external diode channels	00h	Page 43
Current Sense Control and Measurement					
50h	R/W	Voltage Sampling Configuration	Controls voltage sampling	80h	Page 43
51h	R/W	Current Sense Sampling Configuration	Controls the current sensing sampling and update times	03h	Page 44
52h	R/W	Peak Detection Config	Controls the peak detection configuration	00h	Page 46
54h	R	Sense Voltage High Byte	Stores the voltage measured across R_{SENSE}	00h	Page 48
55h	R	Sense Voltage Low Byte		00h	Page 48
58h	R	Source Voltage High Byte	Stores voltage measured on the source side of R_{SENSE}	00h	Page 49
59h	R	Source Voltage Low Byte		00h	Page 49
5Bh	R	Power Ratio High Byte	Stores the power ratio value	00h	Page 49
5Ch	R	Power Ratio Low Byte		00h	Page 49
Current Sense and Source Voltage Limits					
60h	R/W	Sense Voltage High Limit	Stores the high limit for V_{SENSE}	7Fh	Page 50
61h	R/W	Sense Voltage Low Limit	Stores the low or negative limit for the V_{SENSE} voltage	80h	Page 50
64h	R/W	Source Voltage High Limit	Stores the high limit for the voltage on the source side of R_{SENSE}	FFh	Page 50
65h	R/W	Source Voltage Low Limit	Stores the low limit for the voltage on the source side of R_{SENSE}	00h	Page 50

Table 5.1 Register Set in Hexadecimal Order (continued)

REGISTER ADDRESS	R/W	REGISTER NAME	FUNCTION	DEFAULT VALUE	PAGE
66h	R/W	Sense Voltage Vcrit Limit	Stores the critical limit for V_{SENSE}	7Fh	Page 50
68h	R/W	Source Voltage Vcrit Limit	Stores the critical limit for the voltage on the source side of R_{SENSE}	FFh	Page 50
69h	R/W	Sense Vcrit Hysteresis	Stores the hysteresis for the V_{SENSE} Vcrit limit	0Ah	Page 50
6Ah	R/W	Source Voltage Vcrit Hysteresis	Stores the hysteresis for the source voltage Vcrit limits	0Ah	Page 50
FCh	R	Product Features	Stores information about which pin controlled product features are set	00h	Page 51
FDh	R	Product ID	Stores a fixed value that identifies each product	39h	Page 51
FEh	R	SMSC ID	Stores a fixed value that represents SMSC	5Dh	Page 52
FFh	R	Revision	Stores a fixed value that represents the revision number	82h	Page 52

5.1 Data Read Interlock

When any measurement channel high byte register is read (temperature or V_{SOURCE} or V_{SENSE}), the corresponding low byte is copied into an internal 'shadow' register. The user is free to read the low byte at any time and be guaranteed that it will correspond to the previously read high byte. Regardless if the low byte is read or not, reading from the same high byte register again will automatically refresh this stored low byte data.

5.2 Block Mode Support

All of the status and temperature data may be retrieved with a block read of 8 bytes starting at register address 34h.

All of the voltage measurement, current sense data, and power information may be retrieved with a block read of 6 bytes starting at register address 54h.

5.3 Temperature Data Registers

Table 5.2 Temperature Data Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
00h	R	Internal Diode High Byte	Sign	64	32	16	8	4	2	1	00h
38h											
29h	R	Internal Diode Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
39h											

Table 5.2 Temperature Data Registers (continued)

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
01h	R	External Diode 1 High Byte	Sign	64	32	16	8	4	2	1	00h
3Ah											
10h	R	External Diode 1 Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
3Bh											

As shown in Table 5.2, temperature data is stored as an 11-bit value with the high byte representing the integer value and the low byte representing the fractional value left justified to occupy the MSBits.

Table 5.3 Temperature Data Format

TEMPERATURE (°C)	BINARY	HEX (AS READ BY REGISTERS)
Diode Fault	1000_0000_000b	80_00h
-63.875	1100_0000_001b	C0_20h
-63	1100_0001_000b	C1_00h
-1	1111_1111_000b	FF_00h
-0.125	1111_1111_111b	FF_E0h
0	0000_0000_000b	00_00h
0.125	0000_0000_001b	00_20h
1	0000_0001_000b	01_00h
63	0011_1111_000b	3F_00h
64	0100_0000_000b	40_00h
65	0100_0001_000b	41_00h
127	0111_1111_000b	7F_00h
127.875	0111_1111_111b	7F_E0h

5.4 Status Register

Table 5.4 Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
02h	R	Status	BUSY	PEAK	-	HIGH	LOW	FAULT	CRIT	-	00h
34h											

The Status Register reports general error conditions. To identify specific channels, refer to Section 5.10, Section 5.15, Section 5.16, and Section 5.17. The individual Status Register bits are cleared when the appropriate High Limit, Low Limit, or Crit Limit status register has been read or cleared.

Bit 7 - BUSY - This bit indicates that one of the ADCs is currently converting. This bit does not cause either the $\overline{\text{ALERT}}$ or $\overline{\text{THERM}}$ pins to be asserted.

Bit 6 - PEAK - This bit is set when the Peak Detector circuitry has detected a current peak that is greater than the programmed threshold for longer than the programmed duration. This bit is not sticky and will be cleared when the condition has been removed. When set, the $\overline{\text{THERM}}$ pin or $\overline{\text{ALERT}}$ pin (Comparator mode only) may be asserted (see Section 5.19).

Bit 4 - HIGH - This bit is set when any of the temperature channels meets or exceeds its programmed high limit. This bit will also be set if the V_{SENSE} or V_{SOURCE} channels meet or exceed their respective high limits. See the High Limit Status Register for specific channel information (Section 5.15). When set, the $\overline{\text{ALERT}}$ pin is asserted.

Bit 3 - LOW - This bit is set when any of the temperature channels drops below its programmed low limit. This bit will also be set if the V_{SENSE} or V_{SOURCE} channels drop below their respective low limits. See the Low Limit Status Register for specific channel information (Section 5.16). When set, the $\overline{\text{ALERT}}$ pin is asserted.

Bit 2 - FAULT - This bit is set when a diode fault is detected on any of the external diode channels. See the External Diode Fault Register for specific channel information (Section 5.10). When set, the $\overline{\text{ALERT}}$ pin is asserted.

Bit 1 - CRIT - This bit is set when any of the temperature channels meets or exceeds its programmed Tcrit limit. This bit will also be set if the V_{SENSE} or V_{SOURCE} channels meet or exceed their respective Vcrit limits (see the Section 5.17, "Crit Limit Status Register" for specific channel information). When set, the $\overline{\text{THERM}}$ pin is asserted. This bit is not sticky and will be cleared when the error condition has been removed.

5.5 Configuration Register

Table 5.5 Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
03h	R/W	Configuration	MASK_ ALL	TMEAS /STOP	ALERT/ COMP	DIS_ REC1	-	IMEAS /STOP	DAVG_ DIS	-	00h
09h											

The Configuration Register controls the basic operation of the device. This register is fully accessible at either address.

Bit 7 - MASK_ALL - Masks the $\overline{\text{ALERT}}$ pin from asserting.

- '0' (default) - The $\overline{\text{ALERT}}$ pin is not masked. If any of the appropriate status bits are set, the $\overline{\text{ALERT}}$ pin will be asserted.
- '1' - The $\overline{\text{ALERT}}$ pin is masked if configured in Interrupt mode (see Section 4.4.1, "ALERT Pin Interrupt Mode"). The Status Registers will be updated normally.

Bit 6 - TMEAS / STOP - Controls Temperature measurement modes.

- '0' (default) - The device is active, measuring all of the temperature channels.
- '1' - The device is not measuring temperature channels. It will update all of the temperature channels when a One-Shot command is given.

Bit 5 - ALERT/COMP - Controls the operation of the $\overline{\text{ALERT}}$ pin.

- '0' (default) - The $\overline{\text{ALERT}}$ pin acts in Interrupt mode as described in Section 4.4.1.
- '1' - The $\overline{\text{ALERT}}$ pin acts in Comparator mode as described in Section 4.4.2. In this mode the MASK_ALL bit is ignored.

Bit 4 - DIS_REC1- Disables the Resistance Error Correction (REC) for External Diode 1.

- '0' (default) - REC is enabled for External Diode 1.
- '1' - REC is disabled for External Diode 1.

Bit 2 - IMEAS / STOP - Controls V_{SENSE} and V_{SOURCE} measurement modes.

- '0' (default) - The device is measuring source voltage and sense voltage.
- '1' -The device is not measuring the source voltage and sense voltage. It will update V_{SENSE} and V_{SOURCE} registers when a One-Shot command is given.

Bit 1 - DAVG_DIS - Disables the dynamic averaging feature on all temperature channels.

- '0' (default) - The dynamic averaging feature is enabled. All temperature channels will be converted with an averaging factor that is based on the conversion rate as shown in Table 4.3.
- '1' - The dynamic averaging feature is disabled. All temperature channels will be converted with a maximum averaging factor of 1x (equivalent to 11-bit conversion).

5.6 Conversion Rate Register

Table 5.6 Conversion Rate Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
04h	R/W	Conversion Rate	-	-	-	-		T_CONV[2:0]			06h (4/sec)
0Ah											

The Conversion Rate Register controls how often the V_{SOURCE} and temperature measurement channels are updated and compared against the limits. This register is fully accessible at either address.

Bits 2-0 - T_CONV[2:0] - Determines the conversion rate as shown in Table 5.7. This conversion rate applies to temperature measurement and source voltage measurement.

Table 5.7 Conversion Rate

T_CONV[2:0]			CONVERSION RATE
2	1	0	
0	0	0	1 per 16 sec
0	0	1	1 per 8 sec
0	1	0	1 per 4 sec
0	1	1	1 per 2 sec
1	0	0	1 per sec
1	0	1	2 per sec
1	1	0	4 per sec (default)
1	1	1	8 per sec

5.7 Temperature Limit Registers

Table 5.8 Temperature Limit Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
05h 0Bh	R/W	Internal Diode High Limit	Sign	64	32	16	8	4	2	1	55h (85°C)
06h 0Ch	R/W	Internal Diode Low Limit	Sign	64	32	16	8	4	2	1	80h (-128°C)
07h 0Dh	R/W	External Diode 1 High Limit High Byte	Sign	64	32	16	8	4	2	1	55h (85°C)
13h	R/W	External Diode 1 High Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h
08h 0Eh	R/W	External Diode 1 Low Limit High Byte	Sign	64	32	16	8	4	2	1	80h (-128°C)
14h	R/W	External Diode 1 Low Limit Low Byte	0.5	0.25	0.125	-	-	-	-	-	00h

The device contains both high and low limits for the temperature channels. If the measured temperature meets or exceeds the high limit, the corresponding status bit is set, and the $\overline{\text{ALERT}}$ pin is asserted. Likewise, if the measured temperature is less than or equal to the low limit, the corresponding status bit is set and the $\overline{\text{ALERT}}$ pin is asserted.

The limit registers with multiple addresses are fully accessible at either address.

When the device is Standby or Current Sense only mode, updating the limit registers will have no effect until the next conversion cycle occurs. This conversion cycle can be initiated via a write to the One-Shot Register or by clearing the TMEAS_STOP bit in the Configuration Register (see Section 5.5).

5.8 One-Shot Register

Table 5.9 One-Shot Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
0Fh	W	One-Shot	Writing to this register initiates a single conversion cycle. Data is not stored and always reads 00h								00h

Writing to the One-Shot register will automatically update those channels that are not currently measured. If the device is Fully Active, writing to this register will have no effect. If the IMEAS_STOP bit is set, writing to this register will update the V_{SENSE} and V_{SOURCE} voltage measurements. If the TMEAS_STOP bit is set, writing to this register will update all of the temperature channel measurements.

5.9 Tcrit Limit Registers

Table 5.10 Tcrit Limit Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
19h	R/W	External Diode 1 Tcrit Limit	Sign	64	32	16	8	4	2	1	64h (100°C)
20h	R/W	Internal Diode Tcrit Limit	Sign	64	32	16	8	4	2	1	64h (100°C)
21h	R/W	Tcrit Hysteresis	-	64	32	16	8	4	2	1	0Ah (10°C)

The Tcrit Limit Registers are used to determine whether a critical thermal event has occurred. If the measured temperature meets or exceeds the Tcrit Limit, the $\overline{\text{THERM}}$ pin is asserted.

Unlike the $\overline{\text{ALERT}}$ pin, the $\overline{\text{THERM}}$ pin cannot be masked. Additionally, the $\overline{\text{THERM}}$ pin will be released once the temperature drops below the corresponding threshold minus the Tcrit Hysteresis.

5.10 External Diode Fault Register

Table 5.11 External Diode Fault Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Bh	R-C	External Diode Fault	-	-	-	-	-	-	E1FLT	-	00h

The External Diode Fault Register indicates that External Diode 1 caused the FAULT bit in the Status Register to be set. This register is cleared when it is read.

Bit 1 - E1FLT - This bit is set if the External Diode 1 channel reported a diode fault.

5.11 Channel Mask Register

Table 5.12 Channel Mask Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
1Fh	R/W	Channel Mask	VSENSE_ MASK	VSRC_ MASK	PEAK_ MASK	-	-	-	E1 MASK	INT MASK	00h

The Channel Mask Register controls individual channel masking. When a channel is masked, the $\overline{\text{ALERT}}$ pin will not be asserted when the masked channel reads a diode fault or out-of-limit error. The channel mask does not mask the $\overline{\text{THERM}}$ pin.

Bit 7 - VSENSE_MASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the V_{SENSE} value meets or exceeds the high limit or drops below the low limit. This bit will have no effect on the $\overline{\text{THERM}}$ pin functionality.

- '0' (default) - The V_{SENSE} voltage channel will cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
- '1' - The V_{SENSE} voltage channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).

Bit 6 - VSRC_MASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the V_{SOURCE} value meets or exceeds the high limit or drops below the low limit. This bit will have no effect on the $\overline{\text{THERM}}$ pin functionality.

- '0' (default) - The V_{SOURCE} voltage channel will cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
- '1' - The V_{SOURCE} voltage channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).

BIt 5 - PEAK_MASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the Peak Detector circuitry detects a current spike. This bit will have no effect on the $\overline{\text{THERM}}$ pin functionality.

- '0' (default) - The Peak Detector circuitry will cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).
- '1' - The Peak Detector circuitry will not cause the $\overline{\text{ALERT}}$ pin to be asserted (if enabled).

Bit 1 - E1MASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the External Diode 1 channel is out-of-limit or reports a diode fault.

- '0' (default) - The External Diode 1 channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault.
- '1' - The External Diode 1 channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit or reports a diode fault.

Bit 0 - INTMASK - Masks the $\overline{\text{ALERT}}$ pin from asserting when the Internal Diode temperature is out-of-limit.

- '0' (default) - The Internal Diode channel will cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit.
- '1' - The Internal Diode channel will not cause the $\overline{\text{ALERT}}$ pin to be asserted if it is out-of-limit.

5.12 Consecutive Alert Register

Table 5.13 Consecutive Alert Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
22h	R/W	Consecutive Alert	TIME OUT	CTHRM[2:0]			CALRT[2:0]			-	70h

The Consecutive Alert Register determines how many times an out-of-limit error or diode fault must be detected in consecutive measurements before the interrupt status registers are asserted. This applies to temperature limits only. The voltage measurement and current sense measurements are controlled via the Voltage Channel Configuration register and Current Sense Configuration register respectively (see Section 5.19 and Section 5.20).

When the $\overline{\text{ALERT}}$ pin is configured as a comparator, the consecutive alert counter will ignore diode fault and low limit errors and only increment if the measured temperature meets or exceeds the High Limit.

Each measurement channel has a separate fault queue associated with the high limit, low limit, and diode fault condition except the internal diode.

Bit 7 - TIMEOUT - Determines whether the SMBus Timeout function is enabled.

- '0' (default) - The SMBus Timeout feature is disabled. The SMCLK line can be held low indefinitely without the device resetting its SMBus protocol.
- '1' - The SMBus Timeout feature is enabled. If the SMCLK line is held low for more than 30ms, the device will reset the SMBus protocol.

Bits 6-4 - CTHRM[2:0] - Determines the number of consecutive measurements that must exceed the corresponding Tcrit Limit before the $\overline{\text{THERM}}$ pin is asserted.

Bits 3-1 - CALRT[2:0] - Determines the number of consecutive measurements that must have an out-of-limit condition or diode fault before the $\overline{\text{ALERT}}$ pin is asserted. All temperature channels use this value to set the respective counters. The bits are decoded as shown in Table 5.14. The default setting is 1 consecutive out-of-limit conversion.

Table 5.14 Consecutive $\overline{\text{ALERT}}$ / $\overline{\text{THERM}}$ Settings

2	1	0	NUMBER OF CONSECUTIVE OUT-OF-LIMIT MEASUREMENTS
0	0	0	1 (default for CALRT[2:0])
0	0	1	2
0	1	1	3
1	1	1	4 (default for CTHRM[2:0])

5.13 Beta Configuration Registers

Table 5.15 Beta Configuration Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
25h	R/W	External Diode 1 Beta Configuration	-	-	-	AUTO1	BETA1[3:0]				10h

This register is used to set the Beta Compensation factor that is used for the external diode channels.

Bit 4 - AUTO - Enables the Beta Compensation factor autodetection function.

- '0' - The Beta Compensation Factor autodetection circuitry is disabled. The External Diode will always use the Beta Compensation factor set by the BETAx[3:0] bits.
- '1' (default) - The Beta Compensation factor autodetection circuitry is enabled. At the beginning of every conversion, the optimal Beta Compensation factor setting will be determined and applied. The BETAx[3:0] bits will be automatically updated to indicate the current setting.

Bit 3-0 - BETA[3:0] - These bits always reflect the current beta configuration settings. If autodetection circuitry is enabled, these bits will be updated automatically and writing to these bits will have no effect. If the autodetection circuitry is disabled, these bits will determine the beta configuration setting that is used for their respective channels.

Care should be taken when setting the BETA1[3:0] bits when the autodetection circuitry is disabled. If the Beta Compensation factor is set at a beta value that is higher than the transistor beta, the circuit may introduce measurement errors. When measuring a discrete thermal diode (such as 2N3904) or a CPU diode that functions like a discrete thermal diode (such as an AMD processor diode), the BETA1[3:0] bits should be set to '1111b'.

Table 5.16 Beta Compensation

AUTO	BETA1[3:0]				MINIMUM BETA
	3	2	1	0	
0	0	0	0	0	0.050
0	0	0	0	1	0.066
0	0	0	1	0	0.087
0	0	0	1	1	0.114
0	0	1	0	0	0.150
0	0	1	0	1	0.197
0	0	1	1	0	0.260
0	0	1	1	1	0.342
0	1	0	0	0	0.449
0	1	0	0	1	0.591
0	1	0	1	0	0.778
0	1	0	1	1	1.024
0	1	1	0	0	1.348
0	1	1	0	1	1.773
0	1	1	1	0	2.333
0	1	1	1	1	Disabled
1	X	X	X	X	Automatically detected

5.14 External Diode Ideality Factor Registers

Table 5.17 Ideality Configuration Registers

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
27h	R/W	External Diode 1 Ideality Factor	-	-	0	1	0	IDCF1[2:0]			12h

These registers store the ideality factors that are applied to the external diodes. Table 5.18 defines each setting and the corresponding ideality factor. Beta Compensation and Resistance Error Correction automatically correct for most diode ideality errors; therefore, it is not recommended that these settings be updated without consulting SMSC.

Table 5.18 Ideality Factor Look-Up Table (Diode Model)

SETTING	FACTOR
10h	1.0053
11h	1.0066
12h	1.0080
13h	1.0093
14h	1.0106
15h	1.0119
16h	1.0133
17h	1.0146

APPLICATION NOTE: When measuring a 65nm Intel CPUs, the Ideality Setting should be the default 12h. When measuring 45nm Intel CPUs, the Ideality Setting should be 15h.

5.15 High Limit Status Register

Table 5.19 High Limit Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
35h	R-C	High Limit Status	VSENSE_ HIGH	VSRC_ HIGH	-	-	-	-	E1 HIGH	I HIGH	00h

The High Limit Status Register contains the status bits that are set when a temperature or voltage channel high limit is met or exceeded. If any of these bits are set, the HIGH status bit in the Status Register is set. Reading from the High Limit Status Register will clear all bits if the error condition has been removed. Reading from the register will also clear the HIGH status bit in the Status Register if the error condition has been removed.

If not masked, the $\overline{\text{ALERT}}$ pin will be set if the programmed number of consecutive alert counts have been met and any of these status bits are set. Once set, the status bits will remain set until read unless the $\overline{\text{ALERT}}$ pin is configured as a comparator output (see Section 4.4.2).

Bit 7 - VSENSE_HIGH - This bit is set when the V_{SENSE} value meets or exceeds its programmed high limit.

Bit 6 - VSRC_HIGH - This bit is set when the V_{SOURCE} value meets or exceeds its programmed high limit.

Bit 1 - E1HIGH - This bit is set when the External Diode 1 channel meets or exceeds its programmed high limit.

Bit 0 - IHIGH - This bit is set when the Internal Diode channel meets or exceeds its programmed high limit.

5.16 Low Limit Status Register

Table 5.20 Low Limit Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
36h	R-C	Low Limit Status	VSENSE_ LOW	VSRC_ LOW	-	-	-	-	E1 LOW	ILOW	00h

The Low Limit Status Register contains the status bits that are set when a temperature or voltage channel drops below the low limit. If any of these bits are set, the LOW status bit in the Status Register is set. Reading from the Low Limit Status Register will clear all bits. Reading from the register will also clear the LOW status bit in the Status Register if the error status has been removed.

If not masked, the $\overline{\text{ALERT}}$ pin will be set if the programmed number of consecutive alert counts have been met and any of these status bits are set.

Once set, the status bits will remain set until read.

Bit 7 - VSENSE_LOW - This bit is set when the V_{SENSE} value drops below its programmed low limit.

Bit 6 - VSRC_LOW - This bit is set when the V_{SOURCE} value drops below its programmed low limit.

Bit 1 - E1LOW - This bit is set when the External Diode 1 channel drops below its programmed low limit.

Bit 0 - ILOW - This bit is set when the Internal Diode channel drops below its programmed low limit.

5.17 Crit Limit Status Register

Table 5.21 Crit Limit Status Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
37h	R-C	Crit Limit Status	VSENSE_ VCRIT	VSRC_ VCRIT	-	-	-	-	E1 TCRIT	ITCRIT	00h

The Crit Limit Status register contains the status bits that are set when a temperature or voltage channel Tcrit or Vcrit Limit is met or exceeded (see Section 5.9 and Section 5.27). If any of these bits are set, the CRIT status bit in the Status register is set. Reading from the Crit Limit Status register will not clear the status bits. Once the temperature drops below the Tcrit Limit minus the Tcrit Hysteresis, the corresponding status bits will be automatically cleared. Once the voltage drops below the Vcrit Limit minus the Vcrit Hysteresis, the corresponding status bits will be automatically cleared. The CRIT bit in the Status register will be cleared when all individual bits are cleared.

Bit 7 - VSENSE_VCRIT - This bit is set when the V_{SENSE} value meets or exceeds its programmed Vcrit limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

Bit 6 - VSRC_VCRIT- This bit is set when the V_{SOURCE} value meets or exceeds its programmed Vcrit limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

Bit 1 - E1TCRIT - This bit is set when the External Diode 1 channel meets or exceeds its programmed Tcrit limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

Bit 0 - ITCRIT - This bit is set when the Internal Diode channel meets or exceeds its programmed Tcrit limit. When set, this bit will assert the $\overline{\text{THERM}}$ pin.

5.18 Averaging Control Register

Table 5.22 Filter Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
40h	R/W	Filter Control	-	-	-	-	-	-	AVG1[1:0]		00h

The Averaging Control Register controls the digital averaging on the external diode channels.

Bits 1-0 - AVG1[1:0] - Controls the digital averaging that is applied to the External Diode 1 temperature measurements as shown in Table 5.23.

Table 5.23 Averaging Settings

AVGX[1:0]		AVERAGING
1	0	
0	0	Disabled (default)
0	1	2x
1	0	4x
1	1	8x

5.19 Voltage Sampling Configuration Register

Table 5.24 Voltage Sampling Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
50h	R/W	Voltage Sampling Config	PK_ ALERT_ THERM	-	-	-	V_QUEUE[1:0]		V_AVG[1:0]		80h

The Voltage Sampling Configuration register controls functionality for the source voltage measurement and Peak Detector circuitry.

Bit 7 - PK_ALERT_THERM - Determines whether the $\overline{\text{ALERT}}$ pin or $\overline{\text{THERM}}$ pin is asserted if the Peak Detector detects a current spike. If configured to assert the $\overline{\text{ALERT}}$ pin, the PEAK_MASK can block the pin assertion normally. If configured to assert the $\overline{\text{THERM}}$ pin, it will not be masked.

- '0' - The Peak Detector circuitry will assert the $\overline{\text{ALERT}}$ pin when a current spike is detected. The $\overline{\text{ALERT}}$ pin must be configured to operate in Comparator mode or it will not be asserted.
- '1' (default) - The Peak Detector circuitry will assert the $\overline{\text{THERM}}$ pin when a current spike is detected.

Bits 3 - 2 - V_QUEUE[1:0] - Determine the number of consecutive measurements that V_{SOURCE} must exceed the limits before flagging an interrupt.

Table 5.25 Voltage Queue Settings

V_QUEUE[1:0]		NUMBER OF CONSECUTIVE OUT-OF-LIMIT MEASUREMENTS
1	0	
0	0	1 (default)
0	1	2
1	0	3
1	1	4

Bits 1-0 - V_AVG[1:0] - Controls the digital averaging that is applied to the source voltage measurement, as shown in Table 5.26.

Table 5.26 Voltage Averaging Settings

V_AVG[1:0]		AVERAGING
1	0	
0	0	Disabled (default)
0	1	2x
1	0	4x
1	1	8x

5.20 Current Sense Sampling Configuration Register

Table 5.27 Current Sense Sampling Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
51h	R/W	Current Sense Sampling Config	CS_QUEUE [1:0]		CS_SAMP_ AVG [1:0]		CS_SAMP_ TIME[1:0]		CS_RNG [1:0]		03h

The Current Sense Sampling Configuration register stores the controls for determining the Current Sense sampling / update time.

Bits 7 - 6 - CS_QUEUE[1:0] - Determine the number of consecutive measurements that the measured V_{SENSE} must exceed the limits before flagging an interrupt.

Table 5.28 Sense Queue Settings

CS_QUEUE[1:0]		NUMBER OF CONSECUTIVE OUT-OF-LIMIT MEASUREMENTS
1	0	
0	0	1 (default)

Table 5.28 Sense Queue Settings (continued)

CS_QUEUE[1:0]		NUMBER OF CONSECUTIVE OUT-OF-LIMIT MEASUREMENTS
1	**0**	
0	1	2
1	0	3
1	1	4

Bits 5 - 4 - CS_SAMP_AVG[1:0] - Determines the number of averages that the Current Sensing Circuitry will take as shown in Table 5.29.

Table 5.29 Current Sense Averaging Settings

CS_SAMP_AVG[1:0]		AVERAGING
1	**0**	
0	0	1x (default)
0	1	2x
1	0	4x
1	1	8x

Bits 3 - 2 - CS_SAMP_TIME[1:0] - Determines the sampling time of the Current Sensing Circuitry as shown in Table 5.30. The V_{SENSE} voltage will be updated at this rate representing the average current over the Sampling Time multiplied by the Averaging factor as shown in Table 5.31.

Table 5.30 Current Sensing Sampling Time Settings

CS_SAMP_TIME[1:0]		CURRENT SENSOR SAMPLING TIME
1	**0**	
0	0	82ms (default)
0	1	82ms
1	0	164ms
1	1	328ms

Table 5.31 Total Sampling Times

SAMPLING TIME	AVERAGING SELECTION			
	1X	2X	4X	8X
82ms	82ms	164ms	328ms	655ms
164ms	164ms	328ms	655ms	1310ms
328ms	328ms	655ms	1310ms	2620ms

Bits 1 - 0 - CS_RNG[1:0] - Determines the Current Sense maximum expected voltage (full scale range) as shown in Table 5.32.

Table 5.32 Current Sensing Range (Full Scale Range) Settings

CS_RNG[1:0]		CURRENT SENSOR RANGE
1	0	
0	0	10mV
0	1	20mV
1	0	40mV
1	1	80mV (default)

5.21 Peak Detection Configuration Register

Table 5.33 Peak Detection Configuration Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
52h	R/W	Peak Detection Config	PEAK_DET_TH[3:0]				PEAK_DET_DUR[3:0]				00h

The Peak Detection Configuration register controls the threshold and durations used by the Peak Detection circuitry. At all times, the Peak Detection threshold and duration are set by the values written into this register. The resistors on the TH_SEL and DUR_SEL pins are used to determine the initial values of this register and will not be retained if the value is over written by the user.

These values may be updated at any time via the SMBus.

Bits 7-4 - PEAK_DET_TH[3:0] - Determines the Peak Detector Threshold level as shown in Table 5.34.

Table 5.34 PEAK_DET_TH[3:0] Bit Decode

PEAK_DET_TH[3:0]				PEAK DETECTION THRESHOLD
3	**2**	**1**	**0**	
0	0	0	0	10mV
0	0	0	1	15mV
0	0	1	0	20mV
0	0	1	1	25mV
0	1	0	0	30mV
0	1	0	1	35mV
0	1	1	0	40mV
0	1	1	1	45mV
1	0	0	0	50mV
1	0	0	1	55mV
1	0	1	0	60mV
1	0	1	1	65mV
1	1	0	0	70mV
1	1	0	1	75mV
1	1	1	0	80mV
1	1	1	1	85mV

Bits 4-0 - PEAK_DET_DUR[3:0] - Determines the Peak Detector minimum time threshold as shown in Table 5.35.

Table 5.35 PEAK_DET_DUR[3:0] Bit Decode

PEAK_DET_DUR[3:0]				PEAK DETECTION MINIMUM DURATION
3	**2**	**1**	**0**	
0	0	0	0	1ms
0	0	0	1	5.12ms
0	0	1	0	25.6 ms
0	0	1	1	51.2 ms
0	1	0	0	76.8 ms
0	1	0	1	102.4ms
0	1	1	0	128.0ms
0	1	1	1	256.0ms

Table 5.35 PEAK_DET_DUR[3:0] Bit Decode (continued)

PEAK_DET_DUR[3:0]				PEAK DETECTION MINIMUM DURATION
3	2	1	0	
1	0	0	0	384.0ms
1	0	0	1	512.0ms
1	0	1	0	768.0ms
1	0	1	1	1024.0ms
1	1	0	0	1536.0ms
1	1	0	1	2048.0ms
1	1	1	0	3072.0ms
1	1	1	1	4096.0ms

5.22 Sense Voltage Registers

Table 5.36 Sense Voltage Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
54h	R	Sense Voltage High Byte	Sign	1024	512	256	128	64	32	16	00h
55h	R	Sense Voltage Low Byte	8	4	2	1					00h

The Sense Voltage registers store the measured V_{SENSE} voltage across the sense resistor (R_{SENSE}) placed between the SENSE+ and SENSE- pins (see Section 4.1.1, "Current Measurement"). Note that the bit weighting values are for representation of the voltage relative to full scale. There is no internal scaling of data and all normal binary bit weightings still apply.

The Sense Voltage register data format is standard 2's complement format with the positive full scale value (7F_Fh) and negative full scale value (80_0h) equal to the programmed maximum sense voltage (see Section 5.20, "Current Sense Sampling Configuration Register").

The Sign bit indicates the direction of current flow. If the Sign bit is '0', current is flowing through R_{SENSE} from the SENSE+ pin to the SENSE- pin. If the Sign bit is '1', the current is flowing through R_{SENSE} from the SENSE- pin to the SENSE+ pin. See Section 4.1.1, "Current Measurement" for examples.

Table 5.37 V_{SENSE} Data Format

V_{SENSE}	BINARY	HEX (AS READ BY REGISTERS)
Minus Full Scale	1000_0000_0000	80_0h
-2 LSB	1111_1111_1110	FF_Eh
-1 LSB	1111_1111_1111	FF_Fh
Zero	0000_0000_0000	00_0h

Table 5.37 V_{SENSE} Data Format (continued)

V_{SENSE}	BINARY	HEX (AS READ BY REGISTERS)
+1 LSB	0000_0000_0001	00_1h
+2 LSB	0000_0000_0010	00_2h
Plus Full Scale	0111_1111_1111	7F_Fh

5.23 Source Voltage Registers

Table 5.38 Source Voltage Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
58h	R	V_{SOURCE} High Byte	12	6	3	1.5	0.75	0.375	0.1875	0.0938	00h
59h	R	V_{SOURCE} low Byte	0.0469	0.0234	0.0117	-	-	-	-	-	00h

The Source Voltage registers store the voltage measured at the SENSE+ pin (see Section 4.1.2, "Voltage Measurement") as a digital value, V_{SOURCE}, consisting of a high byte and low byte with five of its LSBs always zero.

The measured voltage is determined by summing the bit weights of each bit set. For example, if V_{BUS} was 7.4V, the Source Voltage registers would read 0100_1110 for the high byte and 1100_0000b for the low byte corresponding to 6V + 0.75V + 0.375V + 0.1875V + 0.0469V + 0.0234V = 7.383V.

The bit weightings are assigned for human interpretation. They should be disregarded when translating the information via a computing system as shown in Section 4.1.2, "Voltage Measurement".

The Source Voltage registers cannot support negative values, and all values less than 0V will be recorded as 0V.

5.24 Power Ratio Registers

Table 5.39 Power Ratio Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
5Bh	R	Power Ratio High Byte	32768	16384	8192	4096	2048	1024	512	256	00h
5Ch	R	Power Ratio Low Byte	128	64	32	16	8	4	2	1	00h

The Power Ratio registers store a power factor value that is used to determine the final average power delivered to the system (see Section 4.1.3, "Power Calculation"). The power factor value is the result of the multiplication of the V_{SENSE} reading and the V_{SOURCE} reading values shifted to a 16-bit number. It represents the ratio of delivered power with respect to maximum power.

5.25 V_{SENSE} Limit Registers

Table 5.40 V_{SENSE} Limit Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
60h	R/W	Sense Voltage High Limit	Sign	1024	512	256	128	64	32	16	7Fh
61h	R/W	Sense Voltage Low Limit	Sign	1024	512	256	128	64	32	16	80h

The V_{SENSE} Limit registers store a high and low limit for V_{SENSE}. V_{SENSE} is compared against both limits after each update.

The data format for the limit is a raw binary form that is relative to the maximum V_{SENSE} that has been programmed.

If the measured sense voltage meets or exceeds the high limit or drops below the low limit, the $\overline{ALERT}$ pin is asserted and the VSENSE_HIGH or VSENSE_LOW status bits are set in the High Limit Status or Low Limit Status registers (see Section 5.15 and Section 5.16).

APPLICATION NOTE: V_{SENSE} is always checked to be greater than the high limit or less than the low limit including when V_{SENSE} is negative.

5.26 Source Voltage Limit Registers

Table 5.41 Source Voltage Limit Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
64h	R/W	Source Voltage High Limit	12	6	3	1.5	0.75	0.375	0.1875	0.0938	FFh
65h	R/W	Source Voltage Low Limit	12	6	3	1.5	0.75	0.375	0.1875	0.0938	00h

The Source Voltage Limit registers store the high and low limits for V_{SOURCE}. V_{SOURCE} is compared against all limits after each update.

If V_{SOURCE} meets or exceeds the corresponding high limit or drops below the low limit, the $\overline{ALERT}$ pin is asserted and the VSRC_HIGH or VSRC_LOW status bits are set in the High Limit Status or Low Limit Status registers (see Section 5.15 and Section 5.16).

5.27 Critical Voltage Limit Registers

Table 5.42 Critical Voltage Limit Registers

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
66h	R/W	Sense Voltage Vcrit Limit	Sign	1024	512	256	128	64	32	16	7Fh

Table 5.42 Critical Voltage Limit Registers (continued)

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
68h	R/W	Source Voltage Vcrit Limit	12	6	3	1.5	0.75	0.375	0.1875	0.0938	FFh
69h	R/W	Sense Voltage Vcrit Hysteresis	-	-	-	256	128	64	32	16	0Ah
6Ah	R/W	Source Voltage Vcrit Hysteresis	-	-	-	1.5	0.75	0.375	0.1875	0.0938	0Ah

The Critical Voltage Limit registers store the critical voltage limits (Vcrit limits) for V_{SENSE} and V_{SOURCE}.

If the respective value meets or exceeds its critical limit, the $\overline{\text{THERM}}$ pin will be asserted low and the respective VCRIT status bit will be set (see Section 5.17, "Crit Limit Status Register"). It will remain asserted until the respective value drops below its limit minus the respective Vcrit Hysteresis value.

5.28 Product Features Register

Table 5.43 Product Features

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FCh	R	Product Features	TH_SEL[3:0]				DUR_SEL[3:0]				00h

The Product Features register indicates functionality that is selected by the user based on pin states upon device power up.

Bits 7-4 - TH_SEL[3:0] - Indicates the selected Peak Detector Threshold setting as determined by the TH_SEL pin. This value will be the default setting for the PEAK_DET_TH[3:0] bits and uses the same decode as given in Table 5.34.

Bits 3-0 - DUR_SEL[3:0] - Indicates the selected Peak Detector minimum duration setting as determined by the DUR_SEL pin. This value will be the default setting for the PEAK_DET_DUR[3:0] bits and uses the same decode as given in Table 5.35.

5.29 Product ID Register

Table 5.44 Product ID Register

ADDR	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FDh	R	Product ID	0	0	1	1	1	0	0	1	39h

The Product ID Register holds a unique value that identifies the device.

5.30 SMSC ID Register

Table 5.45 Manufacturer ID Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FEh	R	SMSC ID	0	1	0	1	1	1	0	1	5Dh

The Manufacturer ID register contains an 8-bit word that identifies SMSC as the manufacturer of the EMC1702.

5.31 Revision Register

Table 5.46 Revision Register

ADDR.	R/W	REGISTER	B7	B6	B5	B4	B3	B2	B1	B0	DEFAULT
FFh	R	Revision	1	0	0	0	0	0	1	0	82h

The Revision register contains an 8-bit word that identifies the die revision.

Chapter 6 Package Description

6.1 EMC1702 Package Drawing (12-Pin QFN 4mm x 4mm)

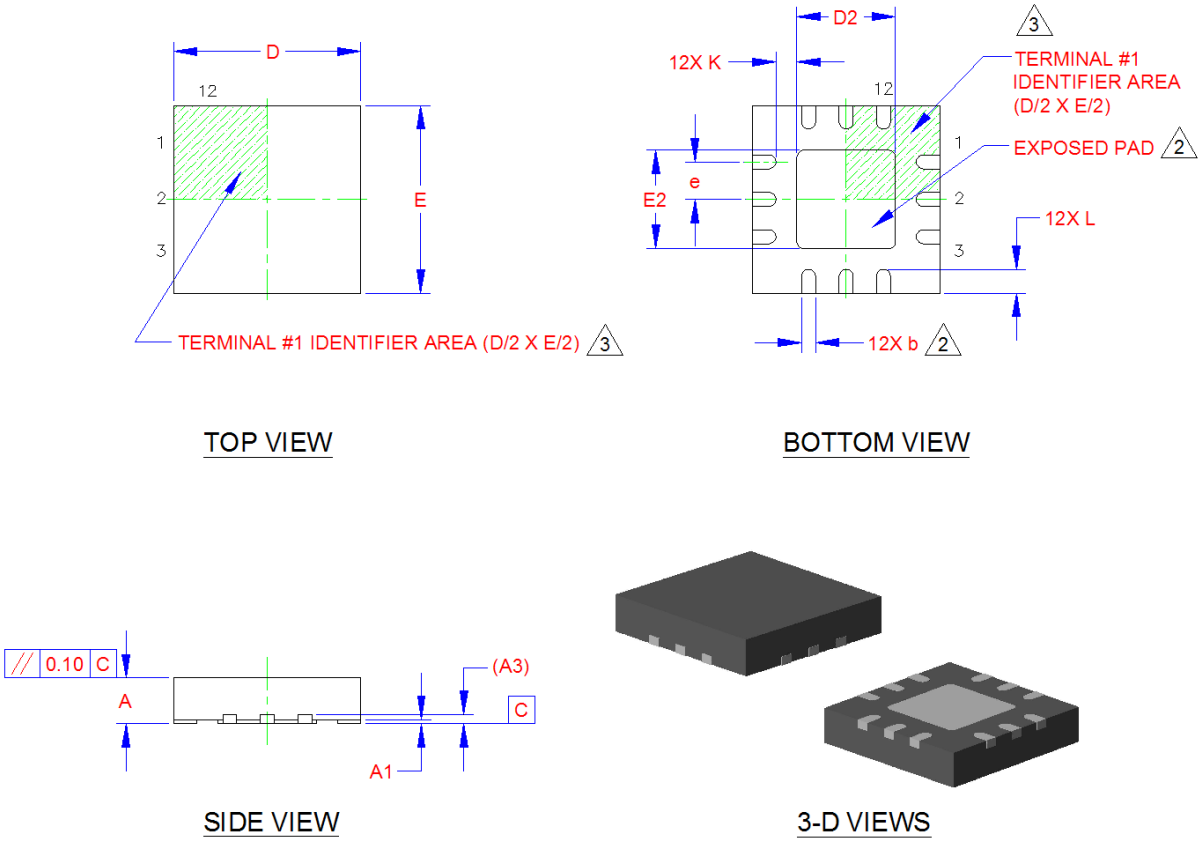
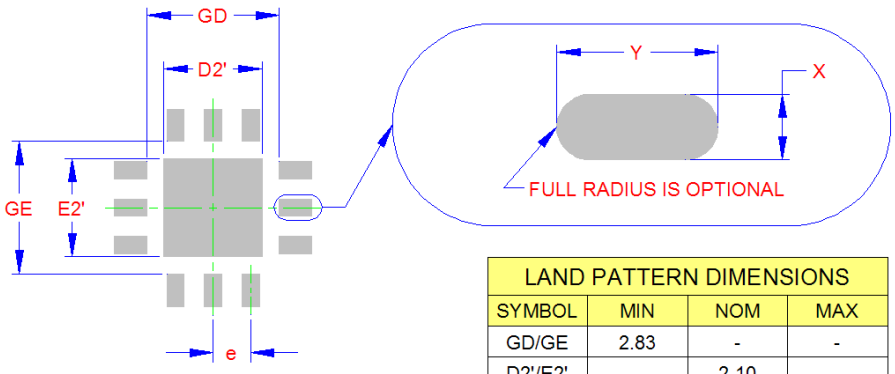


Figure 6.1 12-Pin QFN 4mm x 4mm Package Drawings

COMMON DIMENSIONS					
SYMBOL	MIN	NOM	MAX	NOTE	REMARK
A	0.80	0.85	0.90	-	OVERALL PACKAGE HEIGHT
A1	0	0.02	0.05	-	STANDOFF
A3		0.20 REF		-	LEAD-FRAME THICKNESS
D/E	3.90	4.00	4.10	-	X/Y BODY SIZE
D2/E2	2.00	2.10	2.20	2	X/Y EXPOSED PAD SIZE
L	0.45	0.50	0.55	-	TERMINAL LENGTH
b	0.25	0.30	0.35	2	TERMINAL WIDTH
K	0.20	-	-	-	TERMINAL TO PAD DISTANCE
e		0.80 BSC		-	TERMINAL PITCH

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. POSITION TOLERANCE OF EACH TERMINAL AND EXPOSED PAD IS ± 0.05mm AT MAXIMUM MATERIAL CONDITION. DIMENSIONS "b" APPLIES TO PLATED TERMINALS AND IT IS MEASURED BETWEEN 0.15 AND 0.30 mm FROM THE TERMINAL TIP.
3. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL BUT MUST BE LOCATED WITHIN THE AREA INDICATED.

Figure 6.2 12-Pin QFN 4mm x 4mm Package Dimensions and Notes



LAND PATTERN DIMENSIONS			
SYMBOL	MIN	NOM	MAX
GD/GE	2.83	-	-
D2'/E2'	-	2.10	-
X	-	-	0.37
Y	-	-	0.69
e		0.80	

RECOMMENDED PCB LAND PATTERN

Figure 6.3 12-Pin QFN 4mm x 4mm PCB Footprint

6.2 EMC1702 Package Markings

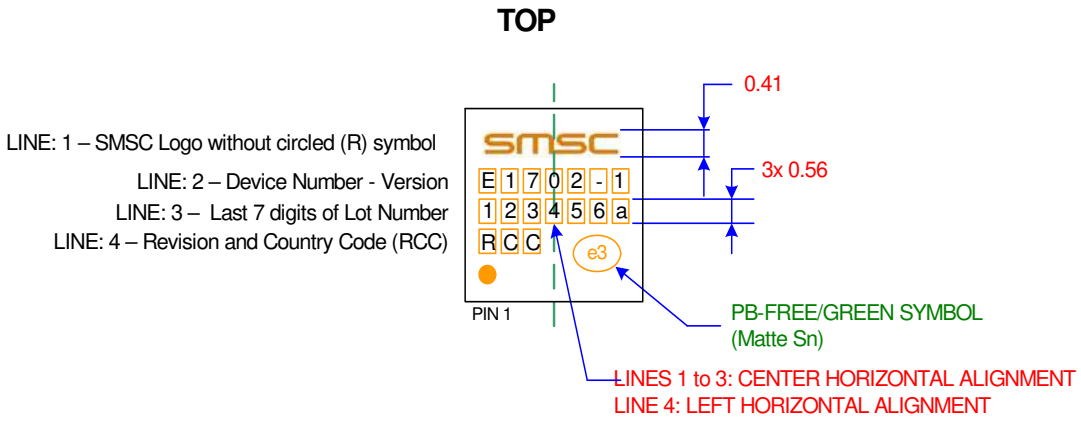


Figure 6.4 EMC1702 Package Markings

Chapter 7 Datasheet Revision History

Table 7.1 Customer Revision History

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
Rev. 1.2 (09-27-10)	Table 2.1, "Absolute Maximum Ratings"	Added spec for voltage between SENSE pins.
	Table 2.2, "Electrical Specifications"	Updated all electrical specs for current sense measurement, supply current, and peak detector.
	Electrical Specifications APPLICATION NOTE:	Added note: The EMC1702 is trimmed at the 80mV range for best accuracy.
	Section 5.13, "Beta Configuration Registers"	“BETAx[2:0] bits” changed to “BETAx[3:0] bits”.
Rev. 1.1 (06-16-10)	System Diagram	Updated.
	Section 5.15, "High Limit Status Register" and Section 5.16, "Low Limit Status Register"	ALERT# pin won’t be set if masked.
	Table 5.32, "Current Sensing Range (Full Scale Range) Settings"	Changed title from Current Sensing Range to Current Sensing Range (Full Scale Range) Settings.
	Table 2.2, "Electrical Specifications"	T_A upper limit changed from 125°C to 85°C. Bus voltage symbol changed from V_{SOURCE} to V_{BUS}. I_{DD} at 4 conversions/second with dynamic averaging enabled changed from 0.95 typ and 1.375 max to 0.9 typ and 1.3 max. I_{DD} at 4 conversions/second with dynamic averaging disabled changed from 0.80 typ to 0.8 typ. I_{DD} at 1 conversion/second with dynamic averaging disabled changed from 650 typ and 1 max to 0.7 typ and 1.0 max. V_{SENSE} Full Scale Sense Range values changed from 0 min and +/- max values to - min values and + max values; conditions changed. Total Unadjusted V_{SENSE} Measurement Error (V_{SENSE_TUE}) renamed V_{SENSE} Measurement Error (V_{SENSE_ERR}); typ value at 20-80mV FSR changed from 0.8 to +/-0.5 and max changed from +/-1.5 to +/-1; typ value at 10mV FSR changed from 0.2 to +/-0.8 and max changed from +/-2 to +/-1.5. V_{SENSE_OFF} condition added. V_{SENSE} Measurement Gain Error has new symbol V_{SENSE_GN}; added typ +/-0.2 and changed max from 0.5 to +/-0.5. V_{TH_ERR} changed from +/-20 to +/-2. V_{SOURCE_ERR} changed conditions; typ changed from 0.05 to +/-0.2 and max changed from 1 to +/-0.5. Added Power Ratio Measurement specs. Data hold time changed from 0.6 min and 6 max to 0 min and no max.
	Figure 4.1, "EMC1702 System Diagram"	Diagram modified

Table 7.1 Customer Revision History (continued)

REVISION LEVEL & DATE	SECTION/FIGURE/ENTRY	CORRECTION
	Section 5.31, "Revision Register"	Functional revision C changed default from 81h to 82h.
Rev. 1.0 (11-09-09)	Formal release	