TPS65381EVM User's Guide

The TPS65381EVM evaluation module (EVM) helps engineers evaluate the operation and performance of the TPS65381x-Q1 (TPS65381-Q1 or TPS65381A-Q1) multi-rail power supply for microcontrollers in safety relevant applications. This document describes how to setup and configure the EVM for operation. The document also includes the board layout, schematic, and bill of materials (BOM) for the EVM.

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Trademarks

PowerPAD is a trademark of Texas Instruments.

1 Introduction

The TPS65381EVM evaluation module (EVM) helps engineers evaluate the operation and performance of the TPS65381x-Q1 (TPS65381-Q1 or TPS65381A-Q1) multi-rail power supply for microcontrollers in safety relevant applications. The device is configurable through a serial peripheral interface (SPI) and specific input pins.

The EVM contains the TPS65381x-Q1 device and some circuitry for basic operation, see Figure 1 for the top board view of the EVM. It has a connection for an optional TIGER board (not included) to configure the TPS65381x-Q1 device through the SPI. It can also be used with a microcontroller (MCU) board or other 3rd party SPI tool connected to the TPS65381EVM SPI connections.

Table 1. Device and Package Configurations

VERSION	Multi-Rail Power Supply	IC	PACKAGE
001	IC1	TPS65381QDAPRQ1	DAP-32
002	IC1	TPS65381AQDAPRQ1	DAP-32

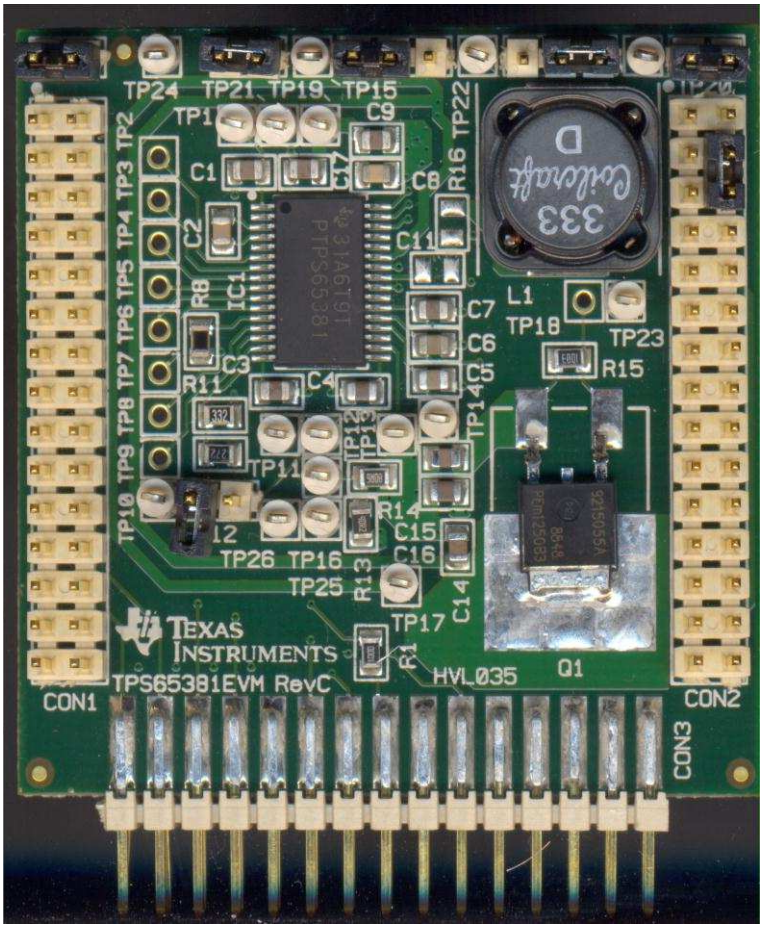


Figure 1. EVM Top Board View

2 TPS65381x-Q1 Description

The TPS65381x-Q1 device is a multi-rail power supply designed to supply microcontrollers (MCUs) in safety relevant applications, such as those found in automotive and industrial markets. The device supports Texas Instruments' Hercules™ TMS570 MCU and C2000™ families, and various other MCUs with dual-core lockstep (LS) or loosely-coupled architectures (LC).

The TPS65381x-Q1 device integrates multiple supply rails to power the MCU, Controller Area Network (CAN), or FlexRay, and an external sensor. An asynchronous buck switch mode power supply converter with an internal FET converts the input supply (battery) voltage to a 6-V preregulator output. This 6-V preregulator supplies the other regulators. The device supports wake-up from IGNITION or wake-up from the CAN transceiver.

The integrated fixed 5-V linear regulator with internal FET can be used for a CAN or FlexRay transceiver supply for example. A second linear regulator, also with an internal FET, regulates to a selectable 5-V or 3.3-V output which for example can be use for the MCU I/O voltage.

The TPS65381x-Q1 device includes an adjustable linear regulator controller, requiring an external FET and resistor divider, that regulates to an adjustable voltage of between 0.8 V and 3.3 V which may be used for the MCU core supply.

The integrated sensor supply can be run in tracking mode or adjustable output mode and includes short-to-ground and short-to-battery protection. Therefore, this regulator can power a sensor outside the module or electronic control unit (ECU).

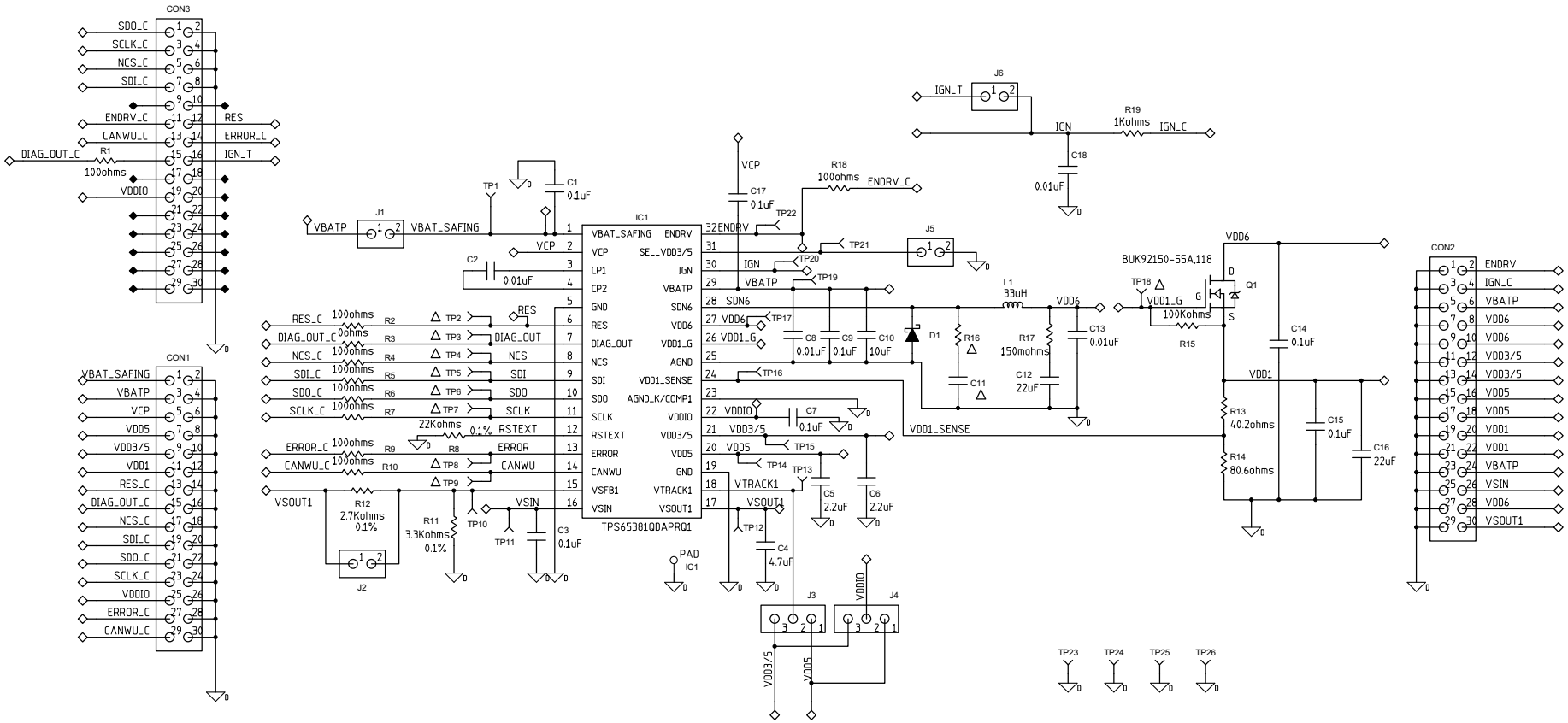
The integrated charge pump to provides overdrive voltage for the internal regulators. The charge pump may also be used in a reverse-battery protection circuit by using the charge-pump output to control an external NMOS transistor. This solution allows for a lower minimum-battery-voltage operation compared to a traditional reverse-battery blocking diode when the device must be operational at the lowest possible supply voltages.

The device monitors undervoltage and overvoltage on all regulator outputs, battery voltage, and internal supply rails. A second bandgap reference, independent from the main bandgap reference, is used for the undervoltage and overvoltage monitoring, to avoid any drifts in the main bandgap reference from being undetected. In addition, regulator current-limits and temperature protections are implemented.

The TPS65381x-Q1 has monitoring and protection functions, which include the following: watchdog with trigger and *question and answer* modes, MCU error-signal monitor, clock monitoring on internal oscillators, self-check on the clock monitor, cyclic redundancy check (CRC) on non-volatile memory, a diagnostic output pin allowing the MCU to observe internal analog and digital signals of the device, a reset circuit and output pin for the MCU, and an enable drive output to disable the safing-path or external-power stages on detected faults. A built-in self-test (BIST) monitors the device functionality automatically at power-up. A dedicated DIAGNOSTIC state allows the MCU to check TPS65381x-Q1 monitoring and protection functions.

3 Schematic, Bill of Materials, and Layout

3.1 Schematic



Version 001 shown for TPS65381-Q1. Version 002 is for TPS65381A-Q1.

R16 and C11 can be populated to bring the effective capacitance for VDD6 output higher. See datasheet for C_{VDD6} requirements in the parametric section and see the VDD6 Preregulator section on how to choose L, R and C to balance operation of VDD6.

Figure 2. TPS65381EVM Schematic

3.2 Bill of Materials

ITEM	QTY (001)	QTY (002)	MFG	MFG PART NO.	REF DES	DESCRIPTION	VALUE or FUNCTION
	REF	REF	-	-C	-	ASSEMBLY	-
	REF	REF	-	-C	-	SCHEMATIC	-
	1	1	-	-C	-	FABRICATION	-
	REF	REF	-	-C	-	ARTWORK	-
	1	1	Any	HLV035	PCB	Printed Circuit Board	SIZE 50.35 x 50 x 1.5 mm
1	0	0	UNINSTALLED	CAP_0805 (UN)	C11		UNINSTALLED CAP0805
2	4	4	SULLINS	PEC02SAAN	J1, J2, J5, J6		HEADER, THU, 1 x 2, 2.54 mm
3	2	2	SULLINS	PEC03SAAN	J3, J4		HEADER, THU, 1 x 3, 2.54 mm
4	3	3	SULLINS	PEC15DAAN	CON1, CON2, CON3		HEADER, THU, 2 x 15, 2.54 mm
5	0	0	UNINSTALLED	RES_0805 (UN)	R16		UNINSTALLED RES0805
6	3	3	AVX	08051C103JAT2A	C8, C13, C18	CAP, SMT, 0805	CAPACITOR, SMT, 0805, CERAMIC, 0.01 µF, 100 V, 5%, X7R
7	7	7	AVX	08055C104KAT2A	C1, C3, C7, C9, C14, C15, C17	CAP, SMT, 0805	CAPACITOR, SMT, 0805, CERAMIC, 0.1 µF, 50 V, 10%, X7R
8	1	1	KEMET	C0805C103K5RAC	C2	CAP, SMT, 0805	CAPACITOR, SMT, 0805, CER, 0.01 µF, 50 V, 10%, X7R
9	1	1	MURATA	GRM21BR60J226ME39L	C16	CAP, SMT, 0805	CAPACITOR, SMT, 0805, CERAMIC, 22 µF, 6.3 V, 20%, X5R
10	2	2	MURATA	GRM21BR71C225KA12L	C5, C6	CAP, SMT, 0805	CAPACITOR, SMT, 0805, CERAMIC, 2.2 µF, 16 V, 10%, X7R
11	1	1	MURATA	GRM21BR71C475KA73L	C4	CAP, SMT, 0805	CAPACITOR, SMT, 0805, CERAMIC, 4.7 µF, 16 V, 10%, X7R
12	1	1	MURATA	GRM31CR61C226ME15L	C12	CAP, SMT, 1206	CAPACITOR, SMT, 1206, CER, 22 µF,16 V, 20%, X5R
13	1	1	TDK	C3216X5R1H106K	C10	CAPACITOR, SMT1206	CAPACITOR, SMT, 1206, CERAMIC, 10 µF, 50 V, 10%, X5R
14	1	1	ON SEMI	MBRS340T3G	D1	DIODE, SMT, SMC-2	SCHOTTKY DIODE, SMT, 40 V, 3 A
15	1	1	PHILIPS	BUK92150-55A,118	Q1	DPAK, SOT428	N-CHANNEL TRENCHMOS DPAK
16	1	0	TI	TPS65381QDAPRQ1 or TPS65381AQDAPRQ1	IC1	IC, SMT, HTSSOP-32	DUT, SMT, HTSSOP, 32DAP, 0.65 mmLS, 11.1 x 8.3 x 1.2 mm, THERMAL PAD
17	1	1	COILCRAFT	MSS1246T-333ML	L1	INDUCTOR, SMT, 2P	INDUCTOR, SMT, 33 µH, 20%, 3.6 A, SHIELD
18	1	1	VISHAY	CRCW08050000Z	R3	RES, SMT, 0805	RESISTOR, SMT, 0805, THICK FILM, 1/8 W, 0 Ω

ITEM	QTY (001)	QTY (002)	MFG	MFG PART NO.	REF DES	DESCRIPTION	VALUE or FUNCTION
19	1	1	VISHAY	CRCW0805100KF	R15	RES, SMT, 0805	RESISTOR, SMT, 0805, THICK FILM, 1%, 1/8 W, 100K
20	9	9	VISHAY	CRCW0805100RF	R1, R2, R4, R5, R6, R7, R9, R10, R18	RES, SMT, 0805	RESISTOR, SMT, 0805, THICK FILM, 1%, 1/8 W, 100 Ω
21	1	1	VISHAY	CRCW08051K00F	R19	RES, SMT, 0805	RESISTOR, SMT, 0805, THICK FILM, 1%, 1/8 W, 1.00K
22	1	1	VISHAY	CRCW080540R2F	R13	RES, SMT, 0805	RESISTOR, SMT, 0805, THICK FILM, 1%, 1/8 W, 40.2 Ω
23	1	1	VISHAY	CRCW080580R6F	R14	RES, SMT, 0805	RESISTOR, SMT, 0805, THICK FILM, 1%, 1/8 W, 80.6 Ω
24	1	1	PANASONIC	ERJ-6RSJR15V	R17	RES, SMT, 0805	RESISTOR, SMT, 0805, 0.15 Ω, 5%, 1/8 W
25	1	1	PANASONIC	ERA-6YEB223V	R8	RES, SMT, 2P	RESISTOR, SMT, 0805, 22K, 0.1%, 1/10 W, 25 ppm
26	1	1	PANASONIC	ERA-6YEB272V	R12	RES, SMT, 2P	RESISTOR, SMT, 0805, 2.7K, 0.1%, 1/10 W, 25 ppm
27	1	1	PANASONIC	ERA-6YEB332V	R11	RES, SMT, 2P	RESISTOR, SMT, 0805, 3.3K, 0.1%, 1/10 W, 25 ppm
28	17	17	KEYSTONE	5002	TP1, TP10, TP11, TP12, TP13, TP14, TP15, TP16, TP17, TP19, TP20, TP21, TP22, TP23, TP24, TP25, TP26	TESTPOINT, THU, 1P	TESTPOINT, THU, MINIATURE, 0.1LS, 120TL, WHITE
29	0	0	KEYSTONE	5002 (UN)	TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP18	TESTPOINT, THU, 1P	UNINSTALLED TESTPOINT, THU, MINIATURE, 0.1LS, 120TL, WHITE
30	6	6	FISCHER	CAB 4 G S	J1, J2, J3, J4, J5, J6	2.54 mm JUMPER	2.54 mm JUMPER

3.3 Layout and Component Placement

3.3.1 Top View

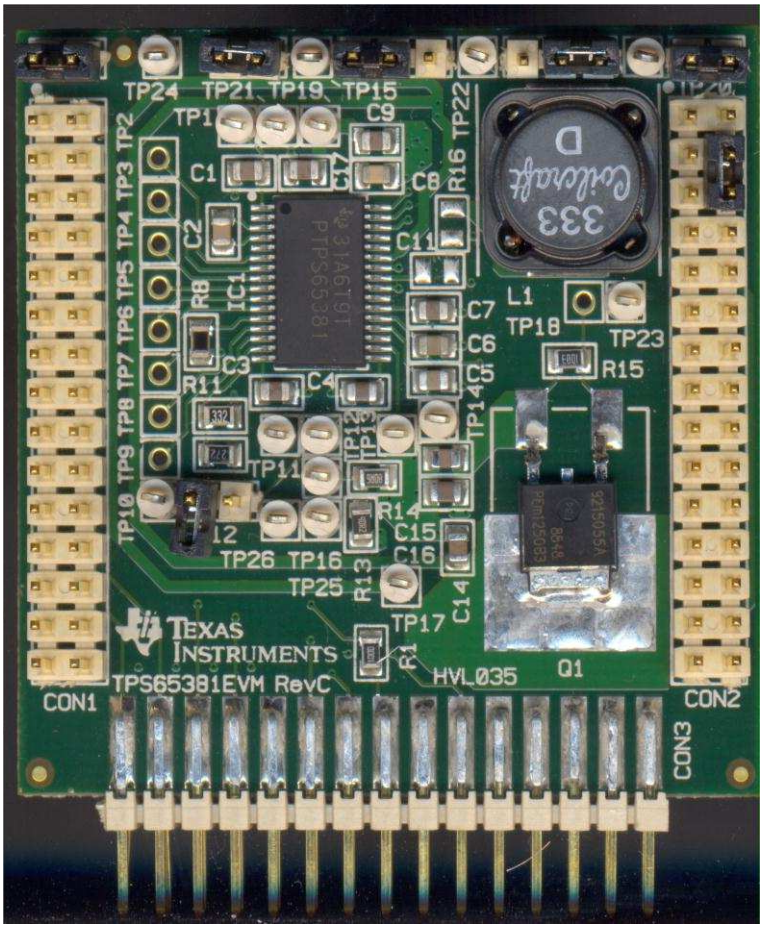


Figure 3. EVM Top View

3.3.2 Bottom View

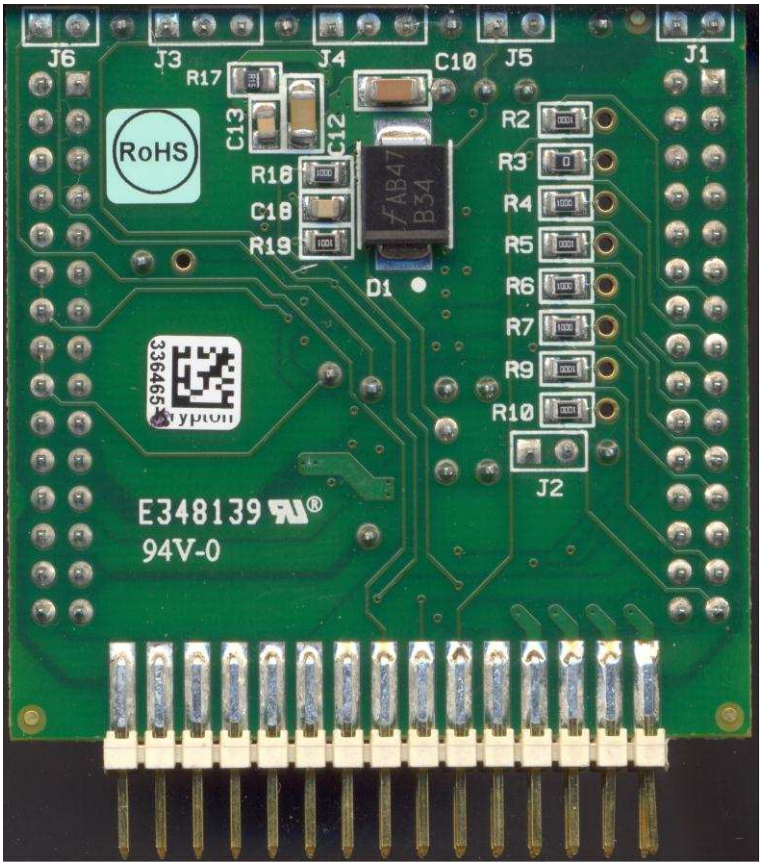


Figure 4. EVM Bottom View

3.3.3 Board Assembly

Figure 2 shows the EVM schematic. Figure 3 and Figure 4 show photos of the EVM. Figure 5 and Figure 6 show the board assembly layers.

While the TPS65381x-Q1 converter offers high efficiency, there may still be high power dissipation. The power dissipation will vary depending on input supply voltage, output voltages programmed on the various rails and load currents. The PowerPAD™ package offers an exposed thermal pad to enhance thermal performance which must be soldered to the copper landing on the PCB for optimal performance. The EVM PCB provides 2 oz. copper planes on the top and bottom to dissipate heat. Power dissipation and thermal analysis should be done to ensure the thermal management and design for each specific application and PCB design.

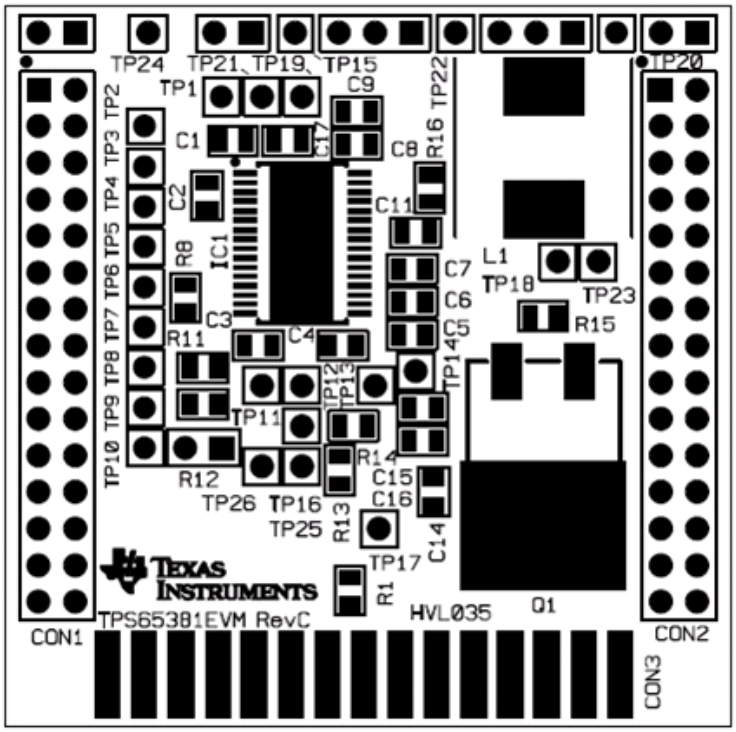


Figure 5. Top Assembly Layer

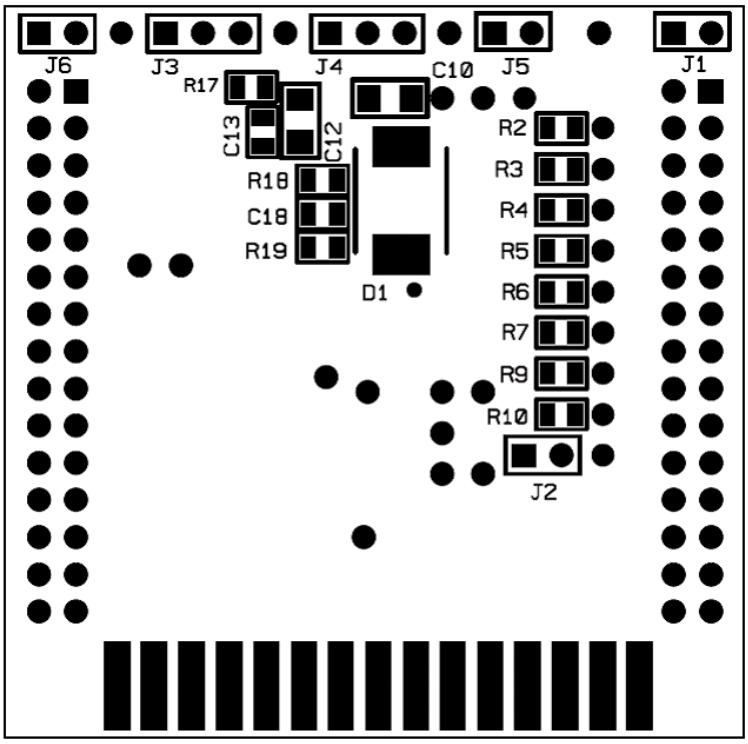


Figure 6. Bottom Assembly Layer

3.3.4 Board Layout

Figure 7 through Figure 10 show the board layout.

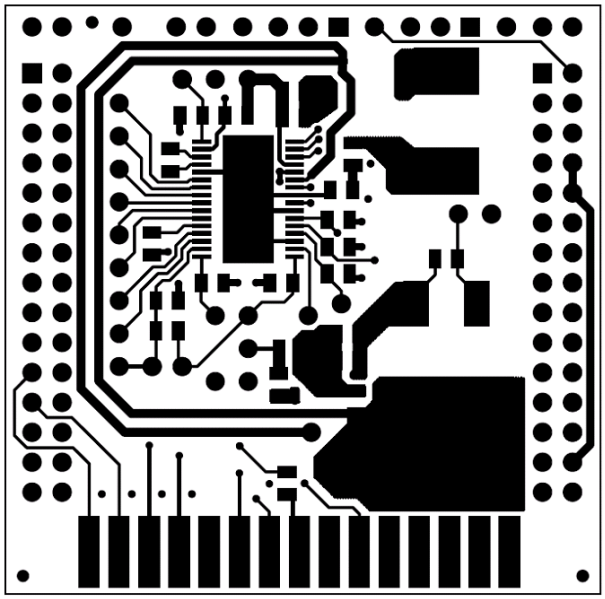


Figure 7. Top Layer Routing

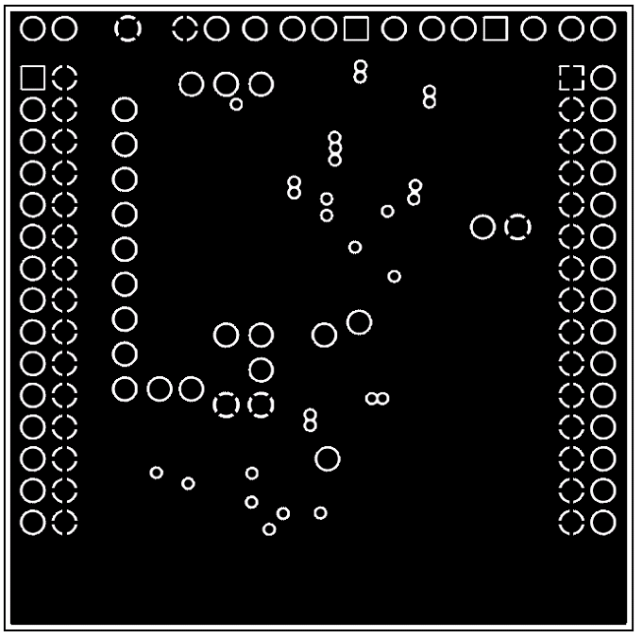


Figure 8. Layer 2 (AGND) Routing

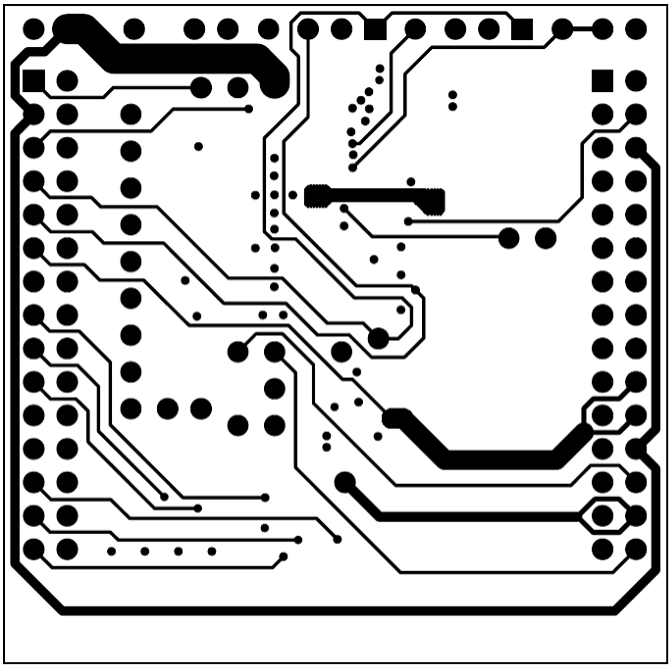


Figure 9. Layer 3 Routing

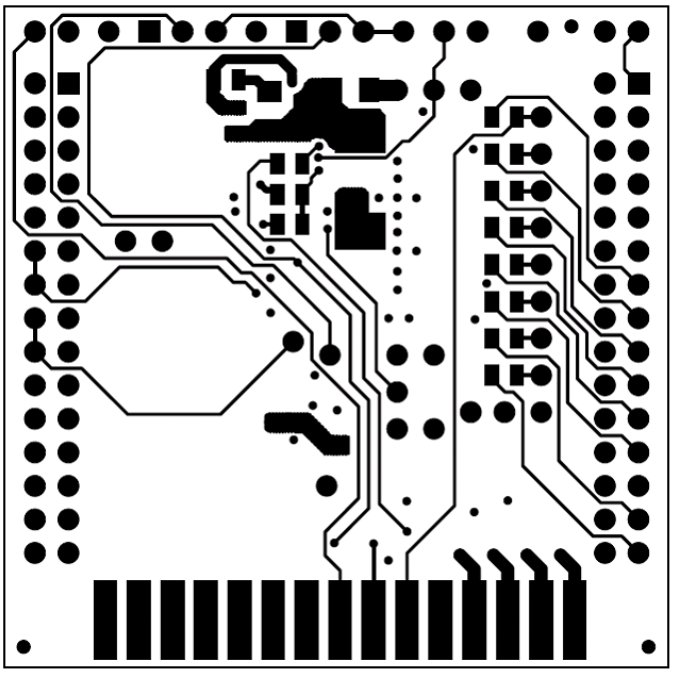


Figure 10. Layer 4 Routing

4 Setup and Operation

This section describes the jumpers and connectors on the EVM and how to properly connect, set up and use the TPS65381EVM.

4.1 I/O Connector Description

Three connectors are placed to supply the device under test (DUT) to get access to different signals for programming or to measure.

CON1 is the supply connector to provide the battery voltage and offer a connection to SPI.

CON2 is the output connector to deliver the output voltage of the different regulators.

CON3 is a connector to either the SPI of an application circuit, or the optional TIGER board which provides a universal serial bus (USB) to SPI connection.

Table 2. EVM Connectors

CON1		CON2		CON3	
PIN NO.	SIGNALS	PIN NO.	SIGNALS	PIN NO.	SIGNALS
1	VBAT_SAFING	1	GND	1	SDO
2	GND	2	ENDRV	2	GND
3	VBATP	3	GND	3	SCLK
4	GND	4	IGN	4	GND
5	VCP	5	GND	5	NCS
6	GND	6	VBATP	6	GND
7	VDD5	7	GND	7	SDI
8	GND	8	VDD6	8	GND
9	VDD3/5	9	GND	9	Open
10	GND	10	VDD6	10	Open
11	VDD1	11	GND	11	ENDRV
12	GND	12	VDD3/5	12	RES
13	RES	13	GND	13	CANWU
14	GND	14	VDD3/5	14	ERROR
15	DIAG_OUT	15	GND	15	DIAGOUT
16	GND	16	VDD5	16	IGN
17	NCS	17	GND	17	Open
18	GND	18	VDD5	18	Open
19	SDI	19	GND	19	VDDIO
20	GND	20	VDD1	20	Open
21	SDO	21	GND	21	Open
22	GND	22	VDD1	22	Open
23	SCLK	23	GND	23	Open
24	GND	24	VBATP	24	Open
25	VDDIO	25	GND	25	Open
26	GND	26	VSIN	26	Open
27	ERROR	27	GND	27	Open
28	GND	28	VDD6	28	Open
29	CANWU	29	GND	29	Open
30	GND	30	VSOUT1	30	Open

4.2 Supply

The input voltage range for the converter is VBATP = VBAT_SAFING = 5.8 volts to 36 volts. It should be supplied to CON1, pin 1 (VBAT_SAFING) and 3 (VBATP) with respect to pin 2 and 4 (GND).

NOTE: VBATP = VBAT_SAFING may be lowered to 4.5 volts after the device has been powered up, but VDD6 will be in dropout mode (100% duty) cycle, VDD5 will be in dropout and VDD3/5 will be in dropout and may cause RESET state if configured to 5 V mode depending on the detected output voltage, it will be operational if used in 3.3V mode.

Table 3. EVM Voltages

PARAMETER	TEST CONDITIONS	CONx CONNECTOR	PIN	MIN	TYP	MAX	UNIT
VBATP	Can be connected to VBAT_SAFING by placing J1	1	3	5.8	14	36	V
VBAT_SAFING	Can be connected to VBAT_P by placing J1	1	1	5.8	14	36	V
VDD6		2	8, 10	5.4	6	6.6	V
VDD1		2	20, 22	0.8	1.2	3.3	V
VDD3/5		2	12, 14	3.23 / 4.9	3 / 5	3.36 / 5.1	V
VDD5		2	16, 18	4.9	5	5.1	V
VSOUT1		2	30	3.3	5	9.5	V
VDDIO		1	25	3.3		5	V

4.3 Jumper Setting

For proper operation of the TPS65381x-Q1 device, the jumpers should be properly configured. The recommended setting is shown in the table below.

Table 4. EVM Jumper[(1)]

J NO.	DESCRIPTION	OPTION	STANDARD
J1	Connect VBAT_SAFING to VBATP.	Open and supply VBAT_SAFING with separate supply voltage.	Set
J2	Use VSOUT1 as follower or with gain.	Open VSOUT1 has gain defined by R11 and R12. Set is VSOUT1 is follower.	Open
J3	Select the tracking input.	Open for non-tracking mode or connect to VDD3/5 or VDD5 for tracking mode.	Open
J4	Select the VDDIO voltage.	Connect to VDD3/5 or VDD5.	VDD5
J5	Select output voltage VDD3/5.	Open VDD3/5 = 3.3 V. Set VDD3/5 = 5 V.	Set
J6	IGN supported by TIGER board and SPI connector CON3.	Open is not supported by SPI. Closed can be supported by SPI.	Open
CON2, pin 4	Connector 2 (pin 4) is the IGN pin; must be connected to CON2, pin 4 to turn the DUT on.	Remove the jumper to use the EVM together with TIGER board.	Set

(1) For start-up without using the TIGER board or external IGN signal, IGN (pin 4 of CON2) can be connected to VBATP (pin 6 of CON2) by setting a jumper to start up the device.

4.4 Test Points

Test points are placed to measure different nodes on the board.

Table 5. EVM Test Points

NO.	TEST POINT
1	VBAT_SAFING
2	RES
3	DIAG_OUT
4	NCS
5	SDI
6	SDO
7	SCLK
8	ERROR
9	CANWU
10	VSOUT1
11	VSIN
12	VSOUT1
13	VTRACK1
14	VDD5
15	VDD3/5
16	VDD1_SENSE
17	VDD6
18	VDD1_G
19	VBATP
20	IGN
21	SEL_VDD3/5
22	ENDRV

4.5 VDD6 Voltage Preregulator

The VDD6 preregulator is supplied by VBATP. Blocking capacitors C8, C9 and C10 are connected from VBATP to GND, stabilizing the input supply voltage. For long supply cables, additional higher capacitance capacitors could be helpful. The node SDN6 is the switching node of the buck converter. L1 is the inductor connected to SDN6 and VDD6. The freewheeling diode D1 allows current flow when the device internal high-side transistor is turned off. C11 and C12 are the output capacitors of the VDD6 regulator. R16 is the ESR of C11 and R17 is the ESR of C12 required for stability. C13 is a filter capacitor against high frequencies.

NOTE: VDD6 output capacitance requires controlled ESR. See the device datasheet electrical parameters and VDD6 Preregulator section for details on R, L and C choices to ensure stable and balanced operation of VDD6.

The VDD6 pin is the feedback line to close the control loop of the VDD6 regulator, and is also the supply node for the VDD3/5 and VDD5 regulators. The output voltage VDD6 is available at CON2, pins 8 and 10.

4.6 VDD1 Voltage Regulator (LDO Controller requiring external FET)

The VDD1 regulator has an internal control amplifier and an external NMOS power transistor. The regulator is supplied externally by VDD6. C14 stabilizes the input voltage of the VDD1 regulator. The voltage dividers R13 and R14 define the output voltage and close the control loop to VDD1_SENSE. Additionally, a minimum required current flows though both resistors. The output capacitors C15 and C16 are needed to stabilize the control loop. The output voltage VDD1 is available at CON1, pin 11, and CON2, pins 20 and 22.

4.7 VDD3/5 Voltage Regulator

The VDD3/5 regulator is supplied internally by VDD6. SEL_VDD3/5 can select the output voltage. If the pin is open, 3.3 V is selected. If the pin is shorted to GND, 5 V is selected. The output capacitor C6 is needed to stabilize the output voltage. The output voltage VDD3/5 is available at CON1, pin 9, and CON2, pins 12 and 14.

4.8 VDD5 Voltage Regulator

The VDD5 regulator is supplied internally by VDD6. The output capacitor C5 is needed to stabilize the output voltage. The output voltage VDD5 is available at CON1, pin 7, and CON2, pins 16 and 18.

4.9 VSOUT1 Voltage Regulator

VSIN is the supply pin of VSOUT1 voltage regulator. If VSIN is connected to VDD6, lower power dissipation can be achieved. VSIN is supplied by VDD6 by placing a jumper to short pin 26 and 28 of CON2. If VSIN is connected to VBATP, output voltages higher than 5V are possible at the expense of higher power dissipation. To supply VSIN from VBATP, place a jumper to short pin 24 and 26 of CON2. The capacitor C3 stabilizes the input voltage. The voltage regulator can be used in tracking or non-tracking mode. Additionally, the voltage dividers R11 and R12 are used to define the output voltage. The capacitor C4 is needed for stable operation. The output voltage VSOUT1 is available at CON2, pin 30.

4.10 Operation

4.10.1 Go into ACTIVE Mode - Step by Step Description

To go into active mode several steps are needed, please refer to the data sheet SLVSBC4.

1. Install the GUI software on a Windows PC.
2. Connect the EVM with the TIGER board, and the TIGER board to a PC USB connector.
3. Provide power to the EVM by connecting VBATP and VBAT_SAFING to a 12-V power supply. Observe the quiescent current, it should be low since the device will be in STANDBY state unless IGN or CANWU has been pulled high.
4. Drive the watchdog (WD) with t = 74 ms, $t_{(high)}$ = 1%, (to match default setting for watchdog) on CON 1 pin 27 (ERROR). The values can be changed but the TPS65381x-Q1 watchdog settings must also be updated to match the changed trigger pulse waveform.
   (see SLVSBC4).

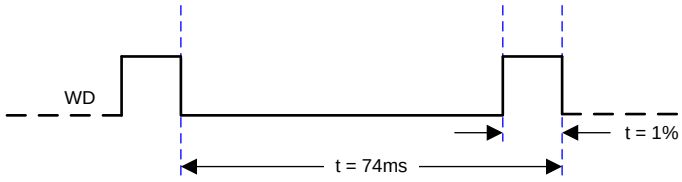


Figure 11. WD Timing

5. Start the GUI software.

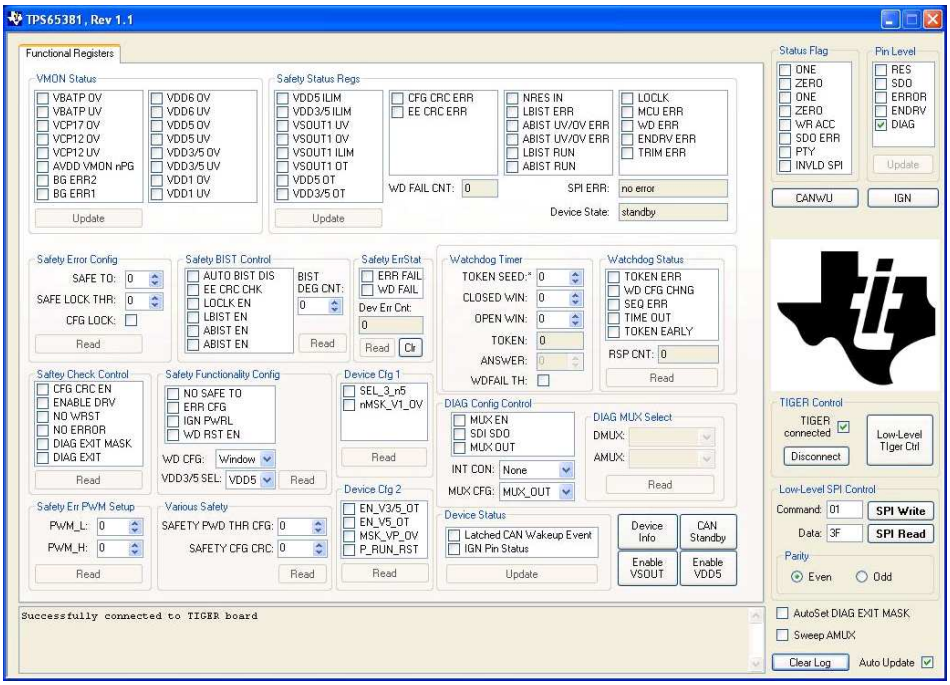


Figure 12. Start-Up Screen

6. Click the "AutoSet DIAG EXIT MASK" box in the lower right to "set" this function in the GUI. Setting this in the GUI causes the GUI to set the DIAG_EXIT_MASK bit before the device will have DIAGNOSTIC state timeout when the device is powered up by the IGN or CANWU button. Not doing so will cause the device to end up in SAFE state due to the non-real time nature of the GUI while the TPS65381x-Q1 is running in real time.
7. To wake up the device, click the IGN button.

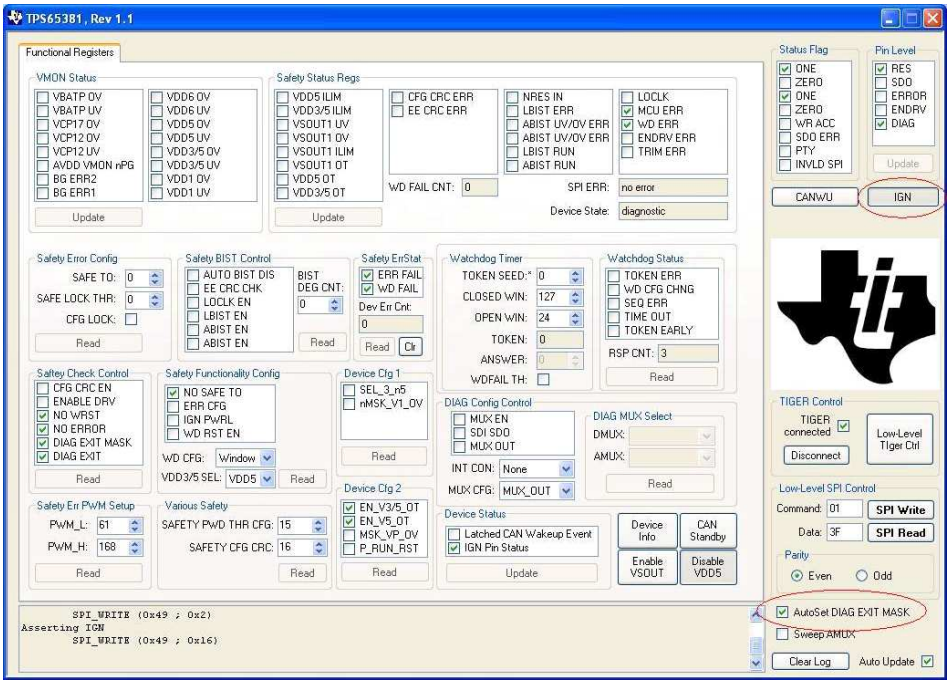


Figure 13. After Clicking IGN, Device Has Started, I_q is About 30 mA, Device is in Diagnostic Mode

8. Click the Clr button below ERR Fail and WD Fail to clear these flags and allow the device to go ACTIVE state.

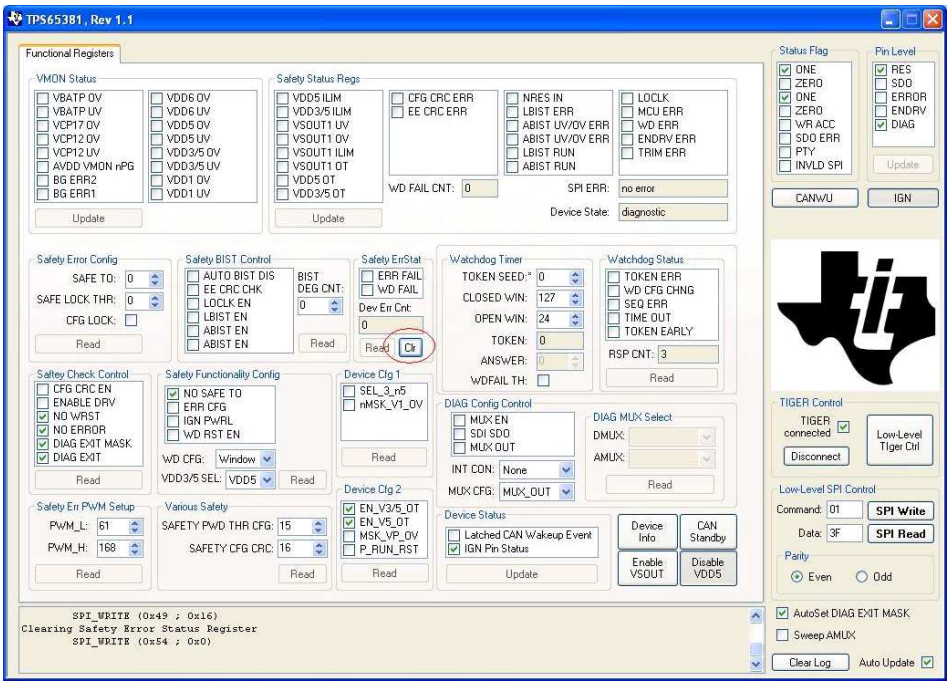


Figure 14. Clear ERR Fail and WD Fail Flags

9. Click on the box for DIAG EXIT MASK to clear it and thus the control bit in the device. Once this bit is cleared the device will transition to ACTIVE state.

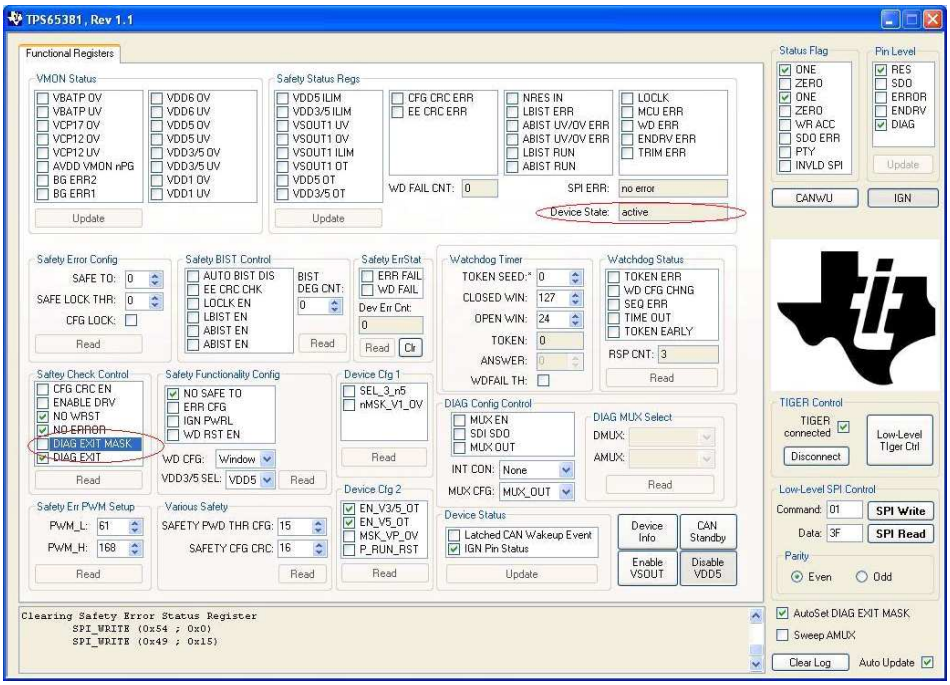


Figure 15. Clear DIAG EXIT MASK = Device is in Active Mode

10. Click the box next to ENABLE_DRV, middle left in the GUI, to set the bit in the device. Because the external signal on the EVM ERROR pin is connected to the device ERROR/WDI pin and the trigger pulse matches the configuration of the watchdog in trigger mode the WD_FAIL_CNT has been decremented to 0. Once ENABLE_DRV is set, ENDRV pin will go high and this will be shown by the GUI in the upper right because the conditions allowing ENDRV to be high have been met.

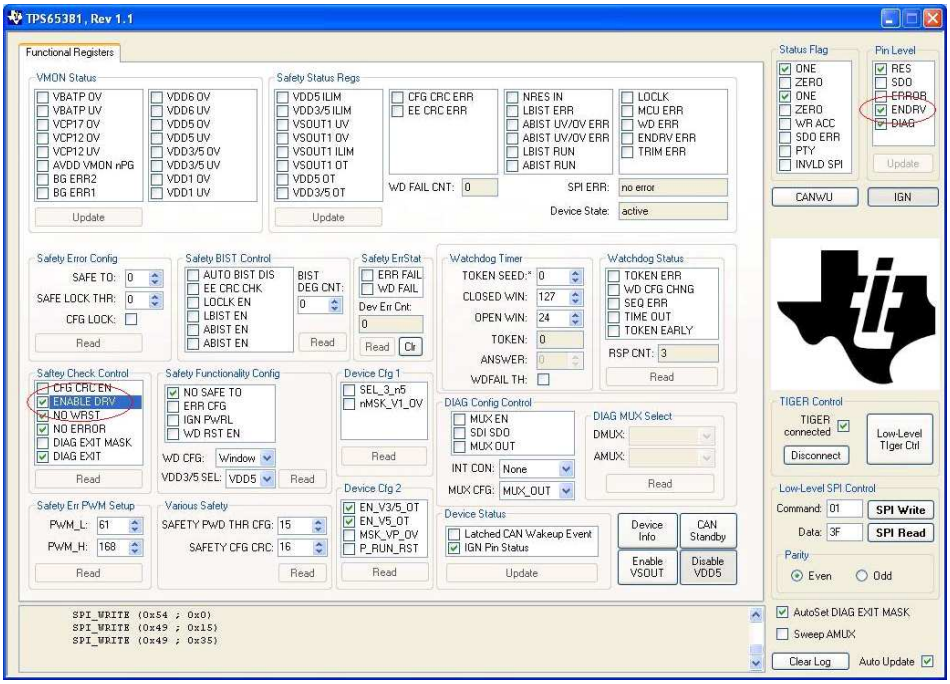


Figure 16. Set ENABLE_DRV and Read Back Pin Level ENDRV

Now the device is in active mode and the ENDRV signal would have enabled the power stages in a real safety relevant application.

For details regarding the flags and register setting, please refer to the data sheet (SLVSBC4).

5 TIGER GUI Software

The graphical user interface (GUI) software is intended to support a quick start of the TPS65381x-Q1 evaluation. As the USB to SPI connection, a TIGER board is needed to run the software. It can be connected directly to CON3.

After first starting the software, the installation of a .net environment might be needed. It can be downloaded at microsoft.com.

The software provides the user a GUI for easy set-up and control of the TPS65381x-Q1 device.

Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Original (April 2013) to A Revision	Page
• Changed document format to TI standards	1
• Added TPS65381(A)-Q1 device information	1
• Added EVM board photo to *Introduction* section	2
• Moved *Schematic*, *Board Picture*, *Board Assembly*, *Board Layout*, and *Bill of Material* sections to new *Schematic, Bill of Materials, and Layout* section	4
• Added TPS65381AQDAPRQ1 to the BOM	5
• Moved *TIGER GUI Software* to after *Setup and Operation* section	18

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      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

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      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

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- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

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Concernant les EVMs avec appareils radio:

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Concernant les EVMs avec antennes détachables

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2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
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