MMFT960T1

Preferred Device

Power MOSFET 300 mA, 60 Volts

N−Channel SOT−223

This Power MOSFET is designed for high speed, low loss power switching applications such as switching regulators, dc−dc converters, solenoid and relay drivers. The device is housed in the SOT−223 package which is designed for medium power surface mount applications.

Features

- Silicon Gate for Fast Switching Speeds
- Low Drive Requirement
- The SOT−223 Package can be Soldered Using Wave or Reflow
- The Formed Leads Absorb Thermal Stress During Soldering Eliminating the Possibility of Damage to the Die
- Pb−Free Package is Available

MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DS}	60	V
Gate−to−Source Voltage − Non−Repetitive	V_{GS}	±30	V
Drain Current	I_D	300	mAdc
Total Power Dissipation @ T_A = 25°C (Note 1) Derate above 25°C	P_D	0.8 6.4	W mW/°C
Operating and Storage Temperature Range	T_J, T_{stg}	−65 to 150	°C

THERMAL CHARACTERISTICS

Thermal Resistance, Junction−to−Ambient	$R_{\theta JA}$	156	°C/W
Maximum Temperature for Soldering Purposes Time in Solder Bath	T_L	260 10	°C S

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. Device mounted on a FR−4 glass epoxy printed circuit board using minimum recommended footprint.

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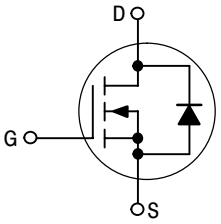
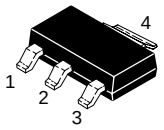
300 mA, 60 VOLTS
$R_{DS(on)}$ = 1.7 Ω

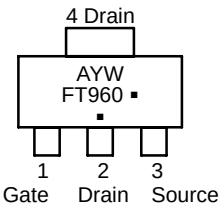
N−Channel





TO−261AA
CASE 318E
STYLE 3

MARKING DIAGRAM AND PIN ASSIGNMENT



A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package
FT960 = Device Code
(Note: Microdot may be in either location)

ORDERING INFORMATION

Device	Package	Shipping†
MMFT960T1	SOT−223	1000 Tape & Reel
MMFT960T1G	SOT−223 (Pb−Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Preferred devices are recommended choices for future use and best overall value.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (V_{GS} = 0, I_D = 10 μA)		$V_{(BR)DSS}$	60	−	−	Vdc
Zero Gate Voltage Drain Current (V_{DS} = 60 V, V_{GS} = 0)		I_{DSS}	−	−	10	μAdc
Gate−Body Leakage Current (V_{GS} = 15 Vdc, V_{DS} = 0)		I_{GSS}	−	−	50	nAdc
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage (V_{DS} = V_{GS}, I_D = 1.0 mAdc)		$V_{GS(th)}$	1.0	−	3.5	Vdc
Static Drain−to−Source On−Resistance (V_{GS} = 10 Vdc, I_D = 1.0 A)		$R_{DS(on)}$	−	−	1.7	Ω
Drain−to−Source On−Voltage (V_{GS} = 10 V, I_D = 0.5 A) (V_{GS} = 10 V, I_D = 1.0 A)		$V_{DS(on)}$	− −	− −	0.8 1.7	Vdc
Forward Transconductance (V_{DS} = 25 V, I_D = 0.5 A)		g_{fs}	−	600	−	mmhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 V, V_{GS} = 0, f = 1.0 MHz)	C_{iss}	−	65	−	pF
Output Capacitance		C_{oss}	−	33	−	
Transfer Capacitance		C_{rss}	−	7.0	−	
Total Gate Charge	(V_{GS} = 10 V, I_D = 1.0 A, V_{DS} = 48 V)	Q_g	−	3.2	−	nC
Gate−Source Charge		Q_{gs}	−	1.2	−	
Gate−Drain Charge		Q_{gd}	−	2.0	−	

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

TYPICAL ELECTRICAL CHARACTERISTICS

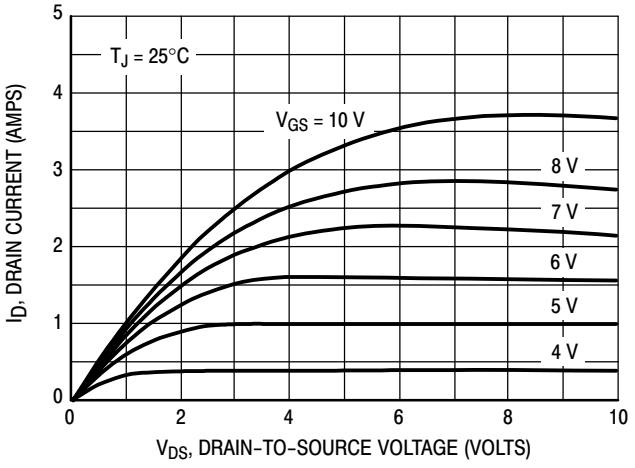


Figure 1. On−Region Characteristics

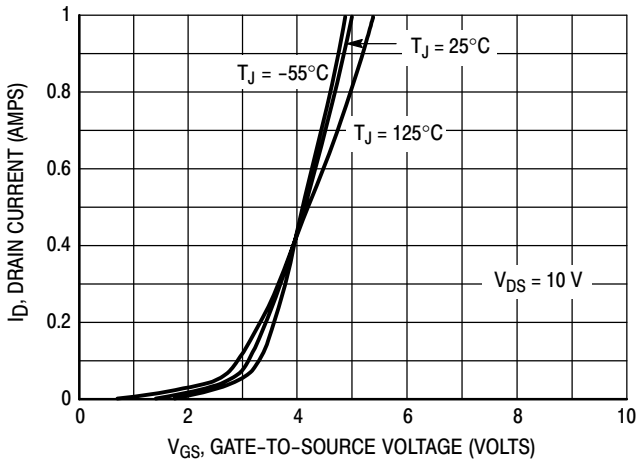


Figure 2. Transfer Characteristics

TYPICAL ELECTRICAL CHARACTERISTICS

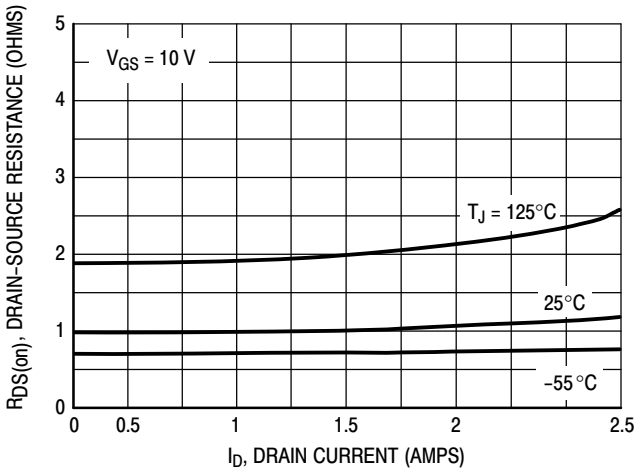


Figure 3. On−Resistance versus Drain Current

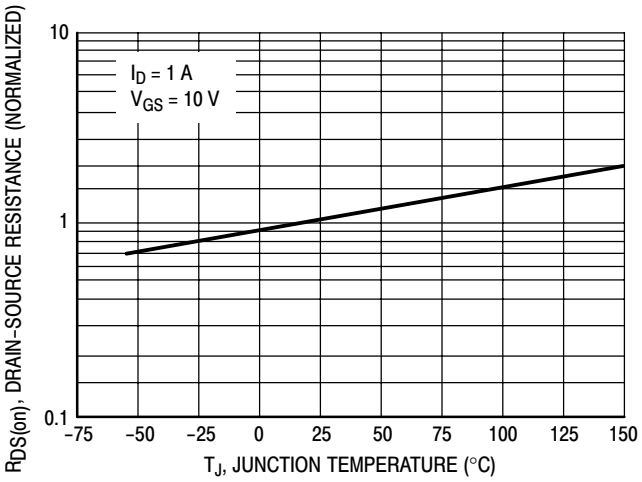


Figure 4. On−Resistance Variation with Temperature

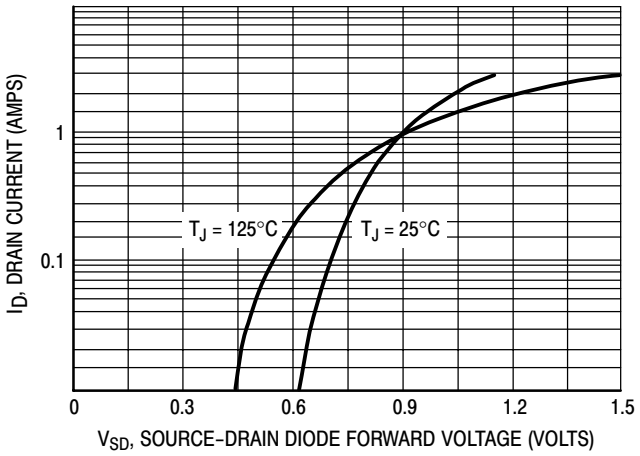


Figure 5. Source−Drain Diode Forward Voltage

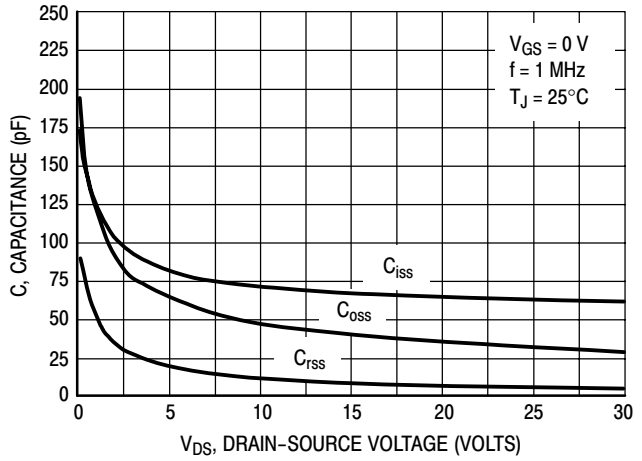


Figure 6. Capacitance Variation

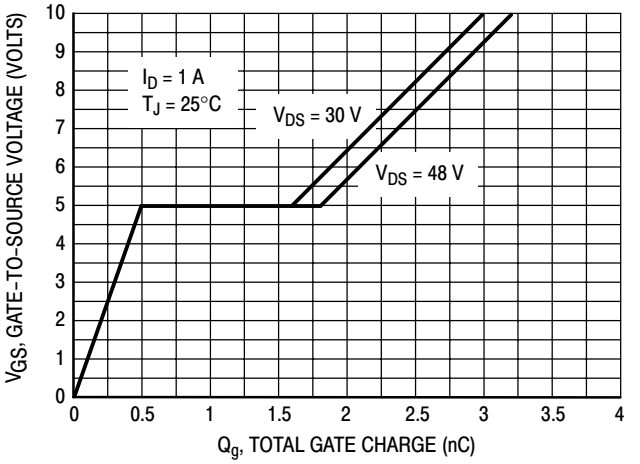


Figure 7. Gate Charge versus Gate−to−Source Voltage

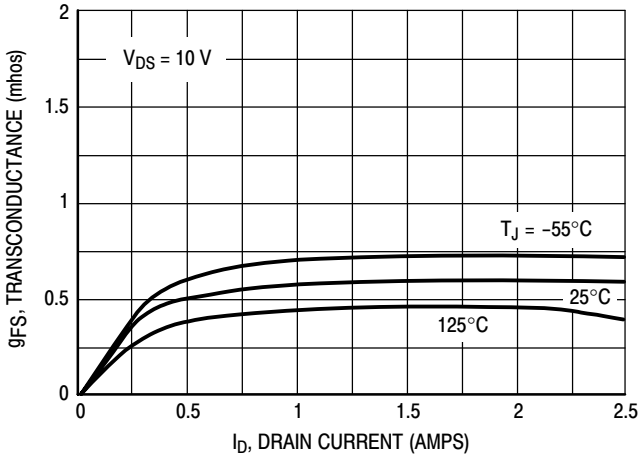


Figure 8. Transconductance

SCALE 1:1

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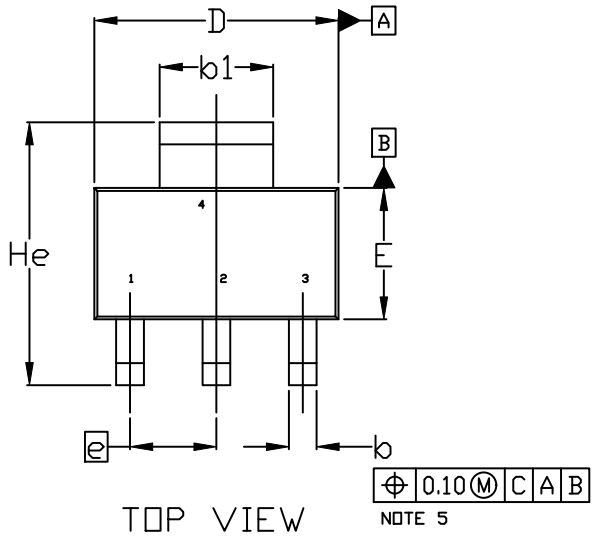
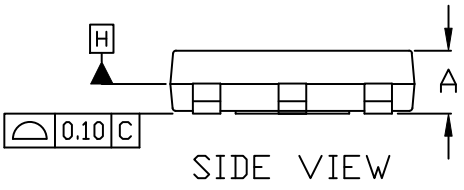
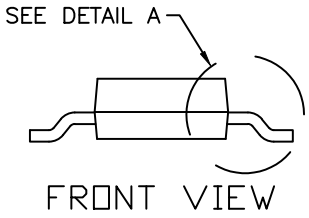
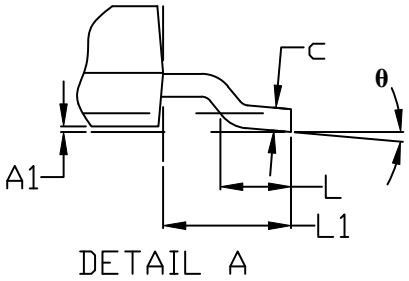
CASE 318E−04
ISSUE R

DATE 02 OCT 2018



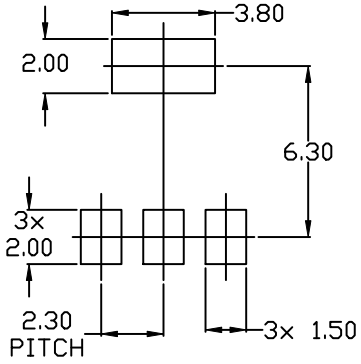






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
θ	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

SOT−223 (TO−261)
CASE 318E−04
ISSUE R

DATE 02 OCT 2018

STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

STYLE 2:
PIN 1. ANODE
2. CATHODE
3. NC
4. CATHODE

STYLE 3:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

STYLE 4:
PIN 1. SOURCE
2. DRAIN
3. GATE
4. DRAIN

STYLE 5:
PIN 1. DRAIN
2. GATE
3. SOURCE
4. GATE

STYLE 6:
PIN 1. RETURN
2. INPUT
3. OUTPUT
4. INPUT

STYLE 7:
PIN 1. ANODE 1
2. CATHODE
3. ANODE 2
4. CATHODE

STYLE 8:
CANCELLED

STYLE 9:
PIN 1. INPUT
2. GROUND
3. LOGIC
4. GROUND

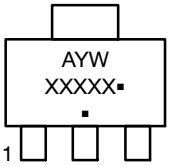
STYLE 10:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE

STYLE 11:
PIN 1. MT 1
2. MT 2
3. GATE
4. MT 2

STYLE 12:
PIN 1. INPUT
2. OUTPUT
3. NC
4. OUTPUT

STYLE 13:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR

GENERIC MARKING DIAGRAM*



A = Assembly Location
Y = Year
W = Work Week
XXXXX = Specific Device Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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