

# TL1451A

## DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS024E – FEBRUARY 1983 – REVISED NOVEMBER 1999

- Complete PWM Power Control Circuitry
- Completely Synchronized Operation
- Internal Undervoltage Lockout Protection
- Wide Supply Voltage Range
- Internal Short-Circuit Protection
- Oscillator Frequency . . . 500 kHz Max
- Variable Dead Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 2.5-V Reference Supply
- Available in Q-Temp Automotive HighRel Automotive Applications Configuration Control / Print Support Qualification to Automotive Standards

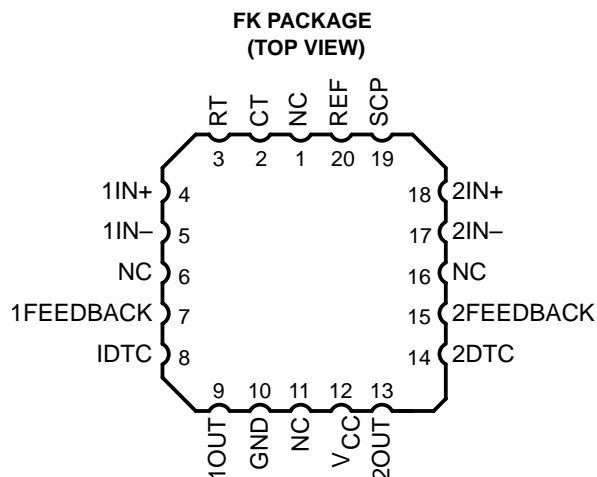
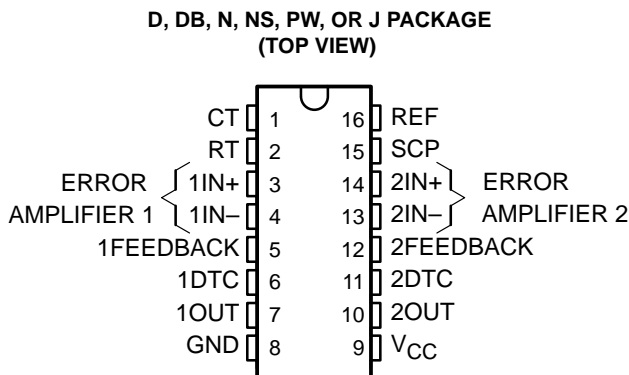
### description

The TL1451A incorporates on a single monolithic chip all the functions required in the construction of two pulse-width-modulation (PWM) control circuits. Designed primarily for power-supply control, the TL1451A contains an on-chip 2.5-V regulator, two error amplifiers, an adjustable oscillator, two dead-time comparators, undervoltage lockout circuitry, and dual common-emitter output transistor circuits.

The uncommitted output transistors provide common-emitter output capability for each

controller. The internal amplifiers exhibit a common-mode voltage range from 1.04 V to 1.45 V. The dead-time control (DTC) comparator has no offset unless externally altered and can provide 0% to 100% dead time. The on-chip oscillator can be operated by terminating RT and CT. During low  $V_{CC}$  conditions, the undervoltage lockout control circuit feature locks the outputs off until the internal circuitry is operational.

The TL1451AC is characterized for operation from  $-20^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ . The TL1451AQ is characterized for operation from  $-40^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The TL1451AM is characterized for operation from  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ .



### AVAILABLE OPTIONS

T <sub>A</sub>	PACKAGED DEVICES						
	SMALL OUTLINE (D)	SMALL OUTLINE (DB) <sup>†</sup>	PLASTIC DIP (N)	SMALL OUTLINE (NS)	TSSOP (PW) <sup>†</sup>	CHIP CARRIER (FK)	CERAMIC DIP (J)
$-20^{\circ}\text{C}$ to $85^{\circ}\text{C}$	TL1451ACD	TL1451ACDB	TL1451ACN	TL1451ACNS	TL1451ACPW	—	—
$-40^{\circ}\text{C}$ to $125^{\circ}\text{C}$	TL1451AQD	—	—	—	—	—	—
$-55^{\circ}\text{C}$ to $125^{\circ}\text{C}$	—	—	—	—	—	TL1451AMFK	TL1451AMJ

<sup>†</sup> The DB and PW packages are only available left-end taped and reeled (add LE suffix, i.e., TL1451ACPWLE).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

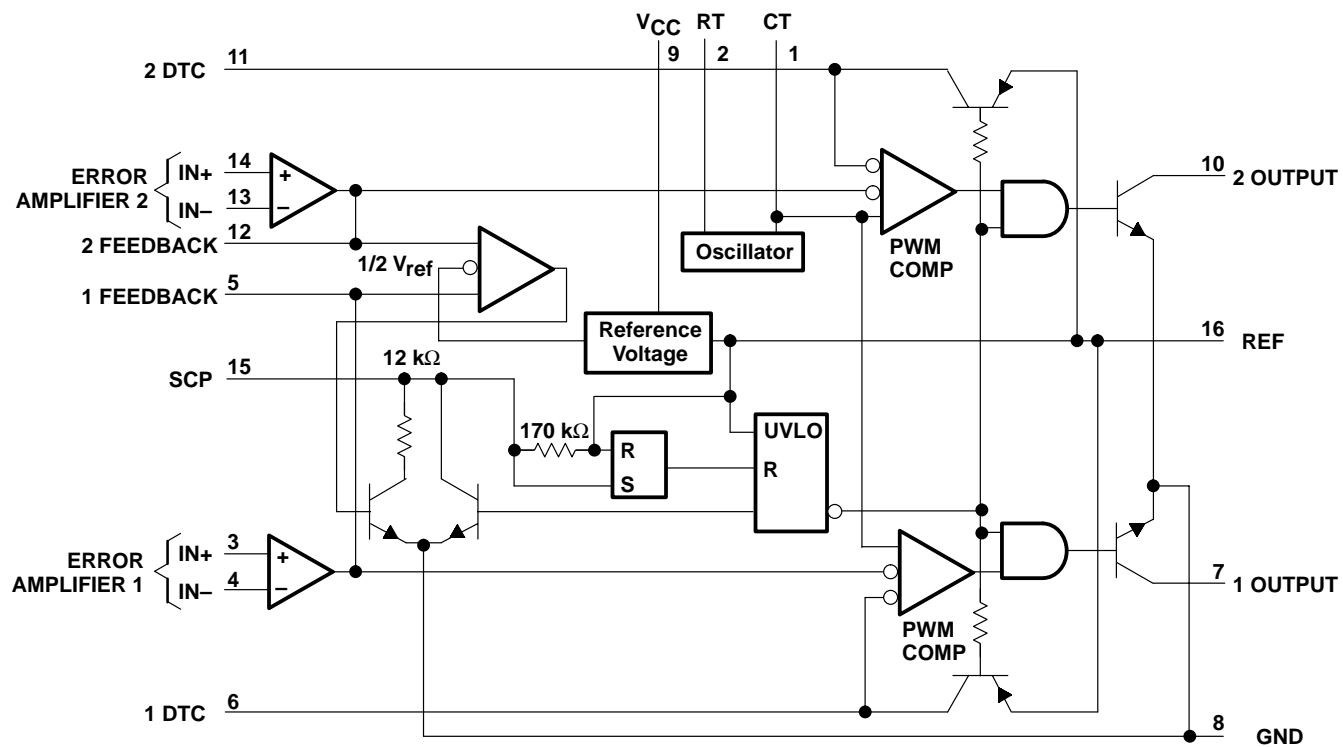
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# TL1451A DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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## functional block diagram



### COMPONENT COUNT

Resistors	65
Capacitors	8
Transistors	105
JFETs	18



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electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6\text{ V}$ ,  $f = 200\text{ kHz}$  (unless otherwise noted)

### reference section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Output voltage (pin 16)	$I_O = 1\text{ mA}$	2.4	2.5	2.6	V
Output voltage change with temperature	$T_A = -20^\circ\text{C}$ to $25^\circ\text{C}$		-0.1%	$\pm 1\%$	
	$T_A = 25^\circ\text{C}$ to $85^\circ\text{C}$		-0.2%	$\pm 1\%$	
Input voltage regulation	$V_{CC} = 3.6\text{ V}$ to $40\text{ V}$		2	12.5	mV
Output voltage regulation	$I_O = 0.1\text{ mA}$ to $1\text{ mA}$		1	7.5	mV
Short-circuit output current	$V_O = 0$	3	10	30	mA

† All typical values are at  $T_A = 25^\circ\text{C}$ .

### undervoltage lockout section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Upper threshold voltage ( $V_{CC}$ )	$I_{O(\text{ref})} = 0.1\text{ mA}$ , $T_A = 25^\circ\text{C}$		2.72		V
Lower threshold voltage ( $V_{CC}$ )			2.6		V
Hysteresis ( $V_{CC}$ )		80	120		mV
Reset threshold voltage ( $V_{CC}$ )		1.5	1.9		V

† All typical values are at  $T_A = 25^\circ\text{C}$ .

### short-circuit protection control section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Input threshold voltage (SCP)	$T_A = 25^\circ\text{C}$	0.65	0.7	0.75	V
Standby voltage (SCP)	No pullup	140	185	230	mV
Latched input voltage (SCP)	No pullup		60	120	mV
Input (source) current	$V_I = 0.7\text{ V}$ , $T_A = 25^\circ\text{C}$	-10	-15	-20	$\mu\text{A}$
Comparator threshold voltage (FEEDBACK)			1.18		V

† All typical values are at  $T_A = 25^\circ\text{C}$ .

### oscillator section

PARAMETER	TEST CONDITIONS	TL1451C			UNIT
		MIN	TYP†	MAX	
Frequency	$C_T = 330\text{ pF}$ , $R_T = 10\text{ k}\Omega$		200		kHz
Standard deviation of frequency	$C_T = 330\text{ pF}$ , $R_T = 10\text{ k}\Omega$		10%		
Frequency change with voltage	$V_{CC} = 3.6\text{ V}$ to $40\text{ V}$		1%		
Frequency change with temperature	$T_A = -20^\circ\text{C}$ to $25^\circ\text{C}$		-0.4%	$\pm 2\%$	
	$T_A = 25^\circ\text{C}$ to $85^\circ\text{C}$		-0.2%	$\pm 2\%$	

† All typical values are at  $T_A = 25^\circ\text{C}$ .

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### dead-time control section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Input bias current (DTC)				1	μA
Latch mode (source) current (DTC)	T <sub>A</sub> = 25°C	-80	-145		μA
Latched input voltage (DTC)	I <sub>O</sub> = 40 μA	2.3			V
Input threshold voltage at f = 10 kHz (DTC)	Zero duty cycle		2.05	2.25	V
	Maximum duty cycle	1.2	1.45		

† All typical values are at T<sub>A</sub> = 25°C.

### error-amplifier section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Input offset voltage	V <sub>O</sub> (FEEDBACK) = 1.25 V			±6	mV
Input offset current	V <sub>O</sub> (FEEDBACK) = 1.25 V			±100	nA
Input bias current	V <sub>O</sub> (FEEDBACK) = 1.25 V		160	500	nA
Common-mode input voltage range	V <sub>CC</sub> = 3.6 V to 40 V	1.05 to 1.45			V
Open-loop voltage amplification	R <sub>F</sub> = 200 kΩ	70	80		dB
Unity-gain bandwidth			1.5		MHz
Common-mode rejection ratio		60	80		dB
Positive output voltage swing				V <sub>ref</sub> -0.1	V
Negative output voltage swing				1	V
Output (sink) current (FEEDBACK)	V <sub>ID</sub> = -0.1 V, V <sub>O</sub> = 1.25 V	0.5	1.6		mA
Output (source) current (FEEDBACK)	V <sub>ID</sub> = 0.1 V, V <sub>O</sub> = 1.25 V	-45	-70		μA

† All typical values are at T<sub>A</sub> = 25°C.

### output section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Collector off-state current	V <sub>O</sub> = 50 V			10	μA
Output saturation voltage	I <sub>O</sub> = 10 mA		1.2	2	V
Short-circuit output current	V <sub>O</sub> = 6 V		90		mA

† All typical values are at T<sub>A</sub> = 25°C.

### pwm comparator section

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Input threshold voltage at f = 10 kHz (FEEDBACK)	Zero duty cycle		2.05	2.25	V
	Maximum duty cycle	1.2	1.45		

† All typical values are at T<sub>A</sub> = 25°C.

### total device

PARAMETER	TEST CONDITIONS	TL1451AC			UNIT
		MIN	TYP†	MAX	
Standby supply current	Off-state		1.3	1.8	mA
Average supply current	R <sub>T</sub> = 10 kΩ		1.7	2.4	mA

† All typical values are at T<sub>A</sub> = 25°C.

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## DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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electrical characteristics over recommended operating free-air temperature range,  $V_{CC} = 6\text{ V}$ ,  $f = 200\text{ kHz}$  (unless otherwise noted)

### reference section

PARAMETER	TEST CONDITIONS		TL1451AQ, TL1451AM			UNIT
			MIN	TYP†	MAX	
Output voltage (pin 16)	$I_O = 1\text{ mA}$	$T_A = 25^\circ\text{C}$	2.40	2.50	2.60	V
		$T_A = \text{MIN and } 125^\circ\text{C}$	2.35	2.46	2.65	
Output voltage change with temperature			-0.63%		*±4%	
Input voltage regulation	$V_{CC} = 3.6\text{ V to } 40\text{ V}$	$T_A = 25^\circ\text{C}$		2.0	12.5	mV
		$T_A = 125^\circ\text{C}$		0.7	15	
		$T_A = \text{MIN}$		0.3	30	
Output voltage regulation	$I_O = 0.1\text{ mA to } 1\text{ mA}$	$T_A = 25^\circ\text{C}$		1.0	7.5	mV
		$T_A = 125^\circ\text{C}$		0.3	14	
		$T_A = \text{MIN}$		0.3	20	
Short-circuit output current	$V_O = 0$		3	10	30	mA

\*These parameters are not production tested.

† All typical values are at  $T_A = 25^\circ\text{C}$  unless otherwise indicated.

### undervoltage lockout section

PARAMETER	TEST CONDITIONS		TL1451AQ, TL1451AM			UNIT
			MIN	TYP†	MAX	
Upper threshold voltage ( $V_{CC}$ )		$T_A = 25^\circ\text{C}$		2.72		V
		$T_A = 125^\circ\text{C}$		1.70		
		$T_A = \text{MIN}$		3.15		
Lower threshold voltage ( $V_{CC}$ )		$T_A = 25^\circ\text{C}$		2.60		V
		$T_A = 125^\circ\text{C}$		1.65		
		$T_A = \text{MIN}$		3.09		
Hysteresis ( $V_{CC}$ )		$T_A = 25^\circ\text{C}$	80	120		mV
		$T_A = 125^\circ\text{C}$	10	50		
		$T_A = \text{MIN}$	10	60		
Reset threshold voltage ( $V_{CC}$ )		$T_A = 25^\circ\text{C}$		1.50		V
		$T_A = 125^\circ\text{C}$		0.95		
		$T_A = \text{MIN}$		1.50		

† All typical values are at  $T_A = 25^\circ\text{C}$  unless otherwise indicated.

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## DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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### short-circuit protection control section

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP†	MAX	
Input threshold voltage (SCP)	$T_A = 25^\circ\text{C}$	650	700	750	mV
	$T_A = 125^\circ\text{C}$	400	478	550	
	$T_A = \text{MIN}$	800	880	950	
Standby voltage (SCP)		140	185	230	mV
Latched input voltage (SCP)	$T_A = 25^\circ\text{C}$		60	120	mV
	$T_A = 125^\circ\text{C}$		70	120	
	$T_A = \text{MIN}$		60	120	
Equivalent timing resistance			170		k $\Omega$
Comparator threshold voltage (FEEDBACK)			1.18		V

† All typical values are at  $T_A = 25^\circ\text{C}$  unless otherwise indicated.

### oscillator section

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP†	MAX	
Frequency	$C_T = 330 \text{ pF}$ , $R_T = 10 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	200		kHz
		$T_A = 125^\circ\text{C}$	195		
		$T_A = \text{MIN}$	193		
Standard deviation of frequency	$C_T = 330 \text{ pF}$ , $R_T = 10 \text{ k}\Omega$		2%		
Frequency change with voltage	$V_{CC} = 3.6 \text{ V to } 40 \text{ V}$	$T_A = 25^\circ\text{C}$	1%		
		$T_A = 125^\circ\text{C}$	1%		
		$T_A = \text{MIN}$	3%		
Frequency change with temperature			1.37%	$\pm 10\%$	

\*These parameters are not production tested.

† All typical values are at  $T_A = 25^\circ\text{C}$  unless otherwise indicated.

### dead-time control section

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP†	MAX	
Input bias current (DTC)	$T_A = 25^\circ\text{C}$			1	$\mu\text{A}$
	$T_A = \text{MIN and } 125^\circ\text{C}$			3	
Latch mode (source) current (DTC)		-80	-145		$\mu\text{A}$
Latched input voltage (DTC)	$T_A = 25^\circ\text{C}$	2.30		V	
	$T_A = 125^\circ\text{C}$	2.22	2.32		
	$T_A = \text{MIN}$	2.28	2.40		
Input threshold voltage at $f = 10 \text{ kHz}$ (DTC)	Zero duty cycle		2.05	*2.25	V
	Maximum duty cycle	*1.20	1.45		

\*These parameters are not production tested.

† All typical values are at  $T_A = 25^\circ\text{C}$  unless otherwise indicated.

# TL1451A

## DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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### error-amplifier section

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP†	MAX	
Input offset voltage	$V_O$ (FEEDBACK) = 1.25 V	$T_A = 25^\circ\text{C}$		±6	mV
		$T_A = 125^\circ\text{C}$		±10	
		$T_A = \text{MIN}$		±12	
Input offset current	$V_O$ (FEEDBACK) = 1.25 V	$T_A = 25^\circ\text{C}$		±100	nA
		$T_A = 125^\circ\text{C}$		±100	
		$T_A = \text{MIN}$		±200	
Input bias current	$V_O$ (FEEDBACK) = 1.25 V	$T_A = 25^\circ\text{C}$	160	500	nA
		$T_A = 125^\circ\text{C}$	100	500	
		$T_A = \text{MIN}$	142	700	
Common-mode input voltage range	$V_{CC} = 3.6 \text{ V to } 40 \text{ V}$	1.05 to 1.45			V
Open-loop voltage amplification	$R_F = 200 \text{ k}\Omega$	$T_A = 25^\circ\text{C}$	70	80	dB
		$T_A = 125^\circ\text{C}$	70	80	
		$T_A = \text{MIN}$	64	80	
Unity-gain bandwidth			1.5		MHz
Common-mode rejection ratio		60	80		dB
Positive output voltage swing		2			V
Negative output voltage swing				1	V
Output (sink) current (FEEDBACK)	$V_{ID} = -0.1 \text{ V}, V_O = 1.25 \text{ V}$	$T_A = 25^\circ\text{C}$	0.5	1.6	mA
		$T_A = 125^\circ\text{C}$	0.4	1.8	
		$T_A = \text{MIN}$	0.3	1.7	
Output (source) current (FEEDBACK)	$V_{ID} = 0.1 \text{ V}, V_O = 1.25 \text{ V}$	$T_A = 25^\circ\text{C}$	-45	-70	μA
		$T_A = 125^\circ\text{C}$	-25	-50	
		$T_A = \text{MIN}$	-15	-70	

† All typical values are at  $T_A = 25^\circ\text{C}$  unless otherwise indicated.

### output section

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP†	MAX	
Collector off-state current	$V_O = 50 \text{ V}$			10	μA
Output saturation voltage	$T_A = 25^\circ\text{C}$		1.20	2.0	V
	$T_A = 125^\circ\text{C}$		1.60	2.4	
	$T_A = \text{MIN}$		1.36	2.2	
Short-circuit output current	$V_O = 6 \text{ V}$		90		mA

† All typical values are at  $T_A = 25^\circ\text{C}$  unless otherwise indicated.

### pwm comparator section

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP†	MAX	
Input threshold voltage at $f = 10 \text{ kHz}$ (FEEDBACK)	Zero duty cycle		2.05	*2.25	V
	Maximum duty cycle	*1.20	1.45		

\*These parameters are not production tested.

† All typical values are at  $T_A = 25^\circ\text{C}$  unless otherwise indicated.



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## DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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### total device

PARAMETER	TEST CONDITIONS	TL1451AQ, TL1451AM			UNIT
		MIN	TYP†	MAX	
Standby supply current	Off-state		1.3	1.8	mA
Average supply current	$R_T = 10\text{ k}\Omega$		1.7	2.4	mA

† All typical values are at  $T_A = 25^\circ\text{C}$  unless otherwise indicated.

### PARAMETER MEASUREMENT INFORMATION

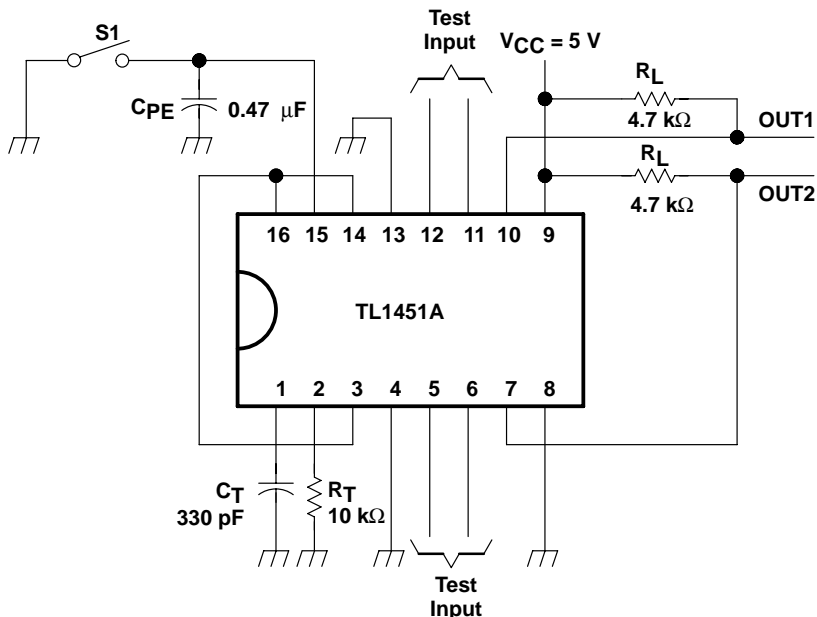
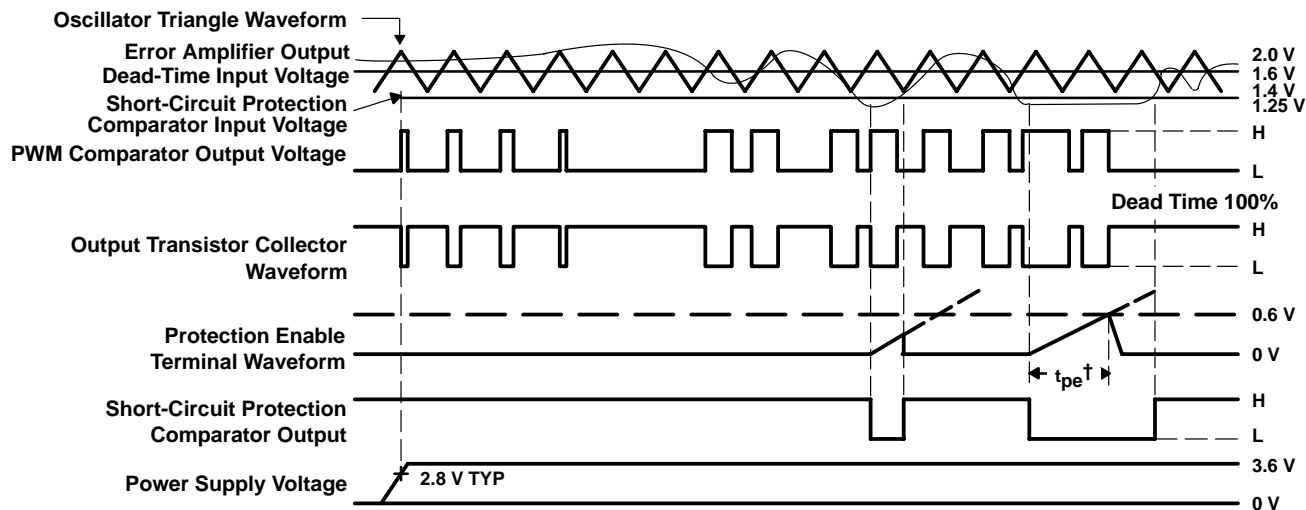


Figure 1. Test Circuit



† Protection Enable Time,  $t_{pe} = (0.051 \times 10^6 \times C_{pe})$  in seconds

Figure 2. TL1451A Timing Diagram

# TL1451A DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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## TYPICAL CHARACTERISTICS

TRIANGLE OSCILLATOR FREQUENCY  
vs  
TIMING RESISTANCE

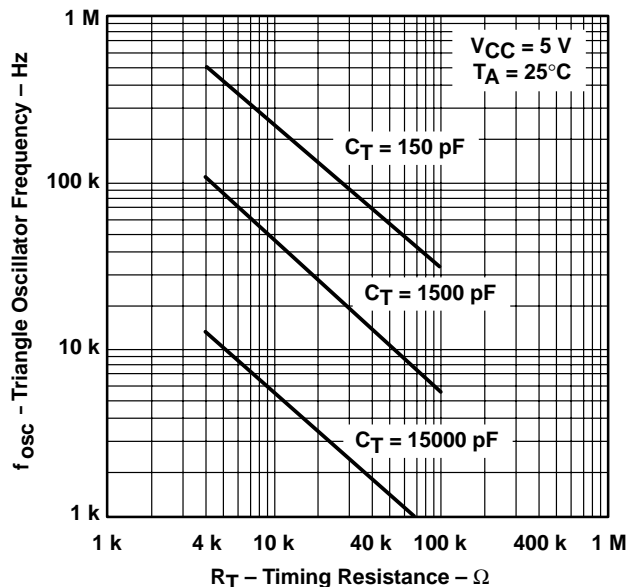


Figure 3

OSCILLATOR FREQUENCY VARIATION  
vs  
FREE-AIR TEMPERATURE

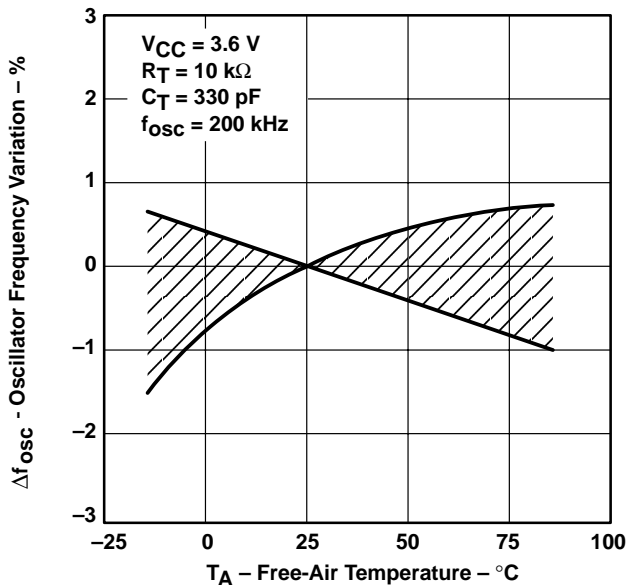


Figure 4

TRIANGLE WAVEFORM SWING VOLTAGE  
vs  
TIMING CAPACITANCE

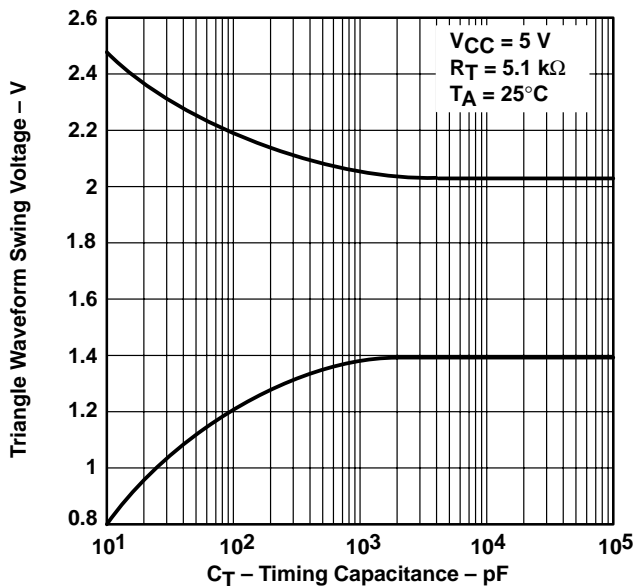


Figure 5

TRIANGLE WAVEFORM PERIOD  
vs  
TIMING CAPACITANCE

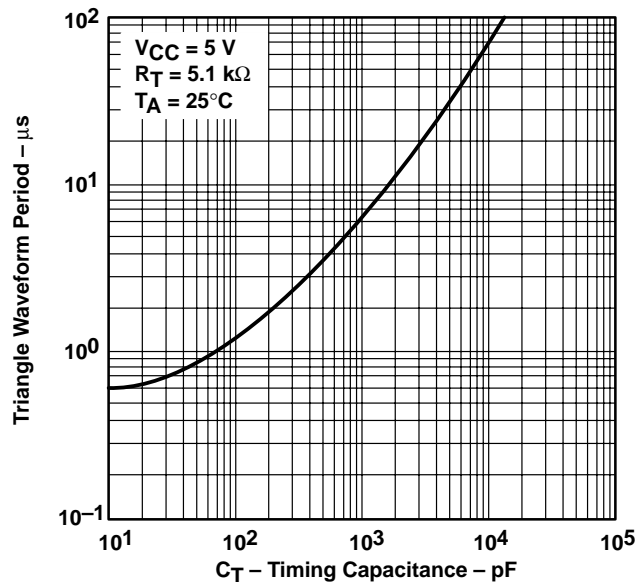
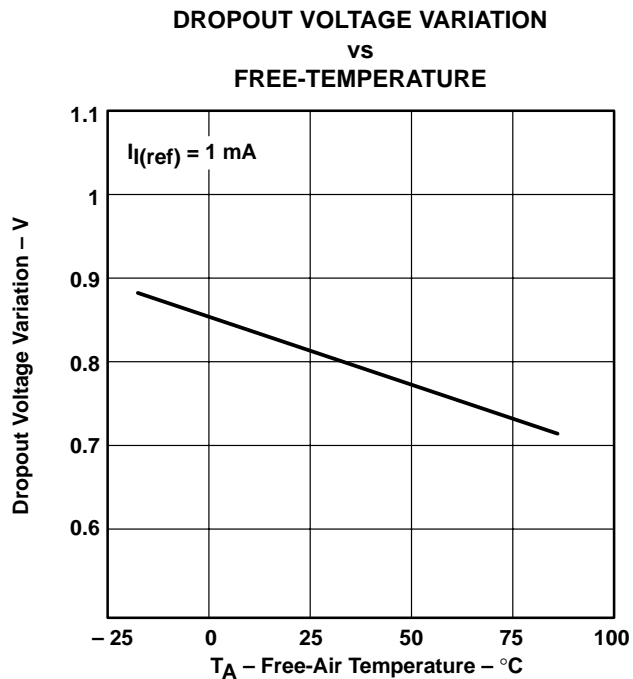
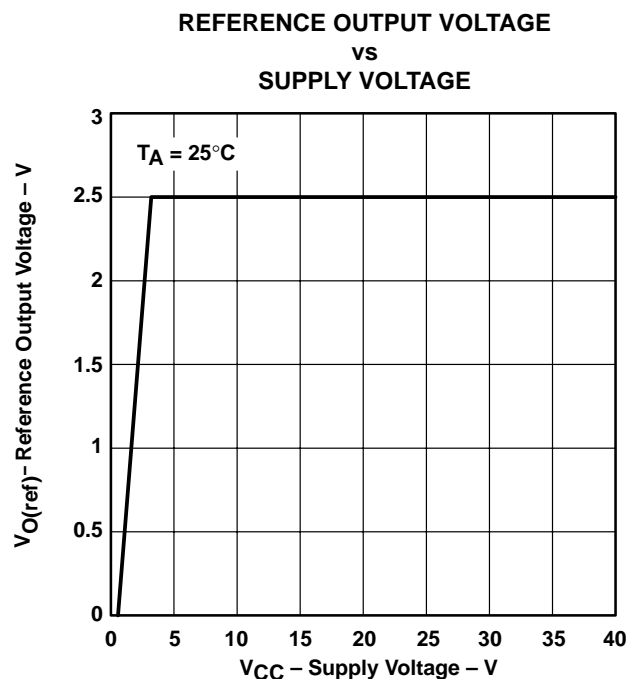
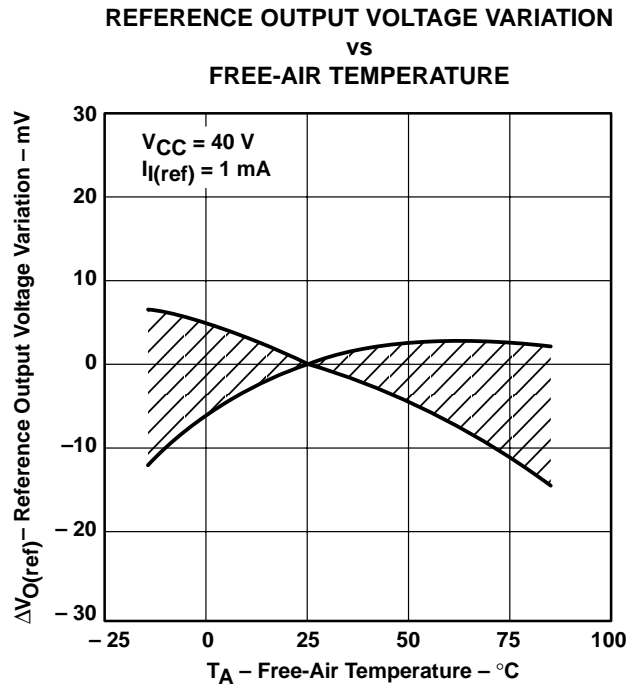
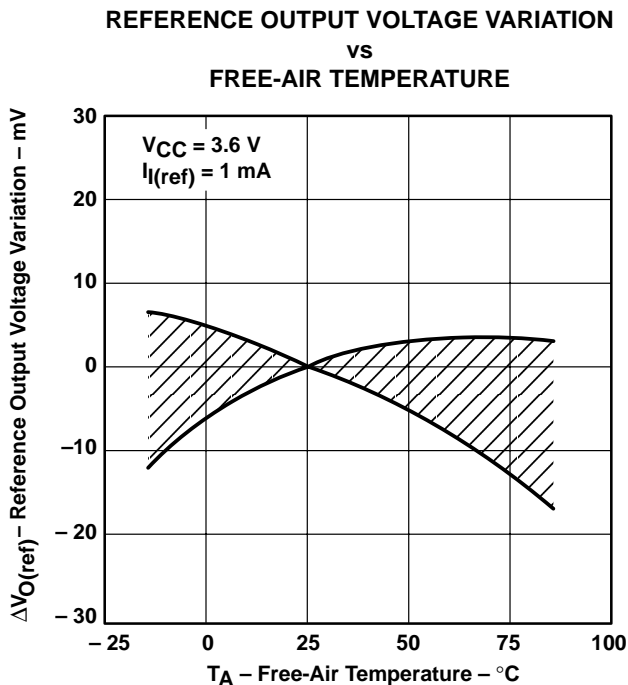


Figure 6

**TYPICAL CHARACTERISTICS**



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## TYPICAL CHARACTERISTICS

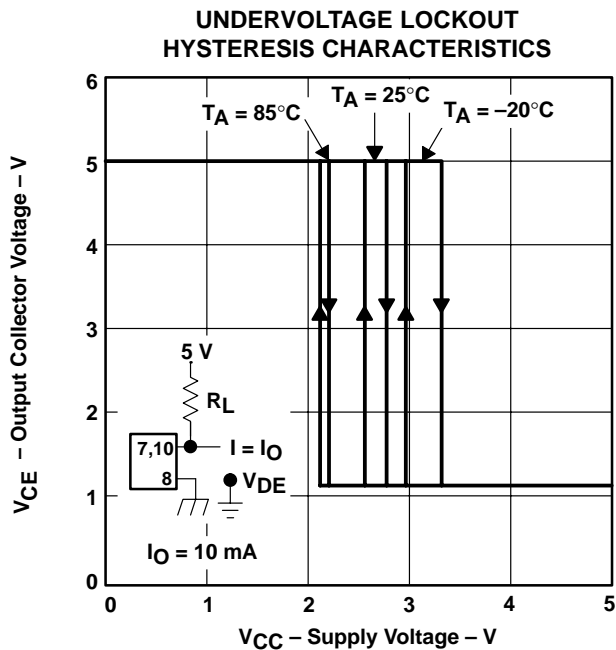


Figure 11

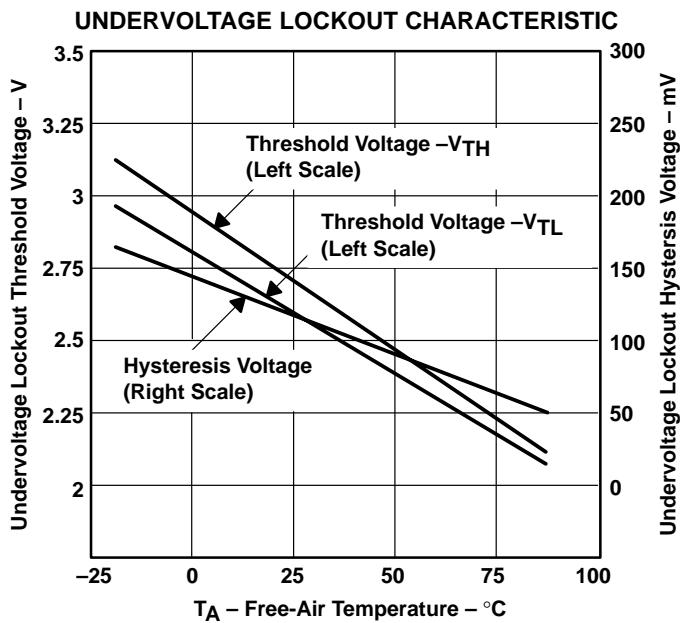


Figure 12

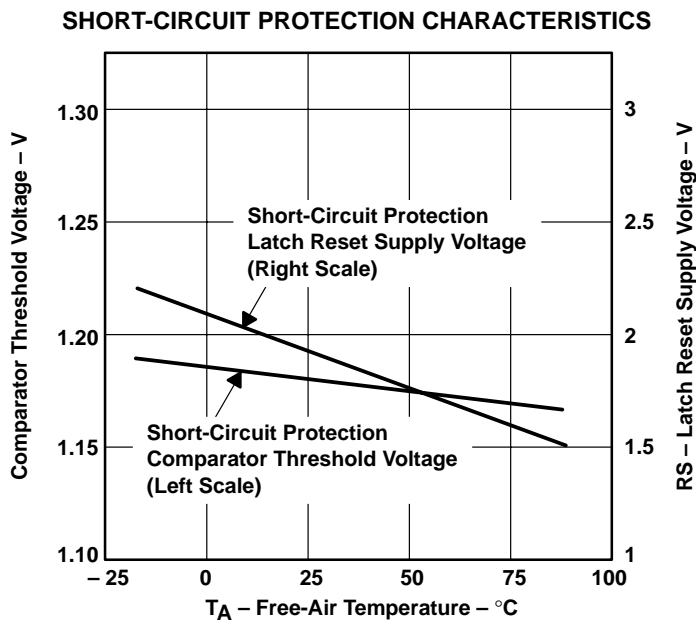
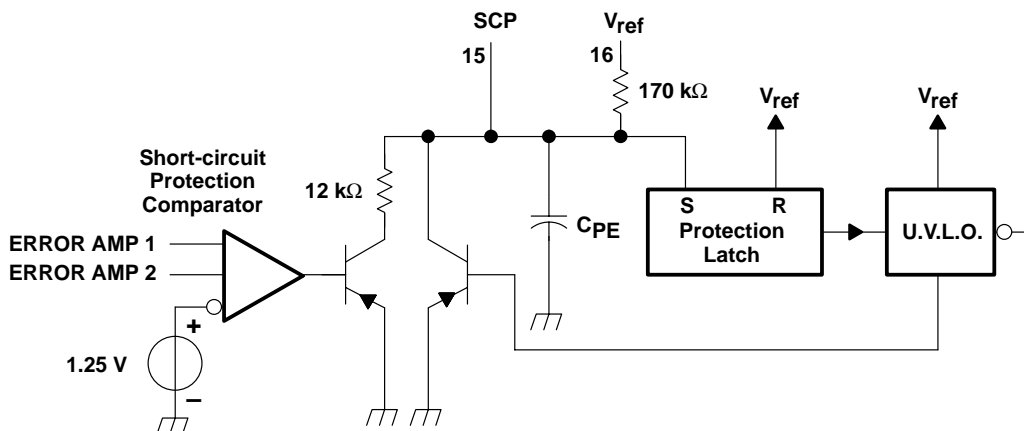
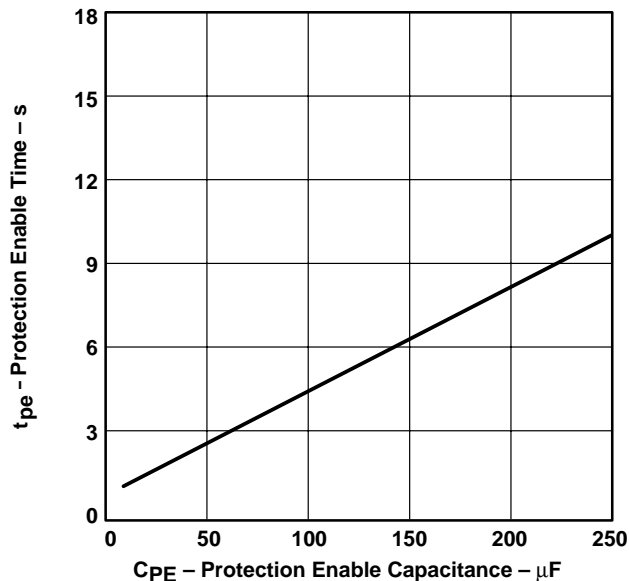


Figure 13

**TYPICAL CHARACTERISTICS**

**PROTECTION ENABLE TIME  
vs  
PROTECTION ENABLE CAPACITANCE**



**Figure 14**

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## DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

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### TYPICAL CHARACTERISTICS

**ERROR AMP MAXIMUM OUTPUT VOLTAGE SWING**  
vs  
**FREQUENCY**

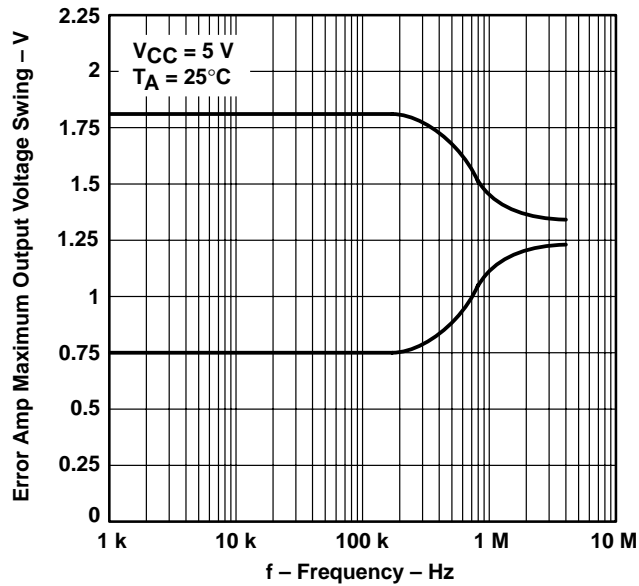


Figure 15

**OPEN-LOOP VOLTAGE AMPLIFICATION**  
vs  
**FREQUENCY**

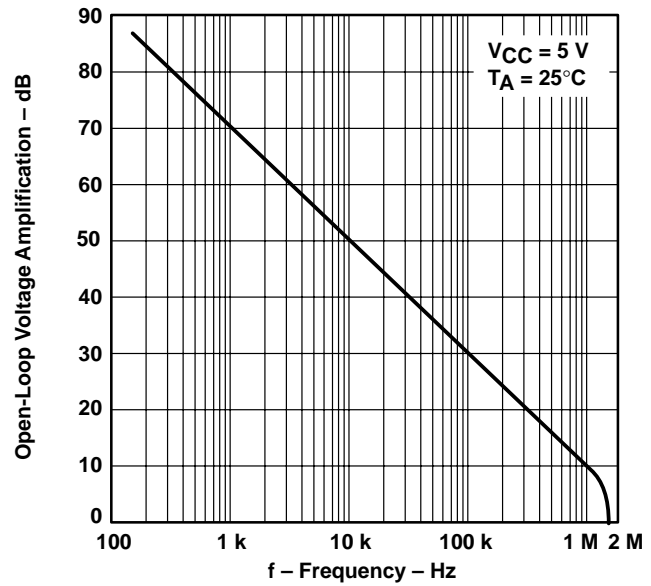


Figure 16

**GAIN (AMPLIFIER IN**  
**UNITY-GAIN CONFIGURATION)**  
vs  
**FREQUENCY**

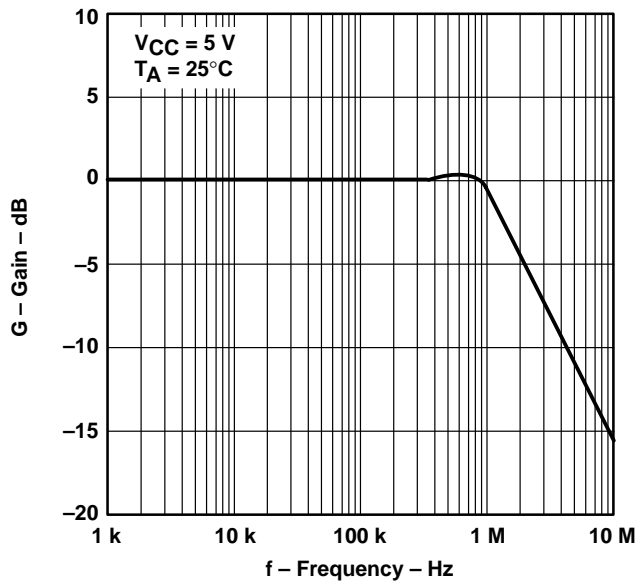
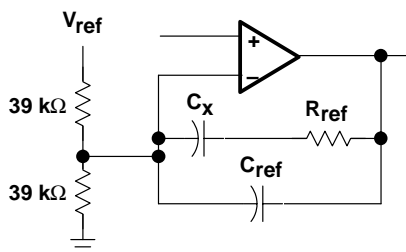
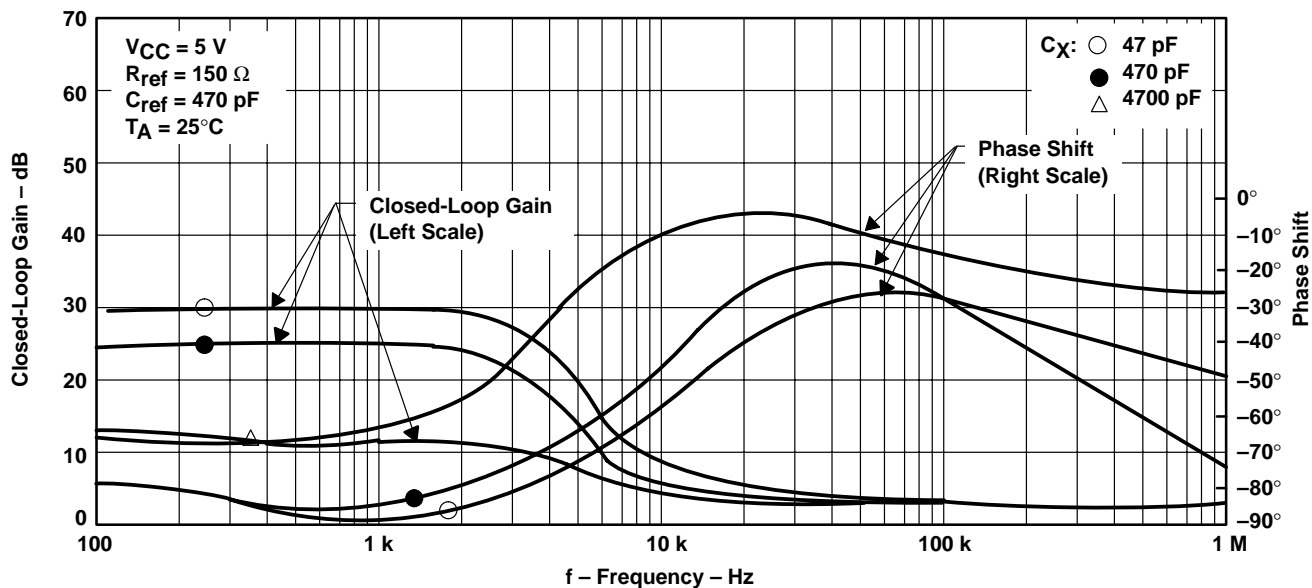


Figure 17

## TYPICAL CHARACTERISTICS

### CLOSED-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



Test Circuit

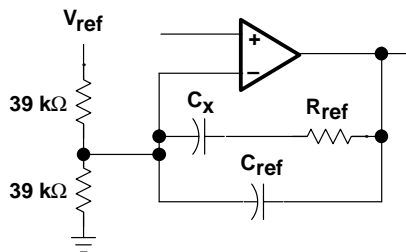
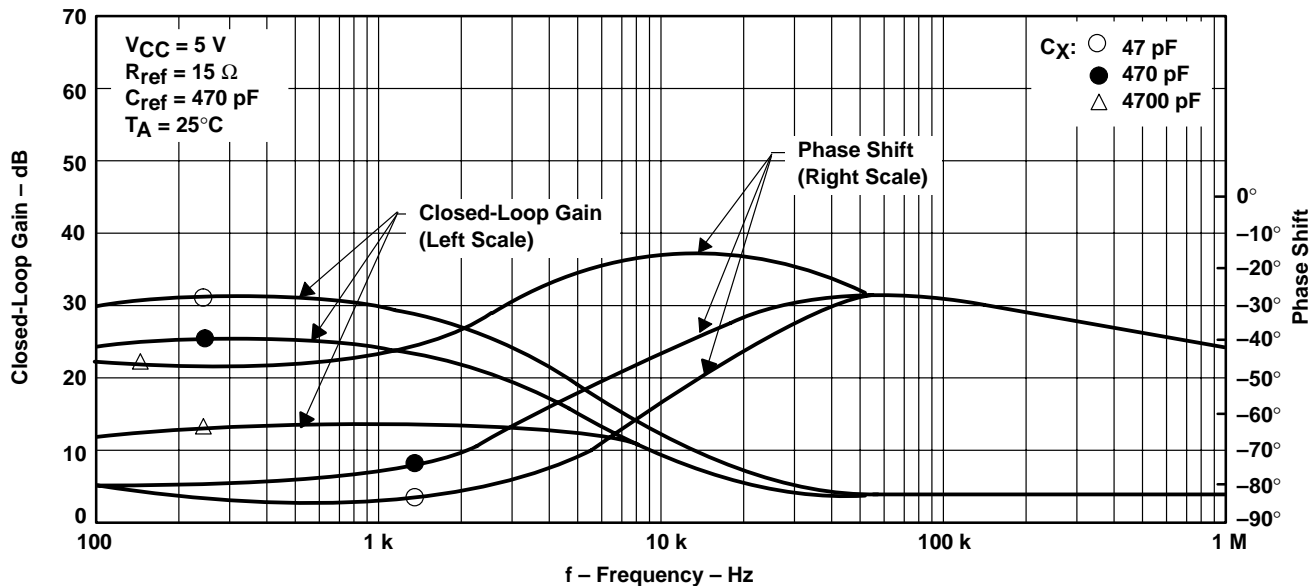
Figure 18

# TL1451A DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS024E – FEBRUARY 1983 – REVISED NOVEMBER 1999

## TYPICAL CHARACTERISTICS

### CLOSED-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



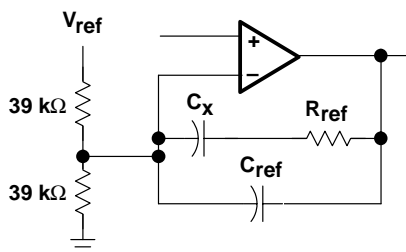
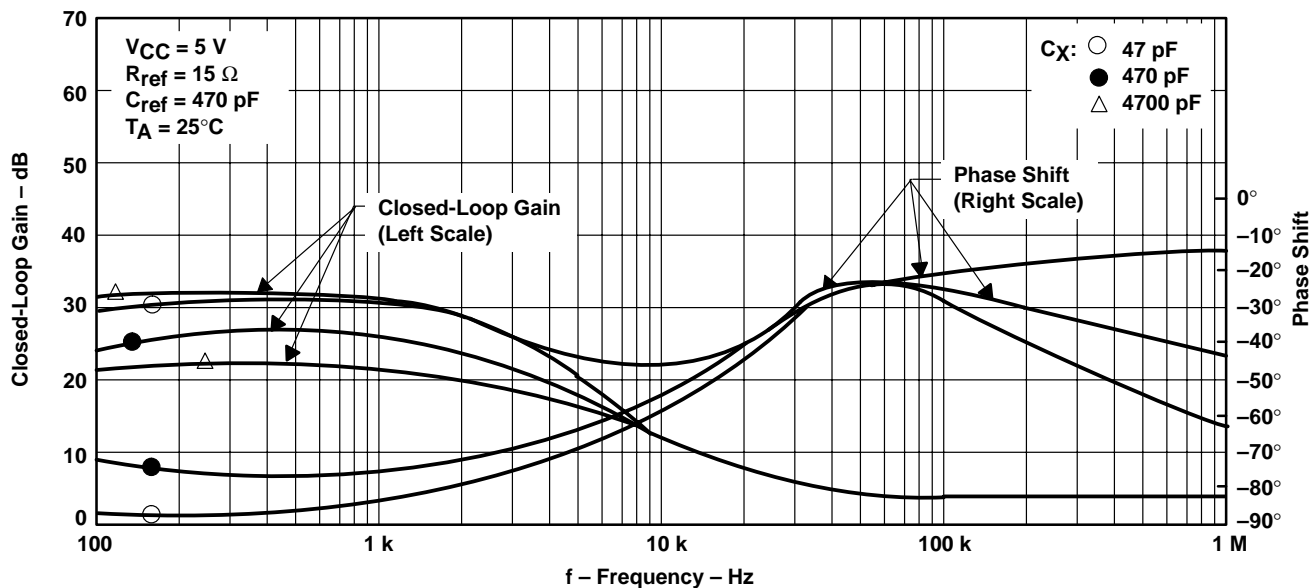
Test Circuit

Figure 19



## TYPICAL CHARACTERISTICS

### CLOSED-LOOP GAIN AND PHASE SHIFT VS FREQUENCY



Test Circuit

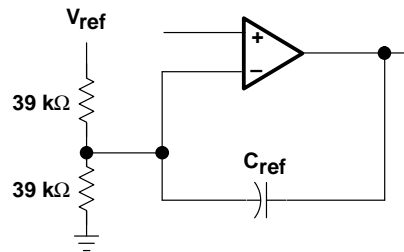
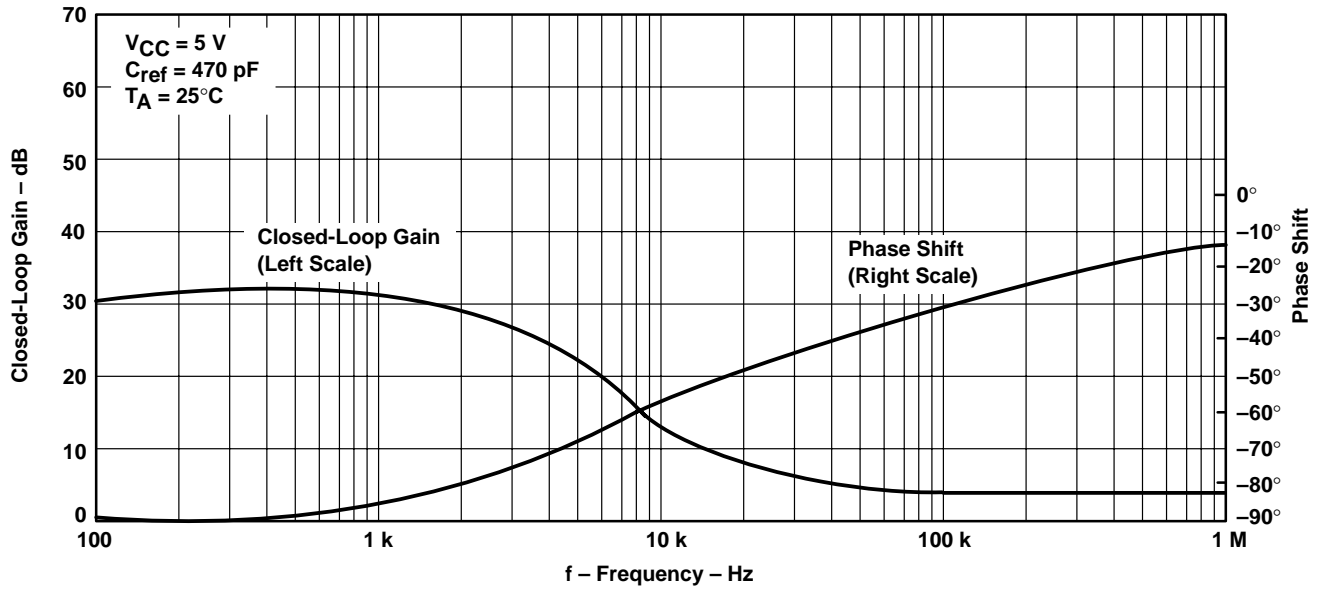
Figure 20

# TL1451A DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS024E – FEBRUARY 1983 – REVISED NOVEMBER 1999

## TYPICAL CHARACTERISTICS

### CLOSED-LOOP GAIN AND PHASE SHIFT vs FREQUENCY



Test Circuit

Figure 21

**TYPICAL CHARACTERISTICS**

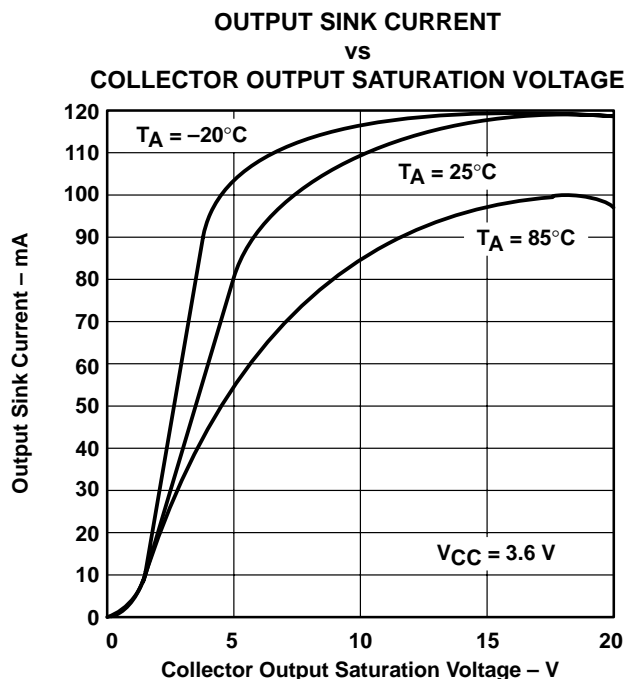
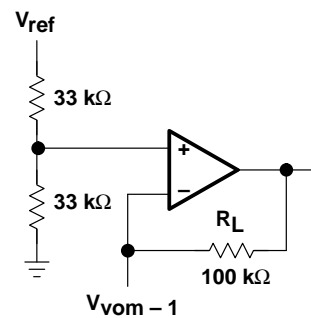
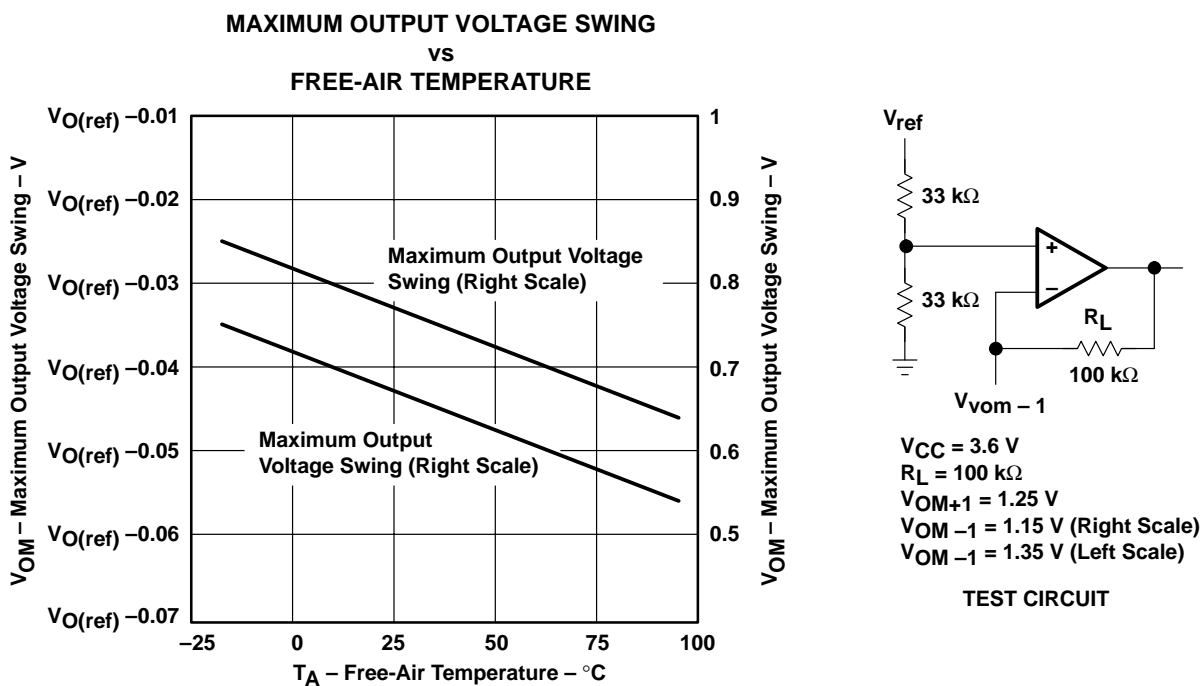


Figure 22



$V_{CC} = 3.6\text{ V}$   
 $R_L = 100\text{ k}\Omega$   
 $V_{\text{OM}+1} = 1.25\text{ V}$   
 $V_{\text{OM} - 1} = 1.15\text{ V}$  (Right Scale)  
 $V_{\text{OM} - 1} = 1.35\text{ V}$  (Left Scale)

TEST CIRCUIT

Figure 23

# TL1451A DUAL PULSE-WIDTH-MODULATION CONTROL CIRCUITS

SLVS024E – FEBRUARY 1983 – REVISED NOVEMBER 1999

## TYPICAL CHARACTERISTICS

OUTPUT TRANSISTOR ON DUTY CYCLE  
vs  
DEAD-TIME INPUT VOLTAGE

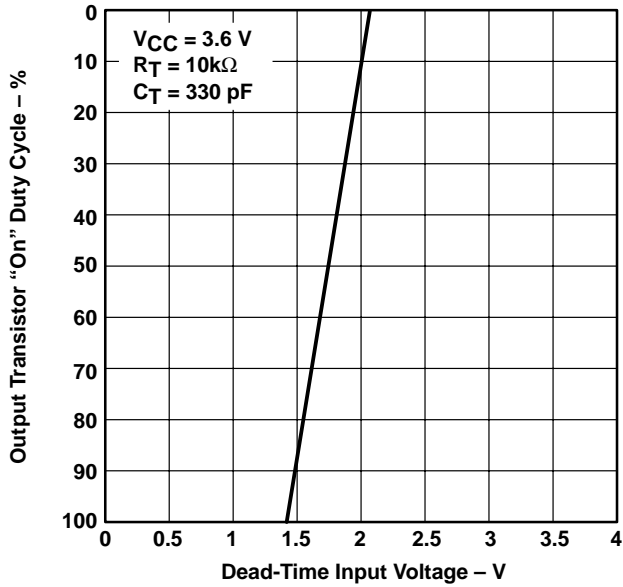


Figure 24

STANDBY CURRENT  
vs  
SUPPLY VOLTAGE

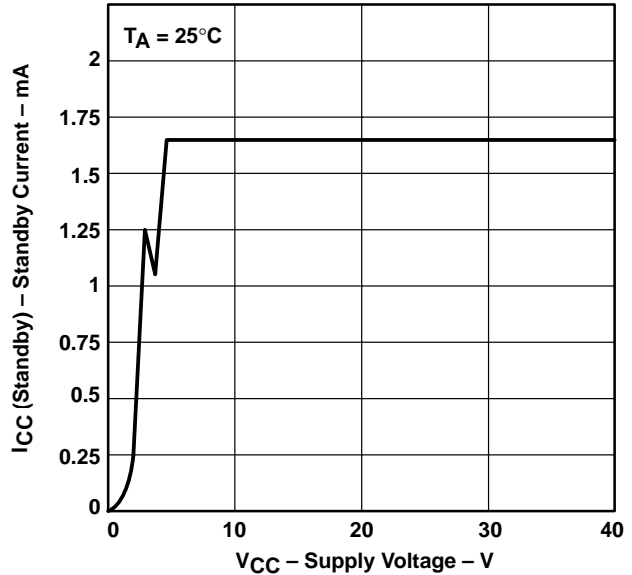


Figure 25

STANDBY CURRENT  
vs  
FREE-AIR TEMPERATURE

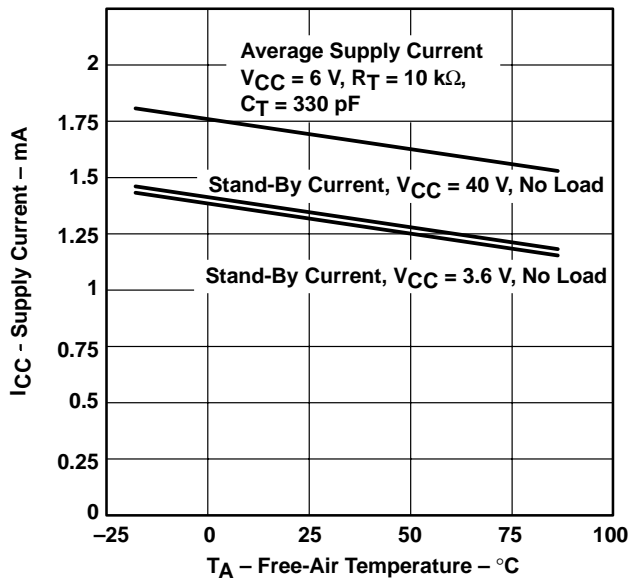


Figure 26

MAXIMUM CONTINUOUS POWER DISSIPATION  
vs  
FREE-AIR TEMPERATURE

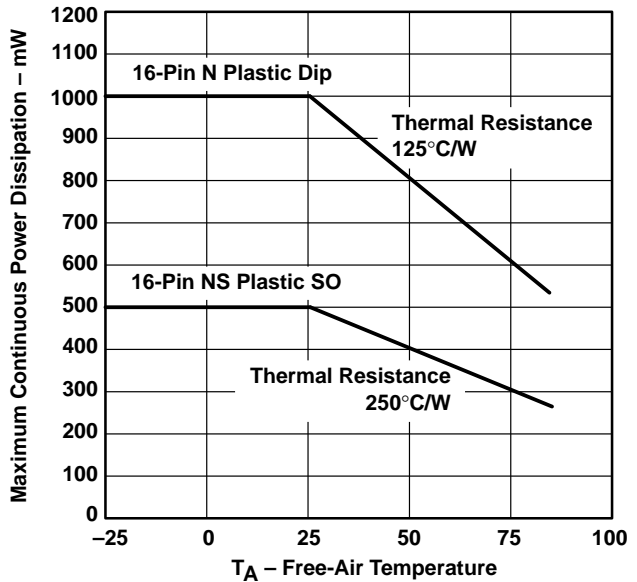
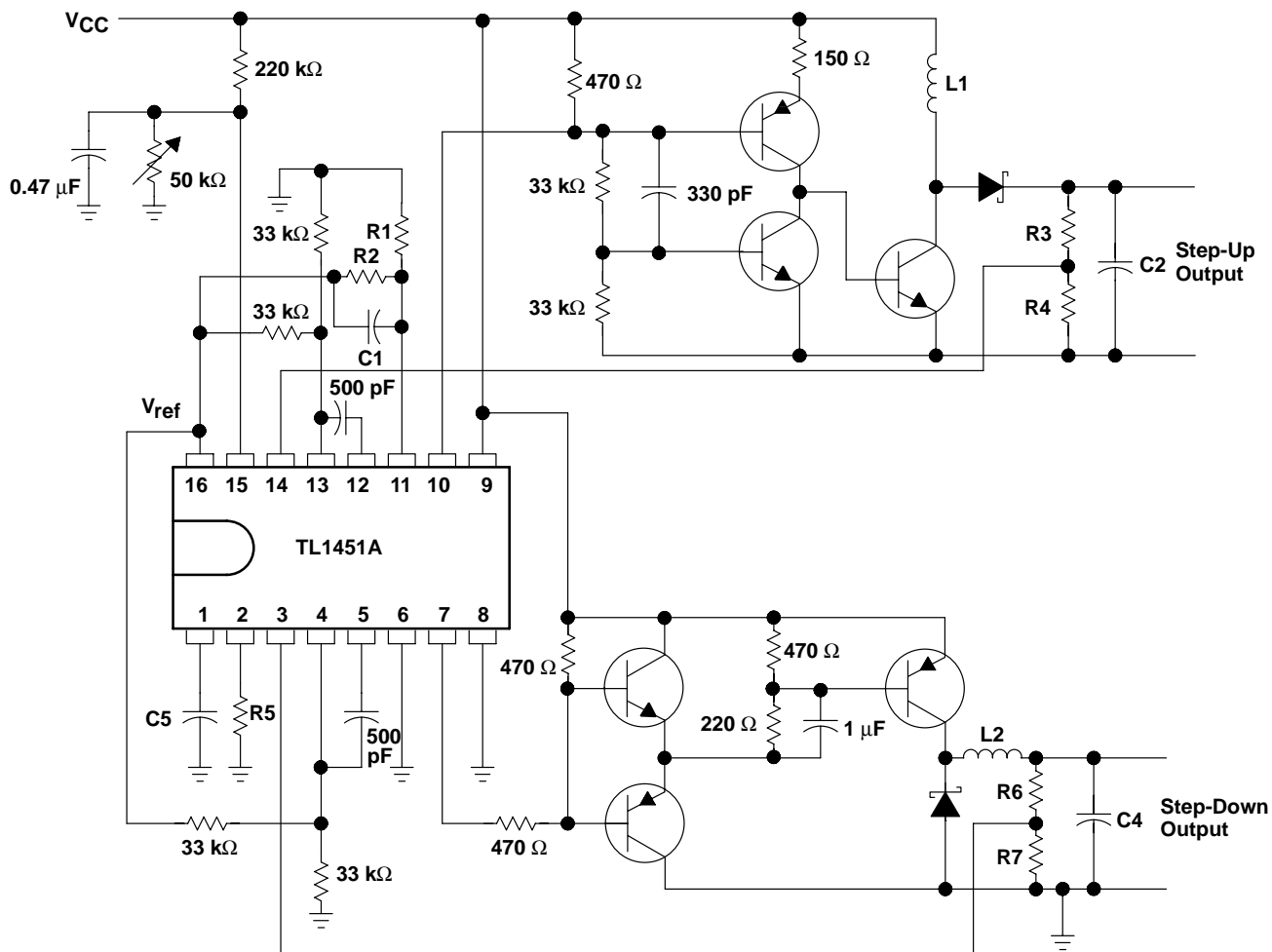


Figure 27

## APPLICATION INFORMATION



NOTE A: Values for R1 through R7, C1 through C4, and L1 and L2 depend upon individual application.

**Figure 28. High-Speed Dual Switching Regulator**

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
5962-9958401Q2A	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		
5962-9958401QEA	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
TL1451ACD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	TL1451AC	<a href="#">Samples</a>
TL1451ACDBLE	NRND	SSOP	DB	16		TBD	Call TI	Call TI	-20 to 85		
TL1451ACDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	T1451A	<a href="#">Samples</a>
TL1451ACDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	T1451A	<a href="#">Samples</a>
TL1451ACDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	TL1451AC	<a href="#">Samples</a>
TL1451ACDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	TL1451AC	<a href="#">Samples</a>
TL1451ACDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	TL1451AC	<a href="#">Samples</a>
TL1451ACN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-20 to 85	TL1451ACN	<a href="#">Samples</a>
TL1451ACNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	-20 to 85	TL1451ACN	<a href="#">Samples</a>
TL1451ACNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	TL1451A	<a href="#">Samples</a>
TL1451ACNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	TL1451A	<a href="#">Samples</a>
TL1451ACPW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	T1451A	<a href="#">Samples</a>
TL1451ACPWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	T1451A	<a href="#">Samples</a>
TL1451ACPWLE	OBSOLETE	TSSOP	PW	16		TBD	Call TI	Call TI	-20 to 85		
TL1451ACPWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	T1451A	<a href="#">Samples</a>
TL1451ACPWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-20 to 85	T1451A	<a href="#">Samples</a>
TL1451AMFKB	OBSOLETE	LCCC	FK	20		TBD	Call TI	Call TI	-55 to 125		

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
TL1451AMJB	OBSOLETE	CDIP	J	16		TBD	Call TI	Call TI	-55 to 125		
TL1451AQD	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1451AQ	<a href="#">Samples</a>
TL1451AQDG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1451AQ	<a href="#">Samples</a>
TL1451AQDR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	TL1451AQ	<a href="#">Samples</a>
TL1451AQDRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		1451AQ	<a href="#">Samples</a>
TL1451CDBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		T1451	<a href="#">Samples</a>
TL1451CDBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		T1451	<a href="#">Samples</a>
TL1451CN	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TL1451CN	<a href="#">Samples</a>
TL1451CNE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type		TL1451CN	<a href="#">Samples</a>
TL1451CNS	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TL1451	<a href="#">Samples</a>
TL1451CNSG4	ACTIVE	SO	NS	16	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TL1451	<a href="#">Samples</a>
TL1451CNSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TL1451	<a href="#">Samples</a>
TL1451CNSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TL1451	<a href="#">Samples</a>
TL1451INSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TL1451I	<a href="#">Samples</a>
TL1451INSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		TL1451I	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

#### **OTHER QUALIFIED VERSIONS OF TL1451A, TL1451AM :**

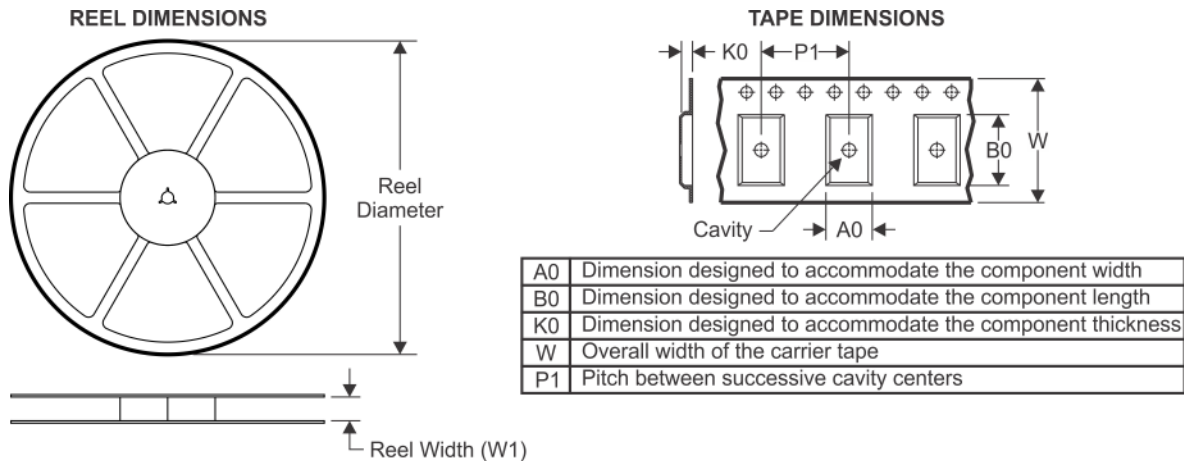
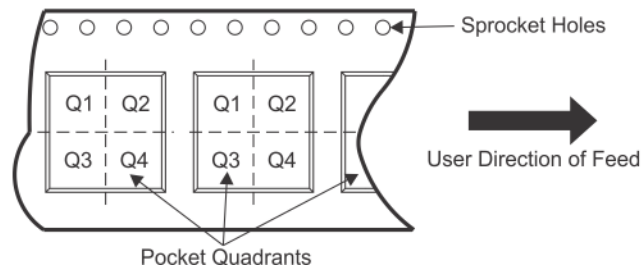
- Catalog: [TL1451A](#)
  
- Automotive: [TL1451A-Q1](#), [TL1451A-Q1](#)
  
- Enhanced Product: [TL1451A-EP](#), [TL1451A-EP](#)
  
- Military: [TL1451AM](#)

#### **NOTE: Qualified Version Definitions:**

- Catalog - TI's standard catalog product
  
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
  
- Enhanced Product - Supports Defense, Aerospace and Medical Applications



- Military - QML certified for Military and Defense Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TL1451ACDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL1451ACDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL1451ACDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL1451ACNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL1451ACPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TL1451AQDR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL1451AQDRG4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TL1451CDBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
TL1451CNSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TL1451INSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

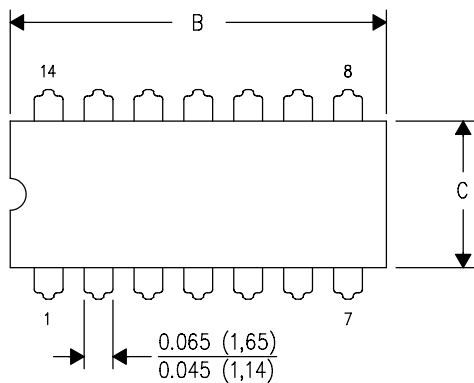

\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TL1451ACDBR	SSOP	DB	16	2000	367.0	367.0	38.0
TL1451ACDR	SOIC	D	16	2500	333.2	345.9	28.6
TL1451ACDR	SOIC	D	16	2500	367.0	367.0	38.0
TL1451ACNSR	SO	NS	16	2000	367.0	367.0	38.0
TL1451ACPWR	TSSOP	PW	16	2000	367.0	367.0	35.0
TL1451AQDR	SOIC	D	16	2500	367.0	367.0	38.0
TL1451AQDRG4	SOIC	D	16	2500	367.0	367.0	38.0
TL1451CDBR	SSOP	DB	16	2000	367.0	367.0	38.0
TL1451CNSR	SO	NS	16	2000	367.0	367.0	38.0
TL1451INSR	SO	NS	16	2000	367.0	367.0	38.0

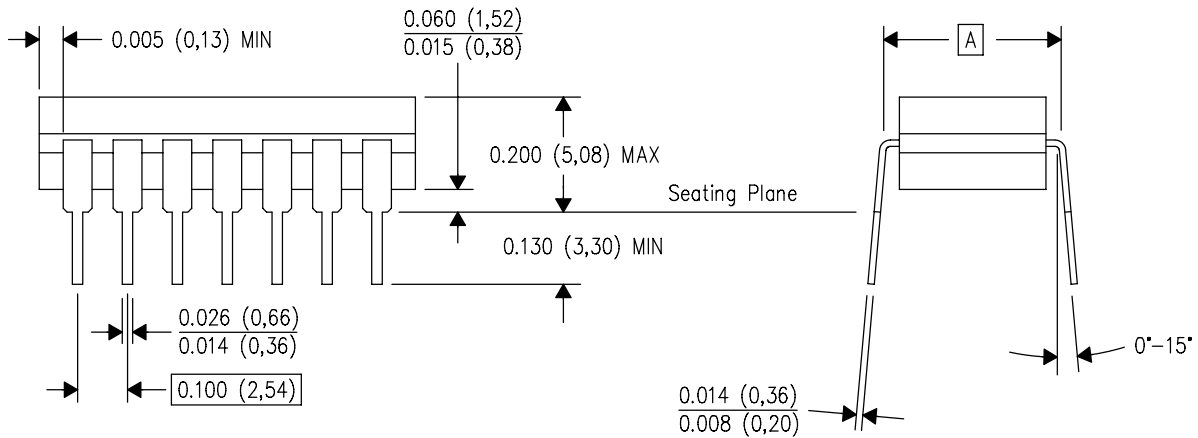
J (R-GDIP-T\*\*)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



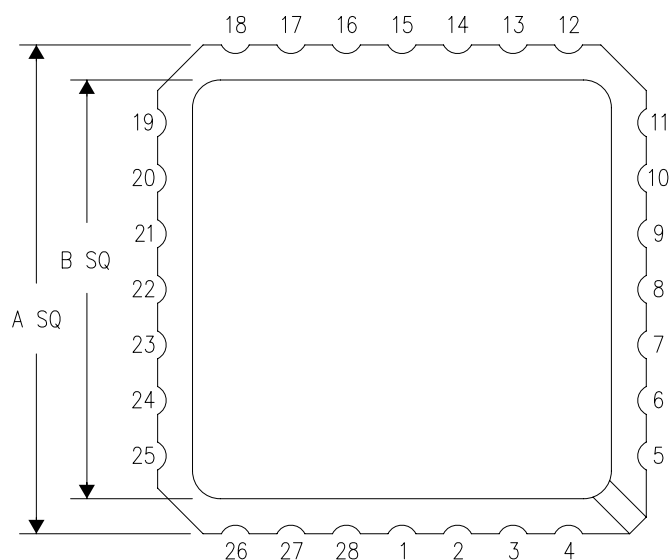
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

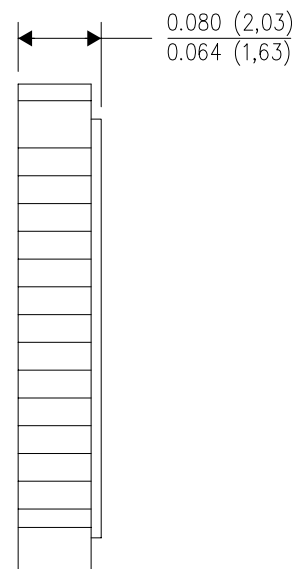
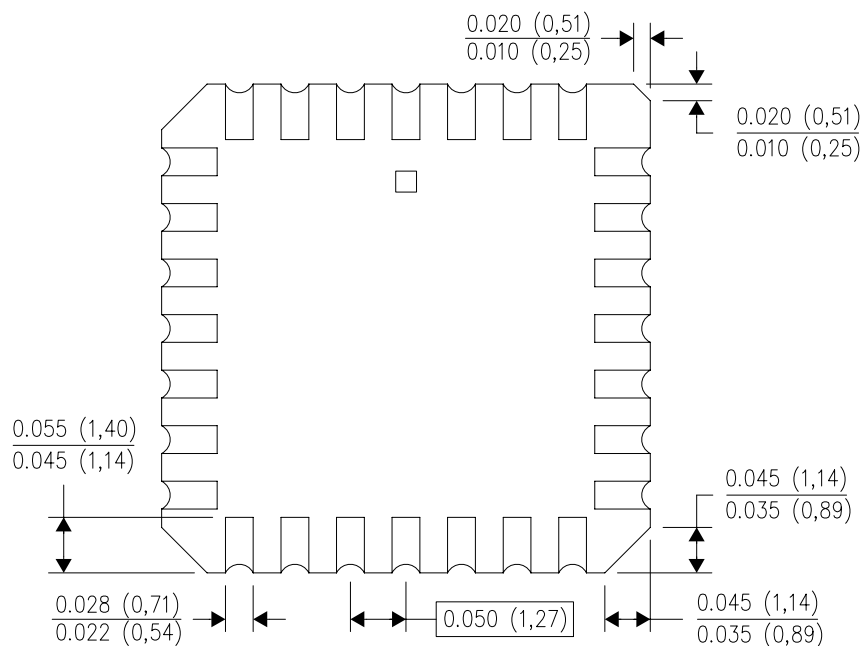
FK (S-CQCC-N\*\*)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



NO. OF TERMINALS **	A		B	
	MIN	MAX	MIN	MAX
20	0.342 (8,69)	0.358 (9,09)	0.307 (7,80)	0.358 (9,09)
28	0.442 (11,23)	0.458 (11,63)	0.406 (10,31)	0.458 (11,63)
44	0.640 (16,26)	0.660 (16,76)	0.495 (12,58)	0.560 (14,22)
52	0.740 (18,78)	0.761 (19,32)	0.495 (12,58)	0.560 (14,22)
68	0.938 (23,83)	0.962 (24,43)	0.850 (21,6)	0.858 (21,8)
84	1.141 (28,99)	1.165 (29,59)	1.047 (26,6)	1.063 (27,0)



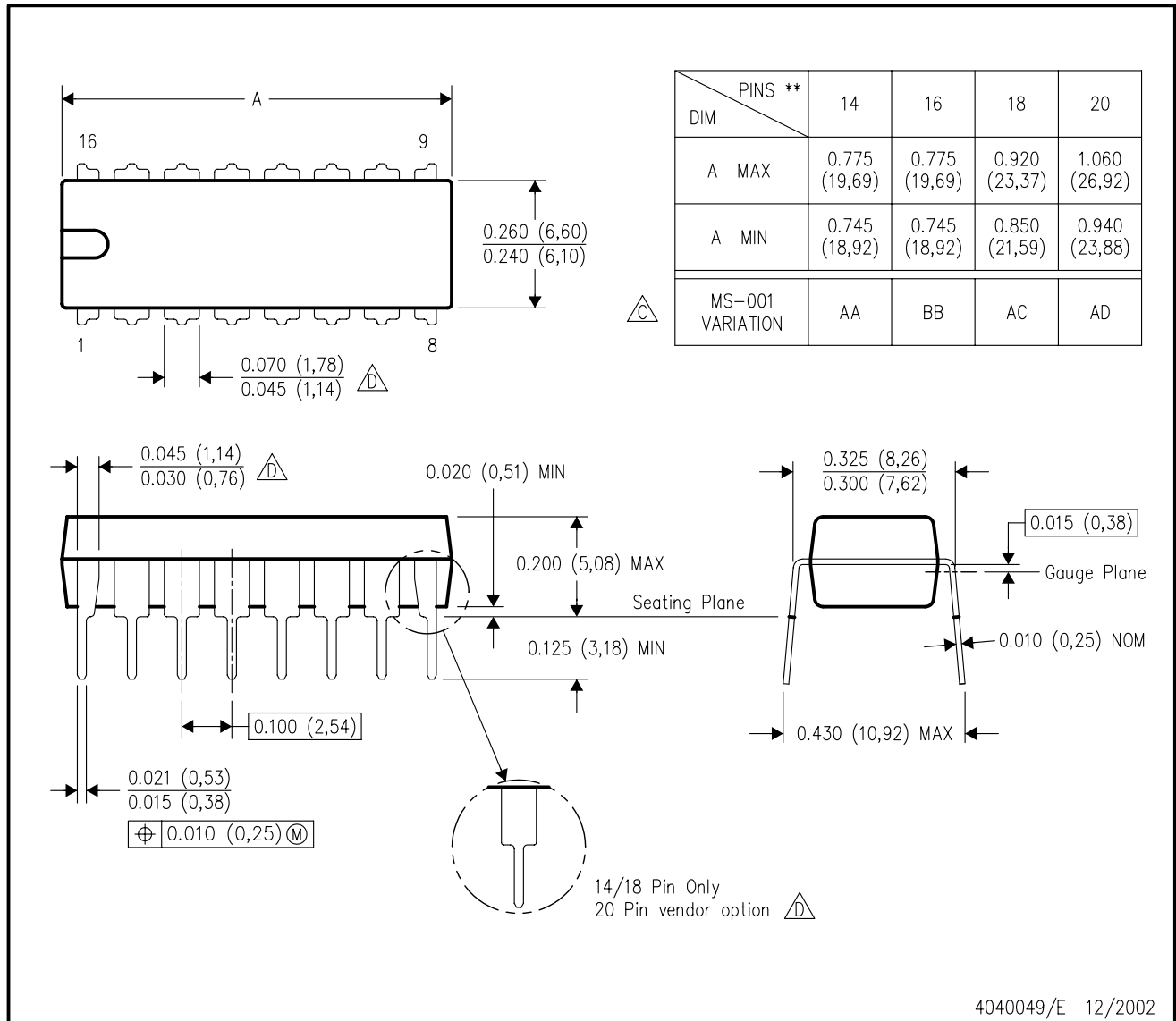
4040140/D 01/11

- NOTES:
- All linear dimensions are in inches (millimeters).
  - This drawing is subject to change without notice.
  - This package can be hermetically sealed with a metal lid.
  - Falls within JEDEC MS-004

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

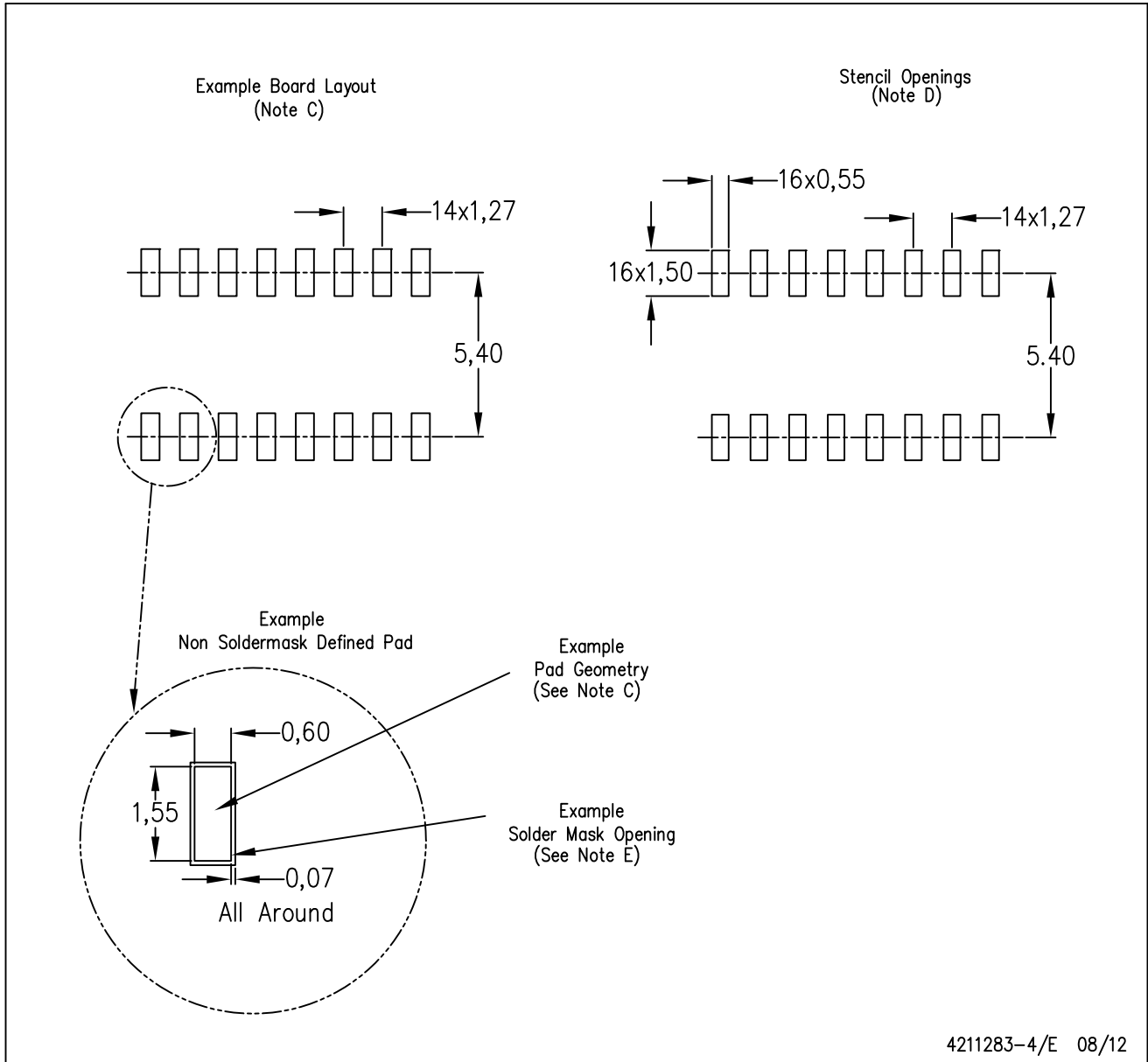


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



D (R-PDSO-G16)

PLASTIC SMALL OUTLINE

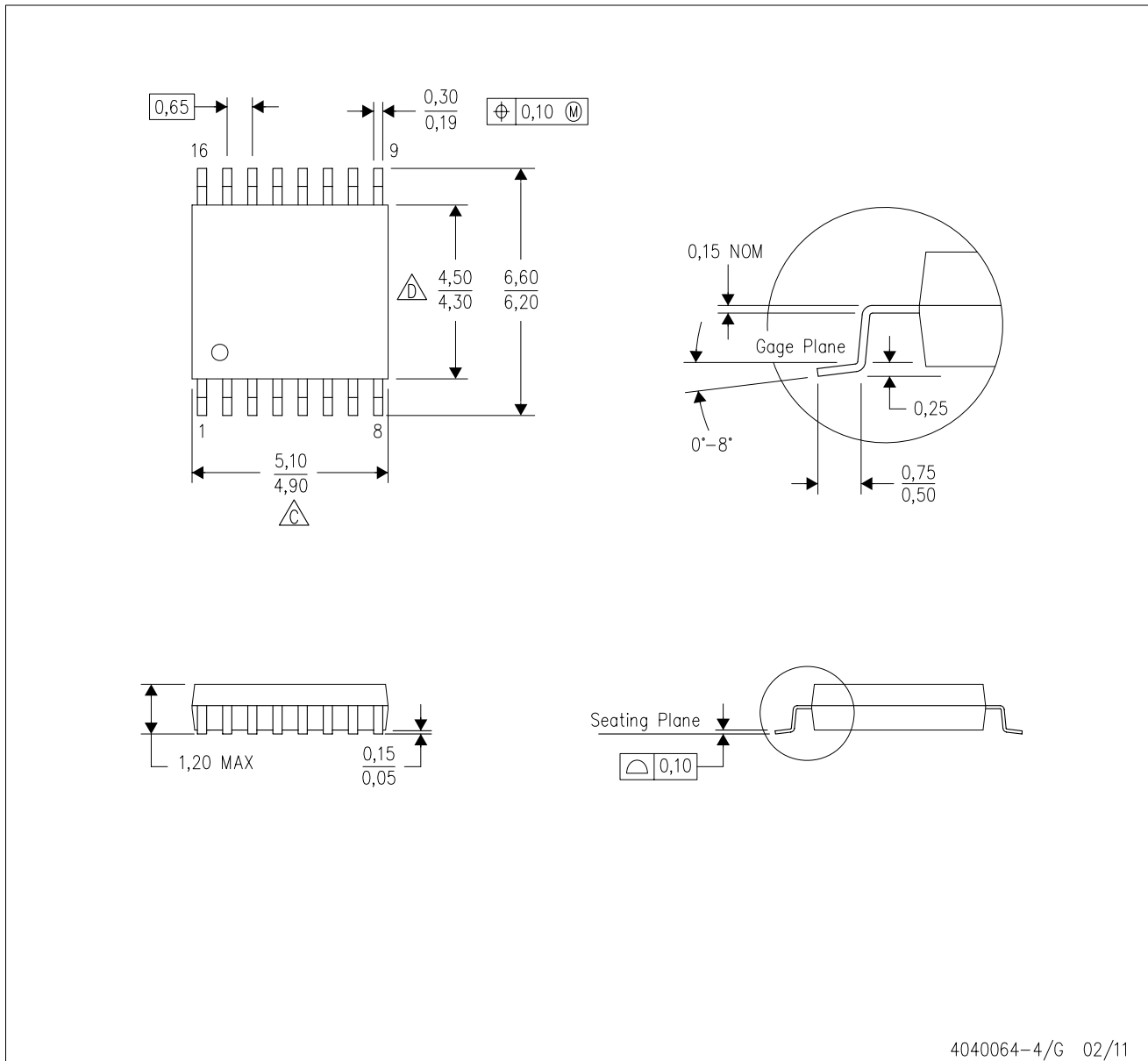


- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.



PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

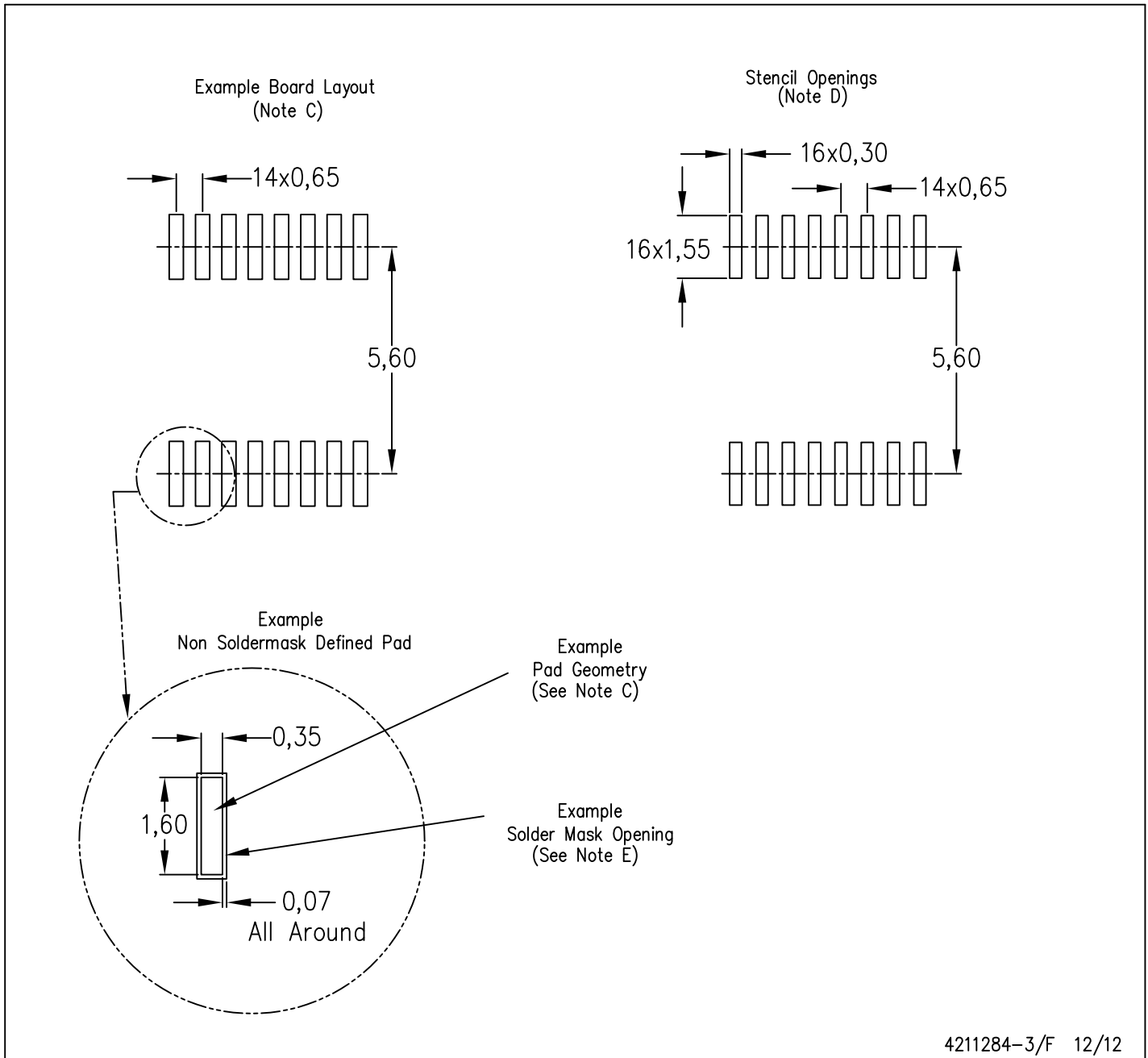


4040064-4/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

PW (R-PDSO-G16)

PLASTIC SMALL OUTLINE

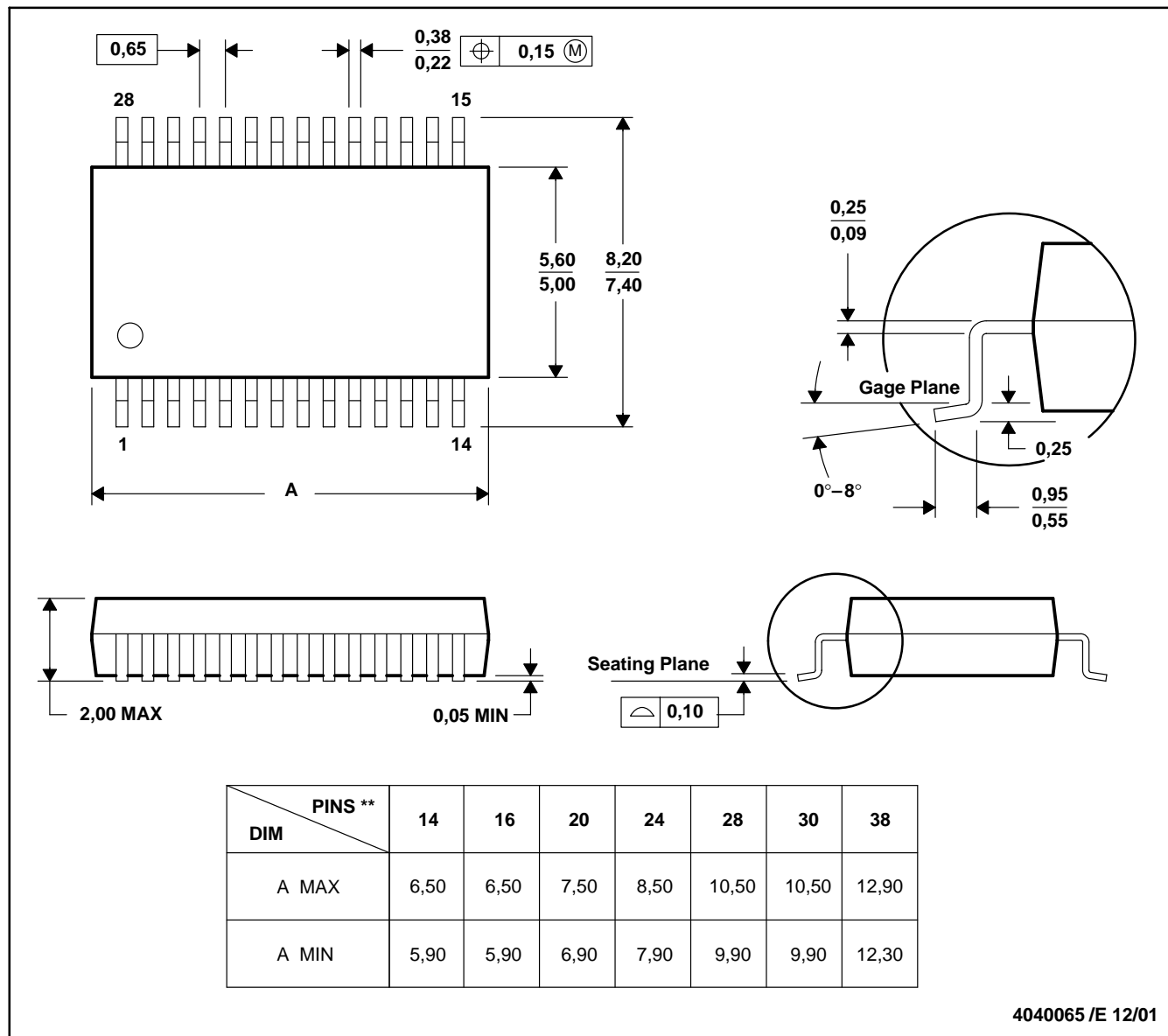


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Publication IPC-7351 is recommended for alternate designs.
  - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
  - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



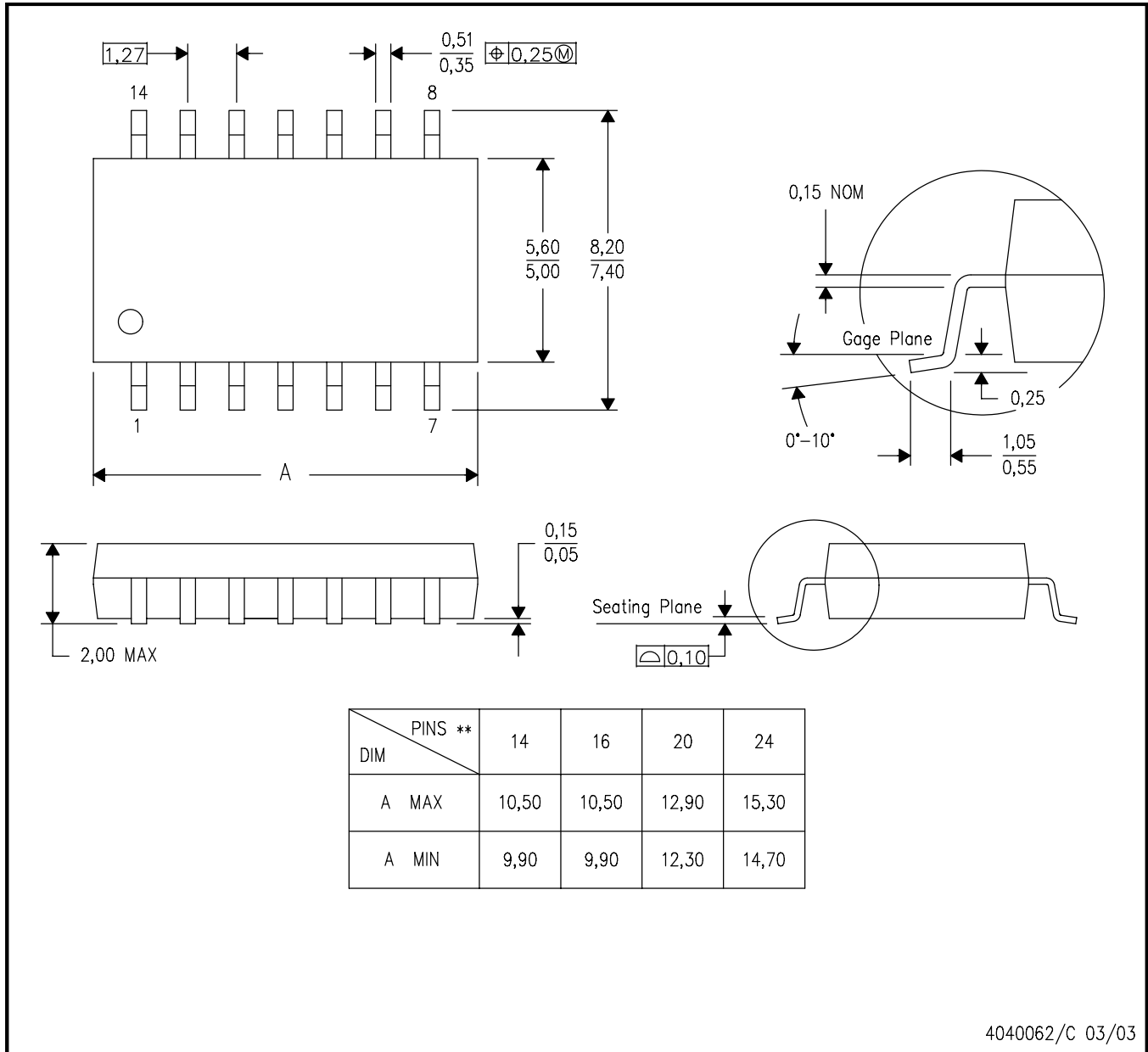
- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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