Product Summary

Device	BV_{DSS}	$R_{DS(ON)}$ Max	I_D Max T_A = +25°C (Note 6 & 8)
Q1	40V	25mΩ @ V_{GS} = 10V	7.5A
		40mΩ @ V_{GS} = 4.5V	6.2A
Q2	-40V	25mΩ @ V_{GS} = -10V	-7.3A
		45mΩ @ V_{GS} = -4.5V	-5.7A

Features and Benefits

- Reduced Footprint with Two Discrete Devices in Single SO-8
- Low On-Resistance
- Fast Switching Speed
- Low Input/Output Leakage
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **The DMC4040SSDQ is suitable for automotive applications requiring specific change control; this part is AEC-Q101 qualified, PPAP capable, and manufactured in IATF16949 certified facilities.**
  https://www.diodes.com/quality/product-definitions/

Description and Applications

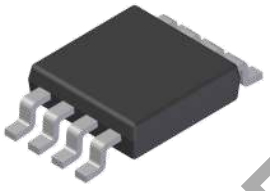
This MOSFET has been designed to ensure that $R_{DS(ON)}$ of N and P channel FET are matched to minimize losses in both arms of the bridge. The DIODES™ DMC4040SSDQ is optimized for use in 3 phases brushless DC motor circuits (BLDC) and CCFL backlighting.

- 3 phases BLDC motors
- CCFL backlighting

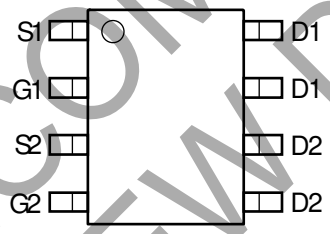
Mechanical Data

- Package: SO-8
- Package Material: Molded Plastic, "Green" Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals Connections: See Diagram Below
- Terminals: Finish – Matte Tin Annealed over Copper Lead Frame. Solderable per MIL-STD-202, Method 208 e3
- Weight: 0.074 grams (Approximate)

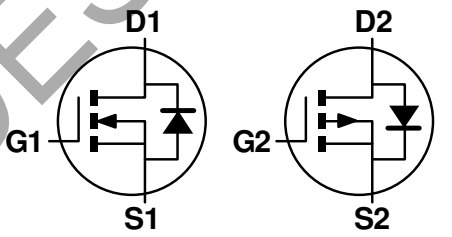
SO-8



Top View



Top View



Q1 N-Channel Q2 P-Channel

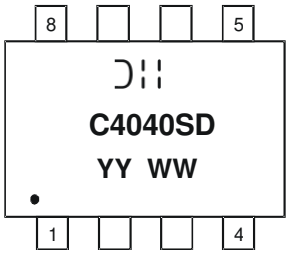
Equivalent Circuit

Ordering Information (Note 4)

Part Number	Package	Packing	
		Qty.	Carrier
DMC4040SSDQ-13	SO-8	2,500	Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
2. See https://www.diodes.com/quality/lead-free/ for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at https://www.diodes.com/design/support/packaging/diodes-packaging/.

Marking Information



= Manufacturer's Marking
C4040SD = Product Type Marking Code
YYWW = Date Code Marking
YY = Year (ex: 22 = 2022)
WW = Week (01 to 53)

Maximum Ratings (@T_A = +25°C, unless otherwise specified.)

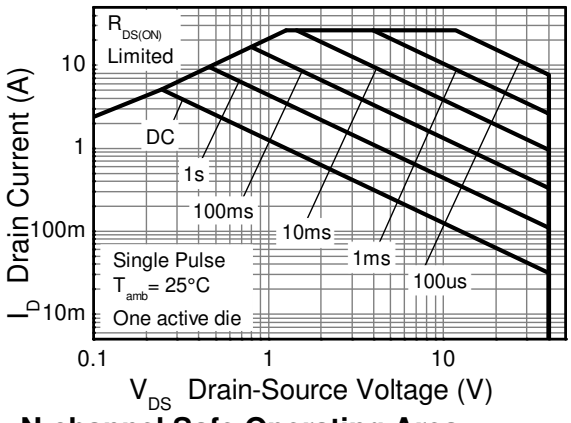
Characteristic			Symbol	N-Channel - Q1	P-Channel - Q2	Units
Drain-Source Voltage			V_{DSS}	40	-40	V
Gate-Source Voltage			V_{GSS}	±20	±20	V
Continuous Drain Current	V_{GS} = 10V	(Notes 6 & 8)	I_D	7.5	-7.5	A
		T_A = +70°C (Notes 6 & 8)		5.8	-5.8	
		(Notes 5 & 8)		5.7	-5.7	
		(Notes 5 & 9)		6.8	-6.8	
Pulsed Drain Current	V_{GS} = 10V	(Notes 7 & 8)	I_{DM}	29.0	-29.0	A
Continuous Source Current (Body Diode)		(Notes 6 & 8)	I_S	3.0	-3.0	A
Pulsed Source Current (Body Diode)		(Notes 7 & 8)	I_{SM}	29.0	-29.0	A

Thermal Characteristics (@T_A = +25°C, unless otherwise specified.)

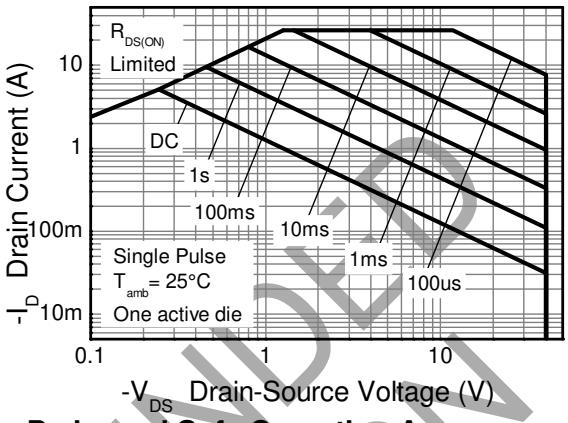
Characteristic		Symbol	N-Channel - Q1	P-Channel - Q2	Unit
Power Dissipation Linear Derating Factor	(Notes 5 & 8)	P_D	1.25 10		W mW/°C
	(Notes 5 & 9)		1.8 14.3		
	(Notes 6 & 8)		2.14 17.2		
Thermal Resistance, Junction to Ambient	(Notes 5 & 8)	$R_{\theta JA}$	100		°C/W
	(Notes 5 & 9)		70		
	(Notes 6 & 8)		58		
Thermal Resistance, Junction to Lead	(Notes 8 & 10)	$R_{\theta JL}$	51		
Operating and Storage Temperature Range		T_J, T_{STG}	-55 to +150		°C

Notes:
5. For a device surface mounted on 25mm x 25mm x 1.6mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions; the device is measured when operating in a steady-state condition.
6. Same as Note 5, except the device is measured at t ≤ 10sec.
7. Same as Note 5, except the device is pulsed with D = 0.02 and pulse width = 300µs. The pulse current is limited by the maximum junction temperature.
8. For a dual device with one active die.
9. For a device with two active dies running at equal power.
10. Thermal resistance from junction to solder-point (at the end of the drain lead).

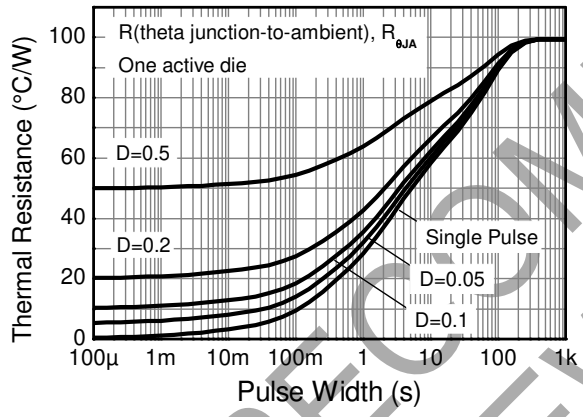
Thermal Characteristics



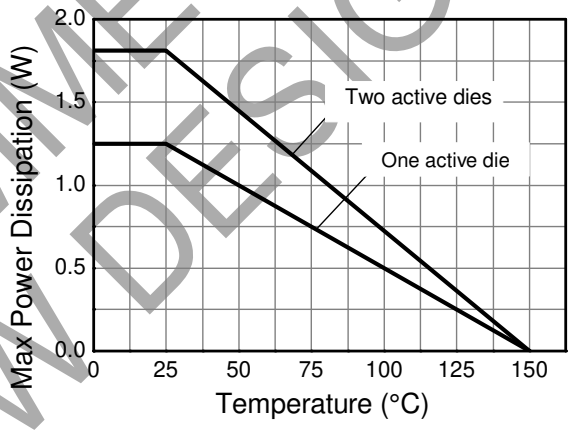
N-channel Safe Operating Area



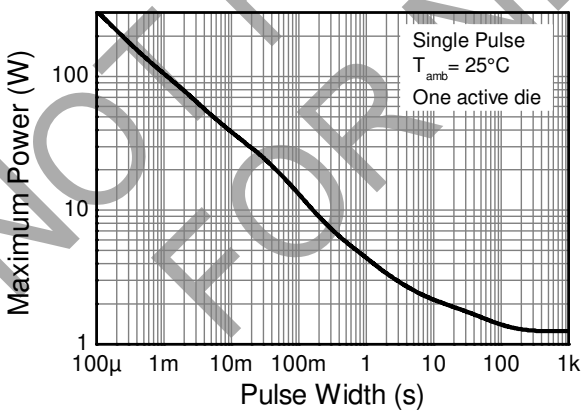
P-channel Safe Operating Area



Transient Thermal Impedance



Derating Curve



Pulse Power Dissipation

Electrical Characteristics – Q1 N-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	40	—	—	V	I_D = 250µA, V_{GS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1.0	µA	V_{DS} = 40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	0.8	1.3	1.8	V	I_D = 250µA, V_{DS} = V_{GS}
Static Drain-Source On-Resistance (Note 11)	$R_{DS(ON)}$	—	0.013	0.025	Ω	V_{GS} = 10V, I_D = 3A
			0.028	0.040		V_{GS} = 4.5V, I_D = 3A
Forward Transconductance (Notes 11 & 12)	g_{fs}	—	12.6	—	S	V_{DS} = 5V, I_D = 3A
Diode Forward Voltage (Note 7)	V_{SD}	—	0.7	1.0	V	I_S = 1A, V_{GS} = 0V
DYNAMIC CHARACTERISTICS (Note 12)						
Input Capacitance	C_{iss}	—	1790	—	pF	V_{DS} = 20V, V_{GS} = 0V F = 1MHz
Output Capacitance	C_{oss}	—	160	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	120	—	pF	
Gate Resistance	R_g	—	1.03	—	Ω	V_{DS} = 0V, V_{GS}= 0V, f = 1MHz
Total Gate Charge (Note 13)	Q_g	—	16.0	—	nC	V_{GS} = 4.5V; V_{DS} = 20V, I_D = 3A
Total Gate Charge (Note 13)	Q_g	—	37.6	—	nC	V_{GS} = 10V; V_{DS} = 20V, I_D = 3A
Gate-Source Charge (Note 13)	Q_{gs}	—	7.8	—	nC	V_{GS} = 10V
Gate-Drain Charge (Note 13)	Q_{gd}	—	6.6	—	nC	V_{GS} = 10V
Turn-On Delay Time (Note 13)	$t_{D(ON)}$	—	8.1	—	ns	V_{DD} = 20V, V_{GS} = 10V I_D = 3A
Turn-On Rise Time (Note 13)	t_R	—	15.1	—	ns	
Turn-Off Delay Time (Note 13)	$t_{D(OFF)}$	—	24.3	—	ns	
Turn-Off Fall Time (Note 13)	t_F	—	5.3	—	ns	

Notes: 11. Measured under pulsed conditions. Pulse width ≤ 300µs; duty cycle ≤ 2%.
12. For design aid only, not subject to production testing.
13. Switching characteristics are independent of operating junction temperatures.

Typical Characteristics – Q1 N-Channel

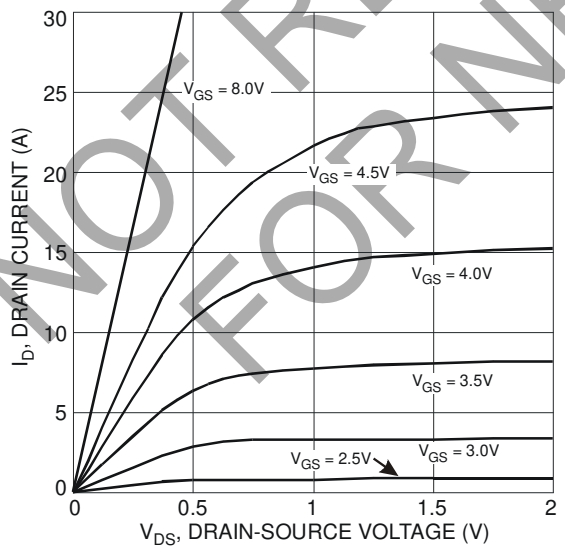


Fig. 1 Typical Output Characteristic

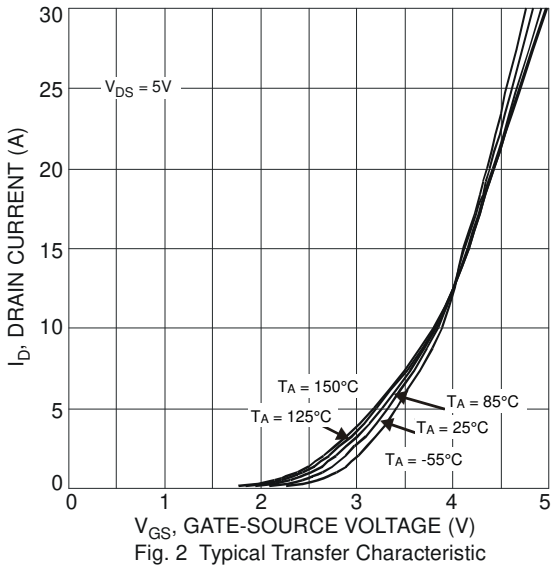


Fig. 2 Typical Transfer Characteristic

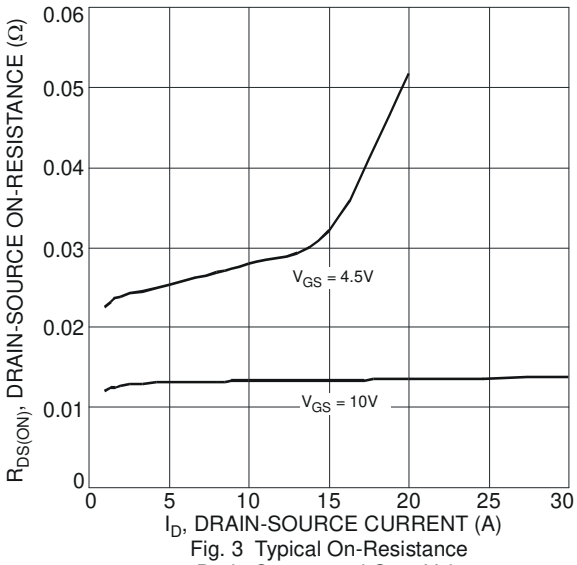


Fig. 3 Typical On-Resistance
vs. Drain Current and Gate Voltage

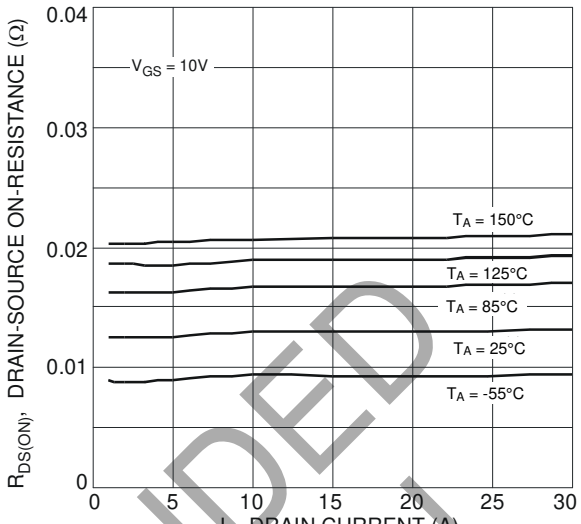


Fig. 4 Typical On-Resistance
vs. Drain Current and Temperature

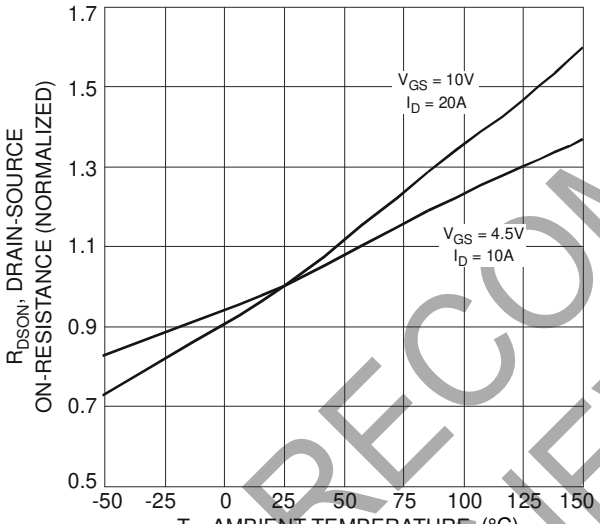


Fig. 5 On-Resistance Variation with Temperature

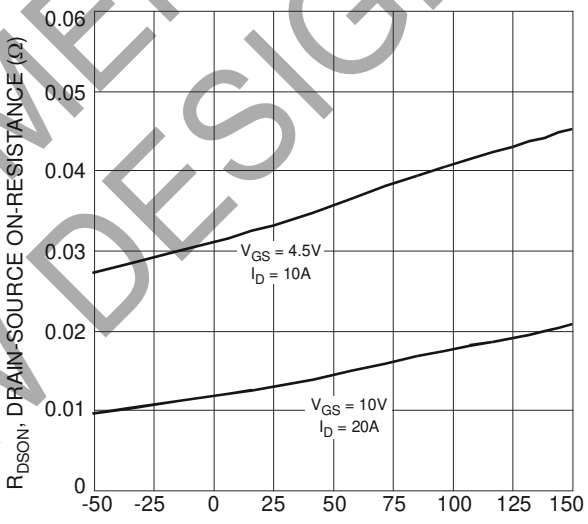


Fig. 6 On-Resistance Variation with Temperature

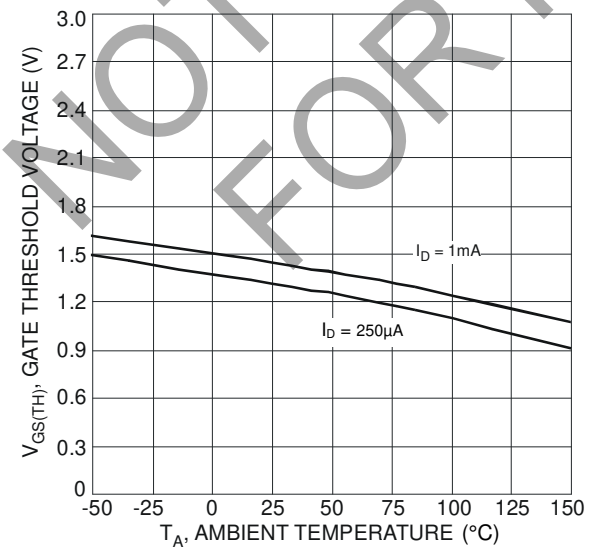


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

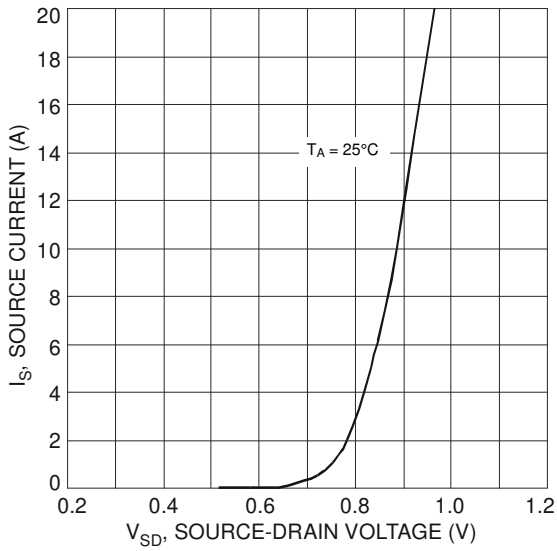


Fig. 8 Diode Forward Voltage vs. Current

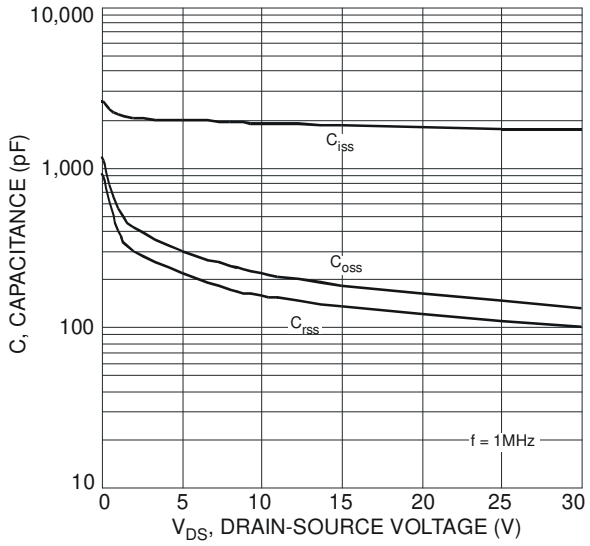


Fig. 9 Typical Total Capacitance

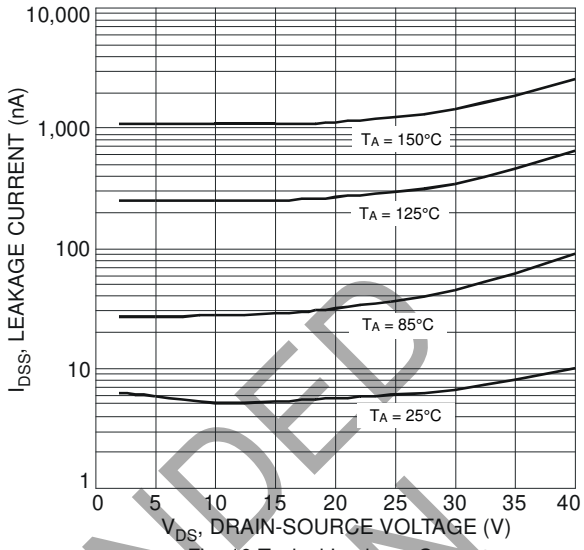


Fig. 10 Typical Leakage Current vs. Drain-Source Voltage

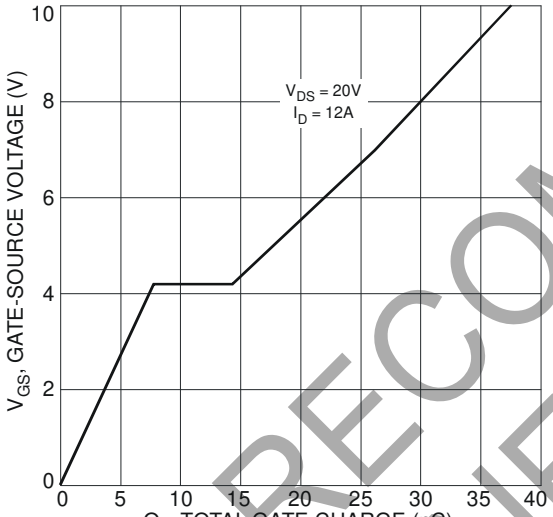


Fig. 11 Gate-Charge Characteristics

Electrical Characteristics – Q2 P-Channel (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	-40	—	—	V	I_D = -250µA, V_{GS} = 0V
Zero Gate Voltage Drain Current	I_{DSS}	—	—	-1.0	µA	V_{DS} = -40V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	—	—	±100	nA	V_{GS} = ±20V, V_{DS} = 0V
ON CHARACTERISTICS						
Gate Threshold Voltage	$V_{GS(TH)}$	-0.8	-1.3	-1.8	V	I_D = -250µA, V_{DS} = V_{GS}
Static Drain-Source On-Resistance (Note 14)	$R_{DS(ON)}$	—	0.018	0.025	Ω	V_{GS} = -10V, I_D = -3A
			0.030	0.045		V_{GS} = -4.5V, I_D = -3A
Forward Transconductance (Notes 14 & 15)	g_{fs}	—	16.6	—	S	V_{DS} = -5V, I_D = -3A
Diode Forward Voltage (Note 14)	V_{SD}	—	-0.7	-1.0	V	I_S = -1A, V_{GS} = 0V
DYNAMIC CHARACTERISTICS (Note 15)						
Input Capacitance	C_{iss}	—	1643	—	pF	V_{DS} = -20V, V_{GS} = 0V f = 1MHz
Output Capacitance	C_{oss}	—	179	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	128	—	pF	
Gate Resistance	R_g	—	6.43	—	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1MHz
Total Gate Charge (Note 16)	Q_g	—	14.0	—	nC	V_{GS} = -4.5V
Total Gate Charge (Note 16)	Q_g	—	33.7	—	nC	V_{DS} = -20V I_D = -3A
Gate-Source Charge (Note 16)	Q_{gs}	—	5.5	—	nC	V_{GS} = -10V
Gate-Drain Charge (Note 16)	Q_{gd}	—	7.3	—	nC	
Turn-On Delay Time (Note 16)	$t_{D(ON)}$	—	6.9	—	ns	V_{DD} = -20V, V_{GS} = -10V I_D = -3A
Turn-On Rise Time (Note 16)	t_R	—	14.7	—	ns	
Turn-Off Delay Time (Note 16)	$t_{D(OFF)}$	—	53.7	—	ns	
Turn-Off Fall Time (Note 16)	t_F	—	30.9	—	ns	

Notes: 14. Measured under pulsed conditions. Pulse width ≤ 300µs; duty cycle ≤ 2%.
15. For design aid only, not subject to production testing.
16. Switching characteristics are independent of operating junction temperatures

Typical Characteristics – Q2 P-Channel

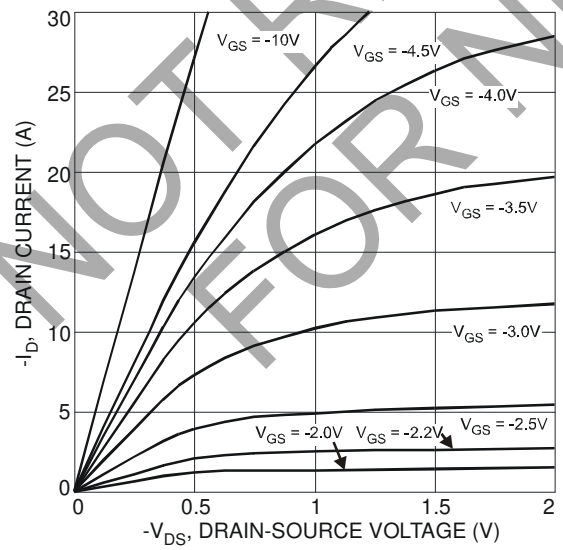


Fig. 12 Typical Output Characteristic

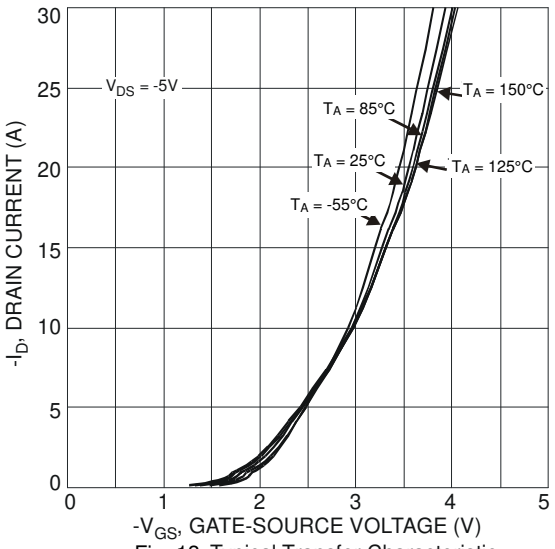


Fig. 13 Typical Transfer Characteristic

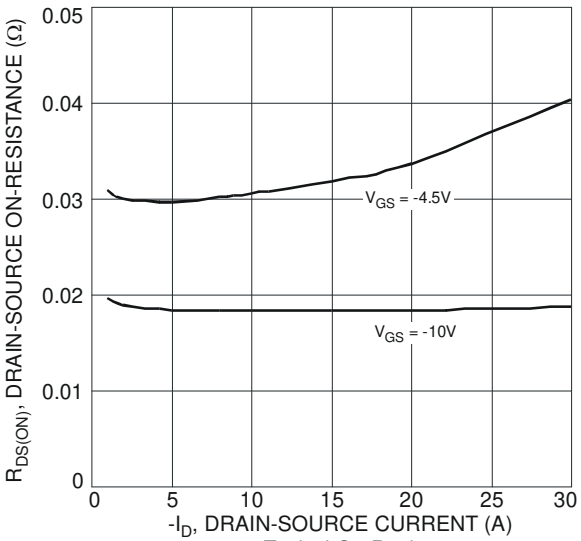


Fig. 14 Typical On-Resistance vs. Drain Current and Gate Voltage

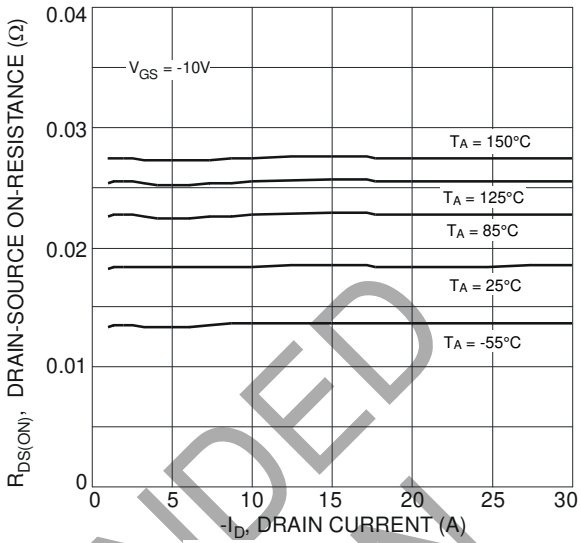


Fig. 15 Typical On-Resistance vs. Drain Current and Temperature

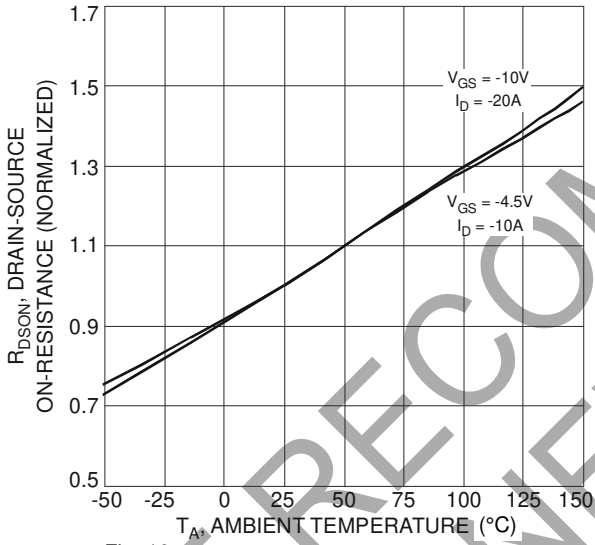


Fig. 16 On-Resistance Variation with Temperature

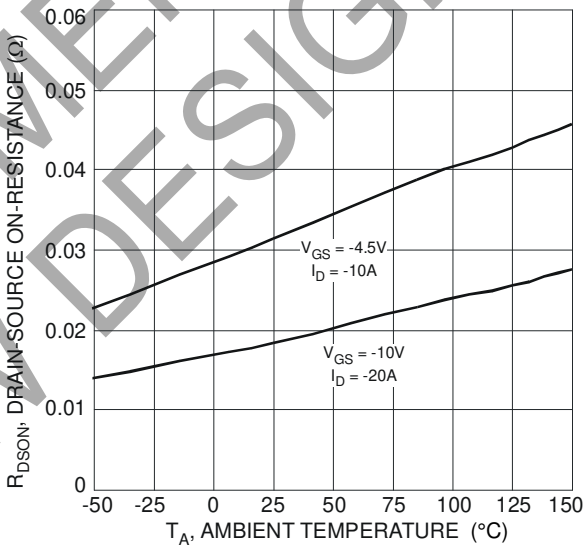


Fig. 17 On-Resistance Variation with Temperature

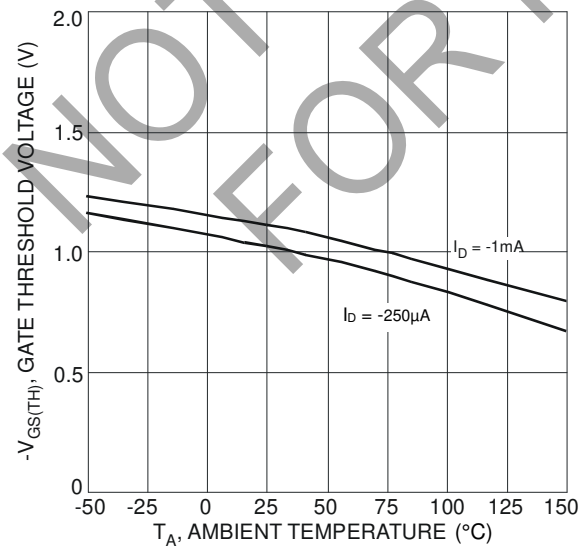


Fig. 18 Gate Threshold Variation vs. Ambient Temperature

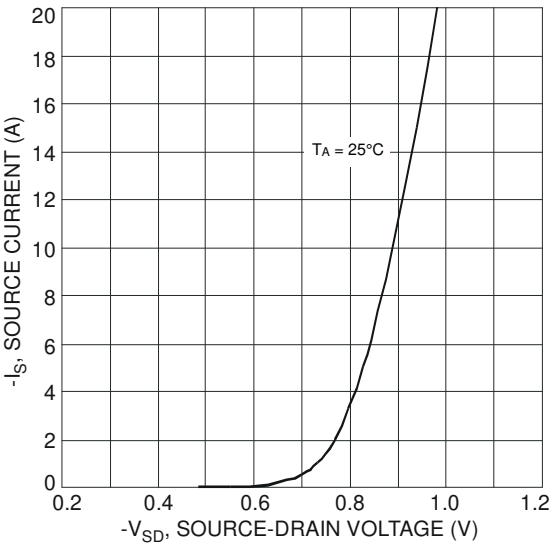


Fig. 19 Diode Forward Voltage vs. Current

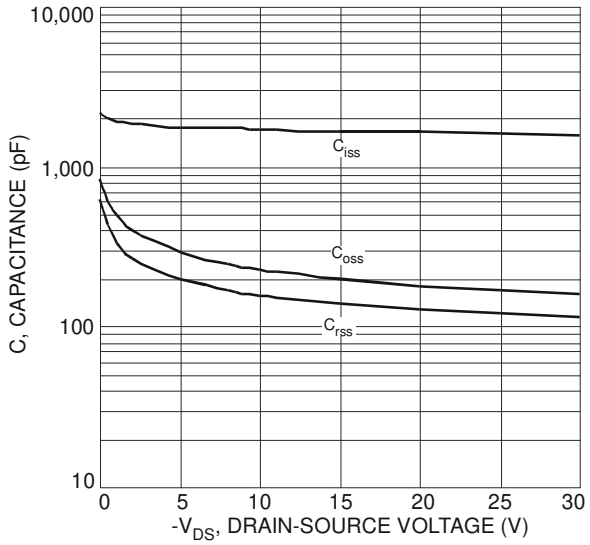


Fig. 20 Typical Total Capacitance

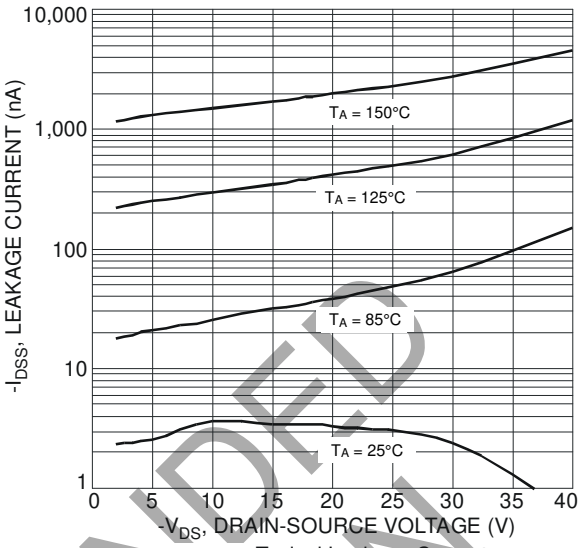


Fig. 21 Typical Leakage Current vs. Drain-Source Voltage

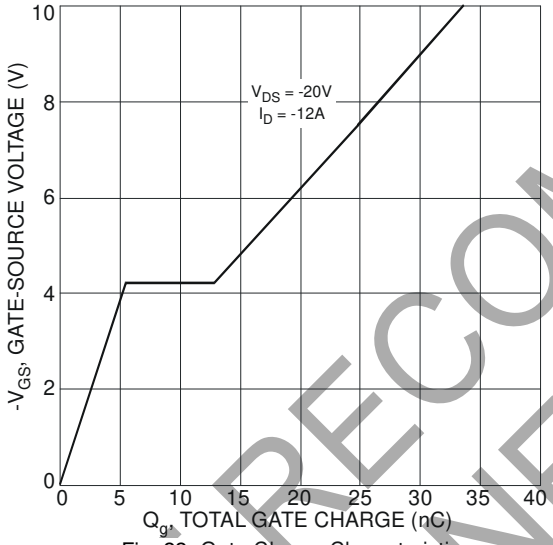
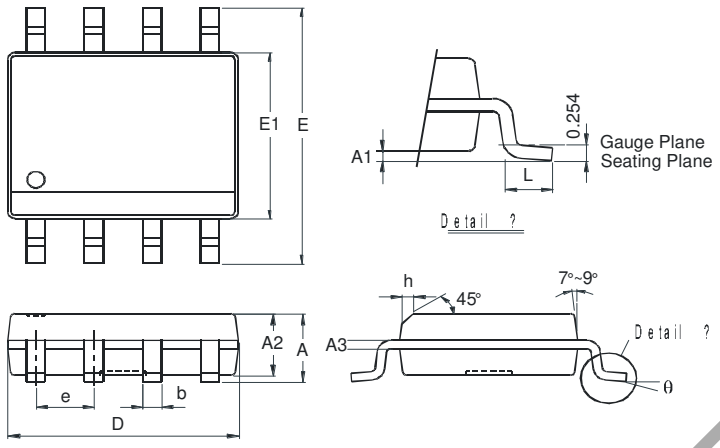


Fig. 22 Gate-Charge Characteristics

Package Outline Dimensions

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8

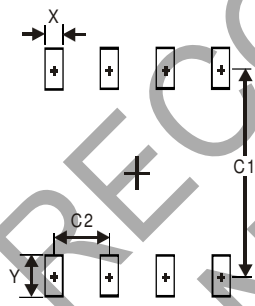


SO-8		
Dim	**Min**	**Max**
A	-	1.75
A1	0.10	0.20
A2	1.30	1.50
A3	0.15	0.25
b	0.3	0.5
D	4.85	4.95
E	5.90	6.10
E1	3.85	3.95
e	1.27 Typ	
h	-	0.35
L	0.62	0.82
θ	0°	8°
All Dimensions in mm		

Suggested Pad Layout

Please see http://www.diodes.com/package-outlines.html for the latest version.

SO-8



Dimensions	Value (in mm)
X	0.60
Y	1.55
C1	5.4
C2	1.27

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