

SN74CBTLV3245 LOW-VOLTAGE OCTAL FET BUS SWITCH

SCDS034F – JULY 1997 – REVISED MAY 1998

- Standard '245-Type Pinout
- 5-Ω Switch Connection Between Two Ports
- Isolation Under Power-Off Conditions
- ESD Protection Exceeds 2000 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Package Options Include Shrink Small-Outline (DB), Thin Very Small-Outline (DGV), Small-Outline (DW), and Thin Shrink Small-Outline (PW) Packages

description

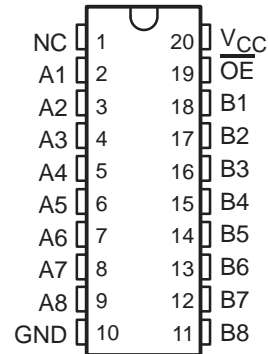
The SN74CBTLV3245 provides eight bits of high-speed bus switching in a standard '245 device pinout. The low on-state resistance of the switch allows connections to be made with minimal propagation delay.

The device is organized as one 8-bit switch. When output enable (\overline{OE}) is low, the 8-bit bus switch is on and port A is connected to port B. When \overline{OE} is high, the switch is open and a high-impedance state exists between the two ports.

To ensure the high-impedance state during power up or power down, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The SN74CBTLV3245 is characterized for operation from -40°C to 85°C .

DB, DGV, DW, OR PW PACKAGE
(TOP VIEW)

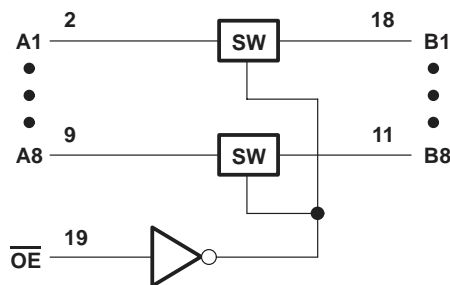


NC – No internal connection

FUNCTION TABLE

INPUT \overline{OE}	FUNCTION
L	A port = B port
H	Disconnect

logic diagram (positive logic)



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS
INSTRUMENTS**

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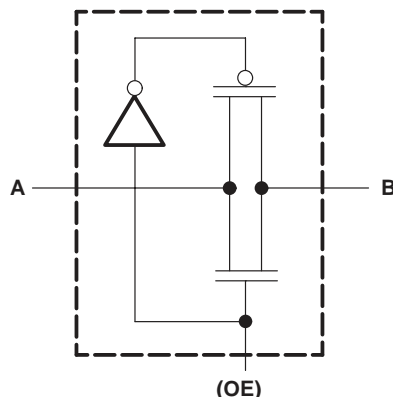
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SN74CBTLV3245

LOW-VOLTAGE OCTAL FET BUS SWITCH

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simplified schematic, each FET switch



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	-0.5 V to 4.6 V
Input voltage range, V_I (see Note 1)	-0.5 V to 4.6 V
Continuous channel current	128 mA
Input clamp current, I_{IK} ($V_{I/O} < 0$)	-50 mA
Package thermal impedance, θ_{JA} (see Note 2):	DB package	115°C/W
	DGV package	146°C/W
	DW package	97°C/W
	PW package	128°C/W
Storage temperature range, T_{stg}	-65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
 2. The package thermal impedance is calculated in accordance with JESD 51.

recommended operating conditions (see Note 3)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	2.3	3.6	V
V_{IH}	High-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	2	
V_{IL}	Low-level control input voltage	$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	0.7	V
		$V_{CC} = 2.7 \text{ V to } 3.6 \text{ V}$	0.8	
T_A	Operating free-air temperature	-40	85	°C

NOTE 3: All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.



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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 3\text{ V}$,	$I_I = -18\text{ mA}$			-0.8	V
I_I		$V_{CC} = 3.6\text{ V}$,	$V_I = V_{CC}$ or GND			±50	μA
I_{off}		$V_{CC} = 0$,	V_I or $V_O = 0$ to 3.6 V			30	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$,	$I_O = 0$, $V_I = V_{CC}$ or GND			20	μA
$\Delta I_{CC}‡$	Control inputs	$V_{CC} = 3.6\text{ V}$,	One input at 3 V, Other inputs at V_{CC} or GND			750	μA
C_i	Control inputs	$V_I = 3\text{ V}$ or 0				3.5	pF
$C_{iO(OFF)}$		$V_O = 3\text{ V}$ or 0,	$\overline{OE} = V_{CC}$			8	pF
$r_{on}§$	$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$			¶	¶
			$I_I = 24\text{ mA}$			¶	¶
		$V_I = 1.7\text{ V}$,	$I_I = 15\text{ mA}$			¶	¶
	$V_{CC} = 3\text{ V}$	$V_I = 0$	$I_I = 64\text{ mA}$			5	7
			$I_I = 24\text{ mA}$			5	7
		$V_I = 2.4\text{ V}$,	$I_I = 15\text{ mA}$			10	15

† All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.

‡ This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.

§ Measured by the voltage drop between the A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

¶ This information was not available at the time of publication.

switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figures 1 and 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
$t_{pd}^\#$	A or B	B or A		¶		0.25	ns
t_{en}	\overline{OE}	A or B	¶	¶	1	5.6	ns
t_{dis}	\overline{OE}	A or B	¶	¶	1	6.5	ns

¶ This information was not available at the time of publication.

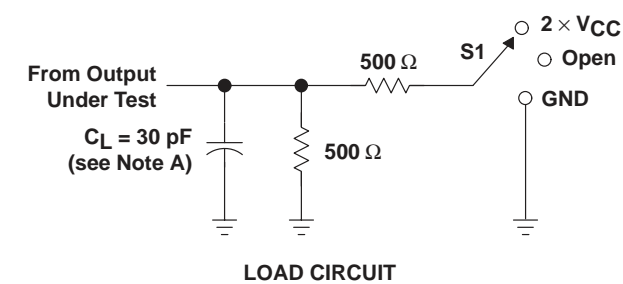
The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

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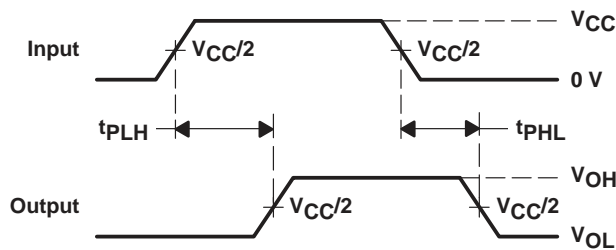
PARAMETER MEASUREMENT INFORMATION

$$V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$$

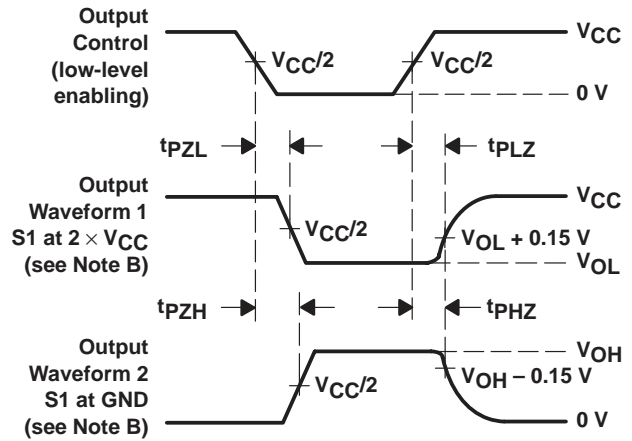


LOAD CIRCUIT

TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	2 \times V_{CC}
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



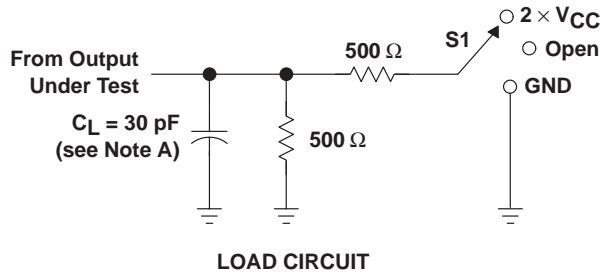
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2 \text{ ns}$, $t_f \leq 2 \text{ ns}$.
 D. The outputs are measured one at a time with one transition per measurement.
 E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 F. t_{PZL} and t_{PZH} are the same as t_{en} .
 G. t_{PLH} and t_{PHL} are the same as t_{pd} .

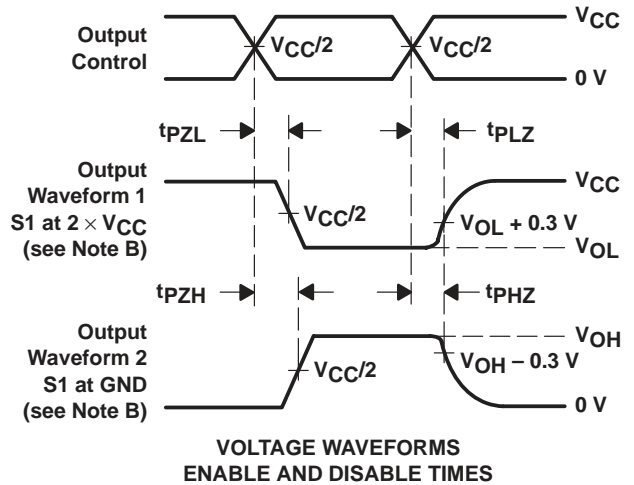
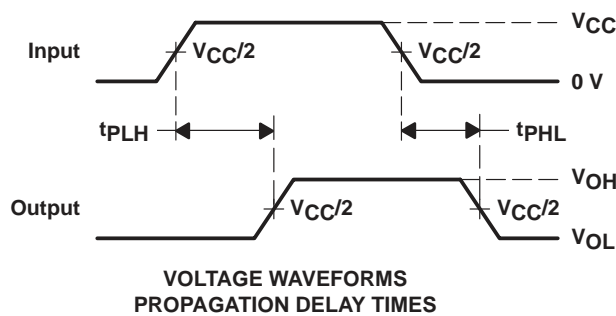
Figure 1. Load Circuit and Voltage Waveforms

PARAMETER MEASUREMENT INFORMATION

$V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$



TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CC}$
t_{PHZ}/t_{PZH}	GND



- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
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 - E. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - F. t_{PZL} and t_{PZH} are the same as t_{en} .
 - G. t_{PLH} and t_{PHL} are the same as t_{pd} .

Figure 2. Load Circuit and Voltage Waveforms

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