FAIRCHILD SEMICONDUCTOR™

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MM74HC595
8-Bit Shift Registers with Output Latches

General Description

The MM74HC595 high speed shift register utilizes advanced silicon-gate CMOS technology. This device possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, as well as the ability to drive 15 LS-TTL loads.

This device contains an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has 8 3-STATE outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output (standard) pins for cascading. Both the shift register and storage register use positive-edge triggered clocks. If both clocks are connected together, the shift register state will always be one clock pulse ahead of the storage register.

The 74HC logic family is speed, function, and pin-out compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

- Low quiescent current: 80 μA maximum (74HC Series)
- Low input current: 1 μA maximum
- 8-bit serial-in, parallel-out shift register with storage
- Wide operating voltage range: 2V–6V
- Cascadable
- Shift register has direct clear
- Guaranteed shift frequency: DC to 30 MHz

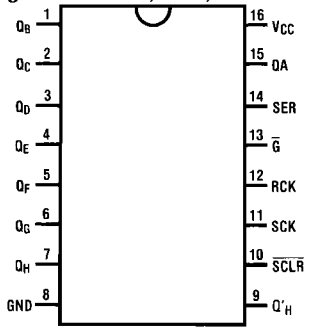
Ordering Code:

Order Number	Package Number	Package Description
MM74HC595M	M16A	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC595WM	M16B	16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
MM74HC595SJ	M16D	16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC595MTC	MTC16	16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC595N	N16E	16-Lead Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram

Pin Assignments for DIP, SOIC, SOP and TSSOP



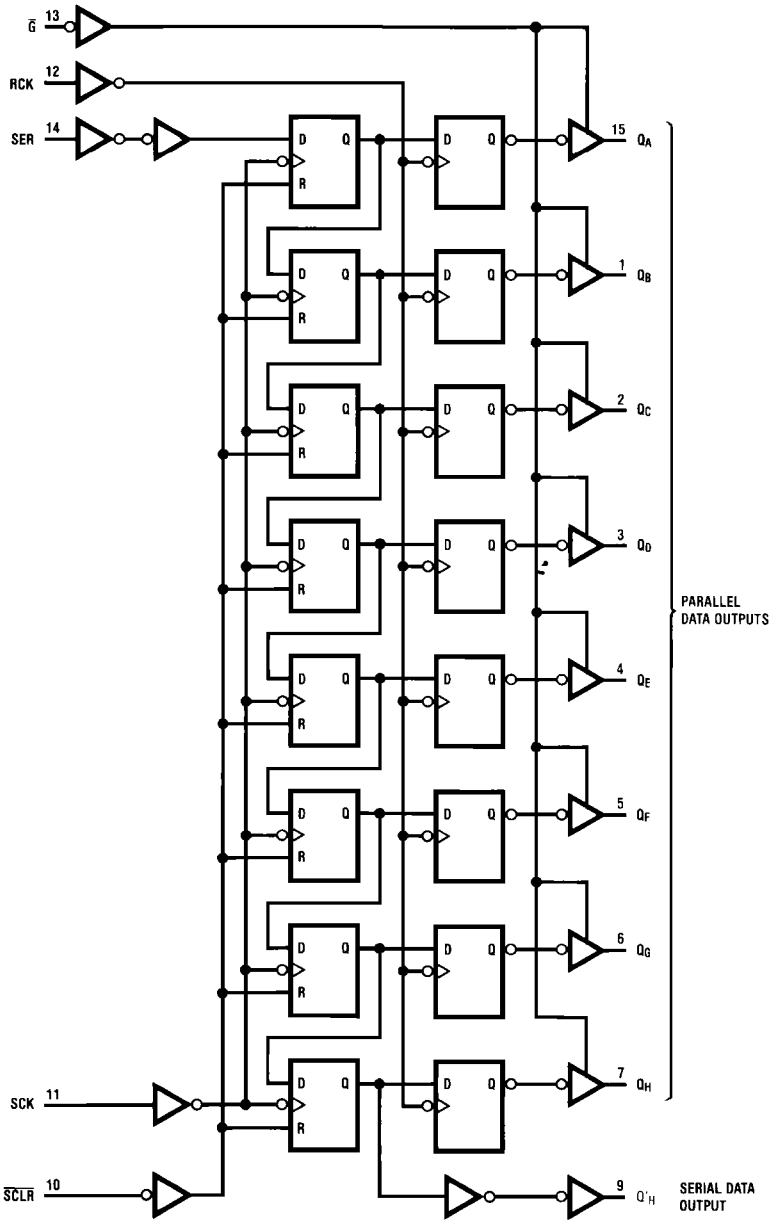
Top View

Truth Table

RCK	SCK	$\overline{SCLR}$	$\overline{G}$	Function
X	X	X	H	Q_A thru Q_H = 3-STATE
X	X	L	L	Shift Register cleared $Q_H = 0$
X	↑	H	L	Shift Register clocked $Q_N = Q_{n-1}$, Q_0 = SER
↑	X	H	L	Contents of Shift Register transferred to output latches

Logic Diagram

(positive logic)



Absolute Maximum Ratings (Note 1)

(Note 2)

Supply Voltage (V_{CC})	−0.5 to +7.0V
DC Input Voltage (V_{IN})	−1.5 to V_{CC} +1.5V
DC Output Voltage (V_{OUT})	−0.5 to V_{CC} +0.5V
Clamp Diode Current (I_{IK}, I_{OK})	±20 mA
DC Output Current, per pin (I_{OUT})	±35 mA
DC V_{CC} or GND Current, per pin (I_{CC})	±70 mA
Storage Temperature Range (T_{STG})	−65°C to +150°C
Power Dissipation (P_D)	
(Note 3)	600 mW
S.O. Package only	500 mW
Lead Temperature (T_L)	
(Soldering 10 seconds)	260°C

Recommended Operating Conditions

	Min	Max	Units
Supply Voltage (V_{CC})	2	6	V
DC Input or Output Voltage (V_{IN}, V_{OUT})	0	V_{CC}	V
Operating Temperature Range (T_A)	−40	+85	°C
Input Rise or Fall Times			
(t_r, t_f) V_{CC} = 2.0V		1000	ns
V_{CC} = 4.5V		500	ns
V_{CC} = 6.0V		400	ns

Note 1: Absolute Maximum Ratings are those values beyond which damage to the device may occur.

Note 2: Unless otherwise specified all voltages are referenced to ground.

Note 3: Power Dissipation temperature derating — plastic "N" package: −12 mW/°C from 65°C to 85°C.

DC Electrical Characteristics (Note 4)

Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C	Units
				Typ	Guaranteed Limits		
V_{IH}	Minimum HIGH Level Input Voltage		2.0V		1.5	1.5	1.5	V
			4.5V		3.15	3.15	3.15	V
			6.0V		4.2	4.2	4.2	V
V_{IL}	Maximum LOW Level Input Voltage		2.0V		0.5	0.5	0.5	V
			4.5V		1.35	1.35	1.35	V
			6.0V		1.8	1.8	1.8	V
V_{OH}	Minimum HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	2.0	1.9	1.9	1.9	V
			4.5V	4.5	4.4	4.4	4.4	V
			6.0V	6.0	5.9	5.9	5.9	V
	Q_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	5.2	5.48	5.34	5.2	V
	Q_A thru Q_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	4.2	3.98	3.84	3.7	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	5.7	5.48	5.34	5.2	V
V_{OL}	Maximum LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 20\ \mu A$	2.0V	0	0.1	0.1	0.1	V
			4.5V	0	0.1	0.1	0.1	V
			6.0V	0	0.1	0.1	0.1	V
	Q_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 4$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 5.2$ mA	6.0V	0.2	0.26	0.33	0.4	V
	Q_A thru Q_H	V_{IN} = V_{IH} or V_{IL} $\lvert I_{OUT}\rvert \le 6.0$ mA	4.5V	0.2	0.26	0.33	0.4	V
		$\lvert I_{OUT}\rvert \le 7.8$ mA	6.0V	0.2	0.26	0.33	0.4	V
I_{IN}	Maximum Input Current	V_{IN} = V_{CC} or GND	6.0V		±0.1	±1.0	±1.0	µA
I_{OZ}	Maximum 3-STATE Output Leakage	V_{OUT} = V_{CC} or GND $\overline{G}$ = V_{IH}	6.0V		±0.5	±5.0	±10	µA
I_{CC}	Maximum Quiescent Supply Current	V_{IN} = V_{CC} or GND I_{OUT} = 0 µA	6.0V		8.0	80	160	µA

Note 4: For a power supply of 5V ±10% the worst case output voltages (V_{OH}, and V_{OL}) occur for HC at 4.5V. Thus the 4.5V values should be used when designing with this supply. Worst case V_{IH} and V_{IL} occur at V_{CC} = 5.5V and 4.5V respectively. (The V_{IH} value at 5.5V is 3.85V.) The worst case leakage current (I_{IN}, I_{CC}, and I_{OZ}) occur for CMOS at the higher voltage and so the 6.0V values should be used.

AC Electrical Characteristics

V_{CC} = 5V, T_A = 25°C, $t_r = t_f$ = 6 ns

Symbol	Parameter	Conditions	Typ	Guaranteed Limit	Units
f_{MAX}	Maximum Operating Frequency of SCK		50	30	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay, SCK to $Q_{H'}$	C_L = 45 pF	12	20	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay, RCK to Q_A thru Q_H	C_L = 45 pF	18	30	ns
t_{PZH}, t_{PZL}	Maximum Output Enable Time from $\overline{G}$ to Q_A thru Q_H	R_L = 1 kΩ C_L = 45 pF	17	28	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable Time from $\overline{G}$ to Q_A thru Q_H	R_L = kΩ C_L = 5 pF	15	25	ns
t_S	Minimum Setup Time from SER to SCK			20	ns
t_S	Minimum Setup Time from $\overline{SCLR}$ to SCK			20	ns
t_S	Minimum Setup Time from SCK to RCK (Note 5)			40	ns
t_H	Minimum Hold Time from SER to SCK			0	ns
t_W	Minimum Pulse Width of SCK or RCK			16	ns

Note 5: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together in which case the storage register state will be one clock pulse behind the shift register.

AC Electrical Characteristics

V_{CC} = 2.0–6.0V, C_L = 50 pF, $t_r = t_f$ = 6 ns (unless otherwise specified)

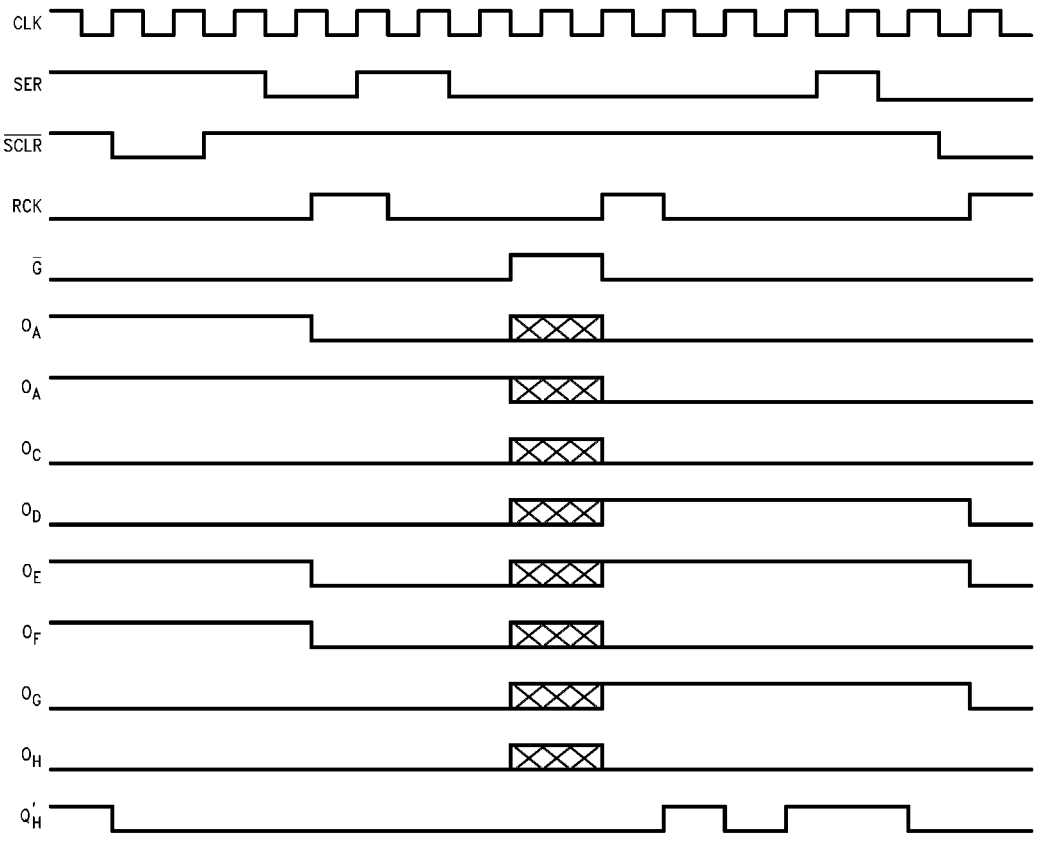
Symbol	Parameter	Conditions	V_{CC}	T_A = 25°C	T_A = −40 to 85°C	T_A = −55 to 125°C		Units
				Typ	Guaranteed Limits			
f_{MAX}	Maximum Operating Frequency	C_L = 50 pF	2.0V	10	6	4.8	4.0	MHz
			4.5V	45	30	24	20	MHz
			6.0V	50	35	28	24	MHz
t_{PHL}, t_{PLH}	Maximum Propagation Delay from SCK to Q_H	C_L = 50 pF	2.0V	58	210	265	315	ns
		C_L = 150 pF	2.0V	83	294	367	441	ns
		C_L = 50 pF	4.5V	14	42	53	63	ns
		C_L = 150 pF	4.5V	17	58	74	88	ns
		C_L = 50 pF	6.0V	10	36	45	54	ns
		C_L = 150 pF	6.0V	14	50	63	76	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from RCK to Q_A thru Q_H	C_L = 50 pF	2.0V	70	175	220	265	ns
		C_L = 150 pF	2.0V	105	245	306	368	ns
		C_L = 50 pF	4.5V	21	35	44	53	ns
		C_L = 150 pF	4.5V	28	49	61	74	ns
		C_L = 50 pF	6.0V	18	30	37	45	ns
		C_L = 150 pF	6.0V	26	42	53	63	ns
t_{PHL}, t_{PLH}	Maximum Propagation Delay from $\overline{SCLR}$ to Q_H		2.0V		175	221	261	ns
			4.5V		35	44	52	ns
			6.0V		30	37	44	ns

AC Electrical Characteristics (Continued)

Symbol	Parameter	Conditions	V_{CC}	$T_A = 25°C$	$T_A = -40$ to $85°C$	$T_A = -55$ to $125°C$	Units
				Typ	Guaranteed Limits		
t_{PZH}, t_{PZL}	Maximum Output Enable	$R_L = 1\ k\Omega$					
	from $\overline{G}$ to Q_A thru Q_H	$C_L = 50$ pF	2.0V	75	175	220	265	ns
		$C_L = 150$ pF	2.0V	100	245	306	368	ns
		$C_L = 50$ pF	4.5V	15	35	44	53	ns
		$C_L = 150$ pF	4.5V	20	49	61	74	ns
		$C_L = 50$ pF	6.0V	13	30	37	45	ns
		$C_L = 150$ pF	6.0V	17	42	53	63	ns
t_{PHZ}, t_{PLZ}	Maximum Output Disable	$R_L = 1\ k\Omega$	2.0V	75	175	220	265	ns
	Time from $\overline{G}$ to Q_A thru Q_H	$C_L = 50$ pF	4.5V	15	35	44	53	ns
			6.0V	13	30	37	45	ns
t_S	Minimum Setup Time		2.0V		100	125	150	ns
	from SER to SCK		4.5V		20	25	30	ns
			6.0V		17	21	25	ns
t_R	Minimum Removal Time		2.0V		50	63	75	ns
	from $\overline{SCLR}$ to SCK		4.5V		10	13	15	ns
			6.0V		9	11	13	ns
t_S	Minimum Setup Time		2.0V		100	125	150	ns
	from SCK to RCK		4.5V		20	25	30	ns
			6.0V		17	21	26	ns
t_H	Minimum Hold Time		2.0V		5	5	5	ns
	SER to SCK		4.5V		5	5	5	ns
			6.0V		5	5	5	ns
t_W	Minimum Pulse Width		2.0V	30	80	100	120	ns
	of SCK or $\overline{SCLR}$		4.5V	9	16	20	24	ns
			6.0V	8	14	18	22	ns
t_r, t_f	Maximum Input Rise and		2.0V		1000	1000	1000	ns
	Fall Time, Clock		4.5V		500	500	500	ns
			6.0V		400	400	400	ns
t_{THL}, t_{TLH}	Maximum Output		2.0V	25	60	75	90	ns
	Rise and Fall Time		4.5V	7	12	15	18	ns
	Q_A–Q_H		6.0V	6	10	13	15	ns
t_{THL}, t_{TLH}	Maximum Output		2.0V		75	95	110	ns
	Rise & Fall Time		4.5V		15	19	22	ns
	Q_H		6.0V		13	16	19	ns
C_{PD}	Power Dissipation	$\overline{G} = V_{CC}$		90				pF
	Capacitance, Outputs	$\overline{G} =$ GND		150				pF
	Enabled (Note 6)							
C_{IN}	Maximum Input			5	10	10	10	pF
	Capacitance							
C_{OUT}	Maximum Output			15	20	20	20	pF
	Capacitance							

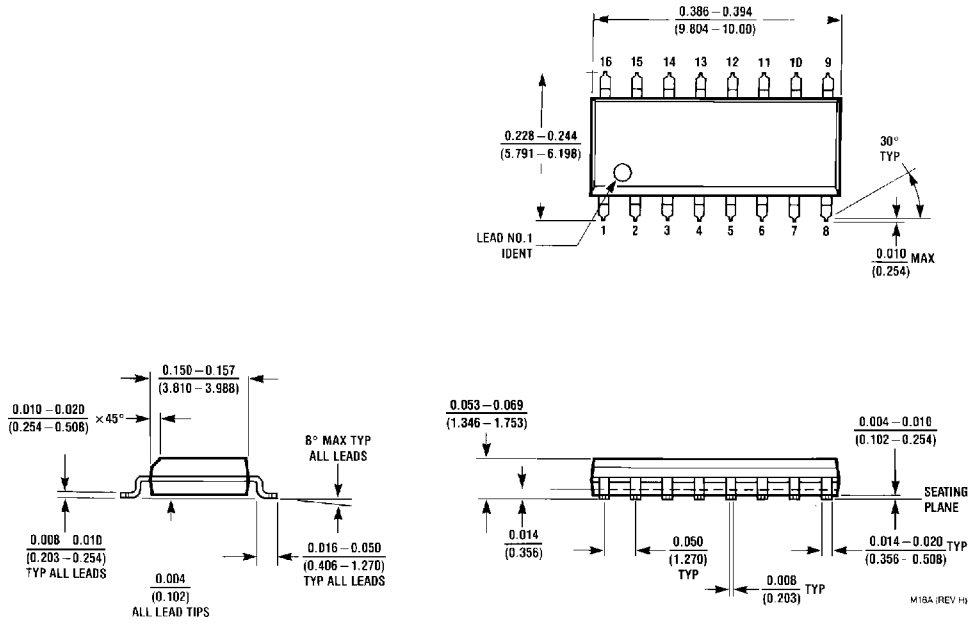
Note 6: C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD}\ V_{CC}^2 f + I_{CC}\ V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD}\ V_{CC}\ f + I_{CC}$.

Timing Diagram

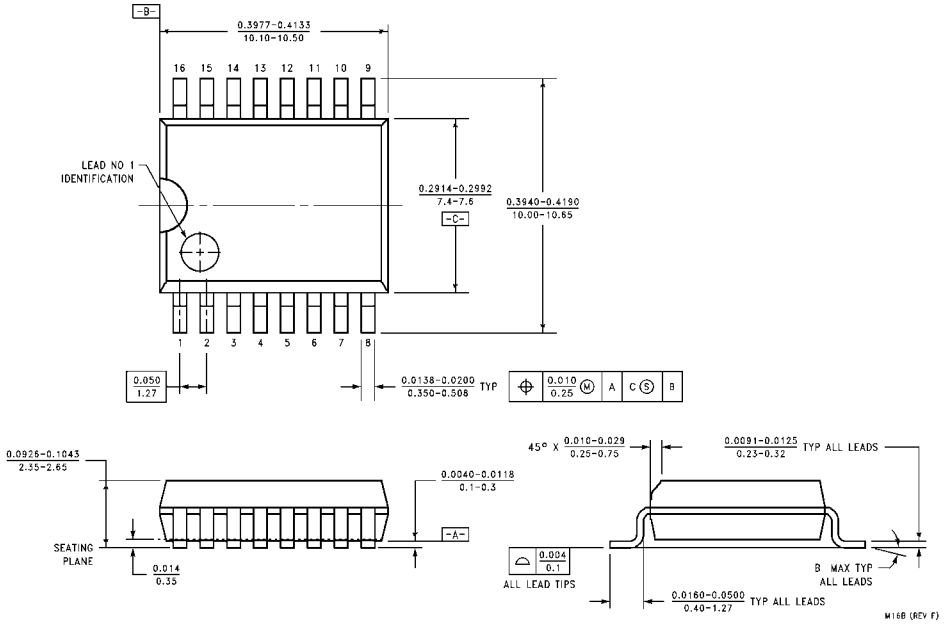


NOTE : ⊠ Implies that the output is in 3-STATE mode.

Physical Dimensions inches (millimeters) unless otherwise noted

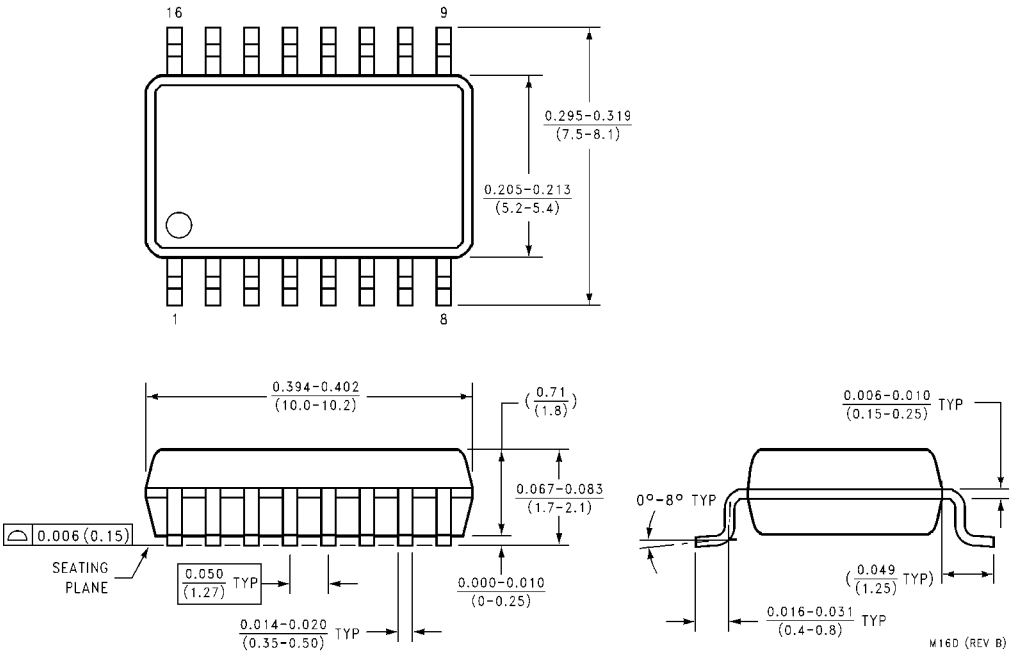


16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M16A



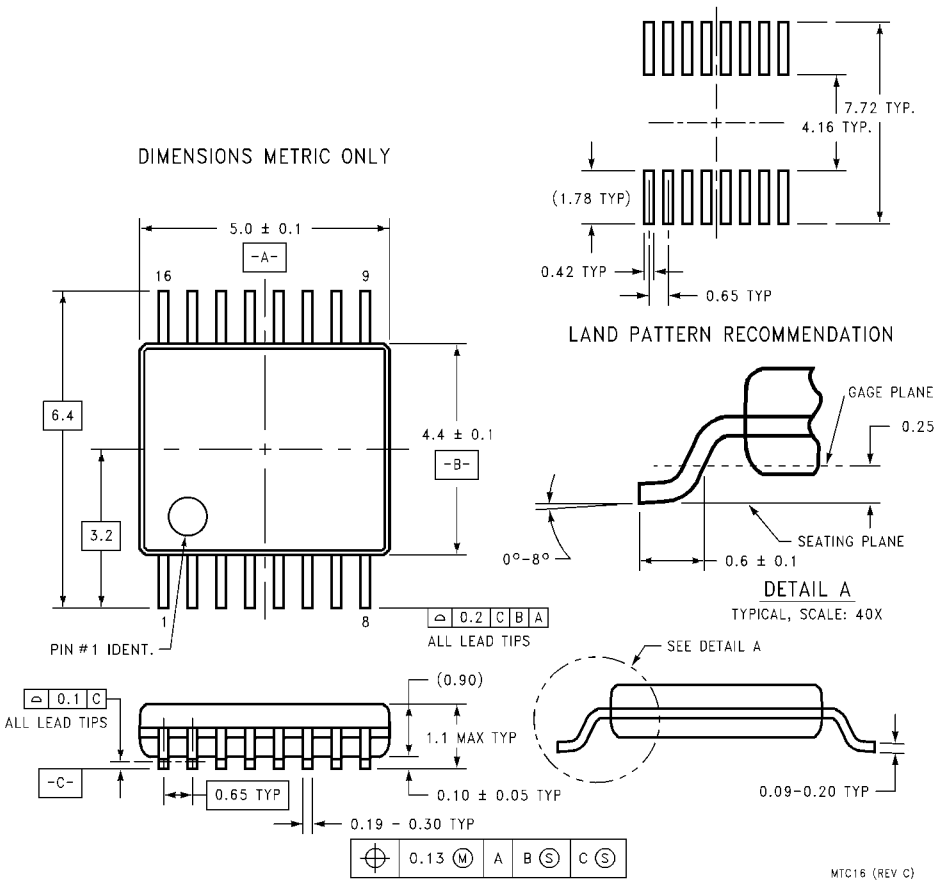
16-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M16B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



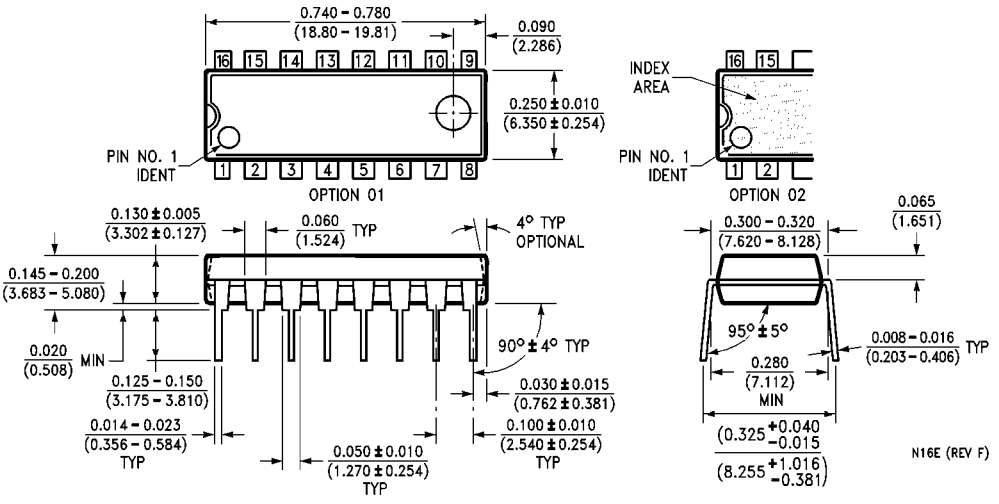
16-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M16D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC16

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



16-Lead Plastic Dual--Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N16E

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