ISO7421-EP Low-Power Dual Digital Isolators

1 Features

- Highest Signaling Rate: 1 Mbps
- Low Power Consumption, Typical I_{CC} per Channel (3.3-V Operation): 1.5 mA
- Low Propagation Delay – 9 ns Typical
- Low Skew – 300 ps Typical
- Wide T_J Range: –55°C to 136°C
- 50-kV/μs Transient Immunity, Typical
- Over 25-Year Isolation Integrity at Rated Voltage
- Operates From 3.3-V and 5-V Supply and Logic Levels
- 3.3-V and 5-V Level Translation
- Narrow Body SOIC-8 Package
- Safety and Regulatory Approvals:
  - 4242 V_{PK} Isolation per DIN V VDE V 0884-10 and DIN EN 61010-1
  - 2500 V_{RMS} Isolation for 1 minute per UL 1577
  - CSA Component Acceptance Notice 5A, IEC 60950-1 and IEC 61010-1 Standards
  - CQC Certification per GB4943.1-2011

2 Applications

- Optocoupler Replacement in:
  - Industrial Fieldbus
    - Profibus
    - Modbus
    - DeviceNet™ Data Buses
  - Servo Control Interface
  - Motor Control
  - Power Supplies
  - Battery Packs

3 Description

The ISO7421-EP device provides galvanic isolation up to 2500 V_{RMS} for 1 minute per UL. The ISO7421-EP device has two isolated channels. Each isolation channel has a logic input and output buffer separated by a silicon dioxide (SiO_2) insulation barrier. Used in conjunction with isolated power supplies, the device prevents noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry.

This device have TTL input thresholds and require two supply voltages, 3.3 or 5 V, or any combination. All inputs are 5-V tolerant when supplied from a 3.3-V supply.

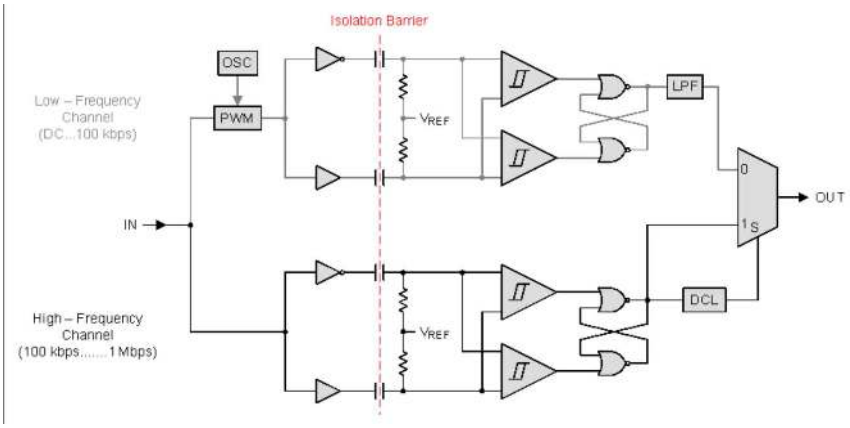
The ISO7421-EP device is specified for signaling rates up to 1 Mbps. Due to its fast response time, under most cases, this device will also transmit data with much shorter pulse widths. Designers should add external filtering to remove spurious signals with input pulse duration <20 ns if desired.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
ISO7421-EP	SOIC (8)	4.90 mm × 3.91 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Conceptual Block Diagram of a Digital Capacitive Isolator



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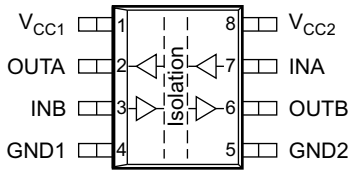
4 Revision History

DATE	REVISION	NOTES
December 2015	*	Initial release.

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND1	4	—	Ground connection for V_{CC1}
GND2	5	—	Ground connection for V_{CC2}
INA	7	I	Input, channel A
INB	3	I	Input, channel B
OUTA	2	O	Output, channel A
OUTB	6	O	Output, channel B
V_{CC1}	1	—	Power supply, V_{CC1}
V_{CC2}	8	—	Power supply, V_{CC2}

6 Specifications

6.1 Absolute Maximum Ratings

see (1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2), V_{CC1}, V_{CC2}	–0.5	6	V
V_I	Voltage at IN, OUT	–0.5	V_{CC} + 0.5(3)	V
I_O	Output current	–15	15	mA
$T_{J(max)}$	Maximum junction temperature		150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values except differential I/O bus voltages are with respect to network ground terminal and are peak voltage values.
(3) Maximum voltage must not exceed 6 V.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±4000	V
		Field-induced charged-device model, JEDEC Standard 22, Test Method C101	±1500	
		Machine model, ANSI/ESDS5.2-1996	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_{CC1}, V_{CC2}	Supply voltage - 3.3-V operation	3	3.3	3.6	V
	Supply voltage - 5-V operation	4.5	5	5.5	
I_{OH}	High-level output current	–4			mA
I_{OL}	Low-level output current			4	mA
V_{IH}	High-level input voltage	2		5.25	V
V_{IL}	Low-level input voltage	0		0.8	V
$1/t_{ui}$	Signaling rate	0		1	Mbps
t_{ui}	Input pulse duration	1			us
T_J(1)	Junction temperature	–55		136	°C

(1) To maintain the recommended operating conditions for T_J, see the *Thermal Information*.

6.4 Thermal Information

THERMAL METRIC(1)			ISO7421-EP D (SOIC) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	Low-K Board	212	°C/W
		High-K Board	116.6	
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance		71.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance		57.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter		28.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter		56.8	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics: V_{CC1} and V_{CC2} at 5 V ±10%

T_J = –55°C to 136°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 6.		V_{CCO} (1) – 0.8	4.6		V
		I_{OH} = –20 µA; see Figure 6.		V_{CCO} – 0.1	5		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 6.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 6.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CCI} (1)				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 8.		25	50		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15 pF load		2	4	mA
I_{CC2}	Supply current for V_{CC2}				2	4	

(1) V_{CCI} = Input-side power supply, V_{CCO} = Output-side power supply

6.6 Electrical Characteristics: V_{CC1} at 5 V ±10%, V_{CC2} at 3.3 V ±10%

T_J = –55°C to 136°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 6.	5-V side	V_{CCO} (1) – 0.8	4.6		V
			3.3-V side	V_{CCO} – 0.4	3		
		I_{OH} = –20 µA; see Figure 6,		V_{CCO} – 0.1	V_{CC}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 6.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 6.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CCI} (1)				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; seeFigure 8 .		25	40		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15 pF load		2	4	mA
I_{CC2}	Supply current for V_{CC2}				1.5	3.5	mA

(1) V_{CCI} = Input-side power supply, V_{CCO} = Output-side power supply

6.7 Electrical Characteristics: V_{CC1} at 3.3 V ±10%, V_{CC2} at 5 V ±10%

T_J = –55°C to 136°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 6.	5-V side	V_{CCO}(1) – 0.8	4.6		V
			3.3-V side	V_{CCO} – 0.4	3		
		I_{OH} = –20 µA; see Figure 6		V_{CCO} – 0.1	V_{CC}		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 6.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 6.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CCI}(1)				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; see Figure 8.		25	40		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15 pF load		1.5	3.5	mA
I_{CC2}	Supply current for V_{CC2}				2	4	

(1) V_{CCI} = Input-side power supply, V_{CCO} = Output-side power supply

6.8 Electrical Characteristics: V_{CC1} and V_{CC2} at 3.3 V ±10%

T_J = –55°C to 136°C

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = –4 mA; see Figure 6.		V_{CCO}(1) – 0.4	3		V
		I_{OH} = –20 µA; see Figure 6.		V_{CCO} – 0.1	3.3		
V_{OL}	Low-level output voltage	I_{OL} = 4 mA; see Figure 6.			0.2	0.4	V
		I_{OL} = 20 µA; see Figure 6.			0	0.1	
$V_{I(HYS)}$	Input threshold voltage hysteresis				400		mV
I_{IH}	High-level input current	INx at 0 V or V_{CCI}(1)				10	µA
I_{IL}	Low-level input current			–10			µA
CMTI	Common-mode transient immunity	V_I = V_{CCI} or 0 V; seeFigure 8 .		25	40		kV/µs
SUPPLY CURRENT (ALL INPUTS SWITCHING WITH SQUARE WAVE CLOCK SIGNAL FOR DYNAMIC ICC MEASUREMENT)							
I_{CC1}	Supply current for V_{CC1}	DC to 1 Mbps	V_I = V_{CCI} or 0 V, 15 pF load		1.5	3.5	mA
I_{CC2}	Supply current for V_{CC2}				1.5	3.5	

(1) V_{CCI} = Input-side power supply, V_{CCO} = Output-side power supply

6.9 Power Dissipation

THERMAL METRIC			ISO7421-EP D (SOIC) 8 PINS	UNIT
P_D	Device power dissipation	V_{CC1} = V_{CC2} = 5.25 V, T_J = 150°C, C_L = 15 pF Input a 1-Mbps 50% duty-cycle square wave	55	mW

6.10 Switching Characteristics: V_{CC1} and V_{CC2} at 5 V ±10%

T_J = –55°C to 136°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6.		9	14	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.3	4	ns
$t_{sk(pp)}$	Part-to-part skew time				4.9	ns
$t_{sk(o)}$	Channel-to-channel output skew time				3.6	ns
t_r	Output signal rise time	See Figure 6.		1		ns
t_f	Output signal fall time			1		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 7.		6		µs

(1) Also known as pulse skew.

6.11 Switching Characteristics: V_{CC1} at 5 V ±10%, V_{CC2} at 3.3 V ±10%

T_J = –55°C to 136°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6.		10	18.5	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.5	6	ns
$t_{sk(pp)}$	Part-to-part skew time				6.3	ns
$t_{sk(o)}$	Channel-to-channel output skew time				7	ns
t_r	Output signal rise time	See Figure 6.		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 7.		6		µs

(1) Also known as pulse skew.

6.12 Switching Characteristics: V_{CC1} at 3.3 V ±10%, V_{CC2} at 5 V ±10%

T_J = –55°C to 136°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6.		10	21	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			0.5	4.5	ns
$t_{sk(pp)}$	Part-to-part skew time				8.5	ns
$t_{sk(o)}$	Channel-to-channel output skew time				10.8	ns
t_r	Output signal rise time	See Figure 6.		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 7.		6		µs

(1) Also known as pulse skew.

6.13 Switching Characteristics: V_{CC1} and V_{CC2} at 3.3 V ±10%

T_J = –55°C to 136°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time	See Figure 6.		12	22.5	ns
PWD (1)	Pulse width distortion $\|t_{PHL} - t_{PLH}\|$			1	5.2	ns
$t_{sk(pp)}$	Part-to-part skew time				6.8	ns
$t_{sk(o)}$	Channel-to-channel output skew time				7.8	ns
t_r	Output signal rise time	See Figure 6.		2		ns
t_f	Output signal fall time			2		ns
t_{fs}	Fail-safe output delay time from input power loss	See Figure 7.		6		µs

(1) Also known as pulse skew.

6.14 Typical Characteristics

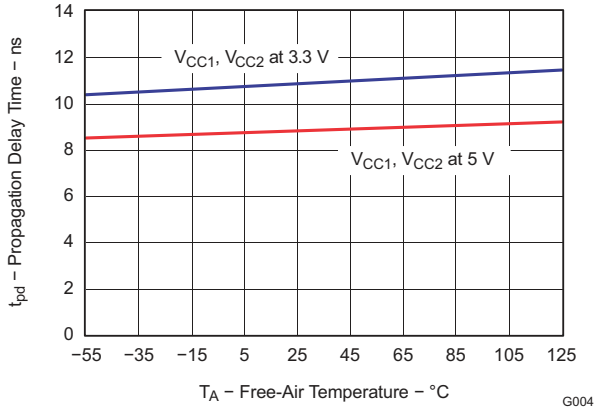


Figure 1. Propagation Delay Time vs Free-Air Temperature

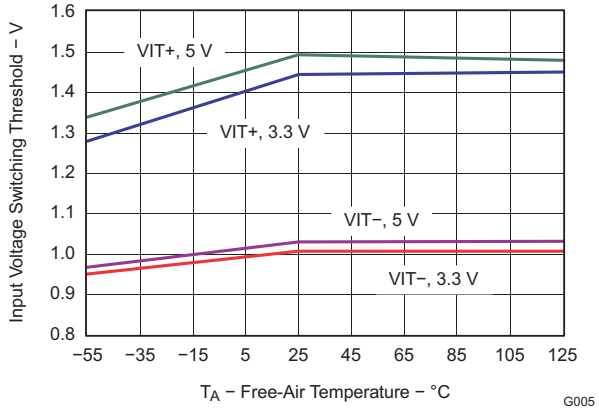


Figure 2. Input Voltage Switching Threshold vs Free-Air Temperature

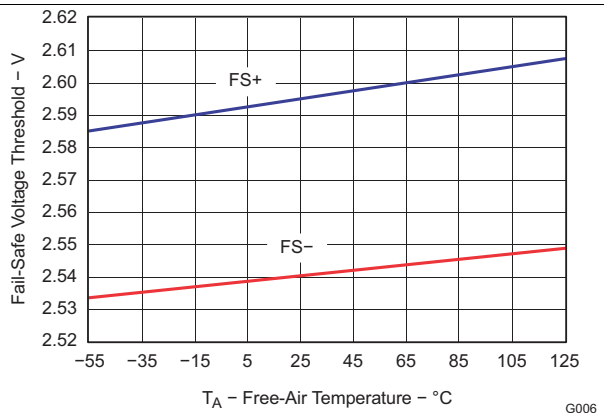


Figure 3. Fail-Safe Voltage Threshold vs Free-Air Temperature

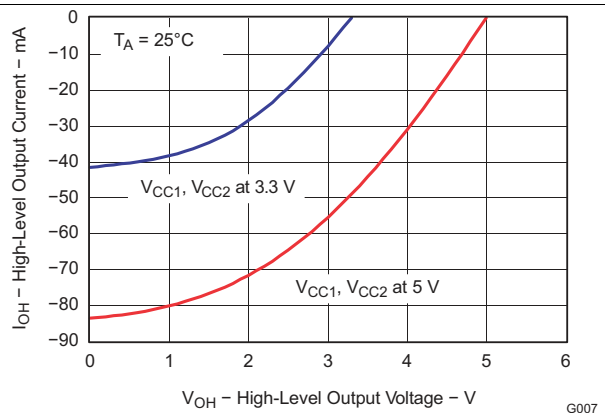


Figure 4. High-Level Output Current vs High-Level Output Voltage

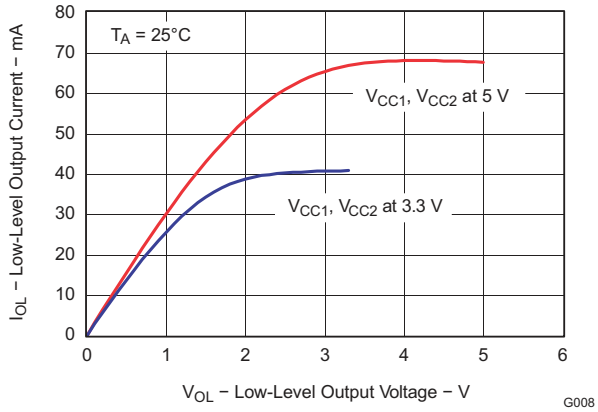
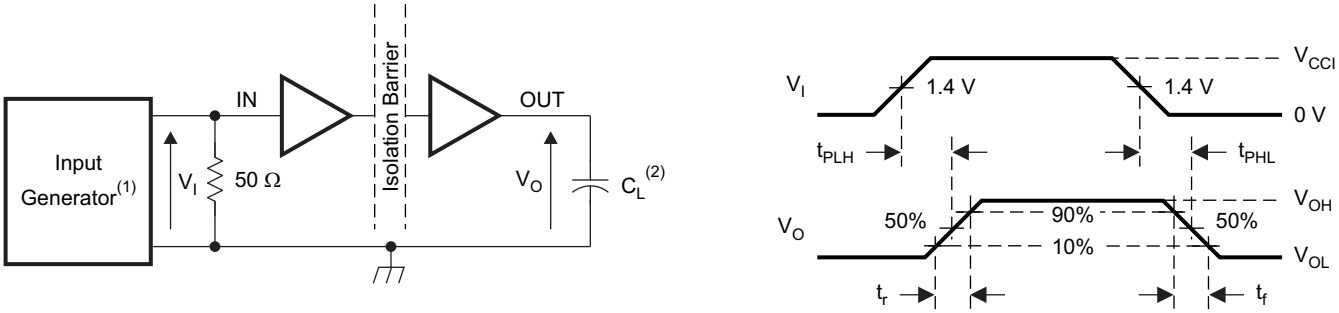


Figure 5. Low-Level Output Current vs Low-Level Output Voltage

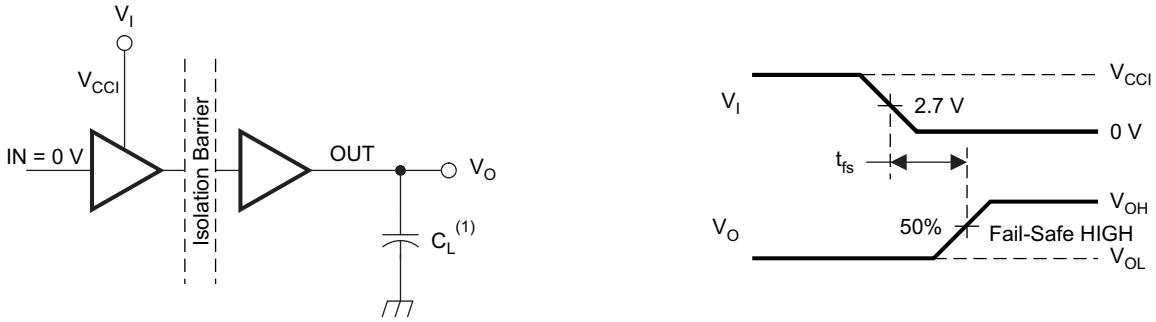
7 Parameter Measurement Information



(1) The input pulse is supplied by a generator having the following characteristics: PRR ≤ 50 kHz, 50% duty cycle, t_r ≤ 3 ns, t_f ≤ 3 ns, Z_O = 50 Ω. At the input, a 50-Ω resistor is required to terminate the Input Generator signal. It is not needed in actual application.

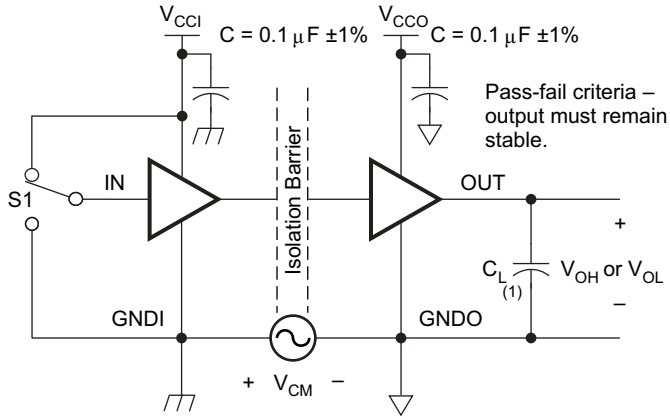
(2) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 6. Switching Characteristic Test Circuit and Voltage Waveforms



(1) C_L = 15 pF ± 20% includes instrumentation and fixture capacitance.

Figure 7. Fail-Safe Output Delay-Time Test Circuit and Voltage Waveforms



(1) C_L = 15 pF and includes instrumentation and fixture capacitance within ±20%.

Figure 8. Common-Mode Transient Immunity Test Circuit

8 Detailed Description

8.1 Overview

The ISO7421 digital isolator has two isolated channels. The ISO7421 provides galvanic isolation up to 2500VRMS for one minute per UL. The isolator in Figure 9 is based on a capacitive isolation barrier technique. The I/O channel of the device consists of two internal data channels, a high-frequency channel (HF) with a bandwidth from 100 kbps up to 1 Mbps, and a low-frequency channel (LF) covering the range from 100 kbps down to DC. In principle, a single- ended input signal entering the HF-channel is split into a differential signal via the inverter gate at the input. The following capacitor-resistor networks differentiate the signal into transients, which then are converted into differential pulses by two comparators. The comparator outputs drive a NOR-gate flip-flop whose output feeds an output multiplexer. A decision logic (DCL) at the driving output of the flip-flop measures the durations between signal transients. If the duration between two consecutive transients exceeds a certain time limit, (as in the case of a low-frequency signal), the DCL forces the output-multiplexer to switch from the high- to the low-frequency channel.

Because low-frequency input signals require the internal capacitors to assume prohibitively large values, these signals are pulse-width modulated (PWM) with the carrier frequency of an internal oscillator, thus creating a sufficiently high frequency signal, capable of passing the capacitive barrier. As the input is modulated, a low-pass filter (LPF) is needed to remove the high-frequency carrier from the actual data before passing it on to the output multiplexer.

8.2 Functional Block Diagram

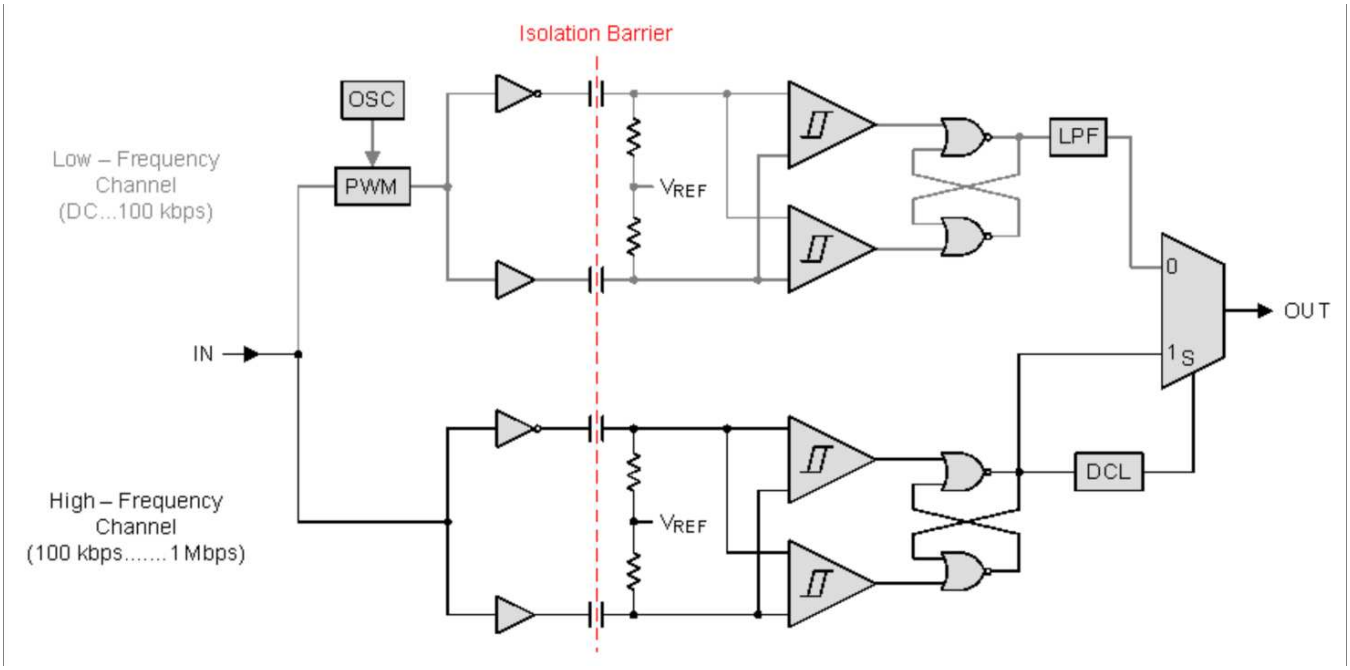


Figure 9. Conceptual Block Diagram of a Digital Capacitive Isolator

8.3 Feature Description

8.3.1 Insulation Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER(1)		TEST CONDITIONS	SPECIFICATION	UNIT
DIN V VDE V 0884-10 (VDE V 0884-10):2006-12				
V_{IORM}	Maximum working insulation voltage		566	V_{PK}
V_{PR}	Input-to-output test voltage	t = 1 s (100% production), partial discharge 5 pC	1062	V_{PK}
V_{IOTM}	Transient overvoltage	t = 60 s (qualification)	4242	V_{PK}
		t = 1 s (100% production)		
R_S	Insulation resistance	V_{IO} = 500 V at T_S	$>10^9$	Ω
	Pollution degree		2	
UL 1577				
V_{ISO}	Isolation voltage per UL	$V_{TEST} = V_{ISO}$ = 2500 V_{RMS}, t = 60 s (qualification) V_{TEST} = 1.2 x V_{ISO} = 3000 V_{RMS}, t = 1 s (100% production)	2500	V_{RMS}

(1) Climatic Classification 40/125/21

Table 1. IEC 60664-1 Ratings Table

PARAMETER	TEST CONDITIONS	SPECIFICATION
Material group		II
Installation classification	Rated mains voltage ≤ 150 V_{RMS}	I–IV
	Rated mains voltage ≤ 300 V_{RMS}	I–III

8.3.2 Package Characteristics

Over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
L(I01)	Minimum air gap (clearance)	Shortest terminal-to-terminal distance through air	4			mm
L(I02)	Minimum external tracking (creepage)	Shortest terminal-to-terminal distance across the package surface	4			mm
CTI	Tracking resistance (comparative tracking index)	DIN EN 60112 (VDE 0303-11); IEC 60112	>400			V
DTI	Distance through the insulation	Minimum internal gap (internal clearance)	0.014			mm
R_{IO}	Isolation resistance, input to output(1)	V_{IO} = 500 V, T_A = 25°C		$>10^{12}$		Ω
		V_{IO} = 500 V, 100°C ≤ T_A ≤ max		$>10^{11}$		Ω
C_{IO}	Barrier capacitance, input to output(1)	V_{IO} = 0.4 sin (2πft), f = 1 MHz		1		pF
C_I	Input capacitance(2)	$V_I = V_{CC}/2$ + 0.4 sin (2πft), f = 1 MHz, V_{CC} = 5 V		1		pF

(1) All pins on each side of the barrier tied together creating a two-terminal device.
(2) Measured from input pin to ground.

NOTE

Creepage and clearance requirements should be applied according to the specific equipment isolation standards of an application. Care should be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed-circuit board do not reduce this distance.

Creepage and clearance on a printed-circuit board become equal in certain cases. Techniques such as inserting grooves and/or ribs on a printed circuit board are used to help increase these specifications.

8.3.3 Safety Limiting Values

Safety limiting intends to prevent potential damage to the isolation barrier upon failure of input or output circuitry. A failure of the I/O can allow low resistance to ground or the supply and, without current limiting, dissipate sufficient power to overheat the die and damage the isolation barrier, potentially leading to secondary system failures.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	$R_{\theta JA}$ = 212°C/W, V_I = 5.25 V, T_J = 150°C, T_A = 25°C			112	mA
		$R_{\theta JA}$ = 212°C/W, V_I = 3.45 V, T_J = 150°C, T_A = 25°C			171	
T_S	Maximum safety temperature				150	°C

The safety-limiting constraint is the absolute-maximum junction temperature specified in the *Absolute Maximum Ratings* table. The power dissipation and junction-to-air thermal impedance of the device installed in the application hardware determines the junction temperature. The assumed junction-to-air thermal resistance in the *Thermal Information* table is that of a device installed in the JESD51-3, Low-Effective-Thermal-Conductivity Test Board for Leaded Surface-Mount Packages and is conservative. The power is the recommended maximum input voltage times the current. The junction temperature is then the ambient temperature plus the power times the junction-to-air thermal resistance.

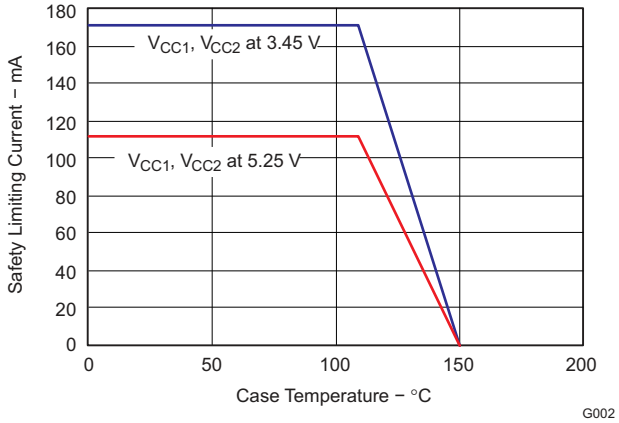


Figure 10. $R_{\theta JC}$ Thermal Derating Curve per VDE

8.3.4 Regulatory Information

VDE	CSA	UL	CQC
Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 and DIN EN 61010-1 (VDE 0411-1): 2011-07	Approved under CSA Component Acceptance Notice #5A	Recognized under UL1577 Component Recognition Program(1)	Certified according to GB4943.1-2011
Basic Insulation Maximum Transient Overvoltage, 4242 V_{PK} Maximum Working Voltage, 566 V_{PK}	Basic insulation per CSA 60950-1-07 and IEC 60950-1 (2nd Ed), 390 VRMS maximum working voltage	Single Protection, 2500 V_{RMS}	Basic Insulation, Altitude ≤ 5000 m, Tropical Climate, 250 V_{RMS} maximum working voltage
Certificate number: 40016131	Master contract number: 220991	File number: E181974	Certificate number: CQC14001109540

(1) Production tested ≥ 3000 V_{RMS} for 1 second in accordance with UL 1577.

8.4 Device Functional Modes

Table 2 shows the device functions.

Table 2. Function Table(1)

VCCI	VCCO	INPUT INA, INB	OUTPUT OUTA, OUTB
PU	PU	H	H
		L	L
		Open	H(2)
PD	PU	X	H(2)
X	PD	X	Undetermined

(1) V_{CCI} = Input-side power supply; V_{CCO} = Output-side power supply; PU = Powered up (V_{CC} ≥ 3.15 V); PD = Powered down (V_{CC} ≤ 2.1 V); X = Irrelevant; H = High level; L = Low level
(2) In fail-safe condition, output defaults to high level.

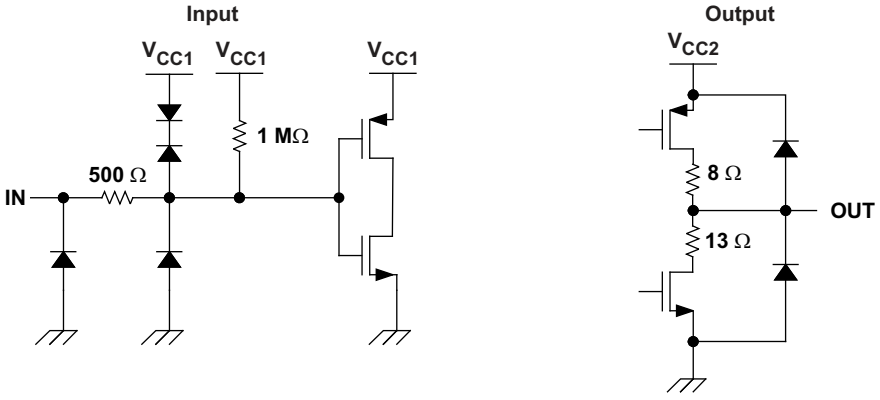


Figure 11. Device I/O Schematics

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The ISO7421-EP device uses a single-ended TTL-logic switching technology. Its supply voltage range is from 3.15 V to 5.25 V for both supplies, V_{CC1} and V_{CC2}. When designing with digital isolators, it is important to keep in mind that due to the single-ended design structure, digital isolators do not conform to any specific interface standard and are only intended for isolating single-ended CMOS or TTL digital signal lines. The isolator is typically placed between the data controller (that is, µC or UART), and a data converter or a line transceiver, regardless of the interface type or standard.

9.2 Typical Application

ISO7421-EP can be used with Texas Instruments' mixed signal micro-controller, digital-to-analog converter, transformer driver, and voltage regulator to create an isolated 4-20 mA current loop.

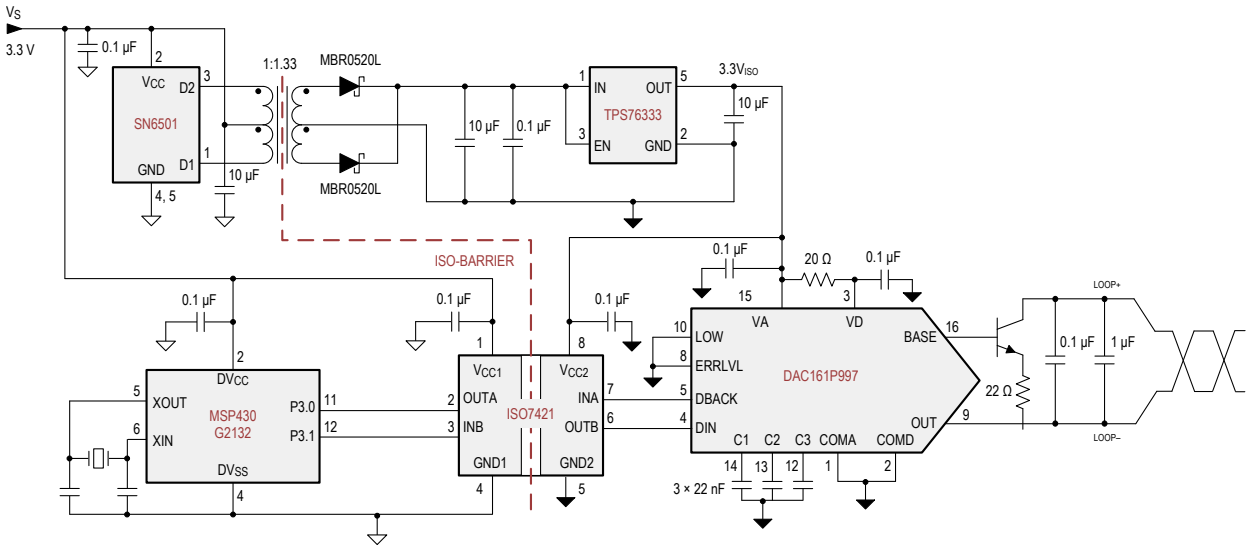


Figure 12. Isolated 4- to 20-mA Current Loop

9.2.1 Design Requirements

For applications that require isolation in place of using x-fmr to provide isolation, ISO7421-EP meets the system needs with small size. Unlike optocouplers, which require external components to improve performance, provide bias, or limit current, the ISO7421-EP device only requires two external bypass capacitors to operate.

Typical Application (continued)

9.2.2 Detailed Design Procedure

ISO7421 digital isolator containing two channels has logic input and output buffer isolated by silicon dioxide (SiO2) isolation barrier. When using ISO7421 in conjunction with isolated power supplies, these devices prevent noise currents on a data bus or other circuit from entering the local ground and interfering with or damaging sensitive circuitry. ISO7421 are specified for signaling rate up to 1Mbps. These devices also transmit data with much shorter pulse widths, in most cases, because of their fast response time. Designer must add external filtering to remove spurious signals with input pulse duration < 20 ns.

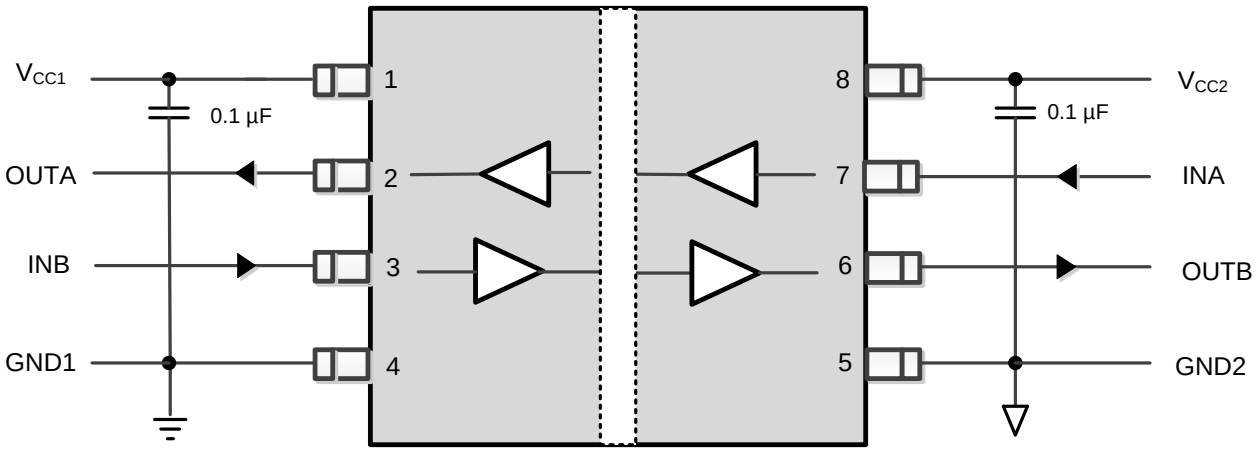


Figure 13. Typical ISO7421-EP Circuit Hookup

9.2.3 Application Curve

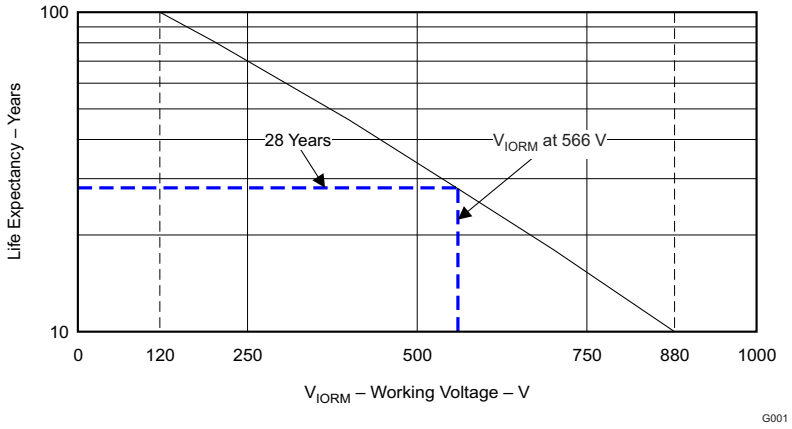


Figure 14. Life Expectancy vs Working Voltage

10 Power Supply Recommendations

Install high quality X7R capacitors typically 0.1 µF close to the device. To ensure reliable operation at all data rates and supply voltages, a 0.1 µF bypass capacitor is recommended at input and output supply pins (V_{CC1} and V_{CC2}). The capacitors should be placed as close to the supply pins as possible. If only a single primary-side power supply is available in an application, isolated power can be generated for the secondary-side with the help of a transformer driver such as Texas Instruments' SN6501. For such applications, detailed power supply design and transformer selection recommendations are available in SN6501 datasheet (SLLSEA0).

11 Layout

11.1 Layout Guidelines

There are several signals that conduct fast charging current or voltages that can interact with stray inductance or parasitic capacitors to generate noise. Thus to eliminate these problems Vin ins of ISO7421 should be bypass to gnd with low esr ceramic bypass capacitor with X7R dielectric. A minimum of four layers is required to accomplish a low EMI PCB design (see Figure 15). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer, ground plane, power plane and low-frequency signal layer.

- Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects between the isolator and the transmitter and receiver circuits of the data link.
- Placing a solid ground plane next to the high-speed signal layer establishes controlled impedance for transmission line interconnects and provides an excellent low-inductance path for the return current flow.
- Placing the power plane next to the ground plane creates additional high-frequency bypass capacitance of approximately 100pF/in^2.
- Routing the slower speed control signals on the bottom layer allows for greater flexibility as these signal links usually have margin to tolerate discontinuities such as vias.

If an additional supply voltage plane or signal layer is needed, add a second power / ground plane system to the stack to keep it symmetrical. This makes the stack mechanically stable and prevents it from warping. Also the power and ground plane of each power system can be placed closer together, thus increasing the high-frequency bypass capacitance significantly.

For detailed layout recommendations, see Application Note *Digital Isolator Design Guide*, SLLA284.

11.1.1 PCB Material

For digital circuit boards operating below 150 Mbps, (or rise and fall times higher than 1 ns), and trace lengths of up to 10 inches, use standard FR-4 epoxy-glass as PCB material. FR-4 (Flame Retardant 4) meets the requirements of Underwriters Laboratories UL94-V0, and is preferred over cheaper alternatives due to its lower dielectric losses at high frequencies, less moisture absorption, greater strength and stiffness, and its self-extinguishing flammability-characteristics.

11.2 Layout Example

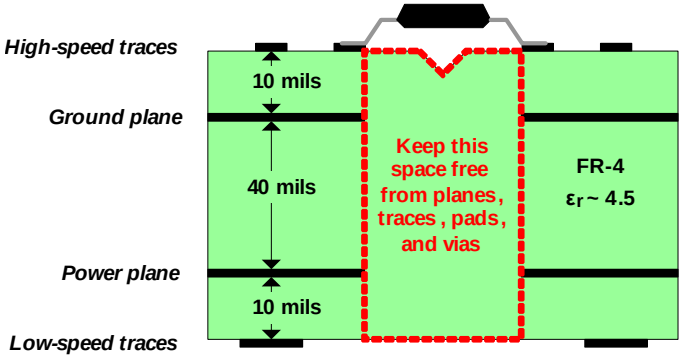


Figure 15. Recommended Layer Stack

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- *SN6501 Transformer Driver for Isolated Power Supplies*, SLLSEA0
- *Isolation Glossary*, SLLA353
- *Digital Isolator Design Guide*, SLLA284

12.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.3 Trademarks

DeviceNet, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

12.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ISO7421MDREP	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7421EP	Samples
V62/16605-01XE	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	7421EP	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

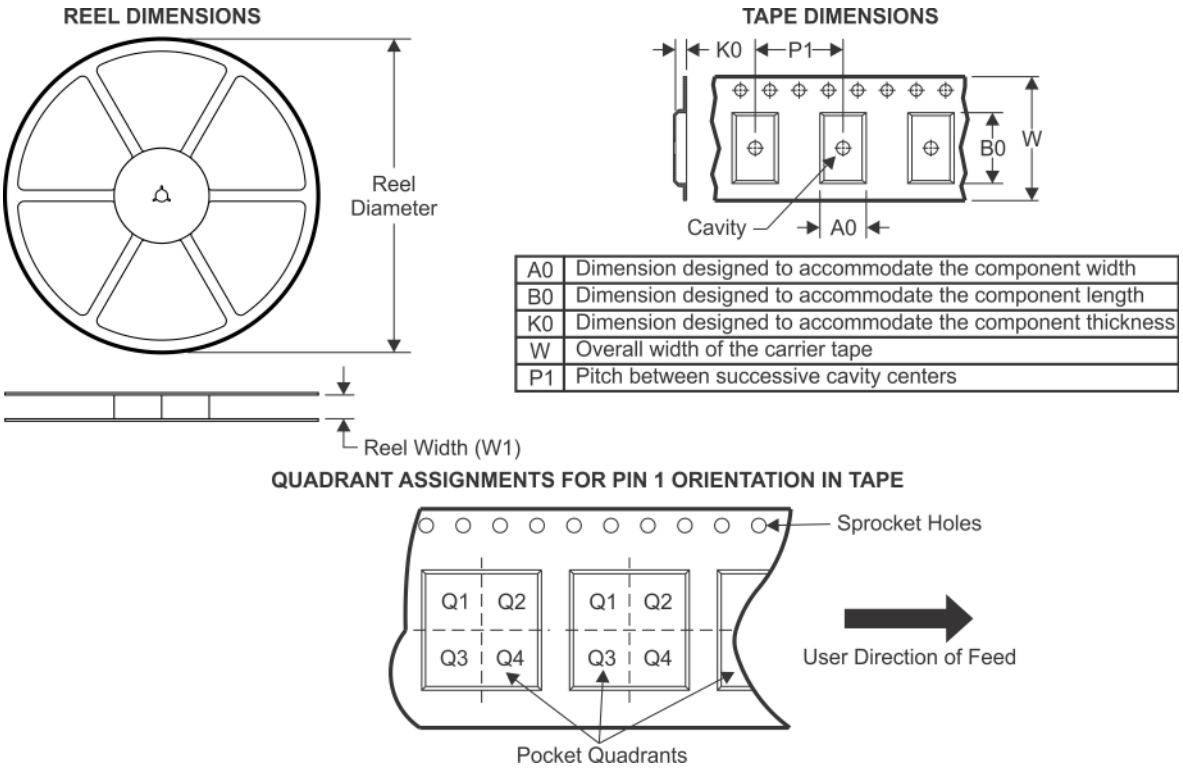
OTHER QUALIFIED VERSIONS OF ISO7421-EP :

- Catalog: ISO7421

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

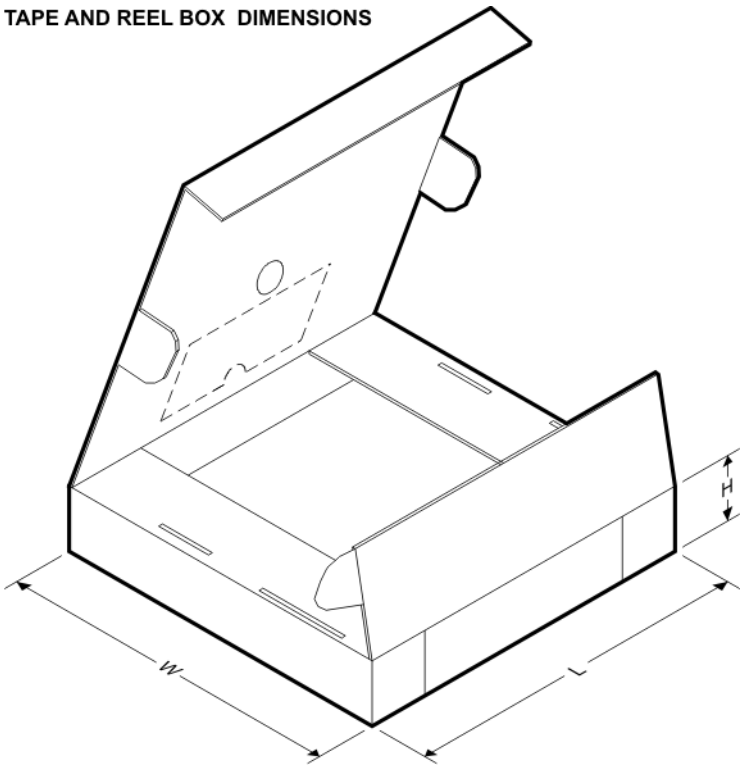


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

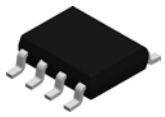
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ISO7421MDREP	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ISO7421MDREP	SOIC	D	8	2500	350.0	350.0	43.0

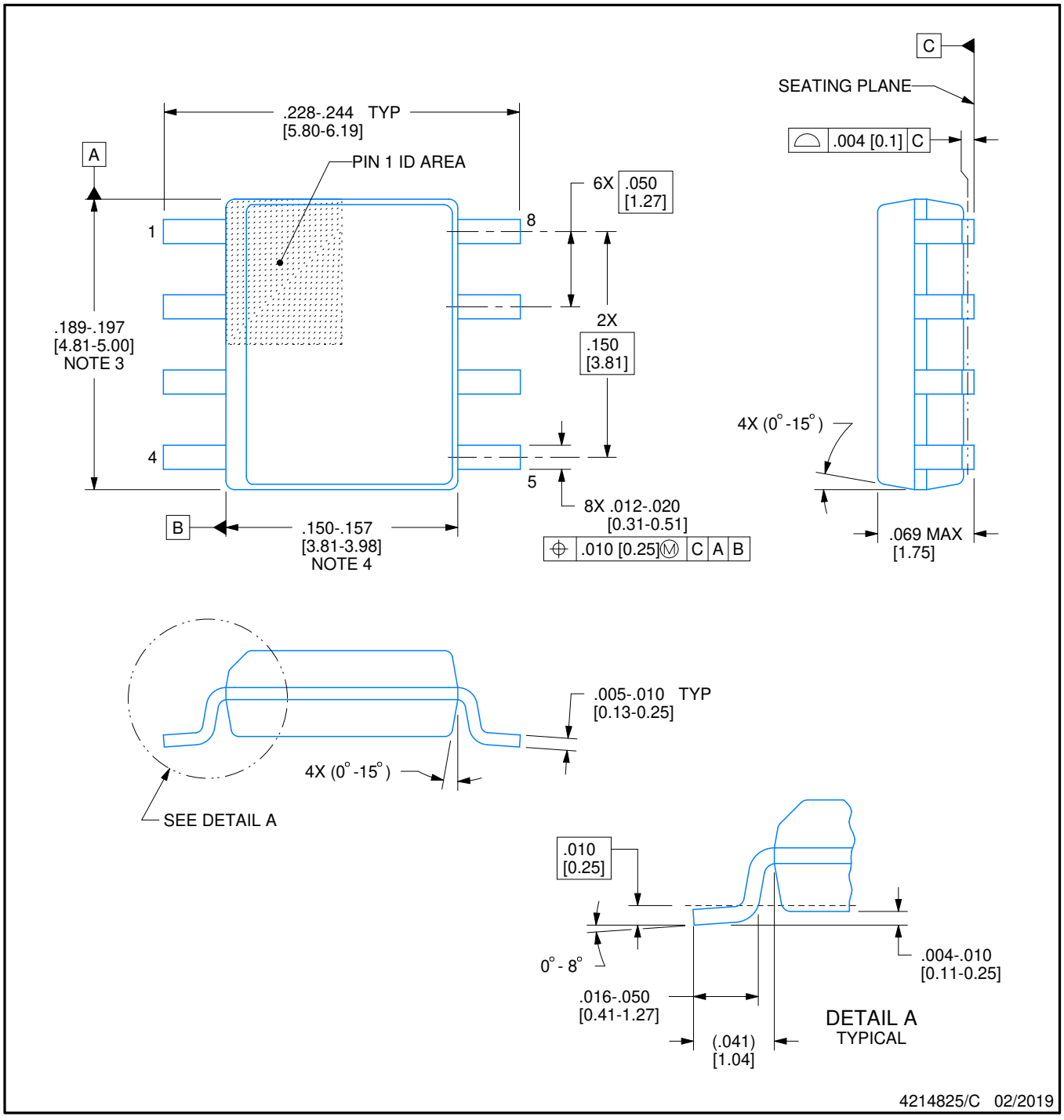


PACKAGE OUTLINE

D0008A

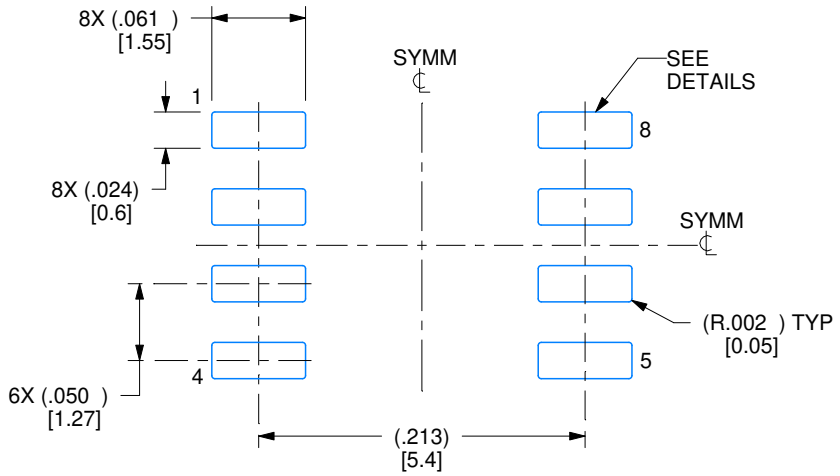
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

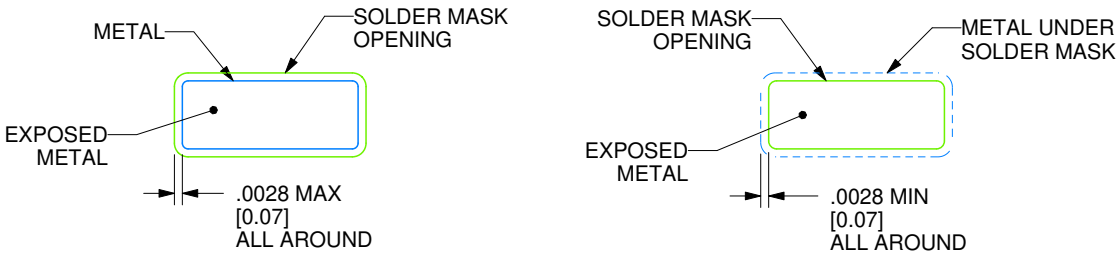


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

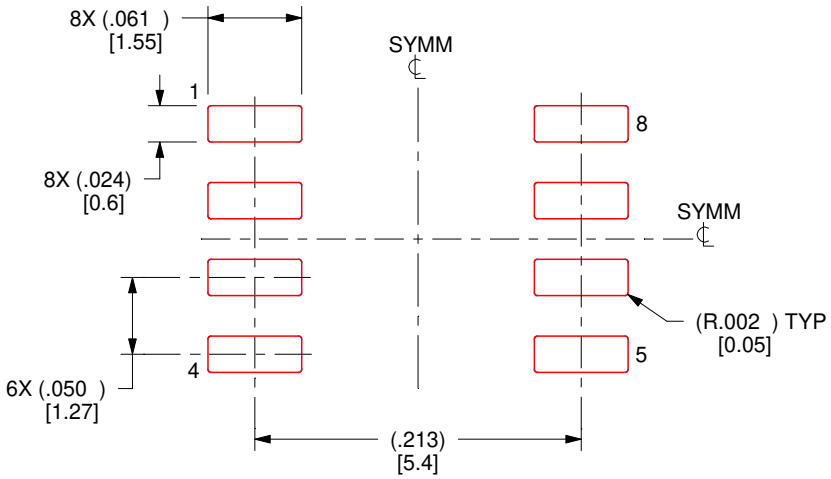
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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