

NTD5C684NL

Power MOSFET

60 V, 16.5 mΩ, 27 A, Single N-Channel

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit	
Drain-to-Source Voltage	V_{DSS}	60	V	
Gate-to-Source Voltage	V_{GS}	± 20	V	
Continuous Drain Current $R_{\theta JC}$ (Notes 1 & 3)	Steady State	$T_C = 25^\circ\text{C}$	27	A
		$T_C = 100^\circ\text{C}$	19	
Power Dissipation $R_{\theta JC}$ (Note 1)	Steady State	$T_C = 25^\circ\text{C}$	25	W
		$T_C = 100^\circ\text{C}$	12	
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2 & 3)	Steady State	$T_A = 25^\circ\text{C}$	10	A
		$T_A = 100^\circ\text{C}$	7.2	
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	Steady State	$T_A = 25^\circ\text{C}$	3.6	W
		$T_A = 100^\circ\text{C}$	1.8	
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	130	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to 175	$^\circ\text{C}$	
Source Current (Body Diode)	I_S	28	A	
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, I_{L(pk)} = 2.0 \text{ A}$)	E_{AS}	93	mJ	
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case (Drain) (Note 1)	$R_{\theta JC}$	6.0	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	41	

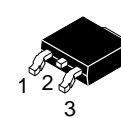
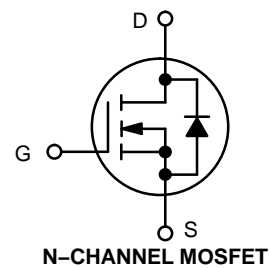
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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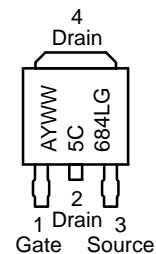
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$V_{(BR)DSS}$	$R_{DS(on)}$	I_D
60 V	16.5 mΩ @ 10 V	27 A
	24.3 mΩ @ 4.5 V	



DPAK
CASE 369C
STYLE 2

MARKING DIAGRAM & PIN ASSIGNMENT



A = Assembly Location
Y = Year
WW = Work Week
5C684L = Device Code
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

NTD5C684NL

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	60			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			27		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 60\text{ V}$	$T_J = 25^\circ\text{C}$		10	μA
			$T_J = 125^\circ\text{C}$		250	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = 20\text{ V}$			100	nA

ON CHARACTERISTICS (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 20\ \mu\text{A}$	1.2		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.5		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 15\text{ A}$		13.7	16.5	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 15\text{ A}$		19.4	24.3	
Forward Transconductance	g_{FS}	$V_{DS} = 5.0\text{ V}, I_D = 15\text{ A}$		30		S

CHARGES, CAPACITANCES AND GATE RESISTANCES

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = 25\text{ V}$		700		pF
Output Capacitance	C_{oss}			300		
Reverse Transfer Capacitance	C_{rss}			13		
Total Gate Charge	$Q_{G(TOT)}$	$V_{DS} = 30\text{ V}, I_D = 15\text{ A}$	$V_{GS} = 4.5\text{ V}$	4.6		nC
			$V_{GS} = 10\text{ V}$	9.6		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}, I_D = 15\text{ A}$		1.2		nC
Gate-to-Source Charge	Q_{GS}			2.0		
Gate-to-Drain Charge	Q_{GD}			1.2		
Plateau Voltage	V_{GP}			2.9		

SWITCHING CHARACTERISTICS (Note 5)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 30\text{ V}, I_D = 15\text{ A}, R_G = 2.5\ \Omega$		8.0		ns
Rise Time	t_r			43		
Turn-Off Delay Time	$t_{d(off)}$			25		
Fall Time	t_f			40		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 15\text{ A}$	$T_J = 25^\circ\text{C}$		0.9	1.2	V
			$T_J = 125^\circ\text{C}$		0.8		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_S/dt = 100\text{ A}/\mu\text{s}, I_S = 15\text{ A}$		20		ns	
Charge Time	t_a			10			
Discharge Time	t_b			10			
Reverse Recovery Charge	Q_{RR}			10			nC

4. Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2\%$.
5. Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

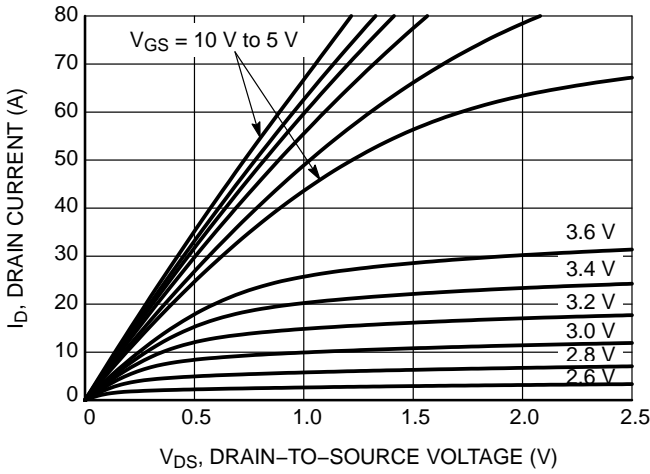


Figure 1. On-Region Characteristics

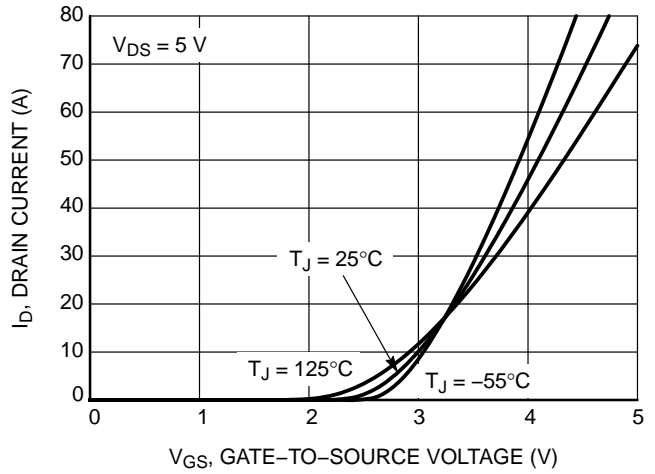


Figure 2. Transfer Characteristics

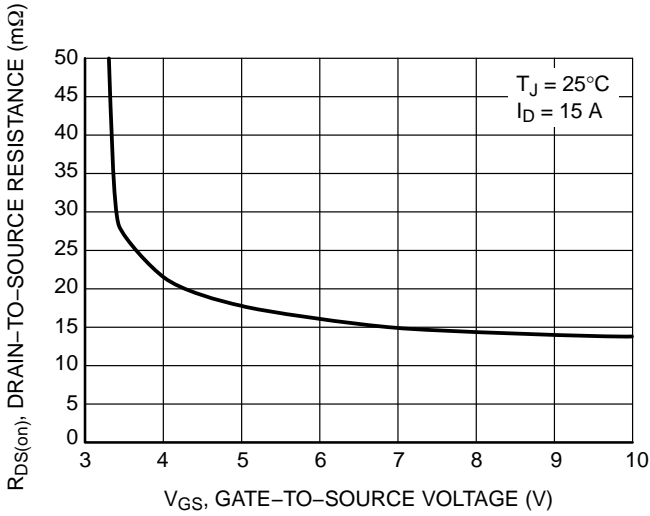


Figure 3. On-Resistance vs. Gate-to-Source Voltage

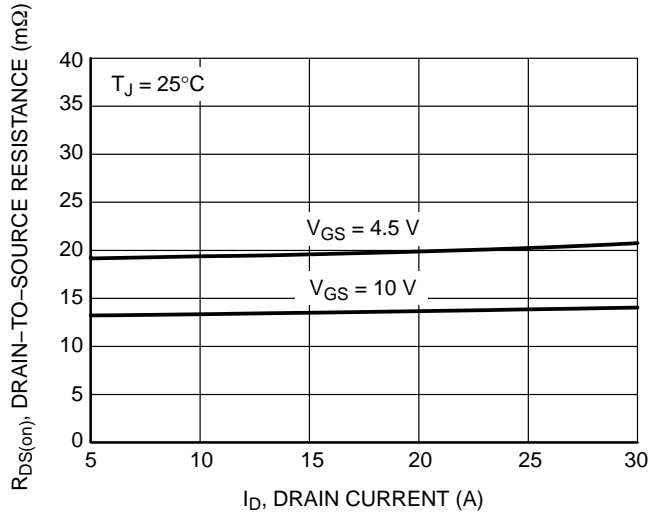


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

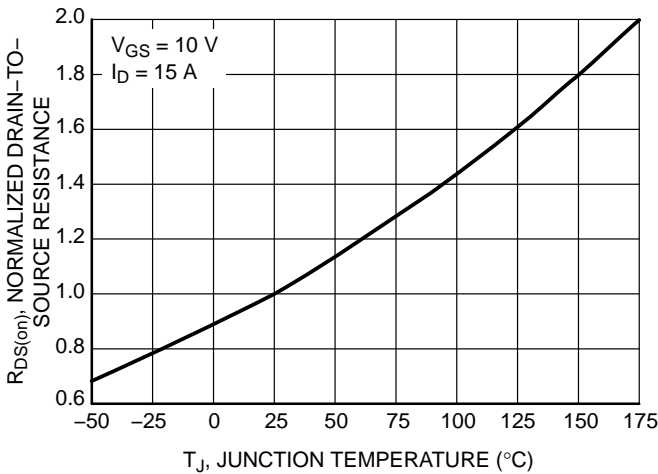


Figure 5. On-Resistance Variation with Temperature

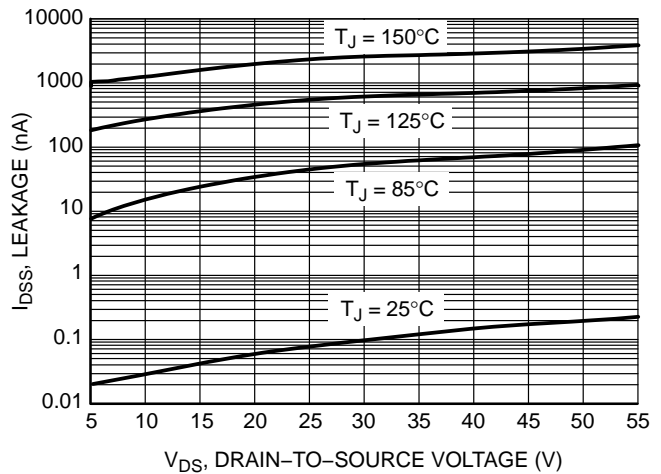


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

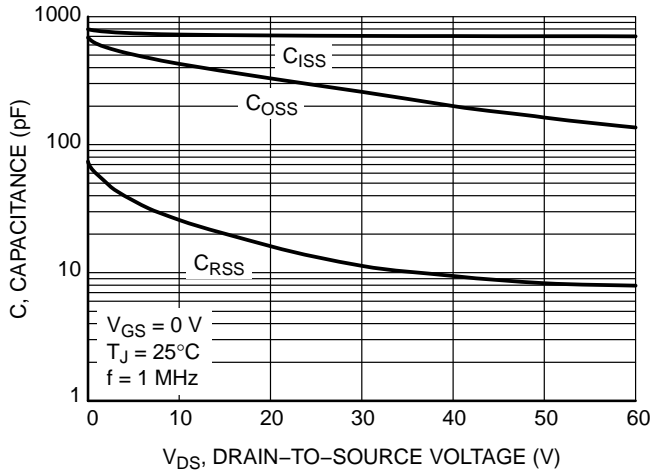


Figure 7. Capacitance Variation

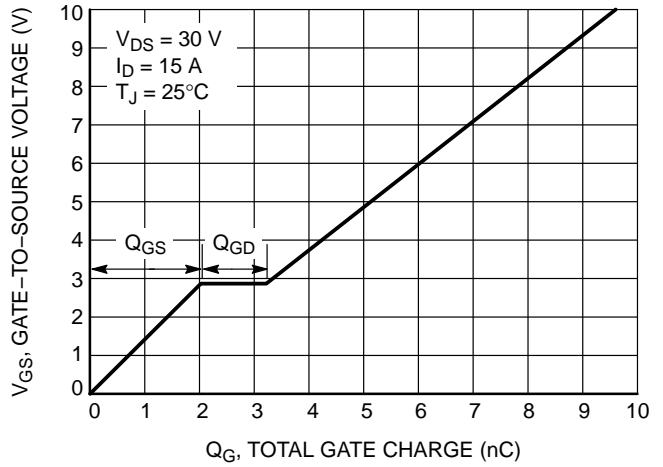


Figure 8. Gate-to-Source vs. Total Charge

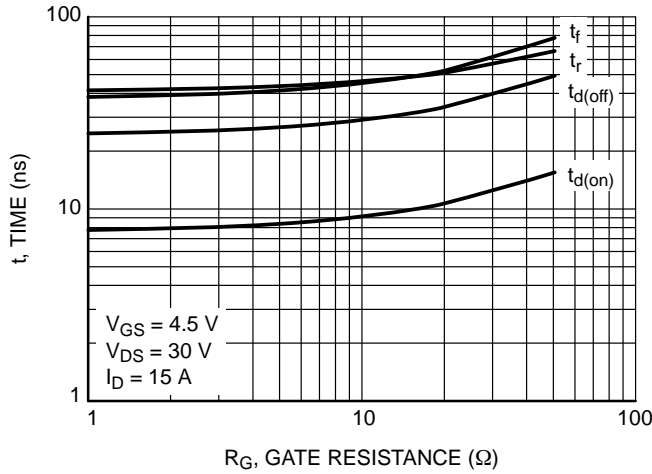


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

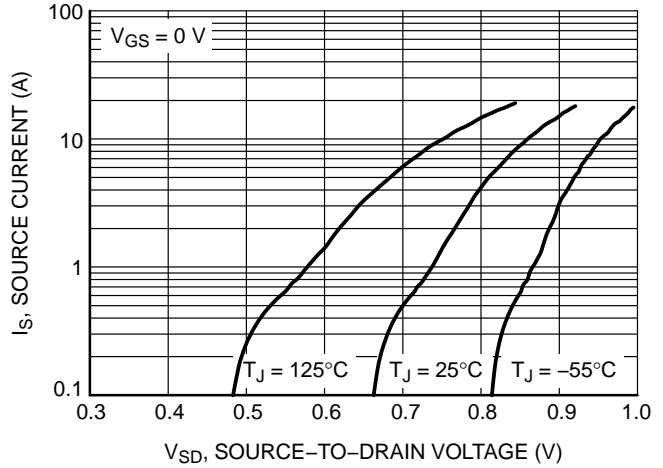


Figure 10. Diode Forward Voltage vs. Current

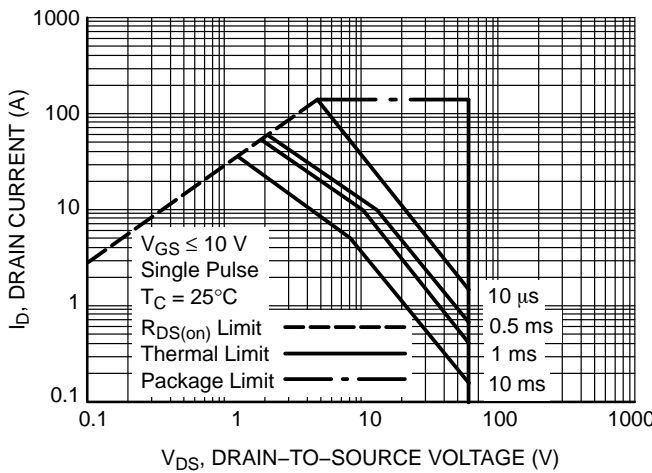


Figure 11. Maximum Rated Forward Biased Safe Operating Area

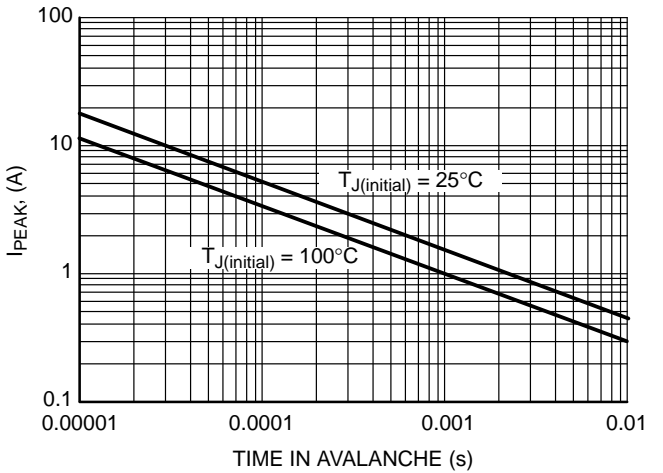


Figure 12. Maximum Drain Current vs. Time in Avalanche

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TYPICAL CHARACTERISTICS

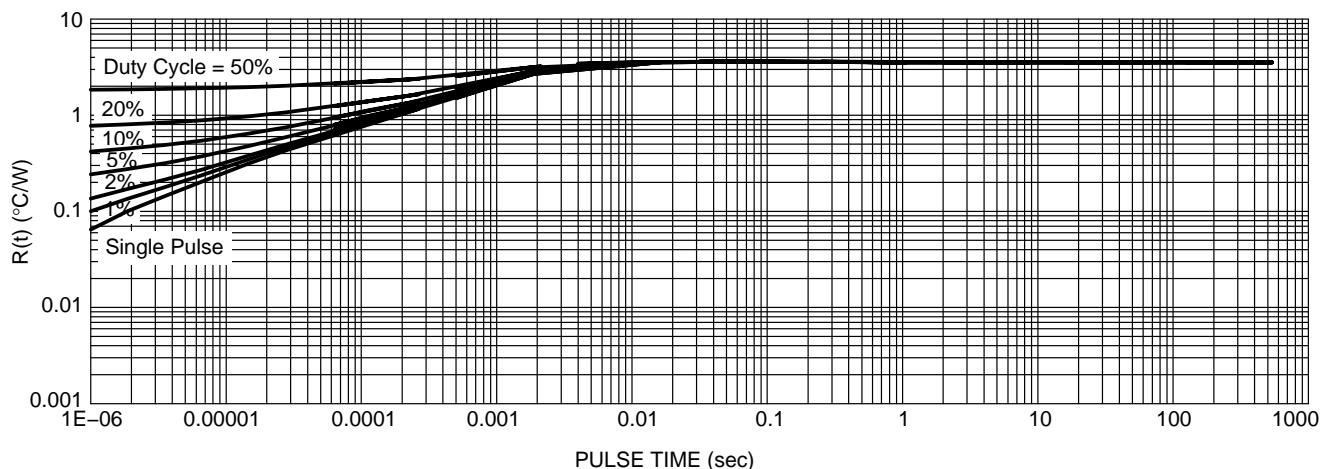


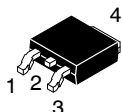
Figure 13. Thermal Response

ORDERING INFORMATION

Order Number	Package	Shipping [†]
NTD5C684NLT4G	DPAK (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

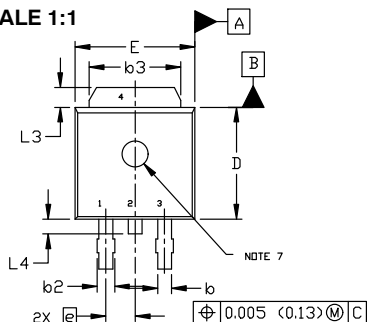
MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



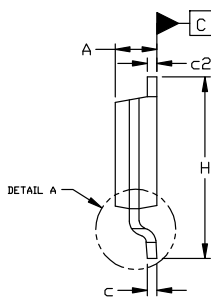
DPAK (SINGLE GAUGE) CASE 369C ISSUE G

DATE 31 MAY 2023

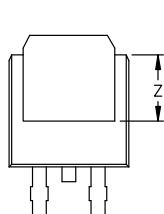
SCALE 1:1



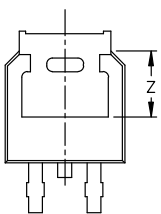
TOP VIEW



SIDE VIEW

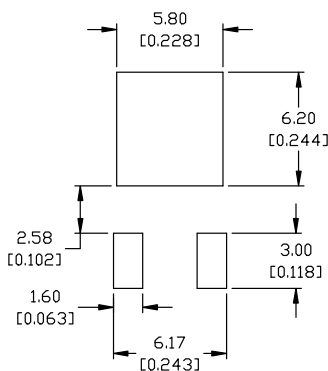


BOTTOM VIEW



BOTTOM VIEW

ALTERNATE CONSTRUCTIONS



RECOMMENDED MOUNTING FOOTPRINT*

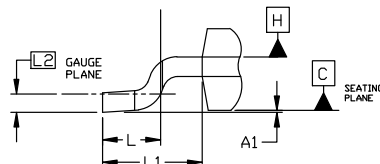
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

- | | | | | |
|---|---|--|--|---|
| STYLE 1:
PIN 1. BASE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN | STYLE 3:
PIN 1. ANODE
2. CATHODE
3. ANODE
4. CATHODE | STYLE 4:
PIN 1. CATHODE
2. ANODE
3. GATE
4. ANODE | STYLE 5:
PIN 1. GATE
2. ANODE
3. CATHODE
4. ANODE |
| STYLE 6:
PIN 1. MT1
2. MT2
3. GATE
4. MT2 | STYLE 7:
PIN 1. GATE
2. COLLECTOR
3. EMITTER
4. COLLECTOR | STYLE 8:
PIN 1. N/C
2. CATHODE
3. ANODE
4. CATHODE | STYLE 9:
PIN 1. ANODE
2. CATHODE
3. RESISTOR ADJUST
4. CATHODE | STYLE 10:
PIN 1. CATHODE
2. ANODE
3. CATHODE
4. ANODE |

NOTES:

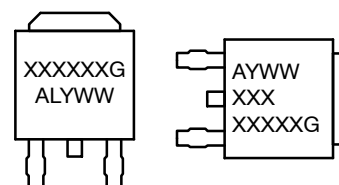
- DIMENSIONING AND TOLERANCING ASME Y14.5M, 1994.
- CONTROLLING DIMENSION: INCHES
- THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3, AND Z.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
- DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
- DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.
- OPTIONAL MOLD FEATURE.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.028	0.045	0.72	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090	BSC	2.29	BSC
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.114	REF	2.90	REF
L2	0.020	BSC	0.51	BSC
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---



DETAIL A
ROTATED 90° CW

GENERIC MARKING DIAGRAM*



IC

Discrete

- XXXXXX = Device Code
- A = Assembly Location
- L = Wafer Lot
- Y = Year
- WW = Work Week
- G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	DPAK (SINGLE GAUGE)	PAGE 1 OF 1

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