64 Mb (8 MB) GL-S MIRRORBIT™ Flash

Parallel, 3.0 V

Distinctive characteristics

- CMOS 3.0 V core with versatile I/O

Architectural advantages

- Single power supply operation
- Manufactured on 65-nm MIRRORBIT™ process technology
- Secure silicon region
  - 128-word/256-byte sector for permanent, secure identification through an 8-word / 16-byte random electronic serial number, accessible through a command sequence
  - Programmed and locked at the factory or by the customer
- Flexible sector architecture
  - 64 Mb (uniform sector models): One hundred twenty-eight 32-Kword (64-KB) sectors
  - 64 Mb (boot sector models): One hundred twenty-seven 32-Kword (64-KB) sectors + eight-4 Kword (8-KB) boot sectors
- Automatic error checking and correction (ECC) - internal hardware ECC with single bit error correction
- Enhanced versatile I/O control
  - All input levels (address, control, and DQ input levels) and outputs are determined by voltage on V_{IO} input. V_{IO} range is 1.65 V to V_{CC}
- Compatibility with JEDEC standards
  - Provides pinout and software compatibility for single-power supply flash, and superior inadvertent write protection
- 100,000 erase cycles per sector minimum
- 20-year data retention typical

Performance characteristics

- High performance
  - 70 ns access time
  - 8-word / 16-byte page read buffer
  - 15 ns page read time
  - 128-word / 256-byte write buffer which reduces overall programming time for multiple-word updates
- Low power consumption
  - 25 mA typical initial read current @ 5 MHz
  - 7.5 mA typical page read current @ 33 MHz
  - 50 mA typical erase / program current
  - 40 µA typical standby mode current
- Package options
  - 48-pin TSOP
  - 56-pin TSOP
  - 64-ball fortified BGA (LAA064 13 mm × 11 mm × 1.4 mm) (LAE064 9 mm × 9 mm × 1.4 mm)
  - 48-ball fine-pitch BGA (VBK048 8.15 mm × 6.15 mm × 1.0 mm)

- Temperature range
  - Industrial (–40°C to +85°C)
  - Industrial Plus (–40°C to +105°C)
  - Automotive, AEC-Q100 grade 3 (–40°C to +85°C)
  - Automotive, AEC-Q100 grade 2(–40°C to +105°C)

Software and hardware features

- Software features
  - Advanced sector protection: offers persistent sector protection and password sector protection
  - Program Suspend and Resume: read other sectors before programming operation is completed
  - Erase Suspend and Resume: read / program other sectors before an erase operation is completed
  - Data# polling and toggle bits provide status
  - Common flash interface (CFI) compliant: allows host system to identify and accommodate multiple flash devices
  - Unlock Bypass Program command reduces overall multiple-word programming time
- Hardware features
  - WP#/ACC input supports manufacturing programming operations (when high voltage is applied). Protects first or last sector regardless of sector protection settings on uniform sector models
  - Hardware reset input (RESET#) resets device
  - Ready/Busy# output (RY/BY#) detects program or erase cycle completion

General description

The S29GL-S mid density family of devices are 3.0-V single-power flash memory manufactured using 65-nm MIRRORBIT™ technology. The S29GL064S is a 64-Mb device organized as 4,194,304 words or 8,388,608 bytes. Depending on the model number, the devices have 16-bit wide data bus only, or a 16-bit wide data bus that can also function as an 8-bit wide data bus by using the BYTE# input. The devices can be programmed either in the host system or in standard EPROM programmers.

Access times as fast as 70 ns are available. Note that each access time has a specific operating voltage range (V_{CC}) as specified in the **"Product selector guide"** on page 6 and **"Ordering information"** on page 111. Package offerings include 48-pin TSOP, 56-pin TSOP, 48-ball fine-pitch BGA, and 64-ball fortified BGA, depending on model number. Each device has separate chip enable (CE#), write enable (WE#) and output enable (OE#) controls.

Each device requires only a **single 3.0-V power supply** for both read and write functions. In addition to a V_{CC} input, a high-voltage **accelerated program (ACC)** feature is supported through increased voltage on the WP#/ACC or ACC input. This feature is intended to facilitate system production.

The device is entirely command set compatible with the **JEDEC single-power-supply flash standard**. Commands are written to the device using standard microprocessor write timing. Write cycles also internally latch addresses and data needed for the programming and erase operations.

The **sector erase architecture** allows memory sectors to be erased and reprogrammed without affecting the data contents of other sectors. The device is fully erased when shipped from the factory.

The **advanced sector protection** features several levels of sector protection, which can disable both the program and erase operations in certain sectors. Persistent sector protection is a method that replaces the previous 12-V controlled protection method. Password sector protection is a highly sophisticated protection method that requires a password before changes to certain sectors are permitted.

Device programming and erasure are initiated through command sequences. Once a program or erase operation begins, the host system need only poll the DQ7 (Data# Polling) or DQ6 (toggle) **status bits** or monitor the **Ready/Busy# (RY/BY#)** output to determine whether the operation is complete. To facilitate programming, an **Unlock Bypass** mode reduces command sequence overhead by requiring only two write cycles to program data instead of four.

Hardware data protection measures include a low V_{CC} detector that automatically inhibits write operations during power transitions. The hardware sector protection feature disables both program and erase operations in any combination of sectors of memory. This can be achieved in-system or via programming equipment.

The **Erase Suspend / Erase Resume** feature allows the host system to pause an erase operation in a given sector to read or program any other sector and then complete the erase operation. The **Program Suspend / Program Resume** feature enables the host system to pause a program operation in a given sector to read any other sector and then complete the program operation.

The **hardware RESET# pin** terminates any operation in progress and resets the device, after which it is then ready for a new operation. The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the device, enabling the host system to read boot-up firmware from the flash memory device.

The device reduces power consumption in the **standby mode** when it detects specific voltage levels on CE# and RESET#, or when addresses are stable for a specified period of time.

The **Write Protect (WP#)** feature protects the first or last sector by asserting a logic low on the WP#/ACC pin or WP# pin, depending on model number. The protected sector is still protected even during accelerated programming.

The **Secure Silicon Region** provides a 128-word / 256-byte area for code or data that can be permanently protected. Once this sector is protected, no further changes within the sector can occur.

MIRRORBIT™ flash technology combines years of flash memory manufacturing experience to produce the highest levels of quality, reliability and cost effectiveness. The device electrically erases all bits within a sector simultaneously via hot-hole assisted erase. The data is programmed using hot electron injection.

Table of contents

Table of contents

1 Product selector guide

Table 1 Product selector guide for industrial temperature range (–40°C to +85°C)

Part number			S29GL064S	
Speed option	V_{CC} = 2.7 V–3.6 V	V_{IO} = 2.7 V–3.6 V	70	
		V_{IO} = 1.65 V–3.6 V		80
Maximum access time (ns)			70	80
Maximum CE# access time (ns)			70	80
Maximum page access time (ns)			15	25
Maximum OE# access time (ns)			15	25

Table 2 Product selector guide for industrial plus temperature range (–40°C to +105°C)

Part number			S29GL064S	
Speed option	V_{CC} = 2.7 V–3.6 V	V_{IO} = 2.7 V–3.6 V	80	
		V_{IO} = 1.65 V–3.6 V		90
Maximum access time (ns)			80	90
Maximum CE# access time (ns)			80	90
Maximum page access time (ns)			15	25
Maximum OE# access time (ns)			15	25

2 Block diagram

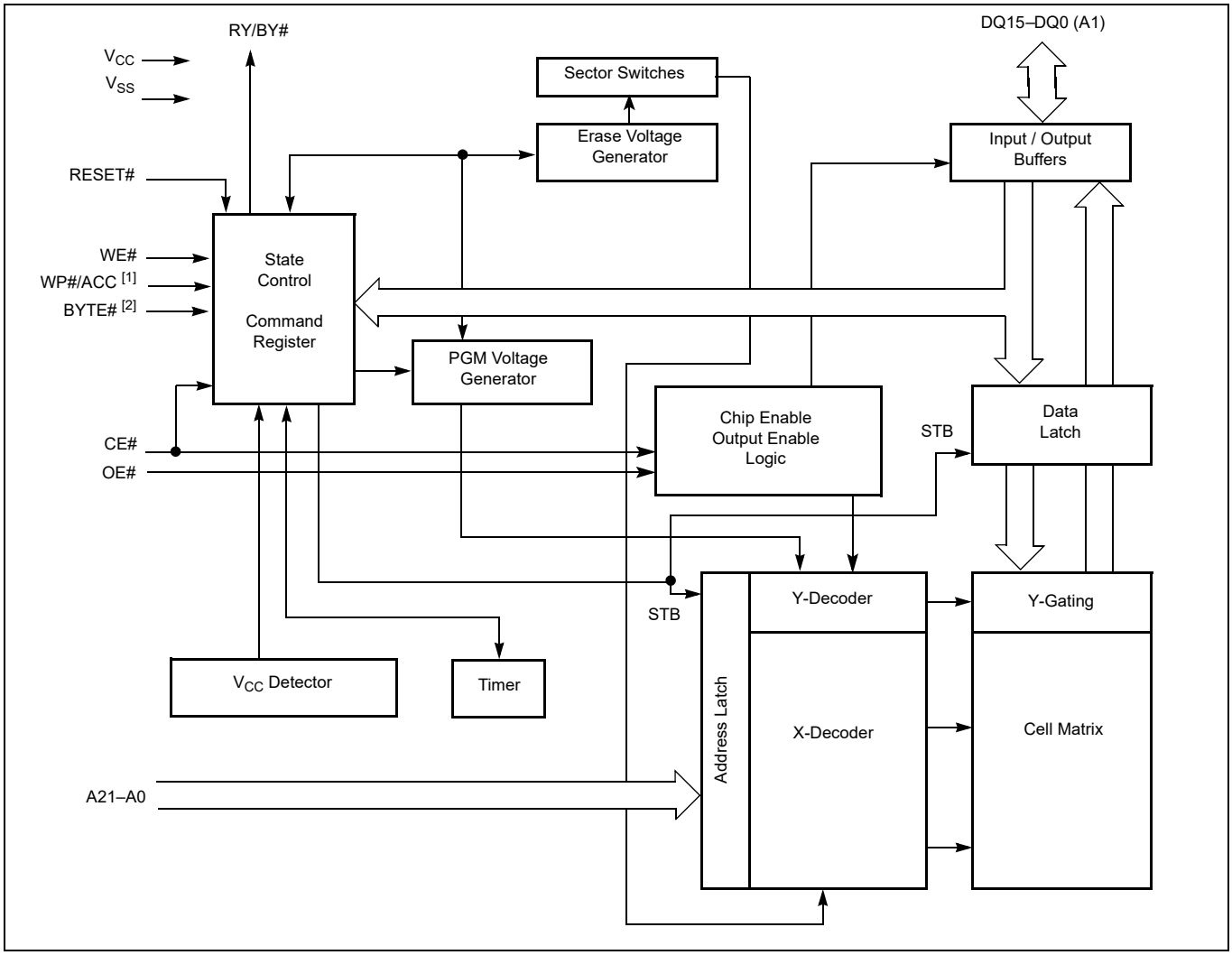


Figure 1 Block diagram

Notes
1. Available on separate pins for models 06, 07, V6, V7.
2. Available only on ×8/×16 devices.

3 Connection diagrams

3.1 Special package handling instructions

Special handling is required for flash memory products in molded packages (TSOP and BGA). The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

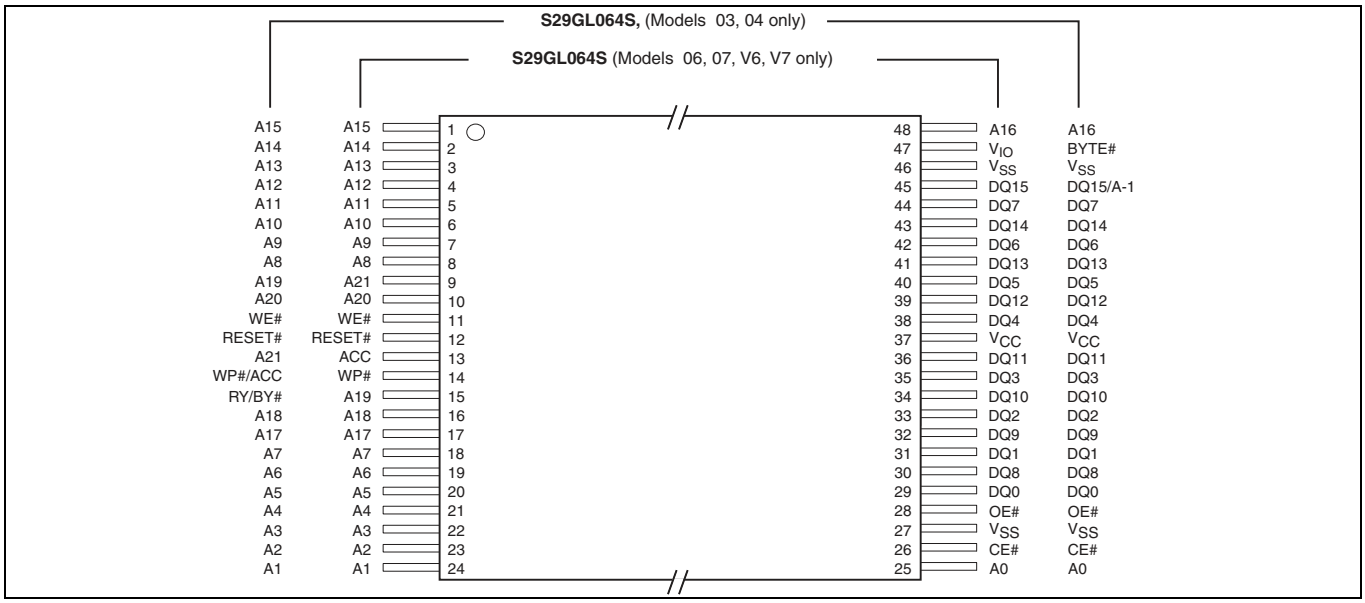


Figure 2 48-pin standard TSOP

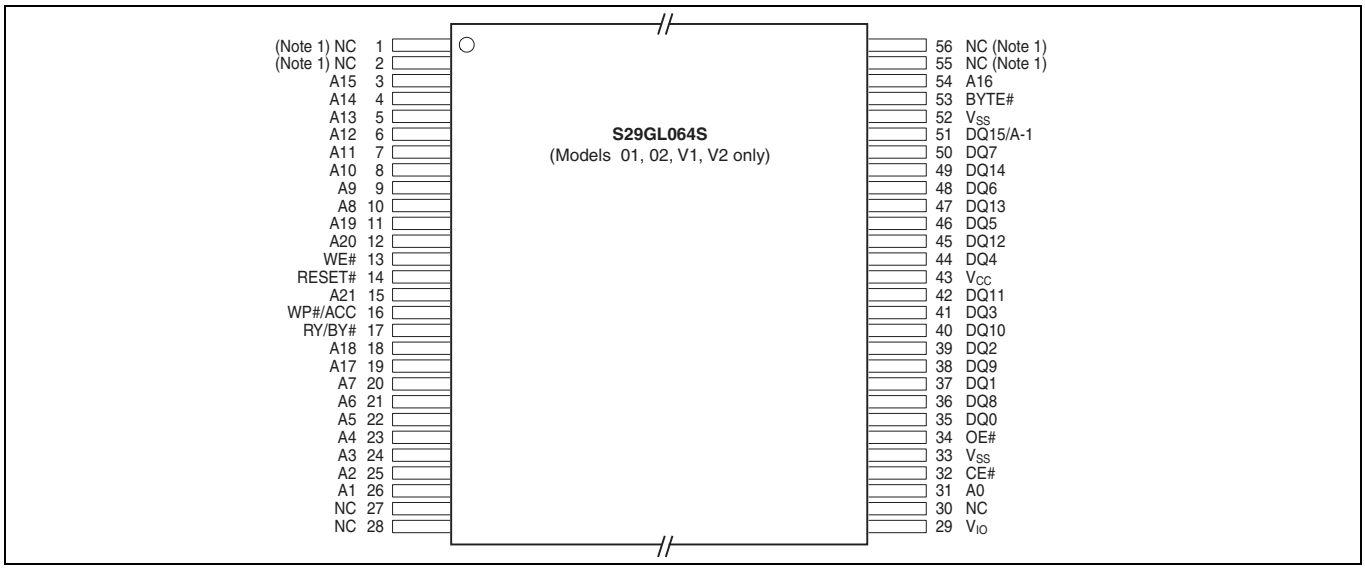


Figure 3 56-pin standard TSOP

Note

3. These pins are NC on the S29GL064S, however, are used by 128-Mbit to 1-Gbit density GL devices as the high order address inputs.

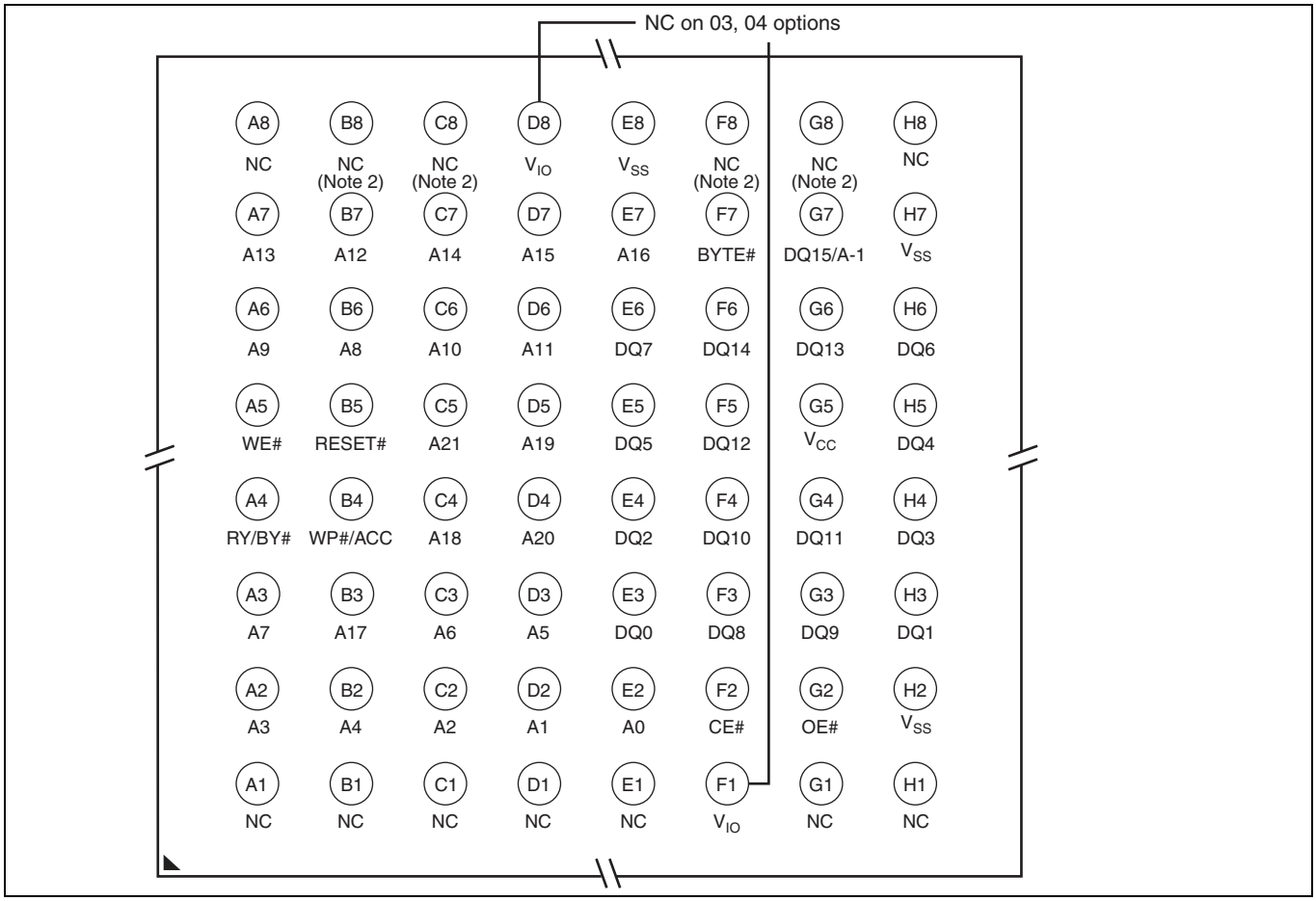


Figure 4 64-ball fortified BGA

Notes
4. S29GL064S (Models 01, 02, 03, 04, V1, V2).
5. These balls are NC on the S29GL064S, however, are used by 128-Mbit to 1-Gbit density GL devices as the high order address inputs.

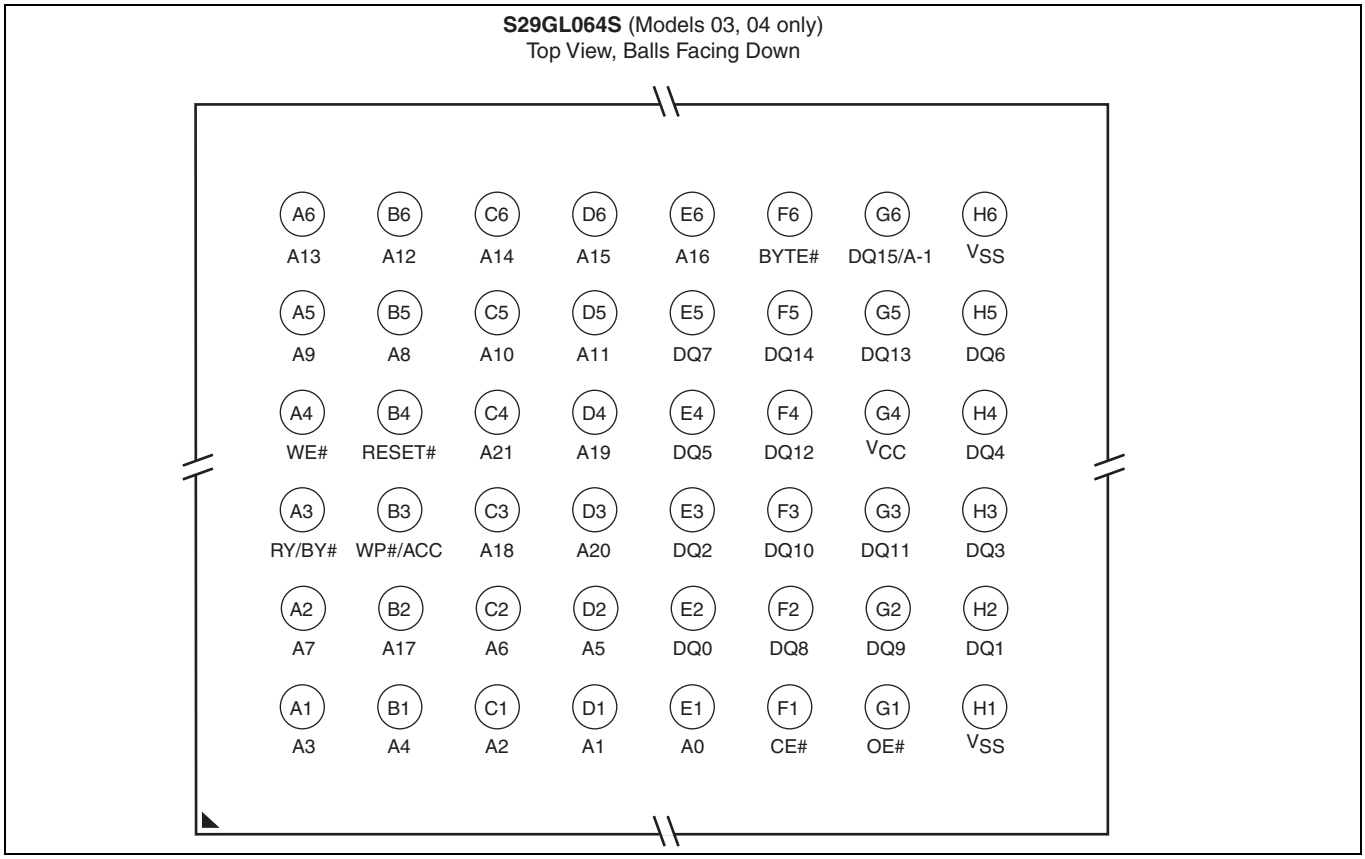


Figure 5 48-ball fine-pitch BGA (VBK 048)

4 Pin description

Table 3 Pin description

Pin	Description
A21–A0	22 address inputs (S29GL064S)
DQ7–DQ0	8 data inputs / outputs
DQ14–DQ0	15 data inputs / outputs
DQ15/A1	DQ15 (Data input / output, word mode), A1 (LSB address input, byte mode)
CE#	Chip Enable input
OE#	Output Enable input
WE#	Write Enable input
WP#/ACC	Hardware Write Protect input / Programming Acceleration input
ACC	Programming Acceleration input
WP#	Hardware Write Protect input
RESET#	Hardware Reset pin input
RY/BY#	Ready/Busy output
BYTE#	Selects 8-bit or 16-bit mode
VCC	3.0 V-only single power supply (see **"Product selector guide"** on page 6 for speed options and voltage supply tolerances)
VIO	Output Buffer Power
VSS	Device Ground
NC	Pin not connected internally
RFU	Reserved for Future Use. Not currently connected internally but the pin/ball location should be left unconnected and unused by PCB routing channel for future compatibility. The pin/ball may be used by a signal in the future.

5 S29GL064S logical symbols

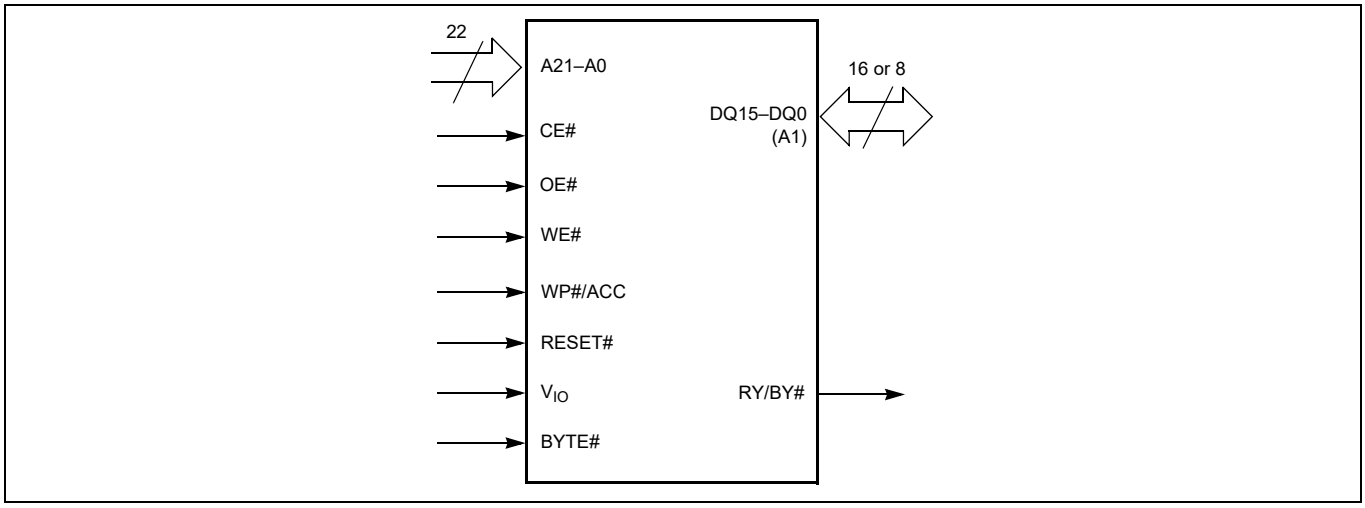


Figure 6 S29GL064S logic symbol (models 01, 02, V1, V2)

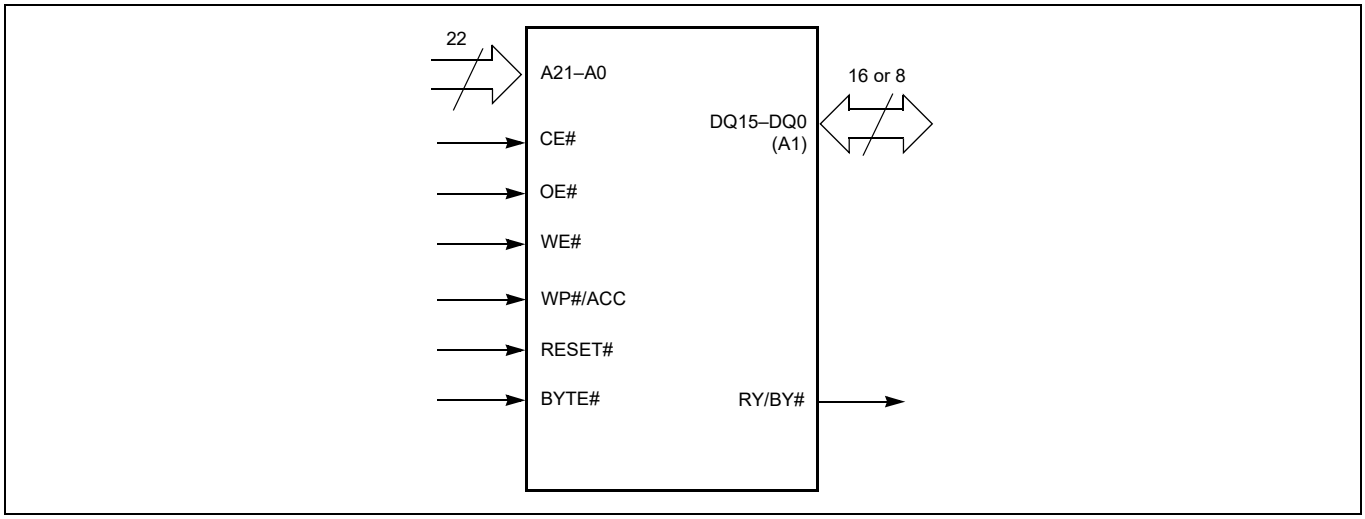


Figure 7 S29GL064S logic symbol (models 03, 04)

S29GL064S logical symbols

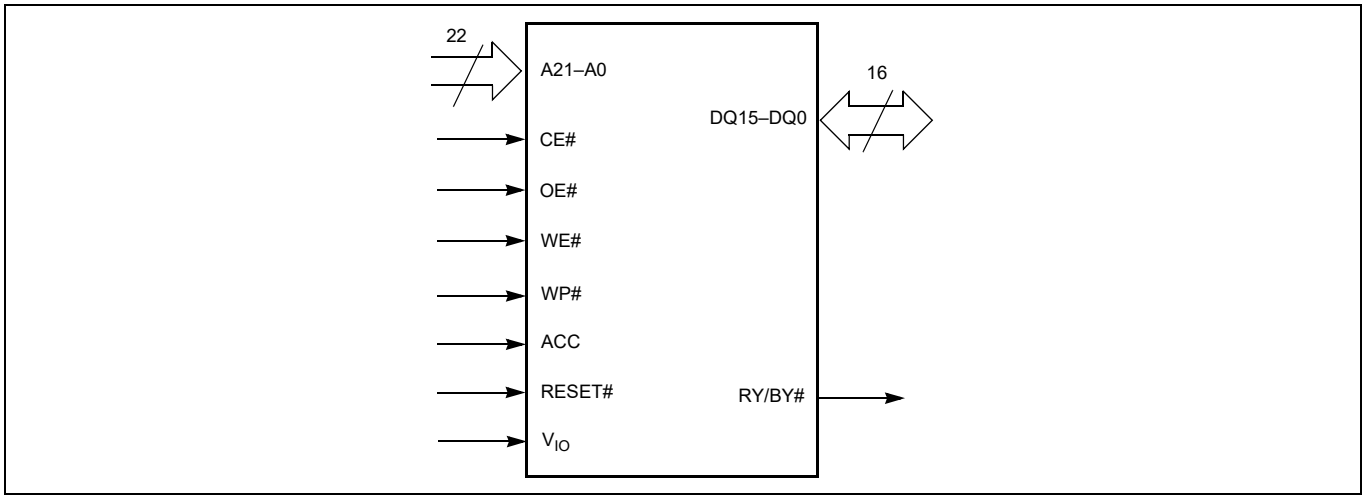


Figure 8 S29GL064S logic symbol (models 06, 07, V6, V7)

6 Device bus operations

This section describes the requirements and use of the device bus operations, which are initiated through the internal command register. The command register itself does not occupy any addressable memory location. The register is a latch used to store the commands, along with the address and data information needed to execute the command. The contents of the register serve as inputs to the internal state machine. The state machine outputs dictate the function of the device. **Table 4** lists the device bus operations, the inputs and control levels they require, and the resulting output. The following subsections describe each of these operations in further detail.

Table 4 Device bus operations

Operation	CE#	OE#	WE#	RESET#	BYTE#[6]	WP#	ACC	Addresses	DQ0–DQ7	DQ8–DQ15	
										BYTE# = V_{IH}	BYTE# = V_{IL}
Read	L	L	H	H	L or H	X	X	A_{IN}	D_{OUT}	D_{OUT}	DQ8–DQ14 = High-Z, DQ15 = A1
Autoselect (HV)	L	L	H	H	L or H	X	H	A_{IN} [7]	D_{OUT}	D_{OUT}	
Write (Program / Erase)	L	H	L	H	L or H	Note 8	X	A_{IN}	Note 9	Note 9	
Accelerated Program	L	H	L	H	L or H	Note 8	V_{HH}	A_{IN}	Note 9	Note 9	
Standby	$V_{IO} \pm 0.3$ V	X	X	$V_{IO} \pm 0.3$ V	L or H	X	H	X	High-Z	High-Z	High-Z
Output Disable	L	H	H	H	L or H	X	X	X	High-Z	High-Z	High-Z
	H	X	X								
Reset	X	X	X	L	L or H	X	X	X	High-Z	High-Z	High-Z

Legend:
L = Logic LOW = V_{IL}
H = Logic HIGH = V_{IH}
V_{HH} = Voltage for ACC program acceleration
V_{ID} = Voltage for autoselect
X = Don’t care
A_{IN} = Address in
D_{IN} = Data in
D_{OUT} = Data out

Notes
6. $V_{IL} = V_{SS}$ and $V_{IH} = V_{IO}$.
7. A9 is raised to V_{ID} to enable autoselect reads.
8. If WP# = V_{IL}, the first or last sector remains protected (for uniform sector devices), and the two outer boot sectors are protected (for boot sector devices).
   If WP# = V_{IH}, the first or last sector, or the two outer boot sectors are protected or unprotected as determined by the method described in write protect (WP#). All sectors are unprotected when shipped from the factory (The secure silicon region may be factory protected depending on version ordered.)
9. D_{IN} or D_{OUT} as required by command sequence, data polling, or sector protect algorithm (see **Figure 13**).

6.1 Word / byte configuration

The BYTE# pin controls whether the device data I/O pins operate in the byte or word configuration. If the BYTE# pin is set at logic 1, the device is in word configuration, DQ0–DQ15 are active and controlled by CE#, WE# and OE#.

If the BYTE# pin is set at logic 0, the device is in byte configuration, and only data I/O pins DQ0–DQ7 are active and controlled by CE#, WE# and OE#. The data I/O pins DQ8–DQ14 are tri-stated, and the DQ15 pin is used as an input for the LSB (A1) address function.

The BYTE# pin must be driven set to a logic 0 or 1 state prior to CE# being driven LOW. The BYTE# pin should not change logic state while CE# is LOW.

6.2 Requirements for reading array data

All memories require access time to output array data. In a read operation, data is read from one memory location at a time. Addresses are presented to the device in random order, and the propagation delay through the device causes the data on its outputs to arrive with the address on its inputs.

The device defaults to reading array data after device power-up or hardware reset. To read data from the memory array, the system must first assert a valid address on Amax–A0, while driving OE# and CE# to V_{IL}. WE# must remain at V_{IH}. Data will appear on DQ15–DQ0 after address access time (t_{ACC}), which is equal to the delay from stable addresses to valid output data. The OE# signal must be driven to V_{IL}. Data is output on DQ15–DQ0 pins after the access time (t_{OE}) has elapsed from the falling edge of OE#.

See **"Reading array data"** on page 33 for more information. Refer to **Table 72** and **Table 73** for timing specifications and the timing diagram. Refer to **Table 63** and **Table 64** for the active current specification on reading array data.

6.2.1 Page mode read

The device is capable of fast page mode read and is compatible with the page mode Mask ROM read operation. This mode provides faster read access speed for random locations within a page. The page size of the device is 8 words / 16 bytes. The appropriate page is selected by the higher address bits A(max)–A3. Address bits A2–A0 in word mode (A2–A1 in byte mode) determine the specific word within a page. This is an asynchronous operation; the microprocessor supplies the specific word location.

The random or initial page access is equal to t_{ACC} or t_{CE} and subsequent page read accesses (as long as the locations specified by the microprocessor falls within that page) is equivalent to t_{PACC}. When CE# is deasserted and reasserted for a subsequent access, the access time is t_{ACC} or t_{CE}. Fast page mode accesses are obtained by keeping the read-page addresses constant and changing the intra-read page addresses.

6.3 Writing commands / command sequences

To write a command or command sequence (which includes programming data to the device and erasing sectors of memory), the system must drive WE# and CE# to V_{IL}, and OE# to V_{IH}.

The device features an **Unlock Bypass** mode to facilitate faster programming. Once the device enters the Unlock Bypass mode, only two write cycles are required to program a word, instead of four. The **Table 19** contains details on programming data to the device using both standard and Unlock Bypass command sequences.

An erase operation can erase one sector, multiple sectors, or the entire device. **Table 5**–**Table 8** indicate the address space that each sector occupies.

Refer to **"DC characteristics"** on page 83 for the active current specification for the write mode. The **"AC characteristics"** on page 90 section contains timing specification tables and timing diagrams for write operations.

6.3.1 Write buffer

Write Buffer programming allows the system write to a maximum of 128 words / 256 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms.

6.3.2 Accelerated program operation

The device offers program operations through the ACC function. This is one of two functions provided by the WP#/ACC or ACC pin, depending on model number. This function is primarily intended to support manufacturing programming operations at the factory.

If the system asserts V_{HH} on this pin, the device automatically enters the Unlock Bypass mode, protected sectors will remain protected. The system would use a two-cycle program command sequence as required by the Unlock Bypass mode. Removing V_{HH} from the WP#/ACC or ACC pin, depending on model number, returns the device to normal operation. Note that the WP#/ACC or ACC pin must be raised to V_{HH} prior to any accelerated operation and should return to V_{IL}/V_{IH} after the completion of the accelerated operation. It should not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# contains an internal pull-up; when unconnected, WP# is at V_{IH}.

6.3.3 Autoselect functions

If the system writes the autoselect command sequence, the device enters the autoselect mode. The system can then read autoselect codes from the internal register (which is separate from the memory array) on DQ7–DQ0. Standard read cycle timings (t_{ACC}) apply in this mode. Refer to **"Autoselect mode"** on page 20 and **"Autoselect command sequence"** on page 34 for more information.

6.4 Automatic ECC

6.4.1 ECC overview

The automatic ECC feature works transparently with normal program, erase, and read operations. As the device transfers each page of data from the Write Buffer to the memory array, internal ECC logic programs the ECC code for that page into a portion of the memory array that is not visible to the host system. The device evaluates the page data and the ECC code during each initial page access. If needed, the internal ECC logic will correct a single bit error during the initial access.

Programming more than once to a particular page will disable the ECC function for that page. The ECC function for that page will remain disabled until the next time the host system erases the sector containing that page. The host system may read data stored in that page following multiple programming operations; however, ECC remains disables and the device will not detect or correct an error in that page.

6.4.2 Program and erase summary

For performance and reliability reasons, the device performs reading and programming operations on full 32-byte pages in parallel. Internal device logic provides ECC on each page by adding an ECC code when the page is first programmed.

6.4.3 ECC implementation

Each 32-byte page in the main flash array, as well as each 32-byte OTP region, features an associated ECC code. Internal ECC logic is able to detect and correct any single bit error found in a page or the associated ECC code during a read access. The first Write Buffer program operation applied to a page programs the ECC code for that page. Subsequent programming operations that occur more than once on a particular page will disable the ECC function for that page. This allows bit or word programming; however, multiple programming operations to the same page will disable the ECC function on the page where incremental programming occurs. An erase of the sector containing the page with ECC disabled will re-enable the ECC function for that page.

The ECC function is automatic and transparent to the user. The transparency of the automatic ECC function enhances data integrity for typical programming operations that write data once to each page. The ECC function also facilitates software compatibility to previous generations of GL family products by allowing single word programming and bit-walking where the user programs the same page or word more than once. When a page has automatic ECC disabled, the ECC function will not detect or correct any errors upon a data read from that page.

6.4.4 Word programming

A word programming operation programs a single word anywhere in the main memory array. Programming multiple words within the same 32-byte page disables the automatic ECC function for that page. An erase of the sector containing that page will re-enable automatic ECC following multiple word programming operation on that page.

6.4.5 Write buffer programming

Each Write Buffer program operation allows the user to program a single bit up to 256 bytes. A 32-byte page is the smallest program granularity that features automatic ECC protection. Programming to the same page more than once will disable the automatic ECC function for that page. Infineon recommends the use of a Write Buffer programming operation to program multiple pages in an operation and to write each page only once. This keeps the automatic ECC function enabled on each page. For the very best performance, program in full lines of 256 bytes aligned on 256-byte boundaries.

6.5 Standby mode

When the system is not reading or writing to the device, it can be placed in to standby mode. In this mode, current consumption is greatly reduced, and the outputs are placed in the high impedance state, independent of the OE# input.

The device enters the CMOS standby mode when the CE# and RESET# pins are both held at $V_{IO} \pm 0.3$ V. (Note that this is a more restricted voltage range than V_{IH}.) If CE# and RESET# are held at V_{IH}, but not within $V_{IO} \pm 0.3$ V, the device is in the standby mode, but the standby current is greater. The device requires standard access time (t_{ACC}/t_{CE}) for read access when the device is in either of these standby modes, before it is ready to read data.

If the device is deselected during erasure or programming, the device draws active current until the operation is completed.

Refer to the **"DC characteristics"** on page 83, for the standby current specification.

6.6 Automatic sleep mode

The automatic sleep mode reduces device interface energy consumption to the sleep level (I_{CC6}) following the completion of a random read access time. The device automatically enables this mode when addresses remain stable for t_{ACC} + 30 ns. While in sleep mode, output data is latched and always available to the system. Output of the data depends on the level of the OE# signal but, the automatic sleep mode current is independent of the OE# signal level. Standard address access timings (t_{ACC} or t_{PACC}) provide new data when addresses are changed. Refer to the **"DC characteristics"** on page 83 for the automatic sleep mode current specification I_{CC6}.

Automatic sleep helps reduce current consumption especially when the host system clock is slowed for power reduction. During slow system clock periods, read and write cycles may extend many times their length versus when the system is operating at high speed. Even though CE# may be LOW throughout these extended data transfer cycles, the memory device host interface will go to the Automatic Sleep current at t_{ACC} + 30 ns. The device will remain at the Automatic Sleep current for t_{ASSB}. Then the device will transition to the standby current level. This keeps the memory at the Automatic Sleep or standby power level for most of the long duration data transfer cycles, rather than consuming full read power all the time that the memory device is selected by the host system.

However, the EAC operates independent of the automatic sleep mode of the host interface and will continue to draw current during an active EA. Only when both the host interface and EAC are in their standby states is the standby level current achieved.

6.7 RESET#: Hardware reset pin

The RESET# pin provides a hardware method of resetting the device to reading array data. When the RESET# pin is driven LOW for at least a period of t_{RP}, the device immediately terminates any operation in progress, output pins go to High-Z, and all read / write commands are ignored for the duration of the RESET# pulse. Program / Erase operations that were interrupted should be reinitiated once the device is ready to accept another command sequence, to ensure data integrity.

Current is reduced for the duration of the RESET# pulse. When RESET# is held at $V_{SS} \pm 0.3$ V long enough, the device draws CMOS standby current (I_{CC5}).

The RESET# pin may be tied to the system reset circuitry. A system reset would thus also reset the flash memory, enabling the system to read the boot-up firmware from the flash memory.

Refer to the **"AC characteristics"** on page 90 for RESET# parameters and to **Figure 22** for the timing diagram.

6.8 Output disable mode

When the OE# input is at V_{IH}, output from the device is disabled. The output pins are placed in a high impedance state.

6.9 Memory map

Table 5 S29GL064S (Models 01, 02, V1, V2) sector addresses

Sector	A21–A15	Sector size (KB/Kwords)	8-bit Address range	16-bit Address range	Sector	A21–A15	Sector size (KB/Kwords)	8-bit Address range	16-bit Address range
SA0	0000000	64/32	000000h–00FFFFh	000000h–007FFFh	...	...	...	...	...
SA1	0000001	64/32	010000h–01FFFFh	008000h–00FFFFh	SA118	1110110	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
SA2	0000010	64/32	020000h–02FFFFh	010000h–017FFFh	SA119	1110111	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
SA3	0000011	64/32	030000h–03FFFFh	018000h–01FFFFh	SA120	1111000	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
SA4	0000100	64/32	040000h–04FFFFh	020000h–027FFFh	SA121	1111001	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
SA5	0000101	64/32	050000h–05FFFFh	028000h–02FFFFh	SA122	1111010	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
SA6	0000110	64/32	060000h–06FFFFh	030000h–037FFFh	SA123	1111011	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
SA7	0000111	64/32	070000h–07FFFFh	038000h–03FFFFh	SA124	1111100	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
SA8	0001000	64/32	080000h–08FFFFh	040000h–047FFFh	SA125	1111101	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA9	0001001	64/32	090000h–09FFFFh	048000h–04FFFFh	SA126	1111110	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
...	...	...	...	...	SA127	1111111	64/32	7F0000h–7FFFFFh	3F8000h–3FFFFFh

Table 6 S29GL064S (Model 03) top boot sector addresses

Sector	A21–A12	Sector size (KB/Kwords)	8-bit Address range	16-bit Address range	Sector	A21–A12	Sector size (KB/Kwords)	8-bit Address range	16-bit Address range
SA0	0000000xxx	64/32	000000h–00FFFFh	000000h–007FFFh	...	...	...	...	...
SA1	0000001xxx	64/32	010000h–01FFFFh	008000h–00FFFFh	SA125	1111101xxx	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA2	0000010xxx	64/32	020000h–02FFFFh	010000h–017FFFh	SA126	1111110xxx	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
SA3	0000011xxx	64/32	030000h–03FFFFh	018000h–01FFFFh	SA127	1111111000	8/4	7F0000h–7F1FFFh	3F8000h–3F8FFFh
SA4	0000100xxx	64/32	040000h–04FFFFh	020000h–027FFFh	SA128	1111111001	8/4	7F2000h–7F3FFFh	3F9000h–3F9FFFh
SA5	0000101xxx	64/32	050000h–05FFFFh	028000h–02FFFFh	SA129	1111111010	8/4	7F4000h–7F5FFFh	3FA000h–3FAFFFh
SA6	0000110xxx	64/32	060000h–06FFFFh	030000h–037FFFh	SA130	1111111011	8/4	7F6000h–7F7FFFh	3FB000h–3FBFFFh
SA7	0000111xxx	64/32	070000h–07FFFFh	038000h–03FFFFh	SA131	1111111100	8/4	7F8000h–7F9FFFh	3FC000h–3FCFFFh
SA8	0001000xxx	64/32	080000h–08FFFFh	040000h–047FFFh	SA132	1111111101	8/4	7FA000h–7FBFFFh	3FD000h–3FDFFFh
SA9	0001001xxx	64/32	090000h–09FFFFh	048000h–04FFFFh	SA133	1111111110	8/4	7FC000h–7FDFFFh	3FE000h–3FEFFFh
...	...	...	...	...	SA134	1111111111	8/4	7FE000h–7FFFFFh	3FF000h–3FFFFFh

Table 7 S29GL064S (Model 04) bottom boot sector addresses

Sector	A21–A12	Sector size (KB/Kwords)	8-bit Address range	16-bit Address range	Sector	A21–A12	Sector size (KB/Kwords)	8-bit Address range	16-bit Address range
SA0	0000000000	8/4	000000h–001FFFh	000000h–000FFFh	...	...	...	...	...
SA1	0000000001	8/4	002000h–003FFFh	001000h–001FFFh	SA125	1110110xxx	64/32	760000h–76FFFFh	3B0000h–3B7FFFh
SA2	0000000010	8/4	004000h–005FFFh	002000h–002FFFh	SA126	1110111xxx	64/32	770000h–77FFFFh	3B8000h–3BFFFFh
SA3	0000000011	8/4	006000h–007FFFh	003000h–003FFFh	SA127	1111000xxx	64/32	780000h–78FFFFh	3C0000h–3C7FFFh
SA4	0000000100	8/4	008000h–009FFFh	004000h–004FFFh	SA128	1111001xxx	64/32	790000h–79FFFFh	3C8000h–3CFFFFh
SA5	0000000101	8/4	00A000h–00BFFFh	005000h–005FFFh	SA129	1111010xxx	64/32	7A0000h–7AFFFFh	3D0000h–3D7FFFh
SA6	0000000110	8/4	00C000h–00DFFFh	006000h–006FFFh	SA130	1111011xxx	64/32	7B0000h–7BFFFFh	3D8000h–3DFFFFh
SA7	0000000111	8/4	00E000h–00FFFFh	007000h–007FFFh	SA131	1111100xxx	64/32	7C0000h–7CFFFFh	3E0000h–3E7FFFh
SA8	0000001xxx	64/32	010000h–01FFFFh	008000h–00FFFFh	SA132	1111101xxx	64/32	7D0000h–7DFFFFh	3E8000h–3EFFFFh
SA9	0000010xxx	64/32	020000h–02FFFFh	010000h–017FFFh	SA133	1111110xxx	64/32	7E0000h–7EFFFFh	3F0000h–3F7FFFh
...	...	...	...	...	SA134	1111111xxx	64/32	7F0000h–7FFFFFh	3F8000h–3FFFFFh

Table 8 S29GL064S (Models 06, 07, V6, V7) sector addresses

Sector	A21–A15	Sector size (KB/Kwords)	16-bit Address range	Sector	A21–A15	Sector size (KB/Kwords)	16-bit Address range
SA0	0000000	64/32	000000–007FFF	...	...	...	...
SA1	0000001	64/32	008000–00FFFF	SA118	1110110	64/32	3B0000–3B7FFF
SA2	0000010	64/32	010000–017FFF	SA119	1110111	64/32	3B8000–3BFFFF
SA3	0000011	64/32	018000–01FFFF	SA120	1111000	64/32	3C0000–3C7FFF
SA4	0000100	64/32	020000–027FFF	SA121	1111001	64/32	3C8000–3CFFFF
SA5	0000101	64/32	028000–02FFFF	SA122	1111010	64/32	3D0000–3D7FFF
SA6	0000110	64/32	030000–037FFF	SA123	1111011	64/32	3D8000–3DFFFF
SA7	0000111	64/32	038000–03FFFF	SA124	1111100	64/32	3E0000–3E7FFF
SA8	0001000	64/32	040000–047FFF	SA125	1111101	64/32	3E8000–3EFFFF
SA9	0001001	64/32	048000–04FFFF	SA126	1111110	64/32	3F0000–3F7FFF
...	...	...	...	SA127	1111111	64/32	3F8000–3FFFFF

6.10 Autoselect mode

The autoselect mode provides manufacturer and device identification, and sector protection verification, through identifier codes output on DQ7–DQ0. This mode is primarily intended for programming equipment to automatically match a device to be programmed with its corresponding programming algorithm. However, the autoselect codes can also be accessed in-system through the command register.

When using programming equipment, the autoselect mode requires V_{ID} on address pin A9. Address pins A6, A3, A2, A1, and A0 must be as shown in **Table 9**. In addition, when verifying sector protection, the sector address must appear on the appropriate highest order address bits (see **Table 5**–**Table 8**). **Table 9** shows the remaining address bits that are don't care. When all necessary bits are set as required, the programming equipment may then read the corresponding identifier code on DQ7–DQ0. Note that the A9 pin must not be at V_{ID} for operations other than autoselect, or device damage may result. Autoselect using V_{ID} is supported at room temperature only. It must be raised to V_{ID} prior to any autoselect operations and should return to V_{IL}/V_{IH} after the completion of the autoselect operation. It should not be at V_{ID} for operations other than autoselect, or device damage may result.

To access the autoselect codes in-system, the host system can issue the autoselect command via the command register, as shown in **Table 23** and **Table 25**. This method does not require V_{ID}. Refer to the **"Autoselect command sequence"** on page 34 for more information.

ID-CFI location 02h displays sector protection status for the sector selected by the sector address (SA) used in the ID-CFI enter command. To read the protection status of more than one sector it is necessary to exit the ID ASO and enter the ID ASO using the new SA. The access time to read location 02h is always t_{ACC} and a read of this location requires CE# to go HIGH before the read and return LOW to initiate the read (asynchronous read access). Page mode read between location 02h and other ID locations is not supported. Page mode read between ID locations other than 02h is supported.

In x8 mode, address A1 is ignored and the lower 8 bits of data will be returned for both address.

Table 9 Autoselect codes, (high voltage method)

Description		CE#	OE#	WE#	A_{max} to A15	A14 to A10	A9	A8 to A7	A6	A5 to A4	A3 to A2	A1	A0	DQ8 to DQ15		DQ7 to DQ0		
																Model number		
														BYTE# = V_{IH}	BYTE# = V_{IL}	01, 02, V1, V2	03, 04	06, 07, V6, V7
Manufacturer ID: Infineon products		L	L	H	X	X	V_{ID}	X	L	X	L	L	L	00	X	01h	01h	01h
S29GL064S	Cycle 1	L	L	H	X	X	V_{ID}	X	L	X	L	L	H	22	X	7Eh	7Eh	7Eh
	Cycle 2										H	H	L	22	X	0Ch	10h	13h
	Cycle 3										H	H	H	22	X	01h	00h (04, bottom boot) 01h (03, top boot)	01h
Sector protection verification		L	L	H	SA	X	V_{ID}	X	L	X	L	H	L	X	X	01h (protected), 00h (unprotected)		
Secure silicon region indicator bit (DQ7), WP# protects highest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	9A (factory locked), 1A (not factory locked)		
Secure silicon region indicator bit (DQ7), WP# protects lowest address sector		L	L	H	X	X	V_{ID}	X	L	X	L	H	H	X	X	8A (factory locked), 0A (not factory locked)		

Legend:
L = Logic LOW = V_{IL}
H = Logic HIGH = V_{IH}
SA = Sector Address
X = Don't care

6.11 Advanced sector protection

The device features several levels of sector protection, which can disable both the program and erase operations in certain sectors.

6.11.1 Persistent sector protection

A command sector protection method that replaces the old 12 V controlled protection method.

6.11.2 Password sector protection

A highly sophisticated protection method that requires a password before changes to certain sectors are permitted.

6.11.3 WP# hardware protection

A write protect pin that can prevent program or erase operations in the outermost sectors.

The WP# hardware protection feature is always available, independent of the software managed protection method chosen.

6.11.4 Selecting a sector protection mode

All parts default to operate in the Persistent Sector Protection mode. The user must then choose if the Persistent or Password Protection method is most desirable. There are two one-time programmable non-volatile bits that define which sector protection method is used. If the user decides to continue using the Persistent Sector Protection method, they must set the Persistent Sector Protection Mode Locking Bit. This permanently sets the part to operate only using Persistent Sector Protection. If the user decides to use the password method, they must set the Password Mode Locking Bit. This permanently sets the part to operate only using password sector protection.

It is important to remember that setting either the Persistent Sector Protection Mode Locking Bit or the Password Mode Locking Bit permanently selects the protection mode. It is not possible to switch between the two methods once a locking bit is set. **It is important that one mode is explicitly selected when the device is first programmed, rather than relying on the default mode alone.** This is so that it is not possible for a system program or virus to later set the Password Mode Locking Bit, which would cause an unexpected shift from the default Persistent Sector Protection Mode into the Password Protection Mode.

The device is shipped with all sectors unprotected. Infineon offers the option of programming and protecting sectors at the factory prior to shipping the device through the ExpressFlash™ Service. Contact your sales representative for details.

It is possible to determine whether a sector is protected or unprotected. See **“Autoselect command sequence”** on page 34 for details.

6.12 Lock Register

The Lock Register consists of 3 bits (DQ2, DQ1, and DQ0). These DQ2, DQ1, DQ0 bits of the Lock Register are programmable by the user. Users are not allowed to program both DQ2 and DQ1 bits of the Lock Register to the 00 state. If the user tries to program DQ2 and DQ1 bits of the Lock Register to the 00 state, the device aborts the Lock Register back to the default 11 state. Once either DQ2 and DQ1 bits of the Lock Register are programmed than no further changes are allow on DQ2 and DQ1. The programming time of the Lock Register is same as the typical word programming time (t_{WHWH1}) without utilizing the Write Buffer of the device. During a Lock Register programming sequence execution, the DQ6 Toggle Bit I toggles until the programming of the Lock Register has completed to indicate programming status. All Lock Register bits are readable to allow users to verify Lock Register statuses.

The customer secure silicon region protection bit is DQ0, persistent protection mode lock bit is DQ1, and password protection mode lock bit is DQ2 are accessible by all users. Each of these bits are non-volatile. DQ15–DQ3 are reserved and must be 1’s when the user tries to program the DQ2, DQ1, and DQ0 bits of the Lock Register. The user is not required to program DQ2, DQ1 and DQ0 bits of the Lock Register at the same time. This allows users to lock the secure silicon region and then set the device either permanently into password protection mode or persistent protection mode and then lock the secure silicon region at separate instances and time frames.

- Secure silicon region protection allows the user to lock the secure silicon region area.
- Persistent protection mode lock bit allows the user to set the device permanently to operate in the persistent protection mode.
- Password protection mode lock bit allows the user to set the device permanently to operate in the password protection mode.

Table 10 Lock register

Bit	DQ15–DQ6	DQ5	DQ4	DQ3	DQ2	DQ1	DQ0
Name	Don’t care	Reserved	Reserved	Reserved	Password protection mode lock bit	Persistent protection mode lock bit	Secure silicon region protection bit
Default value	1	1	1	1	1	1	0

6.13 Persistent sector protection

The persistent sector protection method replaces the old 12 V controlled protection method while at the same time enhancing flexibility by providing three different sector protection states.

Dynamically locked	The sector is protected and can be changed by a simple command.
Persistently locked	A sector is protected and cannot be changed.
Unlocked	The sector is unprotected and can be changed by a simple command.

To achieve these states, three types of “bits” are used:

6.13.1 Dynamic protection bit (DYB)

A volatile protection bit is assigned for each sector. After power-up or hardware reset, the contents of all DYB bits are in the “unprotected state”. Each DYB is individually modifiable through the DYB Set command and DYB Clear command. The DYB bits and persistent protect bits (PPB) lock bit are defaulted to power-up in the cleared state or unprotected state - meaning the all PPB bits are changeable.

The protection state for each sector is determined by the logical OR of the PPB and the DYB related to that sector. For the sectors that have the PPB bits cleared, the DYB bits control whether or not the sector is protected or unprotected. By issuing the DYB Set and DYB Clear command sequences, the DYB bits is protected or unprotected, thus placing each sector in the protected or unprotected state. These are the so-called dynamic locked or unlocked states. They are called dynamic states because it is very easy to switch back and forth between the protected and un-protected conditions. This allows software to easily protect sectors against inadvertent changes yet does not prevent the easy removal of protection when changes are needed.

The DYB bits may be set or cleared as often as needed. The PPB bits allow for a more static, and difficult to change, level of protection. The PPB bits retain their state across power cycles because they are non-volatile. Individual PPB bits are set with a program command but must all be cleared as a group through an erase command.

The PPB lock bit adds an additional level of protection. Once all PPB bits are programmed to the desired settings, the PPB lock bit may be set to the ‘freeze state’. Setting the PPB lock bit to the freeze state disables all program and erase commands to the non-volatile PPB bits. In effect, the PPB lock bit locks the PPB bits into their current state. The only way to clear the PPB lock bit to the ‘unfreeze state’ is to go through a power cycle, or hardware reset. The Software Reset command does not clear the PPB lock bit to the unfreeze state. System boot code can determine if any changes to the PPB bits are needed e.g., to allow new system code to be downloaded. If no changes are needed then the boot code can set the PPB lock bit to disable any further changes to the PPB bits during system operation.

The WP# write protect pin adds a final level of hardware protection. When this pin is low it is not possible to change the contents of the WP# protected sectors. These sectors generally hold system boot code. So, the WP# pin can prevent any changes to the boot code that could override the choices made while setting up sector protection during system initialization.

It is possible to have sectors that have been persistently locked, and sectors that are left in the dynamic state. The sectors in the dynamic state are all unprotected. If there is a need to protect some of them, a simple DYB Set command sequence is all that is necessary. The DYB Set and DYB Clear commands for the dynamic sectors switch the DYB bits to signify protected and unprotected, respectively. If there is a need to change the status of the persistently locked sectors, a few more steps are required. First, the PPB lock bit must be disabled to the unfreeze state by either putting the device through a power-cycle, or hardware reset. The PPB bits can then be changed to reflect the desired settings. Setting the PPB lock bit once again to the freeze state locks the PPB bits, and the device operates normally again.

To achieve the best protection, execute the PPB Lock Bit Set command early in the boot code, and protect the boot code by holding WP# = V_{IL}.

6.13.2 Persistent protection bit (PPB)

A single persistent (non-volatile) protection bit is assigned to each sector. If a PPB is programmed to the protected state through the PPB Program command, that sector is protected from program or erase operations and is therefor read-only. If a PPB requires erasure, all of the sector PPB bits must first be erased in parallel through the All PPB Erase command. The All PPB Erase command preprograms all PPB bits prior to PPB erasing. All PPB bits erase in parallel, unlike programming where individual PPB bits are programmable. The PPB bits are limited to the same number of cycles as a flash memory sector.

Programming the PPB bit requires the typical word programming time without utilizing the write buffer. During a PPB bit programming and all PPB bit erasing sequence executions, the DQ6 Toggle Bit I toggles until the programming of the PPB bit or erasing of all PPB bits has completed to indicate programming and erasing status. Erasing all of the PPB bits at once requires typical sector erase time. During the erasing of all PPB bits, the DQ3 sector erase timer bit outputs '1' to indicate the erasure of all PPB bits are in progress. Reading the PPB status bit requires the initial access time of the device.

6.13.3 Persistent protection bit lock (PPB lock bit)

A global volatile bit. When set to the freeze state, the PPB bits cannot be changed. When cleared to the unfreeze state, the PPB bits are changeable. There is only one PPB lock bit per device. The PPB lock bit is cleared to the unfreeze state at power-up or hardware reset.

Configuring the PPB lock bit to the freeze state requires approximately t_{WC}. Reading the PPB lock status bit requires the initial access time (t_{ACC}) of the device.

Table 11 Sector protection schemes

Protection states			Sector state
DYB bit	PPB bit	PPB lock bit	
Unprotect	Unprotect	Unfreeze	Unprotected – PPB and DYB are changeable
Unprotect	Unprotect	Freeze	Unprotected – PPB not changeable, DYB is changeable
Unprotect	Protect	Unfreeze	Protected – PPB and DYB are changeable
Unprotect	Protect	Freeze	Protected – PPB not changeable, DYB is changeable
Protect	Unprotect	Unfreeze	Protected – PPB and DYB are changeable
Protect	Unprotect	Freeze	Protected – PPB not changeable, DYB is changeable
Protect	Protect	Unfreeze	Protected – PPB and DYB are changeable
Protect	Protect	Freeze	Protected – PPB not changeable, DYB is changeable

Table 11 contains all possible combinations of the DYB bit, PPB bit, and PPB lock bit relating to the status of the sector. In summary, if the PPB bit is set, and the PPB lock bit is set, the sector is protected and the protection cannot be removed until the next power cycle or hardware reset clears the PPB lock bit to unfreeze state. If the PPB bit is cleared, the sector can be dynamically locked or unlocked. The DYB bit then controls whether or not the sector is protected or unprotected. If the user attempts to program or erase a protected sector, the device ignores the command and returns to read mode. A program or erase command to a protected sector enables status polling for t_{DP} before the device returns to read mode without having modified the contents of the protected sector. The programming of the DYB bit, PPB bit, and PPB lock bit for a given sector can be verified by writing a DYB Status Read, PPB Status Read, and PPB Lock Status Read commands to the device.

The autoselect sector protection verification outputs the OR function of the DYB bit and PPB bit per sector basis. When the OR function of the DYB bit and PPB bit is '1', the sector is either protected by DYB or PPB or both. When the OR function of the DYB bit and PPB bit is '0', the sector is unprotected through both the DYB and PPB.

6.14 Password sector protection

The password sector protection method allows an even higher level of security than the persistent sector protection method. There are two main differences between the persistent sector protection and the password sector protection methods:

- When the device is first powered on, or comes out of a reset cycle, the PPB lock bit is set to the locked state, or the freeze state, rather than cleared to the unlocked state, or the unfreeze state.
- The only means to clear and unfreeze the PPB lock bit is by writing a unique 64-bit password to the device.

The password sector protection method is otherwise identical to the persistent sector protection method.

A 64-bit password is the only additional tool utilized in this method.

The password is stored in a one-time programmable (OTP) region outside of the flash memory. Once the password protection mode lock bit is set, the password is permanently set with no means to read, program, or erase it. The password is used to clear and unfreeze the PPB lock Bit. The Password Unlock command must be written to the flash, along with a password. The flash device internally compares the given password with the pre-programmed password. If they match, the PPB lock bit is cleared to the unfreezed *state*, and the PPB bits can be altered. If they do not match, the flash device does nothing. There is a built-in t_{PPB} delay for each password check after the valid 64-bit password is entered for the PPB lock bit to be cleared to the unfreezed state. This delay is intended to thwart any efforts to run a program that tries all possible combinations in order to crack the password.

6.15 Password and password protection mode lock bit

In order to select the password sector protection method, the user must first program the password. Infineon recommends that the password be somehow correlated to the unique electronic serial number (ESN) of the particular flash device. Each ESN is different for every flash device; therefore each password should be different for every flash device. While programming in the password region, the customer may perform password read operations. Once the desired password is programmed in, the customer must then set the password protection mode lock bit. This operation achieves two objectives:

1. It permanently sets the device to operate using the password protection mode. It is not possible to reverse this function.
2. It also disables all further commands to the password region. All program, and read operations are ignored.

Both of these objectives are important, and if not carefully considered, may lead to unrecoverable errors. The user must be sure that the password sector protection method is desired when programming the password protection mode lock bit. More importantly, the user must be sure that the password is correct when the password protection mode lock bit is programmed. Due to the fact that read operations are disabled, there is no means to read what the password is afterwards. If the password is lost after programming the password protection mode lock bit, there is no way to clear and unfreeze the PPB lock bit. The password protection mode lock bit, once programmed, prevents reading the 64-bit password on the DQ bus and further password programming. The password protection mode lock bit is not erasable. Once password protection mode lock bit is programmed, the persistent protection mode lock bit is disabled from programming, guaranteeing that no changes to the protection scheme are allowed.

6.15.1 64-bit password

The 64-bit password is located in its own memory space and is accessible through the use of the Password Program and Password Read commands. The password function works in conjunction with the password protection mode lock bit, which when programmed, prevents the Password Read command from reading the contents of the password on the pins of the device.

6.16 Persistent protection bit lock (PPB lock bit)

A global volatile bit. The PPB lock bit is a volatile bit that reflects the state of the password protection mode lock bit after power-up reset. If the password protection mode lock bit is also programmed after programming the password, the Password Unlock command must be issued to clear and unfreeze the PPB lock bit after a hardware reset (RESET# asserted) or a power-up reset. Successful execution of the Password Unlock command clears and unfreezes the PPB lock bit, allowing for sector PPB bits to be modified. Without issuing the Password Unlock command, while asserting RESET#, taking the device through a power-on reset, or issuing the PPB Lock Bit Set command sets the PPB lock bit to a the freeze state.

If the password protection mode lock bit is not programmed, the device defaults to persistent protection mode. In the persistent protection mode, the PPB lock bit is cleared to the unfreeze state after power-up or hardware reset. The PPB lock bit is set to the freeze state by issuing the PPB Lock Bit Set command. Once set to the freeze state the only means for clearing the PPB lock bit to the unfreeze state is by issuing a hardware or power-up reset. The Password Unlock command is ignored in persistent protection mode.

Reading the PPB lock bit requires the initial access time (t_{ACC}) of the device.

6.17 Secure silicon region flash memory

The secure silicon region feature provides a flash memory region that enables permanent part identification through an electronic serial number (ESN). The secure silicon region is 256 bytes in length, and uses a secure silicon region indicator bit (DQ7) in autoselect mode to indicate whether or not the secure silicon region is locked when shipped from the factory. This bit is permanently set at the factory and cannot be changed, which prevents cloning of a factory locked part. This ensures the security of the ESN once the product is shipped to the field.

The factory offers the device with the secure silicon region either customer lockable (standard shipping option) or factory locked (contact a sales representative for ordering information). The customer-lockable version is shipped with the secure silicon region unprotected, allowing customers to program the sector after receiving the device. The customer-lockable version also has the secure silicon region Indicator bit permanently set to '0'. The factory-locked version is always protected when shipped from the factory, and has the secure silicon region indicator bit permanently set to '1'. Thus, the secure silicon region indicator bit prevents customer-lockable devices from being used to replace devices that are factory locked.

The secure silicon region address space in this device is allocated as follows:

Table 12 Secure silicon region address space allocation

Secure silicon region address range	Customer lockable	ESN factory locked	Express flash factory locked
000000h–000007h	Determined by customer	ESN	ESN or determined by customer
000008h–00007Fh		Unavailable	Determined by customer

The system accesses the secure silicon region through a command sequence (see **Table 23** and **Table 25**). After the system has written the Enter Secure Silicon Region command sequence, it may read the secure silicon region by using the addresses normally occupied by the first sector (SA0). This mode of operation continues until the system issues the Exit Secure Silicon Region command sequence, Reset / ASO Exit command, or until power is removed from the device. On power-up, or following a hardware reset, the device reverts to sending commands to sector SA0.

6.17.1 Customer lockable: Secure silicon region not programmed or protected at the factory

Unless otherwise specified, the device is shipped such that the customer may program and protect the 256-byte secure silicon region.

The system may program the secure silicon region using the write-buffer method, in addition to the standard programming command sequence. See **"Command definitions"** on page 33. Note that the ACC function and unlock bypass modes are not available when the secure silicon region is enabled.

Programming and protecting the secure silicon region must be used with caution since, once protected, there is no procedure available for unprotecting the secure silicon region area and none of the bits in the secure silicon region memory space can be modified in any way.

The secure silicon region area can be protected using one of the following procedures:

- Write the three-cycle Enter Secure Silicon Region command.
- To verify the protect / unprotect status of the secure silicon region, follow the algorithm.

Once the secure silicon region is programmed, locked and verified, the system must write the Exit Secure Silicon Region command sequence or Reset / ASO Exit command to return to reading and writing within the remainder of the array.

6.17.2 Factory locked: Secure silicon region programmed and protected at the factory

In devices with an ESN, the secure silicon region is protected when the device is shipped from the factory. The secure silicon region cannot be modified in any way. An ESN factory locked device has an 16-byte random ESN at addresses 000000h–000007h. Please contact your sales representative for details on ordering ESN factory locked devices.

Customers may opt to have their code programmed by the factory through the ExpressFlash service (Express flash factory locked). The devices are then shipped from the factory with the secure silicon region permanently locked. Contact your sales representative for details on using the ExpressFlash service.

6.18 Write Protect (WP#/ACC)

The Write Protect function provides a hardware method of protecting the first or last sector for uniform sector model or it protects the first or last two sectors for the boot sector model without using V_{ID}. Write Protect is one of two functions provided by the WP#/ACC input.

If the system asserts V_{IL} on the WP#/ACC pin, the device disables program and erase functions in the first or last sector independently of whether those sectors were protected or unprotected. Note that if WP#/ACC is at V_{IL} when the device is in the standby mode, the maximum input load current is increased. See the table in **"DC characteristics"** on page 83.

If the system asserts V_{IH} on the WP#/ACC pin, the device reverts to whether the protected sectors previously set to be protected or unprotected using the method described in **"Advanced sector protection"** on page 21 to **"Persistent protection bit lock (PPB lock bit)"** on page 26. Note that WP#/ACC contains an internal pull-up; when unconnected, WP#/ACC is at V_{IH}.

6.19 Hardware data protection

The command sequence requirement of unlock cycles for programming or erasing provides data protection against inadvertent writes (refer to **Table 23** and **Table 25** for command definitions). In addition, the following hardware data protection measures prevent accidental erasure or programming, which might otherwise be caused by spurious system level signals during V_{CC} power-up and power-down transitions, or from system noise.

6.19.1 Low V_{CC} write inhibit

When V_{CC} is less than V_{LKO}, the device does not accept any write cycles. This protects data during V_{CC} power-up and power-down. The command register and all internal program / erase circuits are disabled, and the device resets to the read mode. Subsequent writes are ignored until V_{CC} is greater than V_{LKO}. The system must provide the proper signals to the control pins to prevent unintentional writes when V_{CC} is greater than V_{LKO}.

6.19.2 Write pulse glitch protection

Noise pulses of less than 5 ns (typical) on OE#, CE# or WE# do not initiate a write cycle.

6.19.3 Logical inhibit

Write cycles are inhibited by holding any one of OE# = V_{IL}, CE# = V_{IH} or WE# = V_{IH}. To initiate a write cycle, CE# and WE# must be a logical zero while OE# is a logical one.

6.19.4 Power-up write inhibit

If WE# = CE# = V_{IL} and OE# = V_{IH} during power-up, the device does not accept commands on the rising edge of WE#. The internal state machine is automatically reset to the read mode on power-up.

7 Common flash memory interface

The common flash interface (CFI) specification outlines device and host system software interrogation handshake, which allows specific vendor-specified software algorithms to be used for entire families of devices. Software support can then be device-independent, JEDEC ID-independent, and forward- and backward-compatible for the specified flash device families. Flash vendors can standardize their existing interfaces for long-term compatibility.

This device enters the CFI query mode when the system writes the CFI Query command, 98h, to address 55h, any time the device is ready to read array data. The system can read CFI information at the addresses given in **Table 13** to **Table 16**. To terminate reading CFI data, the system must write the reset command (0xF0) or 0xFF.

The system can also write the CFI query command when the device is in the autoselect mode. The device enters the CFI query mode, and the system can read CFI data at the addresses given in **Table 13** to **Table 16**. The system must write the reset command to return the device to reading array data.

For further information, please refer to the CFI Specification and CFI Publication 100. Alternatively, contact your sales representative for copies of these documents.

Table 13 CFI query identification string

Addresses (×16)	Addresses (×8)	Data	Description
10h 11h 12h	20h 22h 24h	0051h 0052h 0059h	Query unique ASCII string “QRY”
13h 14h	26h 28h	0002h 0000h	Primary OEM command set
15h 16h	2Ah 2Ch	0040h 0000h	Address for primary extended table
17h 18h	2Eh 30h	0000h 0000h	Alternate OEM command set (00h = none exists)
19h 1Ah	32h 34h	0000h 0000h	Address for alternate OEM extended table (00h = none exists)

Table 14 System interface string

Addresses (×16)	Addresses (×8)	Data	Description
1Bh	36h	0027h	V_{CC} Min. (write / erase) D7–D4: volt, D3–D0: 100 millivolt
1Ch	38h	0036h	V_{CC} Max. (write / erase) D7–D4: volt, D3–D0: 100 millivolt
1Dh	3Ah	0000h	V_{PP} Min. voltage (00h = no V_{PP} pin present)
1Eh	3Ch	0000h	V_{PP} Max. voltage (00h = no V_{PP} pin present)
1Fh	3Eh	0008h	Typical timeout per single write 2^N µs
20h	40h	0008h	Typical timeout for Min. size buffer write 2^N µs (00h = not supported)
21h	42h	0009h	Typical timeout per individual block erase 2^N ms
22h	44h	0010h	Typical timeout for full chip erase 2^N ms (00h = not supported)
23h	46h	0003h	Max. timeout for byte / word program 2^N times typical.
24h	48h	0003h	Max. timeout for buffer write 2^N times typical
25h	4Ah	0001h	Max. timeout per individual block erase 2^N times typical
26h	4Ch	0000h	Max. timeout for full chip erase 2^N times typical (00h = not supported)

Note

10. CFI data related to V_{CC} and time-outs may differ from actual V_{CC} and time-outs of the product. Please consult the ordering information tables to obtain the V_{CC} range for particular part numbers. Please consult the erase and programming performance table for typical timeout specifications.

Table 15 Device geometry definition

Addresses (×16)	Addresses (×8)	Data	Description
27h	4Eh	0017h	Device size = 2^N byte
28h 29h	50h 52h	000xh 0000h	Flash device interface description (refer to CFI publication 100) 0001h = ×16-only bus devices 0002h = ×8/×16 bus devices
2Ah 2Bh	54h 56h	0008h 0000h	Max. number of byte in multi-byte write = 2^N (00h = not supported)
2Ch	58h	00xxh	Number of erase block regions within device 01h = uniform device 02h = boot device
2Dh 2Eh 2Fh 30h	5Ah 5Ch 5Eh 60h	00xxh 0000h 00x0h 000xh	Erase block region 1 information (refer to the CFI specification or CFI publication 100) 007Fh, 0000h, 0000h, 0001h = 64 Mb (01, 02, 06, 07, V1, V2, V6, V7) 0007h, 0000h, 0020h, 0000h = 64 Mb (03, 04)
31h 32h 33h 34h	60h 64h 66h 68h	00xxh 0000h 0000h 000xh	Erase block region 2 information (refer to CFI publication 100) 0000h, 0000h, 0000h, 0000h = 64 Mb (01, 02, 06, 07, V1, V2, V6, V7) 007Eh, 0000h, 0000h, 0001h = 64 Mb (03, 04)
35h 36h 37h 38h	6Ah 6Ch 6Eh 70h	0000h 0000h 0000h 0000h	Erase block region 3 information (refer to CFI publication 100)
39h 3Ah 3Bh 3Ch	72h 74h 76h 78h	0000h 0000h 0000h 0000h	Erase block region 4 information (refer to CFI publication 100)
3Dh 3Eh 3Fh	7Ah 7Ch 7Eh	FFFFh FFFFh FFFFh	Reserved

Table 16 Primary vendor-specific extended query

Addresses (×16)	Addresses (×8)	Data	Description
40h 41h 42h	80h 82h 84h	0050h 0052h 0049h	Query-unique ASCII string “PRI”
43h	86h	0031h	Major version number, ASCII
44h	88h	0033h	Minor version number, ASCII
45h	8Ah	0020h	Address Sensitive Unlock (Bits 1–0) 0 = Required 1 = Not required Process Technology (Bits 5–2) 1000b = 65 nm MIRRORBIT™ Reserved (Bits 7–6)
46h	8Ch	0002h	Erase Suspend 0 = Not supported 1 = To Read Only 2 = To Read and Write
47h	8Eh	0001h	Sector Protect 0 = Not supported X = Number of sectors in smallest sector
48h	90h	0000h	Sector Temporary Unprotect 00 = Not supported 01 = Supported
49h	92h	0008h	Sector Protect / Unprotect scheme 0008h = Advanced sector protection
4Ah	94h	0000h	Simultaneous operation 00 = Not supported X = Number of sectors in bank
4Bh	96h	0000h	Burst mode type 00 = Not supported 01 = Supported
4Ch	98h	0002h	Page mode type 02 = 8 word page
4Dh	9Ah	00B5h	ACC (Acceleration) supply minimum 00h = Not supported D7–D4: Volt D3–D0: 100 mV
4Eh	9Ch	00C5h	ACC (Acceleration) supply maximum 00h = Not supported D7–D4: Volt D3–D0: 100 mV
4Fh	9Eh	00xxh	Top / Bottom boot sector flag 02h = Bottom boot device 03h = Top boot device 04h = Uniform sectors bottom WP# protect 05h = Uniform sectors top WP# protect
50h	A0h	0001h	Program Suspend 00h = Not supported 01h = Supported

8 Command definitions

Writing specific address and data commands or sequences into the command register initiates device operations. **Table 23** and **Table 25** define the valid register command sequences. **Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state**. A reset command is then required to return the device to reading array data.

All addresses are latched on the falling edge of WE# or CE#, whichever happens later. All data is latched on the rising edge of WE# or CE#, whichever happens first. Refer to **"AC characteristics"** on page 90 for timing diagrams.

8.1 Reading array data

The device is automatically set to reading array data after device power-up. No commands are required to retrieve data. The device is ready to read array data after completing an Embedded Program or Embedded Erase algorithm.

After the device accepts an Erase Suspend command, the device enters the erase-suspend-read mode, after which the system can read data from any non-erase-suspended sector. After completing a programming operation in the Erase Suspend mode, the system may once again read array data with the same exception. See **"Erase Suspend / Erase Resume commands"** on page 45 for more information.

The system must issue the reset command to return the device to the read (or erase-suspend-read) mode if DQ5 goes high during an active program or erase operation, or if the device is in the autoselect mode. See **Reset command** below for more information.

See also **"Requirements for reading array data"** on page 15 for more information. The Read-Only Operations – **"AC characteristics"** on page 90 provide the read parameters, and **Figure 23** shows the timing diagram.

8.2 Reset command

Writing the Reset command resets the device to the read or erase-suspend-read mode. Address bits are don't cares for this command.

The Reset command may be written between the sequence cycles in an erase command sequence before erasing begins. This resets the device to the read mode. Once erasure begins, however, the device ignores reset commands until the operation is complete.

The Reset command may be written between the sequence cycles in a program command sequence before programming begins. This resets the device to the read mode. If the program command sequence is written while the device is in the Erase Suspend mode, writing the reset command returns the device to the erase-suspend-read mode. Once programming begins, however, the device ignores reset commands until the operation is complete.

The Reset command may be written between the sequence cycles in an autoselect command sequence. Once in the autoselect mode, the Reset command must be written to return to the read mode. If the device entered the autoselect mode while in the Erase Suspend mode, writing the Reset command returns the device to the erase-suspend-read mode.

If DQ5 goes high during a program or erase operation, writing the Reset command returns the device to the read mode (or erase-suspend-read mode if the device was in Erase Suspend).

Note that if DQ1 goes high during a Write Buffer Programming operation, the system must write the Write-to-Buffer-Abort Reset command sequence to reset the device for the next operation.

8.3 Autoselect command sequence

The Autoselect command sequence allows the host system to read several identifier codes at specific addresses:

Table 17 Autoselect command sequence

Identifier code	A7:A0 (×16)	A6:A1 (×8)
Manufacturer ID	00h	00h
Device ID, Cycle 1	01h	02h
Device ID, Cycle 2	0Eh	1Ch
Device ID, Cycle 3	0Fh	1Eh
Secure Silicon Region Factory Protect	03h	06h
Sector Protect Verify	(SA)02h	(SA)04h

The Autoselect command sequence is initiated by first writing on unlock cycle (two cycles). This is followed by a third write cycle that contains the Autoselect command. The device then enters the autoselect mode. The system may read at any address any number of times without initiating another Autoselect command sequence:

The system must write the reset command to return to the read mode (or erase-suspend-read mode if the device was previously in Erase Suspend).

8.4 Status Register ASO

The Status Register ASO contains a single word of registered volatile status for Embedded Algorithms. When the Status Register Read command is issued, the current status is captured by the register and the ASO is entered. The Status Register content appears at all word locations in the device address space. However, it is recommended to read the status only at word location 0 for future compatibility. The first read access in the Status Register ASO or a Software Reset / ASO Exit write command exits the ASO and returns to the address space map in use when the Status Register Read command was issued. It is not recommended to perform any other command after the Status Register Read command is given and before the Status Register ASO is exited.

8.5 Enter / Exit Secure Silicon Region command sequence

The secure silicon region provides a secured data area containing an 8-word / 16-byte random electronic serial number (ESN). The system can access the secure silicon region by issuing the three-cycle Enter Secure Silicon Region command sequence. The device continues to access the secure silicon region until the system issues the four-cycle Exit Secure Silicon Region command sequence or Reset / ASO Exit command which returns the device to normal operation. **Table 23** and **Table 25** show the address and data requirements for both command sequences. See also **"Secure silicon region flash memory"** on page 26 for further information. Note that the ACC function and unlock bypass modes are not available when the secure silicon region is enabled.

Note
11.The device ID is read over three cycles. SA = Sector Address.

8.6 ECC Status ASO

The system can access the ECC Status ASO by issuing the ECC Status Entry command sequence during Read mode. The ECC Status ASO provides the status of the ECC function, enabled or disabled, or if the ECC function corrected a single-bit error when reading the selected page. **"Automatic ECC"** on page 16 describes the ECC function in greater detail.
The ECC Status ASO allows the following activities:

- Read ECC Status for the selected page.
- ASO exit.

8.6.1 ECC Status

The contents of the ECC Status ASO indicate, for the selected page, whether the ECC logic has corrected an error in the eight bit ECC code, in the 32-byte page of data, or that ECC is disabled for that page. The address specified in the ECC Status Read command, provided in **Table 23** and **Table 25**, selects the desired ECC page.

Table 18 ECC status word - upper byte

Bit	15	14	13	12	11	10	9	8
Name	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU
Value	X	X	X	X	X	X	X	X

Table 19 ECC status word - lower byte

Bit	7	6	5	4	3	2	1	0
Name	RFU	RFU	RFU	RFU	ECC enabled on 16-word page	Single bit error corrected in ECC bits	Singe bit error corrected in data bits	RFU
Value	X	X	X	X	0 = ECC enabled 1 = ECC disabled	0 = No error corrected 1 = Single bit error corrected	0 = No error corrected 1 = Single bit error corrected	X

8.7 Word Program command sequence

Programming is a four-bus-cycle operation. The Program command sequence is initiated by writing two unlock write cycles, followed by the program set-up command. The program address and data are written next, which in turn initiate the Embedded Program algorithm. The system is not required to provide further controls or timings. The device automatically provides internally generated program pulses and verifies the programmed cell margin. **Table 23** and **Table 25** show the address and data requirements for the Word Program command sequence, respectively.

When the Embedded Program algorithm is complete, the device then returns to the read mode and addresses are no longer latched. The system can determine the status of the program operation by using DQ7 or DQ6. Refer to **"Write Operation status"** on page 56 for information on these status bits. Any commands written to the device during the Embedded Program algorithm are ignored. Note that the secure silicon region, autoselect, and CFI functions are unavailable when a program operation is in progress. Note that a hardware reset immediately terminates the program operation. The Program command sequence should be reinitiated once the device returns to the read mode, to ensure data integrity.

Programming is allowed in any sequence of address locations and across sector boundaries. Programming to the same word address multiple times without intervening erases (incremental bit programming) requires a modified programming method. For such application requirements, please contact your local Infineon representative. Word programming is supported for backward compatibility with existing flash driver software and for occasional writing of individual words. Use of write buffer programming (see below) is strongly recommended for general programming use when more than a few words are to be programmed.

Any bit in a word cannot be programmed from '0' back to '1'. Attempting to do so may cause DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read shows that the data is still '0'. Only erase operations can convert '0' to '1'.

8.8 Unlock Bypass command sequence

This device features an Unlock Bypass mode to facilitate shorter programming and erase commands. Once the device enters the Unlock Bypass mode, only two write cycles are required to program or erase data, instead of the normal four or six cycles, respectively.

The Unlock Bypass command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Unlock Bypass command, 20h. The device then enters the Unlock Bypass mode.

This mode dispenses with the initial two unlock cycles required in the standard program sequence and four unlock cycles in the Standard Erase command sequence, resulting in faster total programming and erase times.**Table 23** and **Table 25** show the requirements for the Unlock Bypass command sequences.

During the Unlock Bypass mode, only the Read, Program, Write Buffer Programming, Write-to-Buffer-Abort Reset, Unlock Bypass Sector Erase, Unlock Bypass Chip Erase and Unlock Bypass Reset commands are valid. To exit the Unlock Bypass mode, the system must issue the two-cycle Unlock Bypass Reset command sequence. The first cycle address is 'don't care' and the data 90h. The second cycle need only contain the data 00h. The sector then returns to the read mode.

8.9 Write buffer programming

Write Buffer Programming allows the system write to a maximum of 128 words / 256 bytes in one programming operation. This results in faster effective programming time than the standard programming algorithms. The Write Buffer Programming command sequence is initiated by first writing two unlock cycles. This is followed by a third write cycle containing the Write Buffer Load command written at the sector address in which programming occurs. The fourth cycle writes the sector address and the number of word locations, minus one, to be programmed. For example, if the system programs six unique address locations, then 05h should be written to the device. This tells the device how many write buffer addresses are loaded with data and therefore when to expect the Program Buffer to Flash command. The number of locations to program cannot exceed the size of the write buffer or the operation aborts.

The fifth cycle writes the first address location and data to be programmed. The write-buffer-page is selected by address bits A_{MAX}–A_7. All subsequent address / data pairs must fall within the selected-write-buffer-page. The system then writes the remaining address / data pairs into the write buffer. Write buffer locations may be loaded in any order.

The write-buffer-page address must be the same for all address / data pairs loaded into the write buffer. (This means Write Buffer Programming cannot be performed across multiple write-buffer pages.) This also means that Write Buffer Programming cannot be performed across multiple sectors. If the system attempts to load programming data outside of the selected write-buffer page, the operation aborts.

Note that if a Write Buffer address location is loaded multiple times, the address / data pair counter is decremented for every data load operation. The host system must therefore account for loading a write-buffer location more than once. The counter decrements for each data load operation, not for each unique write-buffer-address location. Note also that if an address location is loaded more than once into the buffer, the final data loaded for that address is programmed.

Once the specified number of write buffer locations are loaded, the system must then write the Program Buffer to Flash command at the sector address. Any other address and data combination aborts the Write Buffer Programming operation. The device then begins programming. Data polling should be used while monitoring the last address location loaded into the write buffer. DQ7, DQ6, DQ5, and DQ1 should be monitored to determine the device status during Write Buffer Programming.

The Write Buffer Programming operation can be suspended using the standard Program Suspend / Resume commands. Upon successful completion of the Write Buffer Programming operation, the device is ready to execute the next command.

The Write Buffer Programming sequence can be aborted in the following ways:

- Load a value that is greater than the page buffer size during the Number of Locations to Program step.
- Write to an address in a sector different than the one specified during the Write-Buffer-Load command.
- Write an Address / Data pair to a different write-buffer-page than the one selected by the Starting Address during the write buffer data loading stage of the operation.
- Write data other than the Confirm Command after the specified number of data load cycles.

The abort condition is indicated by DQ1 = 1, DQ7 = DATA# (for the last address location loaded), DQ6 = toggle, and DQ5 = 0. A Write-to-Buffer-Abort Reset command sequence must be written to reset the device for the next operation.

Note that the secure silicon region, autoselect, and CFI functions are unavailable when a program operation is in progress. This flash device is capable of handling multiple write buffer programming operations on the same write buffer address range without intervening erases. For applications requiring incremental bit programming, a modified programming method is required; please contact your local Infineon representative. **Any bit in a write buffer address range cannot be programmed from ‘0’ back to ‘1’.** Attempting to do so may cause the device to set DQ5 = 1, of cause the DQ7 and DQ6 status bits to indicate the operation was successful. However, a succeeding read shows that the data is still ‘0’. Only erase operations can convert ‘0’ to ‘1’.

8.10 Accelerated program

The device supports program operations when the system asserts V_{HH} on the WP#/ACC or ACC pin. When WP#/ACC or ACC pin is lowered back to V_{IH} or V_{IL} the device exits the Accelerated Programming mode and returns to normal operation. The WP#/ACC is V_{HH} tolerant but is not designed to accelerate the program functions. If the system asserts V_{HH} on this input, the device automatically enters the Unlock Bypass mode. The system can then use the Write Buffer Load command sequence provided by the Unlock Bypass mode. Note that if a Write-to-Buffer-Abort Reset is required while in Unlock Bypass mode, the full 3-cycle RESET command sequence must be used to reset the device. Note that the WP#/ACC pin must not be at V_{HH} for operations other than accelerated programming, or device damage may result. WP# contains an internal pull-up; when unconnected, WP# is at V_{IH}. Accelerated programming is supported at room temperature only.

Figure 9 illustrates the algorithm for the program operation. Refer to **Table 76** for parameters, and **Figure 34** for timing diagrams.

- Sectors must be unlocked prior to raising WP#/ACC to V_{HH}.
- It is recommended that WP#/ACC apply V_{HH} after power-up sequence is completed. In addition, it is recommended that WP#/ACC apply from V_{HH} to V_{IH}/V_{IL} before powering down V_{CC}/V_{IO}.

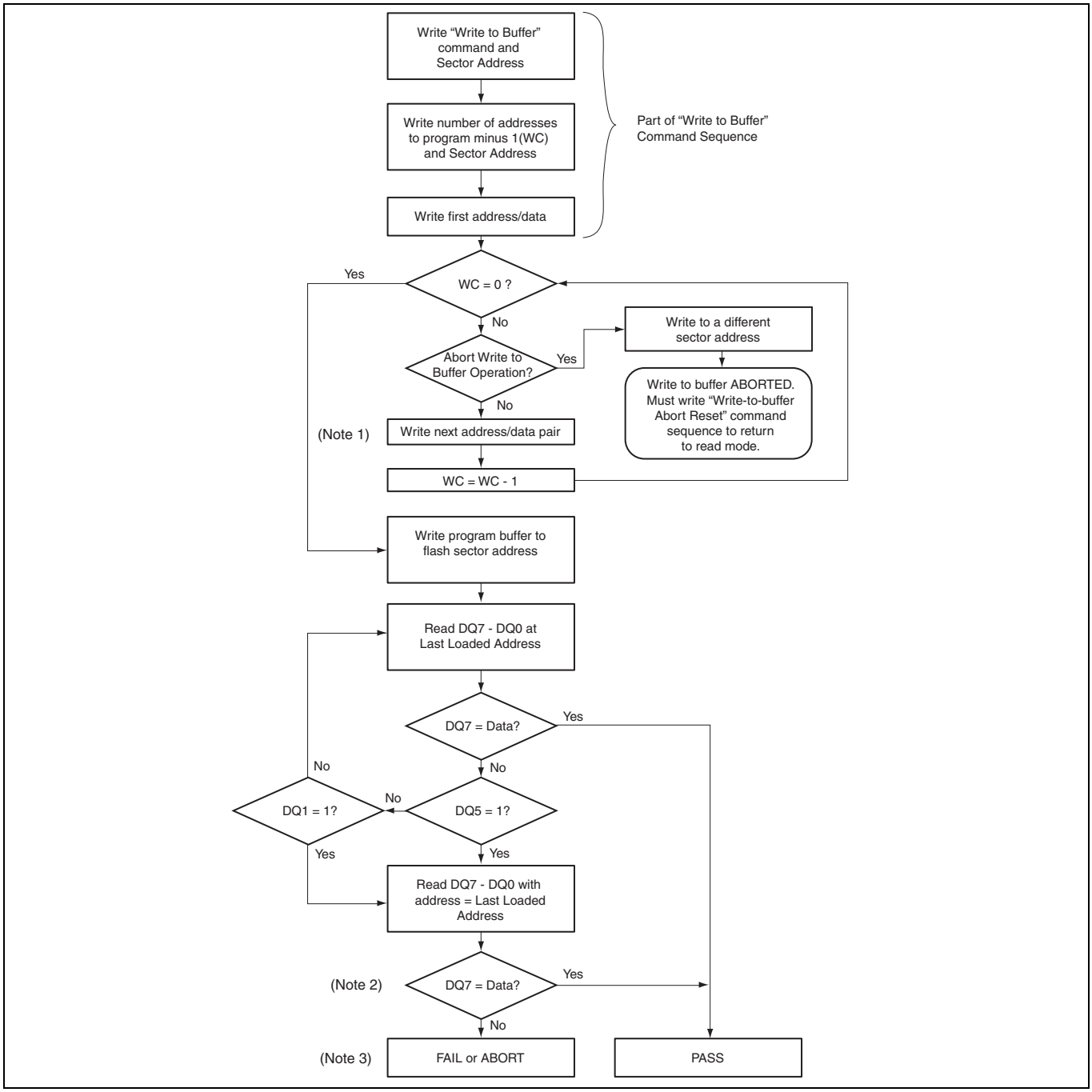


Figure 9 Write buffer programming operation

Notes

12. When sector address is specified, any address in the selected sector is acceptable. However, when loading write-buffer address locations with data, all addresses must fall within the selected write-buffer page.
13. DQ7 may change simultaneously with DQ5. Therefore, DQ7 should be verified.
14. If this flowchart location was reached because DQ5 = 1, then the device failed. If this flowchart location was reached because DQ1 = 1, then the Write to Buffer operation was aborted. In either case, the proper reset command must be written before the device can begin another operation. If DQ1 = 1, write the Write-Buffer-Programming-Abort-Reset command. if DQ5 = 1, write the Reset command.
15. See **Table 23** and **Table 25** for command sequences required for Write Buffer Programming.

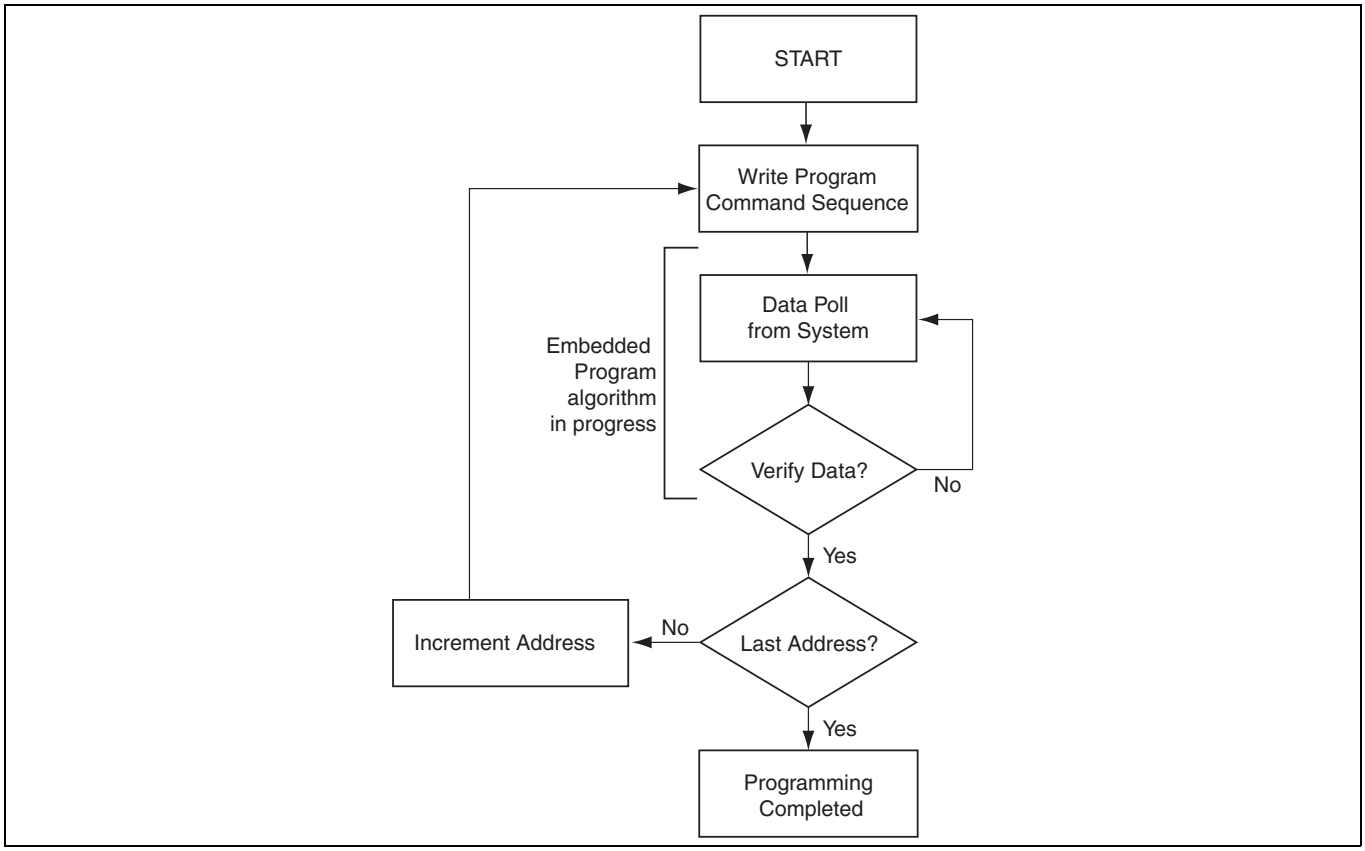


Figure 10 Program operation

Note
16.See **Table 23** and **Table 25** for Program command sequence.

8.11 Program Suspend / Program Resume command sequence

The Program Suspend command allows the system to interrupt a programming operation or a Write to Buffer Programming operation so that data can be read from any non-suspended sector. When the Program Suspend command is written during a programming process, the device halts the program operation within t_{PSL} (program suspend latency) and updates the status bits. Addresses are not required when writing the Program Suspend command.

There are two commands available for program suspend. The legacy combined Erase / Program suspend command (B0h command code) and the separate Program Suspend command (51h command code). There are also two commands for program resume. The legacy combined Erase / Program Resume command (30h command code) and the separate Program Resume command (50h command code). It is recommended to use the separate program suspend and resume commands for programming and use the legacy combined command only for erase suspend and resume.

After the programming operation is suspended, the system can read array data from any non-suspended sector. The Program Suspend command may also be issued during a programming operation while an erase is suspended. In this case, data may be read from any addresses not in Erase Suspend or Program Suspend. If a read is needed from the secure silicon region area (one-time program area), then user must use the proper command sequences to enter and exit this region. Note that the secure silicon region, autoselect, and CFI functions are unavailable when a program operation is in progress.

The system may also write the Autoselect command sequence when the device is in the Program Suspend mode. The system can read as many Autoselect codes as required. When the device exits the Autoselect mode, the device reverts to the Program Suspend mode, and is ready for another valid operation. See **"Autoselect command sequence"** on page 34 for more information.

After the Program Resume command is written, the device reverts to programming. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard program operation. See **"Write Operation status"** on page 56 for more information.

The system must write the Program Resume command (address bits are don't care) to exit the Program Suspend mode and continue the programming operation. Further writes of the Resume command are ignored. Another Program Suspend command can be written after the device resumes programming.

Program operations can be interrupted as often as necessary but in order for a program operation to progress to completion there must be some periods of time between resume and the next suspend command greater than or equal to t_{PRS} as listed in **Table 78** and **Table 79**.

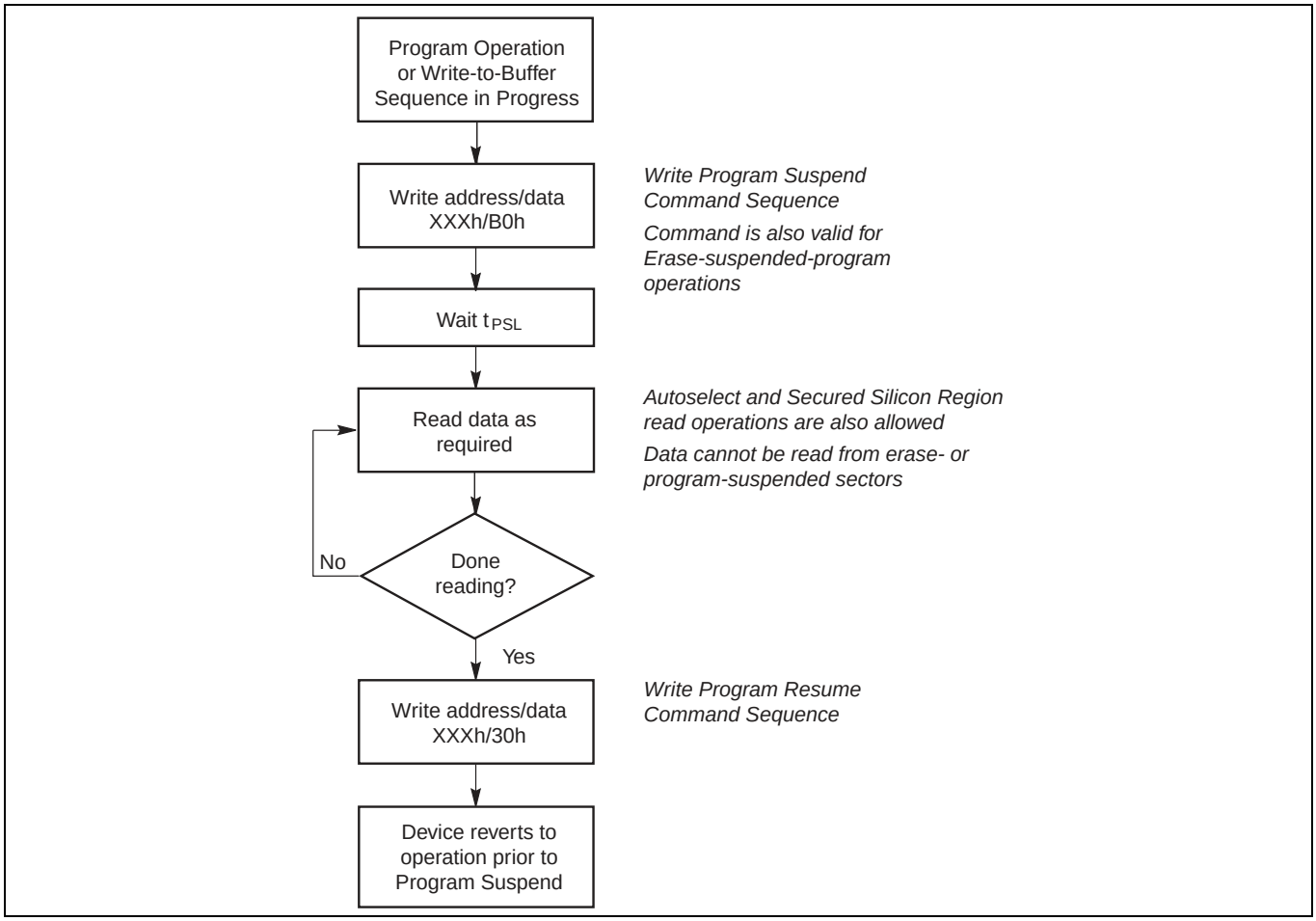


Figure 11 Program suspend / program resume

8.12 Chip Erase command sequence

Chip Erase is a six bus cycle operation. The Chip Erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock write cycles are then followed by the Chip Erase command, which in turn invokes the Embedded Erase algorithm. The device does not require the system to pre-program prior to erase. The Embedded Erase algorithm automatically preprograms and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations. **Table 23** and **Table 25** show the address and data requirements for the Chip Erase command sequence.

When the Embedded Erase algorithm is complete, the device returns to the read mode and addresses are no longer latched. The system can determine the status of the erase operation by using DQ7, DQ6, or DQ2. Refer to **"Write Operation status"** on page 56 for information on these status bits.

The Unlock Bypass feature allows the host system to send program commands to the flash device without first writing unlock cycles within the command sequence. See **"Unlock Bypass command sequence"** on page 36 for details on the Unlock Bypass function.

Any commands written during the Chip Erase operation are ignored. However, note that a hardware reset immediately terminates the erase operation. If this occurs, the Chip Erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

Figure 12 illustrates the algorithm for the erase operation. Refer to **"Asynchronous write operations"** on page 95 for parameters, and **Figure 35** for timing diagrams.

8.13 Sector Erase command sequence

Sector Erase is a six bus cycle operation. The Sector Erase command sequence is initiated by writing two unlock cycles, followed by a set-up command. Two additional unlock cycles are written, and are then followed by the address of the sector to be erased, and the Sector Erase command. **Table 23** and **Table 25** shows the address and data requirements for the Sector Erase command sequence.

The device does not require the system to pre-program prior to erase. The Embedded Erase algorithm automatically programs and verifies the entire memory for an all zero data pattern prior to electrical erase. The system is not required to provide any controls or timings during these operations.

After the command sequence is written, a sector erase time-out of t_{SEA} occurs. During the time-out period, additional sector addresses and sector erase commands may be written. Invalid commands will be ignored during the time-out period. Loading the sector erase buffer may be done in any sequence, and the number of sectors may be from one sector to all sectors. The time between these additional cycles must be less than 50 µs, otherwise erasure may begin. Any sector erase address and command following the exceeded time-out may or may not be accepted. It is recommended that processor interrupts be disabled during this time to ensure all commands are accepted. The interrupts can be re-enabled after the last Sector Erase command is written. Note that the secure silicon region, autoselect, and CFI functions are unavailable when an erase operation is in progress. The system must rewrite the command sequence and any additional addresses and commands.

The system can monitor DQ3 to determine if the sector erase timer has timed out (See **"DQ3: Sector erase timer"** on page 61). The time-out begins from the rising edge of the final WE# pulse in the command sequence.

If the sector is found to have not completed its last erase successfully, the sector is unconditionally erased. If the last erase was successful, the sector is read to determine if the sector is still erased (blank). The erase operation is started immediately after finding any programmed zero. If the sector is already blank (no programmed zero bit found) the remainder of the erase operation is skipped. This can dramatically reduce erase time when sectors being erased do not need the erase operation. When enabled the blank check feature is used within the parameter erase, sector erase, and bulk erase commands. When blank check is disabled an erase command unconditionally starts the erase operation.

When the Embedded Erase algorithm is complete, the device returns to reading array data and addresses are no longer latched. The system can determine the status of the erase operation by reading DQ7, DQ6, or DQ2 in the erasing sector. Refer to **"Write Operation status"** on page 56 for information on these status bits.

Once the sector erase operation begins, only the Erase Suspend command is valid. All other commands are ignored. However, note that a hardware reset immediately terminates the erase operation. If that occurs, the sector erase command sequence should be reinitiated once the device returns to reading array data, to ensure data integrity.

Figure 12 illustrates the algorithm for the erase operation. Refer to **"Asynchronous write operations"** on page 95 for parameters, and **Figure 35** for timing diagrams.

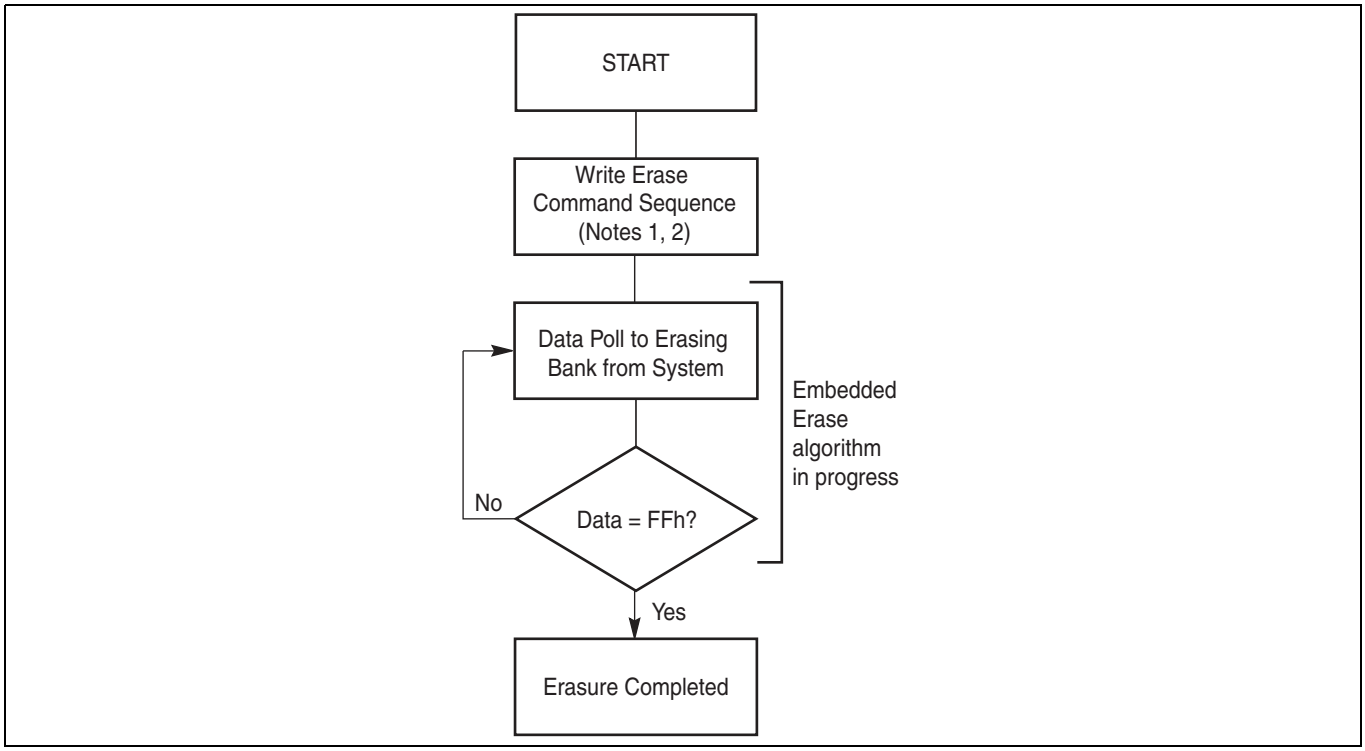


Figure 12 Erase operation

Notes
17. See **Table 23** and **Table 25** for Program command sequence.
18. See **"DQ3: Sector erase timer"** on page 61 for information on the sector erase timer.

8.14 Erase Suspend / Erase Resume commands

The Erase Suspend command, B0h, allows the system to interrupt a sector erase operation and then read data from, or program data to, any sector not selected for erasure. This command is valid only during the sector erase operation, including the t_{ESL} time-out period during the Sector Erase command sequence. The Erase Suspend command is ignored if written during the chip erase operation or Embedded Program algorithm.

When the Erase Suspend command is written during the sector erase operation, the device requires t_{ESL} (erase suspend latency) to suspend the erase operation. However, when the Erase Suspend command is written during the sector erase time-out, the device immediately terminates the time-out period and suspends the erase operation.

After the erase operation is suspended, the device enters the erase-suspend-read mode. The system can read data from or program data to any sector not selected for erasure. (The device erase suspends all sectors selected for erasure.) Reading at any address within erase-suspended sectors produces status information on DQ7–DQ0. The system can use DQ7, or DQ6 and DQ2 together, to determine if a sector is actively erasing or is erase-suspended. Refer to **"Write Operation status"** on page 56 for information on these status bits.

After an erase-suspended program operation is complete, the device returns to the erase-suspend-read mode. The system can determine the status of the program operation using the DQ7 or DQ6 status bits, just as in the standard word program operation. Refer to **"Write Operation status"** on page 56 for more information.

In the erase-suspend-read mode, the system can also issue the Autoselect command sequence. Refer to the **"Autoselect mode"** on page 20 and **"Autoselect command sequence"** on page 34 sections for details.

To resume the sector erase operation, the system must write the Erase Resume command. Further writes of the Resume command are ignored. Another Erase Suspend command can be written after the chip resumes erasing.

During an erase operation, this flash device performs multiple internal operations which are invisible to the system. When an erase operation is suspended, any of the internal operations that were not fully completed must be restarted. As such, if this flash device is continually issued suspend / resume commands in rapid succession, erase progress is impeded as a function of the number of suspends. The result is a longer cumulative erase time than without suspends. Note that the additional suspends do not affect device reliability or future performance. In most systems rapid erase / suspend activity occurs only briefly. In such cases, erase performance is not significantly impacted.

Erase operations can be interrupted as often as necessary but in order for an erase operation to progress to completion there must be some periods of time between resume and the next suspend command greater than or equal to t_{ERS} as listed in **Table 78** and **Table 79**.

8.15 Evaluate Erase Status

The Evaluate Erase Status (EES) command verifies that the last erase operation on the addressed sector was completed successfully. The EES command can be used to detect erase operations failed due to loss of power, reset, or failure during the erase operation.

To initiate a EES on a Sector, write 35h to the sector address (SA), while the EAC is in the standby state

The ESS command may not be written while the device is actively programming or erasing or suspended.

The EES command does not allow for reads to the array during the operation. Reads to the array while this command is executing will return unknown data.

Use the Status Register read to confirm if the device is still busy and when complete if the sector is erased or not. Bit 7 of the Status Register will show if the device is performing a ESS (similar to an erase operation). Bit 5 of the Status Register will be cleared to '0' if the sector is erased and set to '1' if not erased.

As soon as any bit is found to not be erased, the device will halt the operation and report the results.

Once the ESS is completed, the EAC will return to the Standby state.

The EES command requires t_{EES} (refer to **Table 78**) to complete and update the erase status in SR. The DRB bit (SR[7]) may be read to determine when the EES command is finished. If a sector is found not erased with SR[5] = 1, the sector must be erased again to ensure reliable storage of data in the sector.

8.16 Continuity Check

The Continuity Check provides a basic test of connectivity from package connectors to each die pad. This feature is an extension of the legacy unlock cycle sequence used at the beginning of several commands. The unlock sequence is two writes with alternating ones and zeros pattern on the lower portion of the address and data lines with the pattern inverted between the first and second write.

To perform a continuity check these patterns are extended to cover all address and data lines:

Table 20 Continuity Check

	Address bus	Data bus
×16 Mode	AMAX–A0	D15–D0
×8 Mode	AMAX–A1	D7–D0

A logic comparison circuit looks for the alternating one and zero pattern that is inverted between the two write cycles.

When the correct patterns are detected, the status register bit zero is set to '1'. The status register clear command will clear the Status Register bit zero to '0'.

Table 21 x16 data bus

Phase	Access type	S29GL064S Address A21 to A0	Data	Comment
Set-up	Write	555	XX71	Clear die status
	Write	555	XX70	Write Status Register Read command to die
	Read	XXX	RD	Read status from die to confirm status bit zero = 0
Continuity pattern	Write	2AAA55	FF00	First continuity cycle
	Write	1555AA	00FF	Second continuity cycle
Verify continuity pattern detected	Write	555	XX70	Write Status Register Read command to die
	Read	XXX	RD	Read status from die to confirm status bit zero = 1 for continuity pattern detected

Table 22 X8 data bus

Phase	Access type	S29GL064S Address A21 to A1	Data	Comment
Set-up	Write	AAA	71	Clear die status
	Write	AAA	70	Write Status Register Read command to die
	Read	XXX	RD	Read status from die to confirm status bit zero = 0
Continuity pattern	Write	5554AB	FF	First continuity cycle
	Write	2AAB54	00	Second continuity cycle
Verify continuity pattern detected	Write	AAA	70	Write Status Register Read command to die
	Read	XXX	RD	Read status from die to confirm status bit zero = 1 for continuity pattern detected

The alternating one and zero pattern checks for adjacent wire shorts. The inversion of the pattern between cycles checks for stuck-at faults. The status output being cleared and set checks for stuck-at faults on the status output. Checking for different status results from each die checks for working die selection logic.

8.17 Command definitions

Table 23 Command definitions (×16 mode, BYTE# = V_{IH})

Command sequence [19]		Cycles	Bus cycles [20, 21, 22, 23]													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read [23]		1	RA	RD												
Reset [24]		1	XXX	F0												
Status Register Read		2	555	70	XXX	RD										
Status Register Clear		1	555	71												
Autoselect [25]	Manufacturer ID	4	555	AA	2AA	55	555	90	X00	0001						
	Device ID [26]	6	555	AA	2AA	55	555	90	X01	227E	X0E	Note 27	X0F	Note 27		
	Device ID	4	555	AA	2AA	55	555	90	X01	Note 28						
	Secure Silicon Region Factory Protect	4	555	AA	2AA	55	555	90	X03	Note 29						
	Sector Protect Verify [30]	4	555	AA	2AA	55	555	90	(SA) X02	00/01						
	Reset / ASO Exit [24]	1	XXX	F0												
Program		4	555	AA	2AA	55	555	A0	PA	PD						
Write to Buffer [31]		3	555	AA	2AA	55	SA	25	SA	WC	PA	PD	WBL	PD		
Program Buffer to Flash		1	SA	29												
Write to Buffer Abort Reset [32]		3	555	AA	2AA	55	555	F0								
Unlock Bypass	Enter	3	555	AA	2AA	55	555	20								
	Program [33]	2	XXX	A0	PA	PD										
	Write to Buffer [33]	4	SA	25	SA	WC	PA	PD	WBL	PD						
	Sector Erase	2	XXX	80	SA	30										
	Chip Erase	2	XXX	80	XXX	10										
	Reset [34]	2	XXX	90	XXX	00										
Chip Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	555	10		
Sector Erase		6	555	AA	2AA	55	555	80	555	AA	2AA	55	SA	30		
Erase Suspend / Program Suspend Legacy method [35]		1	XXX	B0												
Erase Suspend Enhanced method																
Erase Resume / Program Resume Legacy method [36]		1	XXX	30												
Erase Resume Enhanced method																
Program Suspend Enhanced method		1	XXX	51												
Program Resume Enhanced method		1	XXX	50												
Evaluate Erase status		1	(SA) 555	35												
Secure Silicon Region (SSR) ASO	SSR Entry	3	555	AA	2AA	55	555	88								
	Read [23]	1	RA	RD												
	Word Program	4	555	AA	2AA	55	555	A0	PA	PD						
	Write to Buffer [31]	6	555	AA	2AA	55	SA	25	SA	WC	WBL	PD	WBL	PD		
	Program Buffer to Flash (confirm)	1	SA	29												
	Write-to-Buffer-Abort Reset [32]	3	555	AA	2AA	55	555	F0								
	SSR Exit	4	555	AA	2AA	55	555	90	XX	0						
	Reset / ASO Exit [24]	1	XXX	F0												
CFI Query [28]		1	55	98												
CFI Exit		1	XXX	F0												
CFI Exit (Alternate)		1	XXX	FF												
Continuity Check		7	555	XX71	555	XX70	XXX	RD	2AAA55[37]	FF00	1555AA[38]	00FF	555	XX70	XXX	RD
ECC ASO	ECC ASO Entry	3	555	AA	2AA	55	555	75								
	ECC Status Read	1	RA	RD												
	ECC ASO Exit	2	XXX	F0												

Legend:
X = Don't care.
RA = Read Address of memory location to be read.
RD = Read Data read from location RA during read operation.
PA = Program Address. Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.
PD = Program Data for location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.
SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A_{MAX}–A15 uniquely select any sector for uniform mode device and A_{MAX}–A12 for boot mode device.
WBL = Write Buffer Location. Address must be within same write buffer page as PA.
WC = Word Count. Number of write buffer locations to load minus 1.

Notes
19. See **Table 4** for description of bus operations.
20. All values are in hexadecimal.
21. Shaded cells indicate read cycles. All others are write cycles.
22. During unlock and command cycles, when lower address bits are 555 or 2AA as shown in table, address bits above A11 and data bits above DQ7 are don't care.
23. No unlock or command cycles required when device is in read mode.
24. Reset command is required to return to read mode (or to erase-suspend-read mode if previously in Erase Suspend) when device is in autoselect mode, or if DQ5 goes high while device is providing status information.
25. Fourth cycle of the autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. Except for RD, PD and WC. See **"Autoselect command sequence"** on page 34 for more information.
26. Device ID must be read in three cycles.
27. Refer to **Table 9**, for individual Device IDs per device density and model number.
28. Command is valid when device is ready to read array data or when device is in autoselect mode.
29. Refer to **Table 9** for data indicating Secure Silicon Region factory protect status.
30. Data is 00h for an unprotected sector and 01h for a protected sector.
31. Total number of cycles in command sequence is determined by number of words written to write buffer. Maximum number of cycles in command sequence is 37, including Program Buffer to Flash command.
32. Command sequence resets device for next command after aborted write-to-buffer operation.
33. Unlock Bypass command is required prior to Unlock Bypass Program command.
34. Unlock Bypass Reset command is required to return to read mode when device is in unlock bypass mode.
35. System may read and program in non-erasing sectors, or enter autoselect mode, when in Erase Suspend mode. Erase Suspend command is valid only during a sector erase operation.
36. Erase Resume command is valid only during Erase Suspend mode.
37. The Address for the fourth cycle depends on the number of address lines supported by the device. See **Table 21**.
38. The Address for the fifth cycle depends on the number of address lines supported by the device. See **Table 21**.

Table 24 Sector Protection commands (×16)

Command sequence (Notes)		Cycles	Bus cycles [39, 40, 41, 42]													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register Bits	Command Set Entry [43]	3	555	AA	2AA	55	555	40								
	Program [44]	2	XX	A0	XXX	Data										
	Read [44]	1	00	Data												
	Command Set Exit [45]	2	XX	90	XX	00										
	Reset / ASO Exit [44]	1	XXX	F0												
Password Protection	Command Set Entry [43]	3	555	AA	2AA	55	555	60								
	Program [46]	2	XX	A0	PWAx	PWDx										
	Read [47]	4	00	PWD0	01	PWD1	02	PWD2	03	PWD3						
	Unlock [48]	7	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	00	29
	Command Set Exit [45]	2	XX	90	XX	00										
	Reset / ASO Exit [44]	1	XXX	F0												
Non-Volatile Sector Protection (PPB)	Command Set Entry [43]	3	555	AA	2AA	55	555	C0								
	PPB Program [49]	2	XX	A0	SA	00										
	All PPB Erase [49, 50]	2	XX	80	00	30										
	PPB Status Read	1	SA	RD(0)												
	Command Set Exit [45]	2	XX	90	XX	00										
	Reset / ASO Exit [44]	1	XXX	F0												
Global Volatile Sector Protection Freeze (PPB Lock)	Command Set Entry [43]	3	555	AA	2AA	55	555	50								
	PPB Lock Bit Set	2	XX	A0	XX	00										
	PPB Lock Bit Status Read	1	XXX	RD(0)												
	Command Set Exit [45]	2	XX	90	XX	00										
	Reset / ASO Exit [44]	1	XXX	F0												
Volatile Sector Protection (DYB)	Command Set Entry [43]	3	555	AA	2AA	55	555	E0								
	DYB Set	2	XX	A0	SA	00										
	DYB Clear	2	XX	A0	SA	01										
	DYB Status Read	1	SA	RD(0)												
	Command Set Exit [45]	2	XX	90	XX	00										
	Reset / ASO Exit [44]	1	XXX	F0												

Legend:
X = Don't care.
RA = Address of the memory location to be read.
SA = Sector Address. Any address that falls within a specified sector. See Tables 5–8 for sector address ranges.
PWAx = PPB Password address for word0 = 00h, word1 = 01h, word2 = 02h, and word3 = 03h (Sector Address = Word Line = 0).
PWDx = Password data word0, word1, word2, and word3.
RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 0. If unprotected, DQ0 = 1.
Gray vs. White Box = Read vs. Write Operation.

Notes

39. All values are in hexadecimal.
40. Shaded cells indicate read cycles. All others are write cycles.
41. Address and data bits not specified in table, legend, or notes are don't cares (each hex digit implies 4 bits of data).
42. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.
43. Entry commands are required to enter a specific mode to enable instructions only available within that mode.
44. No unlock or command cycles required when bank is reading array data.
45. Exit command must be issued to reset the device into read mode; device may otherwise be placed in an unknown state.
46. Entire two bus-cycle sequence must be entered for each portion of the password.
47. Full address range is required for reading password.
48. Password may be unlocked or read in any order. Unlocking requires the full password (all seven cycles).
49. ACC must be at V_{IH} when setting PPB or DYB.
50. "All PPB Erase" command pre-programs all PPBs before erasure to prevent over-erasure.

Table 25 Command definitions (×8 Mode, BYTE# = V_{IL})

Command sequence [51]		Cycles	Bus cycles [52, 53, 54, 55]													
			First		Second		Third		Fourth		Fifth		Sixth		Seventh	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Read [56]		1	RA	RD												
Reset [57]		1	XXX	F0												
Status Register Read		2	AAA	70	XXX [58]	RD										
Status Register Clear		1	AAA	71												
Autoselect [59]	Manufacturer ID	4	AAA	AA	555	55	AAA	90	X00	01						
	Device ID [60]	6	AAA	AA	555	55	AAA	90	X02	7E	X1C	Note 61	X1E	Note 61		
	Device ID	4	AAA	AA	555	55	AAA	90	X02	Note 62						
	Secure Silicon Region Factory Protect	4	AAA	AA	555	55	AAA	90	X06	Note 63						
	Sector Protect Verify [64]	4	AAA	AA	555	55	AAA	90	(SA) X04	00/01						
	Reset / ASO Exit [57]	1	XXX	F0												
Program		4	AAA	AA	555	55	AAA	A0	PA	PD						
Write to Buffer [65]		3	AAA	AA	555	55	SA	25	SA	BC	PA	PD	WBL	PD		
Program Buffer to Flash		1	SA	29												
Write to Buffer Abort Reset [66]		3	AAA	AA	555	55	AAA	F0								
Chip Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	AAA	10		
Sector Erase		6	AAA	AA	555	55	AAA	80	AAA	AA	555	55	SA	30		
Unlock Bypass	Enter	3	AAA	AA	555	55	AAA	20								
	Program	2	XXX	A0	PA	PD										
	Write to Buffer	4	SA	25	SA	BC	PA	PD	WBL	PD						
	Sector Erase	2	XXX	80	SA	30										
	Chip Erase	2	XXX	80	XXX	10										
	Reset	2	XXX	90	XXX	00										
Erase Suspend / Program Suspend Legacy method [67]		1	XXX	B0												
Erase Suspend Enhanced method																
Erase Resume / Program Resume Legacy method [62]		1	XXX	30												
Erase Resume Enhanced method																
Program Suspend Enhanced method		1	XXX	51												
Program Resume Enhanced method		1	XXX	50												
Evaluate Erase Status		1	(SA) AAA	35												
Secure Silicon Region (SSR) ASO	SSR Entry	3	AAA	AA	555	55	AAA	88								
	Read [55]	1	RA	RD												
	Word Program	4	AAA	AA	555	55	AAA	A0	PA	PD						
	Write to Buffer [65]	6	AAA	AA	555	55	SA	25	SA	BC	PA	PD	WBL	PD		
	Program Buffer to Flash (confirm)	1	SA	29												
	Write-to-Buffer-Abort Reset [66]	3	AAA	AA	555	55	AAA	F0								
	SSR Exit	4	AAA	AA	555	55	AAA	90	XXX	00						
	Reset / ASO Exit [57]	1	XXX	F0												
CFI Query [62]		1	AA	98												
CFI Exit		1	XXX	F0												
CFI Exit (Alternate)		1	XXX	FF												
Continuity Check		7	AAA	71	AAA	70	XXX	RD	5554AB [68]	FF	2AAB54 [69]	00	AAA	70	XXX	RD
ECC ASO	ECC ASO Entry	3	AAA	AA	555	55	AAA	75								
	ECC Status Read	1	RA	RD												
	ECC ASO Exit	2	XXX	F0												

Legend:
X = Don't care.
RA = Read Address of memory location to be read.
RD = Read Data read from location RA during read operation.
PA = Program Address. Addresses latch on falling edge of WE# or CE# pulse, whichever happens later.
PD = Program Data for location PA. Data latches on rising edge of WE# or CE# pulse, whichever happens first.
SA = Sector Address of sector to be verified (in autoselect mode) or erased. Address bits A_{MAX}–A15 uniquely select any sector for uniform mode device and A_{MAX}–A12 for boot mode device.
WBL = Write Buffer Location. Address must be within same write buffer page as PA.
BC = Byte Count. Number of write buffer locations to load minus 1.

Notes
51. See **Table 4** for description of bus operations.
52. All values are in hexadecimal.
53. Shaded cells indicate read cycles. All others are write cycles.
54. During unlock and command cycles, when lower address bits are 555 or AAA as shown in table, address bits above A11 are don't care.
55. Unless otherwise noted, address bits A21–A11 are don't cares.
56. No unlock or command cycles required when device is in read mode.
57. Reset command is required to return to read mode (or to erase-suspend-read mode if previously in Erase Suspend) when device is in autoselect mode, or if DQ5 goes high while device is providing status information.
58. For ×8 mode, status register bits 0–7 are accessed when address bit A1 is '0' and bits 8–15 are accessed when address bit A1 is '1'.
59. Fourth cycle of autoselect command sequence is a read cycle. Data bits DQ15–DQ8 are don't care. See **"Autoselect command sequence"** on page 34 for more information.
60. For S29GL064S Device ID must be read in three cycles.
61. Refer to **Table 9**, for individual Device IDs per device density and model number.
62. Command is valid when device is ready to read array data or when device is in autoselect mode.
63. Refer to **Table 9**, for data indicating secure silicon region factory protect status.
64. Data is 00h for an unprotected sector and 01h for a protected sector.
65. Total number of cycles in command sequence is determined by number of bytes written to write buffer. Maximum number of cycles in command sequence is 261, including Program Buffer to Flash command.
66. Command sequence resets device for next command after aborted write-to-buffer operation.
67. Erase Resume command is valid only during Erase Suspend mode.
68. The Address for the fourth cycle depends on the number of address lines supported by the device. See **Table 22**.
69. The Address for the fifth cycle depends on the number of address lines supported by the device. See **Table 22**.
70. System may read and program in non-erasing sectors, or enter autoselect mode, when in Erase Suspend mode. Erase Suspend command is valid only during a sector erase operation.

Table 26 Sector Protection commands (x8)

Command Sequence (Notes)		Cycles	Bus Cycles [71, 72, 73, 74]													
			1st/8th		2nd/9th		3rd/10th		4th/11th		5th		6th		7th	
			Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data	Addr	Data
Lock Register Bits	Command Set Entry [75]	3	AAA	AA	555	55	AAA	40								
	Program [76]	2	XXX	A0	XXX	Data										
	Read [76]	1	00	Data												
	Command Set Exit [77]	2	XXX	90	XXX	00										
	Reset / ASO Exit [77]	1	XXX	F0												
Password Protection	Command Set Entry [75]	3	AAA	AA	555	55	AAA	60								
	Program [78]	2	XXX	A0	PWAx	PWDx										
	Read [79]	8	00	PWD0	01	PWD1	02	PWD2	03	PWD3	04	PWD4	05	PWD5	06	PWD6
			07	PWD7												
	Unlock [80]	11	00	25	00	03	00	PWD0	01	PWD1	02	PWD2	03	PWD3	04	PWD4
			05	PWD5	06	PWD6	07	PWD7	00	29						
	Command Set Exit [77]	2	XX	90	XX	00										
	Reset / ASO Exit [77]	1	XXX	F0												
Non-Volatile Sector Protection (PPB)	Command Set Entry [75]	3	AAA	AA	555	55	AAA	C0								
	PPB Program [81]	2	XXX	A0	SA	00										
	All PPB Erase [81, 82]	2	XXX	80	00	30										
	PPB Status Read	1	SA	RD(0)												
	Command Set Exit [77]	2	XXX	90	XXX	00										
	Reset / ASO Exit [77]	1	XXX	F0												
Global Volatile Sector Protection Freeze (PPB Lock)	Command Set Entry [75]	3	AAA	AA	555	55	AAA	50								
	PPB Lock Bit Set	2	XXX	A0	XXX	00										
	PPB Lock Bit Status Read	1	XXX	RD(0)												
	Command Set Exit [77]	2	XXX	90	XX	00										
	Reset / ASO Exit [77]	1	XXX	F0												
Volatile Sector Protection (DYB)	Command Set Entry [75]	3	AAA	AA	555	55	AAA	E0								
	DYB Set	2	XXX	A0	SA	00										
	DYB Clear	2	XXX	A0	SA	01										
	DYB Status Read	1	SA	RD(0)												
	Command Set Exit [77]	2	XXX	90	XXX	00										
	Reset / ASO Exit [77]	1	XXX	F0												

Legend:
X = Don't care.
RA = Address of the memory location to be read.
SA = Sector Address. Any address that falls within a specified sector. See Tables 5–8 for sector address ranges.
PWAx = PPB Password address for byte0 = 00h, byte1 = 01h, byte2 = 02h, byte3 = 03h, byte04= 04h, byte5 = 05h, byte6 = 06h, and byte7 = 07h (Sector Address = Word Line = 0).
PWDx = Password data byte0, byte1, byte2, byte3, byte4, byte5, byte6, and byte7.
RD(0) = DQ0 protection indicator bit. If protected, DQ0 = 0. If unprotected, DQ0 = 1.
Gray vs. White Box = Read vs. Write Operation.

Notes

71. All values are in hexadecimal.
72. Shaded cells indicate read cycles. All others are write cycles.
73. Address and data bits not specified in table, legend, or notes are don't cares (each hex digit implies 4 bits of data).
74. Writing incorrect address and data values or writing them in the improper sequence may place the device in an unknown state. The system must write the reset command to return the device to reading array data.
75. Entry commands are required to enter a specific mode to enable instructions only available within that mode.
76. No unlock or command cycles required when bank is reading array data.
77. Exit command must be issued to reset the device into read mode; device may otherwise be placed in an unknown state.
78. Entire two bus-cycle sequence must be entered for each portion of the password.
79. Full address range is required for reading password.
80. Password may be unlocked or read in any order. Unlocking requires the full password (all seven cycles).
81. ACC must be at V_{IH} when setting PPB or DYB.
82. "All PPB Erase" command pre-programs all PPBs before erasure to prevent over-erasure.

9 Data integrity

9.1 Erase endurance

Table 27 Erase endurance

Parameter	Minimum	Unit
Program/erase cycles per main flash array sectors	100K	PE cycle
Program/erase cycles per PPB array or non-volatile register array [83]	100K	PE cycle

9.2 Data retention

Table 28 Data retention

Parameter	Test conditions	Minimum time	Unit
Data retention time	10K program/erase cycles	20	Years
	100K program/erase cycles	2	Years

Contact Infineon Sales or FAE representative for additional information on the data integrity.

Note
83. Each write command to a non-volatile register causes a PE cycle on the entire non-volatile register array. OTP bits and registers internally reside in a separate array that is not PE cycled.

10 Status monitoring

There are three methods for monitoring EA status. Previous generations of the S29GL flash family used the methods called Data Polling and Ready/Busy# (RY/BY#) Signal. These methods are still supported by the S29GL-S family. One additional method is reading the Status Register.

10.1 Status Register

The status of program and erase operations is provided by a single 16-bit status register. The Status Register Read command is written followed by one read access of the Status Register information. The contents of the Status Register is aliased (overlaid) in all locations of the device address space. The overlay is in effect for one read access, specifically the next read access that follows the Status Register Read command. After the one Status Register access, the Status Register ASO is exited. The CE# or OE# signal must go HIGH following the Status Register read access for t_{CEPH}/t_{OEPH} time to return to the address space active at the time the Status Register Read command was issued.

The Status Register contains bits related to the results - success or failure - of the most recently completed Embedded Algorithms (EA):

- Erase Status (bit 5),
- Program Status (bit 4),
- Write Buffer Abort (bit 3),
- Sector Locked Status (bit 1),
- RFU (bit 0).

and, bits related to the current state of any in process EA:

- Device Busy (bit 7),
- Erase Suspended (bit 6),
- Program Suspended (bit 2),

The current state bits indicate whether an EA is in process, suspended, or completed.

The upper 8 bits (bits 15:8) are reserved. These have undefined HIGH or LOW value that can change from one status read to another. These bits should be treated as don’t care and ignored by any software reading status.

The Clear Status Register command will clear to ‘0’ the results related bits of the Status Register but will not affect the current state bits.

Initiation of an embedded operation will first clear the Status Register bits.

Table 29 Status Register

Bit #	15:8	7	6	5	4	3	2	1	0
Bit description	Reserved	Device Ready Bit	Erase Suspend Status Bit	Erase Status Bit	Program Status Bit	Write Buffer Abort Status Bit	Program Suspend Status Bit	Sector Lock Status Bit	Continuity Check
Bit name		DRB	ESSB	ESB	PSB	WBASB	PSSB	SLSB	CC
Reset status	X	1	0	0	0	0	0	0	0
Busy status	Invalid	0	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Ready status	X	1	0 = No Erase in Suspension 1 = Erase in Suspension	0 = Erase successful 1 = Erase fail	0 = Program successful 1 = Program fail	0 = Program not aborted 1 = Program aborted during Write to Buffer command	0 = No Program in suspension 1 = Program in suspension	0 = Sector not locked during operation 1 = Sector locked error	0 = Continuity Check Pattern not detected 1 = Continuity Check Pattern detected

Notes

84. Bits 15 thru 8, and 0 are reserved for future use and may display as '0' or '1'. These bits should be ignored (masked) when checking status.
85. Bit 7 is '1' when there is no Embedded Algorithm in progress in the device.
86. Bits 6 thru 1 are valid only if Bit 7 is '1'.
87. All bits are put in their reset status by cold reset or warm reset.
88. Bits 5, 4, 3, and 1 and 0 are cleared to '0' by the Clear Status Register command or Reset command.
89. Upon issuing the Erase Suspend command, the user must continue to read status until DRB becomes '1'.
90. ESSB is cleared to '0' by the Erase Resume command.
91. ESB reflects success or failure of the most recent erase operation.
92. PSB reflects success or failure of the most recent program operation.
93. During erase suspend, programming to the suspended sector, will cause program failure and set the Program status bit to '1'.
94. Upon issuing the Program Suspend command, the user must continue to read status until DRB becomes '1'.
95. PSSB is cleared to 0 by the Program Resume command.
96. SLSB indicates that a program or erase operation failed because the sector was locked.
97. SLSB reflects the status of the most recent program or erase operation.

10.2 Write Operation status

The device provides several bits to determine the status of a program or erase operation: DQ2, DQ3, DQ5, DQ6, and DQ7. **Table 30** and the following subsections describe the function of these bits. DQ7 and DQ6 each offer a method for determining whether a program or erase operation is complete or in progress. The device also provides a hardware-based output signal, RY/BY#, to determine whether an Embedded Program or Erase operation is in progress or is completed.

10.3 DQ7: Data# Polling

The Data# Polling bit, DQ7, indicates to the host system whether an Embedded Program or Erase algorithm is in progress or completed, or whether the device is in Erase Suspend. Data# Polling is valid after the rising edge of the final WE# pulse in the command sequence.

During the Embedded Program algorithm, the device outputs on DQ7 the complement of the datum programmed to DQ7. This DQ7 status also applies to programming during Erase Suspend. When programming in ×8 mode, the DQ7 polling value will be the DATA# of the last byte entered, regardless if the byte is at an even or odd address. When the Embedded Program algorithm is complete, the device outputs the datum programmed to DQ7. The system must provide the program address to read valid status information on DQ7. If a program address falls within a protected sector, Data# Polling on DQ7 is active for approximately t_{DP}, then the device returns to the read mode.

During the Embedded Erase algorithm, Data# Polling produces ‘0’ on DQ7. When the Embedded Erase algorithm is complete, or if the device enters the Erase Suspend mode, Data# Polling produces ‘1’ on DQ7. The system must provide an address within any of the sectors selected for erasure to read valid status information on DQ7.

After an erase command sequence is written, if all sectors selected for erasing are protected, Data# Polling on DQ7 is active for approximately t_{DP}, then the device returns to the read mode. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected. However, if the system reads DQ7 at an address within a protected sector, the status may not be valid.

Just prior to the completion of an Embedded Program or Erase operation, DQ7 may change asynchronously with DQ0–DQ6 while Output Enable (OE#) is asserted LOW. That is, the device may change from providing status information to valid data on DQ7. Depending on when the system samples the DQ7 output, it may read the status or valid data. Even if the device completed the program or erase operation and DQ7 has valid data, the data outputs on DQ0–DQ6 may be still invalid. Valid data on DQ0–DQ7 appears on successive read cycles.

Table 30 shows the outputs for Data# Polling on DQ7. **Figure 13** shows the Data# Polling algorithm. **Figure 36** shows the Data# Polling timing diagram.

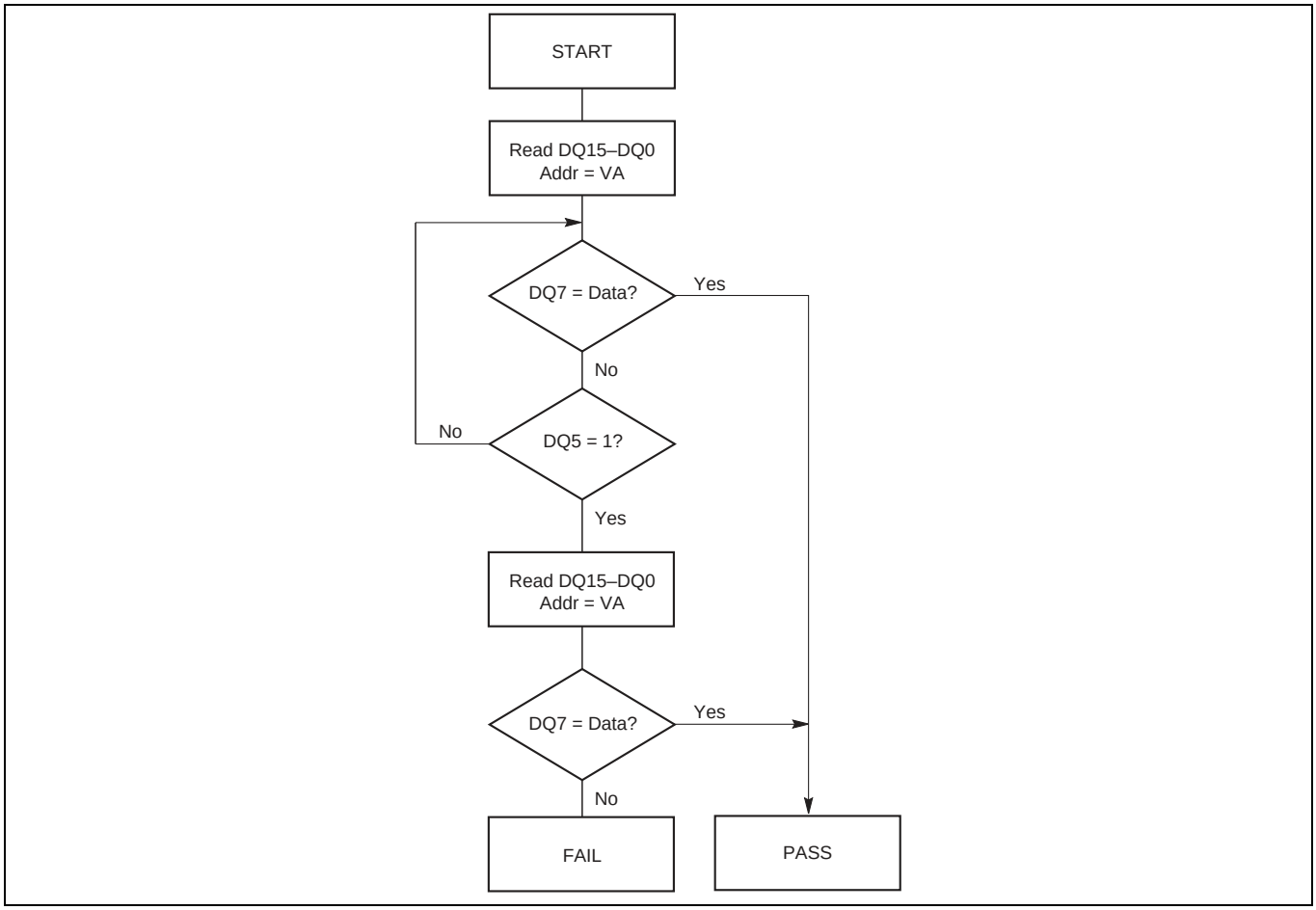


Figure 13 Data# polling algorithm

Notes

98. VA = Valid address for programming. During a sector erase operation, a valid address is any sector address within the sector being erased. During chip erase, a valid address is any non-protected sector address.
99. DQ7 should be rechecked even if DQ5 = 1 because DQ7 may change simultaneously with DQ5.

10.4 DQ6: Toggle Bit I

Toggle Bit I on DQ6 indicates whether an Embedded Program or Erase algorithm is in progress or complete, or whether the device entered the Erase Suspend mode. Toggle Bit I may be read at any address, and is valid after the rising edge of the final WE# pulse in the command sequence (prior to the program or erase operation), and during the sector erase time-out.

During an Embedded Program or Erase algorithm operation, successive read cycles to any address cause DQ6 to toggle. The system may use either OE# or CE# to control the read cycles. When the operation is complete, DQ6 stops toggling.

After an erase command sequence is written, if all sectors selected for erasing are protected, DQ6 toggles for approximately t_{DP}, then returns to reading array data. If not all selected sectors are protected, the Embedded Erase algorithm erases the unprotected sectors, and ignores the selected sectors that are protected.

The system can use DQ6 and DQ2 together to determine whether a sector is actively erasing or is erase-suspended. When the device is actively erasing (that is, the Embedded Erase algorithm is in progress), DQ6 toggles. When the device enters the Erase Suspend mode, DQ6 stops toggling. However, the system must also use DQ2 to determine which sectors are erasing or erase-suspended. Alternatively, the system can use DQ7 (see **"DQ7: Data# Polling"** on page 56).

If a program address falls within a protected sector, DQ6 toggles for approximately t_{DP} after the program command sequence is written, then returns to reading array data.

DQ6 also toggles during the erase-suspend-program mode, and stops toggling once the Embedded Program algorithm is complete.

Table 30 shows the outputs for Toggle Bit I on DQ6. **Figure 14** shows the toggle bit algorithm. **Figure 37** shows the toggle bit timing diagrams. **Figure 38** shows the differences between DQ2 and DQ6 in graphical form. See also **"DQ2: Toggle Bit II"** on page 60.

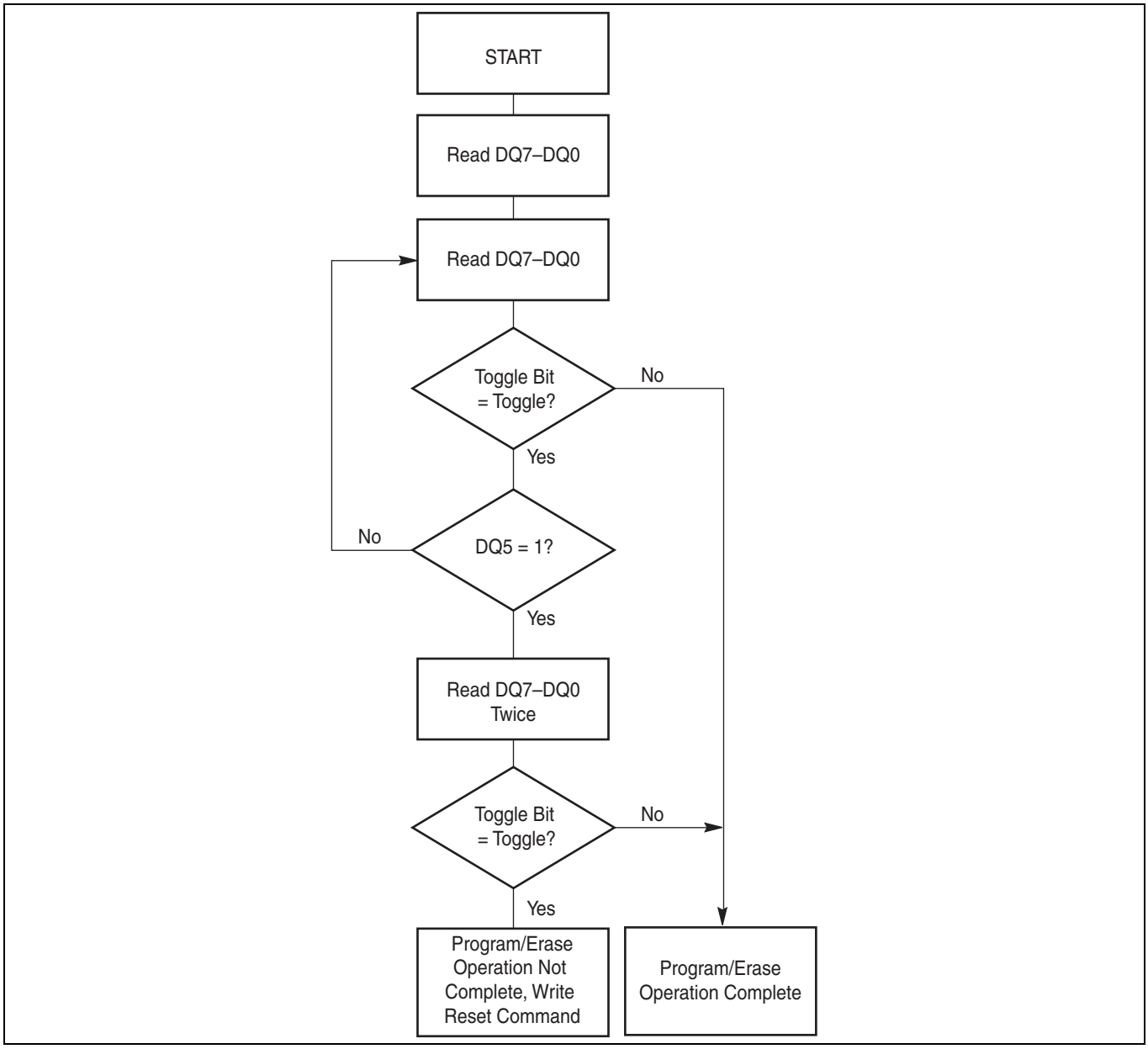


Figure 14 Toggle bit algorithm

Note

100. The system should recheck the toggle bit even if DQ5 = 1 because the toggle bit may stop toggling as DQ5 changes to '1'. See **"Reading Toggle Bits DQ6/DQ2"** on page 60 for more information.

10.5 DQ2: Toggle Bit II

The “Toggle Bit II” on DQ2, when used with DQ6, indicates whether a particular sector is actively erasing (that is, the Embedded Erase algorithm is in progress), or whether that sector is erase-suspended. (The Toggle Bit II does not apply to the PPB Erase command.) Toggle Bit II is valid after the rising edge of the final WE# pulse in the command sequence.

DQ2 toggles when the system reads at addresses within those sectors that were selected for erasure. (The system may use either OE# or CE# to control the read cycles.) But DQ2 cannot distinguish whether the sector is actively erasing or is erase-suspended. DQ6, by comparison, indicates whether the device is actively erasing, or is in Erase Suspend, but cannot distinguish which sectors are selected for erasure. Thus, both status bits are required for sector and mode information. Refer to **Table 30** to compare outputs for DQ2 and DQ6.

Figure 14 shows the toggle bit algorithm in flowchart form. **Figure 37** shows the toggle bit timing diagram. **Figure 38** shows the differences between DQ2 and DQ6 in graphical form.

10.6 Reading Toggle Bits DQ6/DQ2

Refer to **Figure 14** for the following discussion. Whenever the system initially begins reading toggle bit status, it must read DQ7–DQ0 at least twice in a row to determine whether a toggle bit is toggling. Typically, the system would note and store the value of the toggle bit after the first read. After the second read, the system would compare the new value of the toggle bit with the first. If the toggle bit is not toggling, the device completed the program or erase operation. The system can read array data on DQ7–DQ0 on the following read cycle.

However, if after the initial two read cycles, the system determines that the toggle bit is still toggling, the system also should note whether the value of DQ5 is high (see **“DQ5: Exceeded timing limits”** on page 60). If it is, the system should then determine again whether the toggle bit is toggling, since the toggle bit may have stopped toggling just as DQ5 went high. If the toggle bit is no longer toggling, the device successfully completed the program or erase operation. If it is still toggling, the device did not completed the operation successfully, and the system must write the reset command to return to reading array data. It is recommended that data read for polling only be used for polling purposes. Once toggling has stopped array data will be available on subsequent reads.

The remaining scenario is that the system initially determines that the toggle bit is toggling and DQ5 has not gone high. The system may continue to monitor the toggle bit and DQ5 through successive read cycles, determining the status as described in the previous paragraph. Alternatively, it may choose to perform other system tasks. In this case, the system must start at the beginning of the algorithm when it returns to determine the status of the operation (top of **Figure 14**).

10.7 DQ5: Exceeded timing limits

DQ5 indicates whether the program or erase time exceeded a specified internal pulse count limit. Under these conditions DQ5 produces ‘1’ indicating that the program or erase cycle was not successfully completed.

In all these cases, the system must write the reset command to return the device to the reading the array (or to erase-suspend-read if the device was previously in the erase-suspend-program mode). In this case, it is possible that the flash will continue to communicate busy for up to t_{TOR} after the reset command is sent.

10.8 DQ3: Sector erase timer

After writing a sector erase command sequence, the system may read DQ3 to determine whether or not erasure began. (The sector erase timer does not apply to the chip erase command or the PPB erase command.) If additional sectors are selected for erasure, the entire time-out also applies after each additional sector erase command. When the time-out period is complete, DQ3 switches from '0' to '1'. If the time between additional sector erase commands from the system can be assumed to be less than t_{SEA}, the system need not monitor DQ3. See also **"Sector Erase command sequence"** on page 43.

After the sector erase command is written, the system should read the status of DQ7 (Data# Polling) or DQ6 (Toggle Bit I) to ensure that the device accepted the command sequence, and then read DQ3. If DQ3 is '1', the Embedded Erase algorithm has begun; all further commands (except Erase Suspend) are ignored until the erase operation is complete. If DQ3 is '0', the device accepts additional sector erase commands. To ensure the command is accepted, the system software should check the status of DQ3 prior to and following each subsequent sector erase command. If DQ3 is high on the second status check, the last command might not have been accepted. **Table 30** shows the status of DQ3 relative to the other status bits.

10.9 DQ1: Write-to-Buffer abort

DQ1 indicates whether a Write-to-Buffer operation was aborted. Under these conditions DQ1 produces '1'. The system must issue the Write-to-Buffer-Abort-Reset command sequence to return the device to reading array data. See **"Write buffer"** on page 15 for more details.

Table 30 Write operation status

Status			DQ7[101]	DQ6	DQ5[102]	DQ3	DQ2[101]	DQ1	RY/BY#
Standard Mode	Embedded Program Algorithm		DQ7#	Toggle	0	N/A	No toggle	0	0
	Embedded Erase Algorithm		0	Toggle	0	1	Toggle	N/A	0
Program Suspend Mode	Program - Suspend Read	Program-Suspended Sector	Invalid (not allowed)						1
		Non-Program Suspended Sector	Data						1
Erase Suspend Mode	Erase-Suspend Read	Erase-Suspended Sector	1	No toggle	0	N/A	Toggle	N/A	1
		Non-Erase Suspended Sector	Data						1
	Erase-Suspend-Program (Embedded Program) [103]		DQ7#	Toggle	0	N/A	N/A	N/A	0
Write-to-Buffer	Busy [104]		DQ7#	Toggle	0	N/A	N/A	0	0
	Abort [105]		DQ7#	Toggle	0	N/A	N/A	1	0

Notes

101. DQ7 and DQ2 require a valid address when reading status information. Refer to the appropriate subsection for further details.
102. DQ5 switches to '1' when an Embedded Program, Embedded Erase, or Write-to-Buffer operation exceeded the maximum timing limits. Refer to **"DQ5: Exceeded timing limits"** on page 60 for more information.
103. DQ6 will not toggle when the sector being polled is a sector selected for sector erase or one of the selected sectors during multi-sector erase.
104. The Data# Polling algorithm should be used to monitor the last loaded write-buffer address location.
105. DQ1 switches to '1' when the device aborts the write-to-buffer operation.

10.10 RY/BY#: Ready/Busy#

The RY/BY# is a dedicated, open-drain output pin which indicates whether an Embedded Algorithm is in progress or complete. The RY/BY# status is valid after the rising edge of the final WE# pulse in the command sequence. Since RY/BY# is an open-drain output, several RY/BY# pins can be tied together in parallel with a pull-up resistor to V_{CC}.

If the output is low (Busy), the device is actively erasing or programming. (This includes programming in the Erase Suspend mode.) If the output is high (Ready), the device is in the read mode, the standby mode, or in the erase-suspend-read mode. **Table 30** shows the outputs for RY/BY#.

10.11 Error types and clearing procedures

There are three types of errors reported by the embedded operation status methods. Depending on the error type, the status reported and procedure for clearing the error status is different. Following is the clearing of error status:

- If an ASO was entered before the error the device remains entered in the ASO awaiting ASO read or a command write.
- If an erase was suspended before the error the device returns to the erase suspended state awaiting flash array read or a command write.
- Otherwise, the device will be in standby state awaiting flash array read or a command write.

10.11.1 Embedded Operation error

If an error occurs during an embedded operation (program, erase, evaluate erase status, or password unlock) the device (EAC) remains busy. The RY/BY# output remains LOW, data polling status continues to be overlaid on all address locations, and the status register shows ready with valid status bits. The device remains busy until the error status is detected by the host system status monitoring and the error status is cleared.

During embedded algorithm error status the Data Polling status will show the following:

- DQ7 is the inversion of the DQ7 bit in the last word loaded into the write buffer or last word of the password in the case of the password unlock command. DQ7 = 0 for an erase failure
- DQ6 continues to toggle
- DQ5 = 1; Failure of the embedded operation
- DQ4 is RFU and should be treated as don’t care (masked)
- DQ3 = 1 to indicate embedded sector erase in progress
- DQ2 continues to toggle, independent of the address used to read status
- DQ1 = 0; Write buffer abort error
- DQ0 is RFU and should be treated as don’t care (masked)

During embedded algorithm error status the Status Register will show the following:

- SR[7] = 1; Valid status displayed
- SR[6] = X; May or may not be erase suspended during the EA error
- SR[5] = 1 on erase; else = 0
- SR[4] = 1 on program or password unlock error; else = 0
- SR[3] = 0; Write buffer abort
- SR[2] = 0; Program suspended
- SR[1] = 0; Protected sector
- SR[0] = X; RFU, treat as don’t care (masked)

When the embedded algorithm error status is detected, it is necessary to clear the error status in order to return to normal operation, with RY/BY# HIGH, ready for a new read or command write. The error status can be cleared by writing:

- Reset command
- Status Register Clear command

Commands that are accepted during embedded algorithm error status are:

- Status Register Read
- Reset command
- Status Register Clear command

10.11.2 Protection Error

If an embedded algorithm attempts to change data within a protected area (program, or erase of a protected sector or OTP area) the device (EAC) goes busy for a period of 20 to 100 µs then returns to normal operation. During the busy period the RY/BY# output remains LOW, data polling status continues to be overlaid on all address locations, and the status register shows not ready with invalid status bits (SR[7] = 0).

During the protection error status busy period the data polling status will show the following:

- DQ7 is the inversion of the DQ7 bit in the last word loaded into the write buffer. DQ7 = 0 for an erase failure
- DQ6 continues to toggle, independent of the address used to read status
- DQ5 = 0; to indicate no failure of the embedded operation during the busy period
- DQ4 is RFU and should be treated as don't care (masked)
- DQ3 = 1 to indicate embedded sector erase in progress
- DQ2 continues to toggle, independent of the address used to read status
- DQ1 = 0; Write buffer abort error
- DQ0 is RFU and should be treated as don't care (masked)

Commands that are accepted during the protection error status busy period are:

- Status Register Read

When the busy period ends the device returns to normal operation, the data polling status is no longer overlaid, RY/BY# is HIGH, and the status register shows ready with valid status bits. The device is ready for flash array read or write of a new command.

After the protection error status busy period the Status Register will show the following:

- SR[7] = 1; Valid status displayed
- SR[6] = X; May or may not be erase suspended after the protection error busy period
- SR[5] = 1 on erase error, else = 0
- SR[4] = 1 on program error, else = 0
- SR[3] = 0; Program not aborted
- SR[2] = 0; No Program in suspension
- SR[1] = 1; Error due to attempting to change a protected location
- SR[0] = X; RFU, treat as don't care (masked)

Commands that are accepted after the protection error status busy period are:

- Any command

10.11.3 Write Buffer Abort

If an error occurs during a Write to Buffer command the device (EAC) remains busy. The RY/BY# output remains LOW, data polling status continues to be overlaid on all address locations, and the status register shows ready with valid status bits. The device remains busy until the error status is detected by the host system status monitoring and the error status is cleared.

During write to buffer abort (WBA) error status the Data Polling status will show the following:

- DQ7 is the inversion of the DQ7 bit in the last word loaded into the write buffer
- DQ6 continues to toggle, independent of the address used to read status
- DQ5 = 0; to indicate no failure of the programming operation. WBA is an error in the values input by the Write to Buffer command before the programming operation can begin
- DQ4 is RFU and should be treated as don't care (masked)
- DQ3 is don't care after program operation as no erase is in progress. If the Write Buffer Program operation was started after an erase operation had been suspended then DQ3 = 1. If there was no erase operation in progress then DQ3 is a don't care and should be masked.
- DQ2 does not toggle after program operation as no erase is in progress. If the Write Buffer Program operation was started after an erase operation had been suspended then DQ2 will toggle in the sector where the erase operation was suspended and not in any other sector. If there was no erase operation in progress then DQ2 is a don't care and should be masked.
- DQ1 = 1: Write buffer abort error
- DQ0 is RFU and should be treated as don't care (masked)

During embedded algorithm error status the Status Register will show the following:

- SR[7] = 1; Valid status displayed
- SR[6] = X; May or may not be erase suspended during the WBA error status
- SR[5] = 0; Erase successful
- SR[4] = 1; Programming related error
- SR[3] = 1; Write buffer abort
- SR[2] = 0; No Program in suspension
- SR[1] = 0; Sector not locked during operation
- SR[0] = X; RFU, treat as don't care (masked)

When the WBA error status is detected, it is necessary to clear the error status in order to return to normal operation, with RY/BY# HIGH, ready for a new read or command write. The error status can be cleared by writing:

- Write Buffer Abort Reset command
  - Clears the Status Register and returns to normal operation
- Status Register Clear command

Commands that are accepted during embedded algorithm error status are:

- Status Register Read
  - Reads the Status Register and returns to WBA busy state
- Write Buffer Abort Reset command
- Status Register Clear command

11 Command state transitions

Table 31 to Table 57 list the Command State Transitions for the S29GL064S in ×16 mode. States highlighted in yellow indicate the state is documented but not recommended.

Table 31 Read command state transition

Current State	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Unlock 1	Evaluate Erase status	CFI Entry	Continuity Entry	Continuity Test
	Address	RA	xh	x555h	x555h	x555h	(SA)555h	x55h	2AAA55h	1555AAh
	Data	RD	xF0h	x70h	x71h	xAAh	x35h	x98h	FF00h	00FFh
READ [106]	Read Protect = True	READ	READ	READ	READ	READUL1	–	CFI (READ)	–	–
	Read Protect = False						ESS		CONT	
CONT	–	CONT	READ	READ	–	–	–	–	–	READ

Table 32 Read Unlock command state transition

Current State	Command and condition	Read	Unlock 2	Word Program Entry	Write to Buffer Enter	Erase Enter	Unlock Bypass Enter	ID (Autoselect) Entry	SSR Entry	Lock Register Entry	Password ASO Entry	PPB ASO Entry	PPB Lock Entry	DYB ASO Entry
	Address	RA	x2AAh	x555h	(SA)xh	x555h	x555h	x555h	(SA)555h	x555h	x555h	x555h	x555h	x555h
	Data	RD	x55h	xA0h	x25h	x80h	x20h	x90h	x88h	x40h	x60h	xC0h	x50h	xE0h
READUL1	–	READUL1	READUL2	–	–	–	–	–	–	–	–	–	–	–
READUL2 [107]	Read Protect = True	READUL2	–	–	–	–	–	AS (READ)	–	–	PP	–	–	–
	Read Protect = False			PG1	WB	ER	UB		SSR (READ)	LR		PPB (READ)	PPBLB	DYB (READ)

Notes

106. Read Protect = True is defined when LR(5) = 0, LR(2) = 0, and Read Password given does not match the internal password.
107. Read Protect = True is defined when LR(5) = 0, LR(2) = 0, and Read Password given does not match the internal password.

Table 33 Erase State command transition

Current State	Command and condition	Read	Software Reset/ASO Exit	Status Register Read Enter	Unlock 1	Unlock 2	Chip Erase Start	Sector Erase Start	Erase Suspend Enhanced method [108]
	Address	RA	xh	x555h	x555h	x2AAh	x555h	(SA)xh	xh
	Data	RD	xF0h	x70h	xAAh	x55h	x10h	x30h	xB0h
ER	–	ER	–	READ	ERUL1	–	–	–	–
ERUL1	–	ERUL1	–	READ	–	ERUL2	–	–	–
ERUL2	–	ERUL2	–	READ	–	–	CER	SER	–
CER [109]	SR(7) = 0	CER	–	CER	–	–	–	–	–
	SR(7) = 1 and DQ5 = 1 [110]		READ						
SER [109, 111]	SR(7) = 0 and DQ3 = 0	SER	–	SER	–	–	–	SER	ESR
	SR(7) = 0 and DQ3 = 1				–	–		–	
	SR(7) = 1 and DQ5 = 1 [110]		READ						–
ESR [113]	–	ESR	–	ESR	–	–	–	–	–
ESS [109]	SR(7) = 0	ESS	–	ESS	–	–	–	–	–
	SR(7) = 1 and DQ5 = 1		READ						

Table 34 Erase Suspend State command transition

Current State	Command and condition	Read	Software Reset/ASO Exit	Status Register Read Enter	Status Register Clear	Unlock 1	Erase Resume Enhanced method [114]
	Address	RA	xh	x555h	x555h	x555h	xh
	Data	RD	xF0h	x70h	x71h	xAAh	x30h
ES	–	ES	ES	ES	ES	ESUL1	SER

Notes
108. Also known as Erase Suspend / Program Suspend Legacy method.
109. State will automatically move to READ state at the successful completion of the operation.
110. Hang State (time out) only. Sector Protection will have returned to READ state.
111. Issuing a suspend command during the DQ3 = 0 period will force DQR to '1' and queuing of additional sectors will not be allowed after the resume.
112. SR Clear will only clear the SR, not the DQ bits.
113. State will automatically move to ES state by t_{ESL}.
114. Also known as Erase Resume / Program Resume Legacy method.

Table 35 Erase Suspend Unlock State command transition

Current state	Command and condition	Read	Unlock 2	Word Program Entry	Write to Buffer Enter
	Address	RA	x2AAh	x555h	(SA)xh
	Data	RD	x55h	xA0h	x25h
ESUL1	–	ESUL1	ESUL2	–	–
ESUL2	–	ESUL2	–	ESPG1	ES_WB

Table 36 Erase Suspend - Program command state transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Program Buffer to Flash (confirm)	Erase Suspend Enhanced method [115]	Program Suspend Enhanced method	Write Data
	Address	RA	xh	x555h	(SA)xh	xh	xh	xh
	Data	RD	xF0h	x70h	x29h	xB0h	x51h	xh
ES_WB [116]	WC > 127 or SAe ≠ SAc	ES_WB	–	–	–	–	–	PGE (ES)
	WC ≤ 127 and SAe = SAc							ES_WB_D
ES_WB_D [116]	WC = –1 and SAe ≠ SAc	ES_WB_D	–	–	–	–	–	PGE (ES)
	WC = -1 and SAe = SAc				ESPG			
	WC ≥ 0 and Write Buffer ≠ Write Buffer				–			
	WC ≥ 0 and Write Buffer = Write Buffer							ES_WB_D [117]
ESPG1	–	ESPG1	–	–	–	–	–	ESPG
ESPG [118]	SR(7) = 0	ESPG	–	ESPG	–	ESPSR	ESPSR	–
	SR(7) = 1 [119]		ES			–	–	
ESPSR [120]	–	ESPSR	–	ESPSR	–	–	–	–

Notes

115. Also known as Erase Suspend / Program Suspend Legacy method. Not recommend due to the potential of nested loop errors. Instead Program Suspend Enhanced method is recommended.
116. SAe = SAc: SAe is the SA entered with programming command. SAc is the current command.
117. WC counter will automatically decrement by '1'.
118. When Program operation is completed with no errors then it will return to Erase Suspend.
119. Hang State (time out) only. Sector Protection will have returned to ES state.
120. State will automatically move to ESPS state by t_{PSL}.

Table 37 Erase Suspend - Program Suspend command state transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Erase Resume Enhanced method [121]	Program Resume Enhanced method
	Address	RA	xh	x555h	xh	xh
	Data	RD	xF0h	x70h	x30h	x50h
ESPS	–	ESPS	ESPS	ESPS	ESPG	ESPG

Table 38 Program State command transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Program Buffer to Flash (confirm)	Erase Suspend Enhanced method [122]	Program Suspend Enhanced method	Write Data
	Address	RA	xh	x555h	(SA)xh	xh	xh	xh
	Data	RD	xF0h	x70h	x29h	xB0h	x51h	xh
WB [123]	WC > 127 or SAe ≠ SAc	WB	–	–	–	–	–	PGE (READ)
	WC ≤ 127 and SAe = SAc							WB_D
WB_D [123]	WC = -1 and SAe ≠ SAc	WB_D	–	–	–	–	–	PGE (READ)
	WC = -1 and SAe = SAc				PG			
	WC ≥ 0 and Write Buffer ≠ Write Buffer				–			
	WC ≥ 0 and Write Buffer = Write Buffer							WB_D [124]
PG1	–	PG1	–	–	–	–	–	PG
PG [125]	SR(7) = 0	PG	–	PG	–	PSR	PSR	–
	SR(7) = 1 [126]		READ			–	–	
PSR [127]	–	PSR	–	PSR	–	–	–	–

Notes

121. Also known as Erase Resume / Program Resume Legacy method. Not recommend due to the potential of nested loop errors. Instead Program Suspend Enhanced method is recommended.
122. Also known as Erase Suspend / Program Suspend Legacy method. Not recommend due to the potential of nested loop errors. Instead Program Suspend Enhanced Method is recommended.
123. SAe = SAc: SAe is the SA entered with programming command. SAc is the current command.
124. WC counter will automatically decrement by '1'.
125. State will automatically move to READ state at the completion of the operation.
126. Hang State (time out) only. Sector Protection will have returned to READ state.
127. State will automatically move to PS state by t_{PSL}.

Table 39 Program Suspend State command transition

Current state	Command and condition	Read	Status Register Read Enter	Erase Resume Enhanced method [128]	Program Resume Enhanced method
	Address	RA	x555h	xh	xh
	Data	RD	x70h	x30h	x50h
PS	–	PS	PS	PG	PG

Table 40 Program Abort command state transition

Current state	Command and condition	Read	Status Register Read Enter	Unlock 1	Unlock 2	Write-To-Buffer Abort Reset
	Address	RA	x555h	x555h	x2AAh	x555h
	Data	RD	x70h	xAAh	x55h	xF0h
PGE	–	PGE (-)	PGE	PGEUL1	–	–
PGEUL1	–	PGEUL1	–	–	PGEUL2	–
PGEUL2	–	PGEUL2	–	–	–	(return)

Table 41 Lock Register state command transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Command Set Exit Entry	Command Set Exit	PPB Lock Bit Set Entry	Write Data
	Address	RA	xh	x555h	x555h	xh	xh	xh	xh
	Data	RD	xF0h	x70h	x71h	x90h	x00h	xA0h	xh
LR	–	LR	READ	LR	LR	LREXT	–	LRPG1	–
LRPG1	–	LRPG1	–	–	–	–	–	–	LRPG
LRPG [129]	SR(7) = 0	LRPG	–	LRPG	–	–	–	–	–
	SR(7) = 1 [130]		LR		–				
LREXT	–	LREXT	READ	–	–	–	READ	–	–

Notes

128. Also known as Erase Resume / Program Resume Legacy method. Not recommend due to the potential of nested loop errors. Instead Program Suspend Enhanced method is recommended.
129. State will automatically move to LR state at the completion of the operation.
130. Hang state (time out) only.

Table 42 CFI state command transition

Current state	Command and condition	Read	Software Reset / ASO Exit	CFI Exit
	Address	RA	xh	xh
	Data	RD	xF0h	xFFh
CFI	–	CFI	(return)	(return)

Table 43 Autoselect State command transition

Current state	Command and condition	Read	Software Reset / ASO Exit
	Address	RA	xh
	Data	RD	xF0h
AS	–	AS	(return)

Table 44 Secure Silicon Sector State command transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Unlock 1
	Address	RA	xh	x555h	x555h
	Data	RD	xF0h	x70h	xAAh
SSR	–	SSR	(return)	SSR	SSRUL1

Table 45 Secure Silicon Sector Unlock State command transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Unlock 2	Word Program Entry	Write to Buffer Enter	SSR Exit Entry	SSR Exit
	Address	RA	xh	x2AAh	x555h	(SA)xh	x555h	xh
	Data	RD	xF0h	x55h	xA0h	x25h	x90h	x00h
SSRUL1	–	SSRUL1	–	SSRUL2	–	–	–	–
SSRUL2 [131]	SR(2) = 0	SSRUL2	–	–	SSRPG1	SSR_WB	SSREXT	–
	SR(2) = 1				–	–		
SSREXT	–	SSREXT	(return)	–	–	–	–	(return)

Note
131.SSR's are protected from programming once SSR protect bit is set.

Table 46 Secure Silicon Sector Program State command transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Program Buffer to Flash (confirm)	Write Data
	Address	RA	xh	x555h	(SA)xh	xh
	Data	RD	xF0h	x70h	x29h	xh
SSR_WB [132]	WC > 127 or SAe ≠ SAc	SSR_WB	–	–	–	PGE (SSR)
	WC ≤ 127 and SAe = SAc					SSR_WB_D
SSR_WB_D [132]	WC = -1 and SAe ≠ SAc	SSR_WB_D	–	–	–	–
	WC = -1 and SAe = SAc				SSRPG	
	WC ≥ 0 and Write Buffer ≠ Write Buffer				–	
	WC ≥ 0 and Write Buffer = Write Buffer					SSR_WB_D [133]
SSRPG [134]	SR(7) = 0	SSRPG	–	SSRPG	–	–
	SR(7) = 1 [135]		SSR			
SSRPG1	–	SSRPG1	–	–	–	–

Notes
132.SAe = SAc: SAe is the SA entered with programming command. SAc is the current command.
133.WC counter will automatically decrement by '1'.
134.When Program operation is completed with no errors then it will return to SSR State.
135.Hang State (time out) only. Sector Protection will have returned to SSR state.

Table 47 Password Protection command state transition

Current state	Command and condition	Read	Software Reset/ASO Exit	Status Register Read Enter	Status Register Clear	Password ASO Unlock Enter	Password ASO Unlock Start	Command Set Exit Entry	Command Set Exit	Program Entry	Password Word Count	Write Data
	Address	RA	xh	x555h	x555h	0h	0h	xh	xh	xh	0h	xh
	Data	RD	xF0h	x70h	x71h	x25h	x29h	x90h	x00h	xA0h	x03h	xh
PP [136]	Read Protect = True	PP	READ	PP	PP	PPWB25	–	PPEXT	–	–	–	PP
	Read Protect = False									PPPG1		
PPWB25	A10:A0 = 0	PPWB25	–	–	–	–	–	–	–	–	PPD	PGE (PP)
	A10:A0 ≠ 0										PGE (PP)	
PPD [137, 138]	Last Password Loaded and PWD's match	PPD	–	–	–	–	PPV	–	–	–	–	PGE (PP)
	Last Password Loaded and PWD's don't match						PPH [139]					
	Not Last Password Loaded and Addresses match						–					PPD
	Addresses don't match											PGE (PP)
PPV [140]	SR(7) = 0	PPV	–	PPV	–	–	–	–	–	–	–	–
PPH	SR(7) = 1 [141]	PPH	PP	PPH	–	–	–	–	–	–	–	–
PPPG1	–	PPPG1	–	–	–	–	–	–	–	–	–	PPPG
PPPG [142]	SR(7) = 0 [143]	PPPG	–	PPPG	–	–	–	–	–	–	–	–
	SR(7) = 1 [141]		PP		–							
PPEXT	–	PPEXT	READ	PP	–	–	–	–	READ	–	–	–

Notes

136. Read Protect = True is defined when LR(5) = 0, LR(2) = 0, and Read Password given does not match the internal password.
137. In ×16 mode, 4 write cycles are required to load password. In ×8 mode, 8 write cycles are required to load password.
138. On the 1st cycle SA is compared to the SA given during PPWB25. During all other password load cycles SA and WLB are compared to the prior cycle.
139. If the password data does not match the hidden internal one, device goes into hang state (SR = x90h).
140. Well before the completion of t_{PPB} the device will move to the PP State.
141. SR(7) will initially be '0'. SR(7) will transition to '1' at the completion of t_{PPB}.
142. When program operation is completed with no errors then the device will return to PP State.
143. If LR(2) = 0 RDY busy will go LOW for a short time and then the device goes to the PP state and reports it as a security violation.

Table 48 Non-volatile Protection command state transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Status Register Clear	Command Set Exit Entry	Command Set Exit	Program Entry	PPB Set Start	All PPB Erase Enter	All PPB Erase Start
	Address	RA	xh	x555h	x555h	xh	xh	xh	(SA)xh	Xh	0h
	Data	RD	xF0h	x70h	x71h	x90h	x00h	xA0h	x00h	x80h	x30h
PPB	LR(3) = 0	PPB	(return)	PPB	PPB	PPBEXT	–	PPBPG1	–	–	–
	LR(3) = 1									PPBBER	
PPBPG1	–	PPBPG1	PPB	–	–	–	PPBPG	–	PPBPG	–	–
PPBPG [144]	SR(7) = 0	PPBPG	–	PPBPG	–	–	–	–	–	–	–
	SR(7) = 1 [145]		PPB		–						
PPBBER	–	PPBBER	PPB	PPB	–	–	–	–	–	–	PPBSER
PPBSER [144]	SR(7) = 0	PPBSER	–	PPBSER	–	–	–	–	–	–	–
	SR(7) = 1 [145]		PPB		–						
PPBEXT	-	PPBEXT	–	–	–	–	(return)	–	(return)	–	–

Table 49 PPB Lock Bit command state transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Command Set Exit Entry	Command Set Exit [146]	Program Entry	PPB Set
	Address	RA	xh	x555h	xh	xh	xh	xh
	Data	RD	xF0h	x70h	x90h	x00h	xA0h	x00h
PPBLB	–	PPBLB	READ	PPBLB	PPBLBEXT	–	PPBLBSET	–
PPBLBSET	–	PPBLBSET	–	–	–	PPBLB	–	PPBLB
PPBLBEXT	–	PPBLBEXT	–	–	–	READ	–	READ

Table 50 Volatile Sector Protection command state transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Command Set Exit Entry	Command Set Exit	Program Entry	DYB Set Start	DYB Clear Start
	Address	RA	xh	x555h	xh	xh	xh	(SA)xh	(SA)xh
	Data	RD	xF0h	x70h	x90h	x00h	xA0h	x00h	x01h
DYB	–	DYB	(return)	DYB	DYBEXT	–	DYBSET	–	–
DYBSET	–	DYBSET	–	–	–	DYB (–)	–	DYB (-)	DYB (–)
DYBEXT	–	DYBEXT	–	–	–	(return)	–	(return)	–

Notes

144.State will automatically move to PPB state at the completion of the operation.
145.Hang State (time out) only. Locked PPB's will have returned to PPB state.
146.Matches only valid data for the set command.

Command state transitions

Table 51 Unlock Bypass command transition

Current state	Command and condition	Read	Unlock Bypass Word Program Entry	Unlock Bypass Write to Buffer Entry	Unlock Bypass Erase Entry	Unlock Bypass Reset Entry	Unlock Bypass Reset
	Address	RA	xh	PA	xh	xh	xh
	Data	RD	xA0h	x25h	x80h	x90h	x0h
UB	–	UB	UBPG1	UBWB	UBER	UBRST	–
UBRST	–	UBRST	–	–	–	–	READ

Table 52 Unlock Bypass Erase State command transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Chip Erase Start	Sector Erase Start	Erase Suspend Enhanced method [147]
	Address	RA	xh	x555h	xh	(SA)xh	xh
	Data	RD	xF0h	x70h	x10h	x30h	xB0h
UBER	–	UBER	–	UB	UBCER	UBSER	–
UBCER [148]	SR(7) = 0	UBCER	–	UBCER	–	–	–
	SR(7) = 1 [149]		UB				
UBSER [148]	SR(7) = 0 and DQ3 = 0	UBSER	–	UBSER	–	UBSER	UBESR
	SR(7) = 0 and DQ3 =1					–	
	SR(7) = 1 and DQ5 = 1 [149]		UB				–
UBESR [150]	–	UBESR	–	UBESR	–	–	–

Table 53 Unlock Bypass Erase Suspend State command transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Erase Resume Enhanced method [151]	Word Program Entry	Write to Buffer Enter
	Address	RA	xh	x555h	xh	xh	(SA)xh
	Data	RD	xF0h	x70h	x30h	xA0h	x25h
UBES	–	UBES	UBES	UBES	UBSER	UBESPG1	UBES_WB

Notes

147.Also known as Erase Suspend / Program Suspend Legacy method.
148.State will automatically move to UB state at the completion of the operation.
149.Hang State (time out) only. Sector Protection will have returned to UB state.
150.State will automatically move to UBES state by t_{ESL}.
151.Also known as Erase Resume / Program Resume Legacy method.

Table 54 Unlock Bypass Erase Suspend - Program command state transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Program Buffer to Flash (confirm)	Erase Suspend Enhanced method [152]	Program Suspend Enhanced method	Write Data
	Address	RA	xh	x555h	(SA)xh	xh	xh	xh
	Data	RD	xF0h	x70h	x29h	xB0h	x51h	xh
UBES_WB [153]	WC > 127 or SAe ≠ SAc	UBES_WB	–	–	–	–	–	PGE (UBES)
	WC ≤ 127 and SAe = SAc							UBES_WB_D
UBES_WB_D [153]	WC = -1 and SAe ≠ SAc	UBES_WB_D	–	–	–	–	–	PGE (UBES)
	WC = -1 and SAe = SAc				UBESPG			
	WC ≥ 0 and Write Buffer ≠ Write Buffer				–			
	WC ≥ 0 and Write Buffer = Write Buffer							UBES_WB_D [154]
UBESPG1	–	UBESPG1	–	–	–	–	–	UBESPG
UBESPG [155]	SR(7) = 0	UBESPG	–	UBESPG	–	UBESPSR	UBESPSR	–
	SR(7) = 1 [156]		UBES			–	–	
UBESPSR [157]	–	UBESPSR	–	UBESPSR	–	–	–	–

Table 55 Unlock Bypass Erase Suspend - Program Suspend command state transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Erase Resume Enhanced method [158]	Program Resume Enhanced method
	Address	RA	xh	x555h	xh	xh
	Data	RD	xF0h	x70h	x30h	x50h
UBESPS	–	UBESPS	UBESPS	UBESPS	UBESPG	UBESPG

Notes

152. Also known as Erase Suspend / Program Suspend Legacy method. Not recommend due to the potential of nested loop errors. Instead Program Suspend Enhanced method is recommended.
153. SAe = SAc: SAe is the SA entered with programming command. SAc is the current command.
154. WC counter will automatically decrement by '1'.
155. When Program operation is completed with no errors then it will return to Unlock Bypass Erase Suspend.
156. Hang State (time out) only. Sector Protection will have returned to UBES state.
157. State will automatically move to UBESPS state by t_{PSL}.
158. Also known as Erase Resume / Program Resume Legacy method. Not recommend due to the potential of nested loop errors. Instead Program Suspend Enhanced method is recommended.

Table 56 Unlock Bypass Program State command transition

Current state	Command and condition	Read	Software Reset / ASO Exit	Status Register Read Enter	Program Buffer to Flash (confirm)	Erase Suspend Enhanced method [159]	Program Suspend Enhanced method	Write Data
	Address	RA	xh	x555h	(SA)xh	xh	xh	xh
	Data	RD	xF0h	x70h	x29h	xB0h	x51h	xh
UBWB [160]	WC > 127 or SAe ≠ SAc	UBWB	–	–	–	–	–	PGE (UB)
	WC ≤ 127 and SAe = SAc							UBWB_D
UBWB_D [160]	WC = -1 and SAe ≠ SAc	UBWB_D	–	–	–	–	–	PGE (UB)
	WC = -1 and SAe = SAc				UBPG			
	WC ≥ 0 and Write Buffer ≠ Write Buffer				–			
	WC ≥ 0 and Write Buffer = Write Buffer							UBWB_D [161]
UBPG1	–	UBPG1	–	–	–	–	–	UBPG
UBPG [162]	SR(7) = 0	UBPG	-	UBPG	-	UBPSR	UBPSR	–
	SR(7) = 1 [163]		UB		–	–	–	
UBPSR [164]	–	UBPSR	–	UBPSR	–	–	–	–

Table 57 Unlock Bypass Program Suspend State command transition

Current state	Command and condition	Read	Status Register Read Enter	Erase Resume Enhanced method [165]	Program Resume Enhanced method
	Address	RA	x555h	xh	xh
	Data	RD	x70h	x30h	x50h
UBPS	-	UBPS	UBPS	UBPG	UBPG

Notes

159. Also known as Erase Suspend / Program Suspend Legacy method. Not recommend due to the potential of nested loop errors. Instead Program Suspend Enhanced method is recommended.
160. SAe = SAc: SAe is the SA entered with programming command. SAc is the current command.
161. WC counter will automatically decrement by '1'.
162. State will automatically move to UB state at the completion of the operation.
163. Hang State (time out) only. Sector Protection will have returned to UB state.
164. State will automatically move to UBPS state by t_{PSL}.
165. Also known as Erase Resume / Program Resume Legacy method. Not recommend due to the potential of nested loop errors. Instead Program Suspend Enhanced method is recommended.

Table 58 Next state table lookup

Current state	Command transition	Definition
AS	Table 43	ID (Autoselect)
CER	Table 33	Chip Erase Start
CFI	Table 42	CFI Entry
CONT	Table 31	Continuity Enter
DYB	Table 50	DYB ASO
DYBEXT	Table 50	DYB ASO - Command Exit
DYBSET	Table 50	DYB ASO - Set
ER	Table 33	Erase Enter
ERUL1	Table 33	Erase - Unlock Cycle 1
ERUL2	Table 33	Erase - Unlock Cycle 2
ES	Table 34	Erase Suspended
ESPG	Table 36	Erase Suspended - Program
ESPG1	Table 36	Erase Suspended - Word Program
ESPS	Table 37	Erase Suspended - Program Suspended
ESPSR	Table 36	Erase Suspended - Program Suspend
ESS	Table 33	Evaluate Erase Status
ESR	Table 33	Erase Suspend Request
ESUL1	Table 35	Erase Suspended - Unlock Cycle 1
ESUL2	Table 35	Erase Suspended - Unlock Cycle 2
ES_WB	Table 36	Erase Suspended - Write to Buffer
ES_WB_D	Table 36	Erase Suspended - Write to Buffer Data
LR	Table 41	Lock Register
LREXT	Table 41	Lock Register - Command Exit
LRPG	Table 41	Lock Register - Program
LRPG1	Table 41	Lock Register - Program Start
PG	Table 38	Program
PG1	Table 38	Word Program
PGE	Table 40	Programming Error
PGEUL1	Table 40	Programming Error - Unlock 1
PGUUL2	Table 40	Programming Error - Unlock 2
PP	Table 47	Password ASO
PPB	Table 48	PPB
PPBBER	Table 48	PPB - Erase
PPBEXT	Table 48	PPB - Command Exit
PPBLB	Table 49	PPB Lock Bit
PPBLBEXT	Table 49	PPB Lock Bit - Command Exit
PPBLBSET	Table 49	PPB Lock Bit - Set
PPBPG	Table 48	PPB - Program
PPBPG1	Table 48	PPB - Program Request
PPBSER	Table 48	PPB - Erase Start
PPD	Table 47	Password ASO - Data

Table 58 Next state table lookup (Continued)

Current state	Command transition	Definition
PPEXT	Table 47	Password ASO - Command Exit
PPH	Table 47	Password ASO - Hang
PPPG	Table 47	Password ASO - Program
PPPG1	Table 47	Password ASO - Program Request
PPV	Table 47	Password ASO - Valid
PPWB25	Table 47	Password ASO - Unlock
PS	Table 39	Program Suspended
PSR	Table 38	Program Suspend Request
READ	Table 31	Read Array
READUL1	Table 32	Read - Unlock Cycle 1
READUL2	Table 32	Read - Unlock Cycle 2
SER	Table 33	Sector Erase Start
SSR	Table 44	Secure Silicon
SSREXT	Table 45	Secure Silicon - Command Exit
SSRPG	Table 46	Secure Silicon - Program
SSRPG1	Table 46	Secure Silicon - Word Program
SSRUL1	Table 45	Secure Silicon - Unlock Cycle 1
SSRUL2	Table 45	Secure Silicon - Unlock Cycle 2
SSR_WB	Table 46	Secure Silicon - Write to Buffer
SSR_WB_D	Table 46	Secure Silicon - Write to Buffer - Write Data
UB	Table 51	Unlock Bypass - Enter
UBCER	Table 52	Unlock Bypass - Chip Erase Start
UBER	Table 52	Unlock Bypass - Erase Enter
UBES	Table 53	Unlock Bypass Erase Suspended
UBESR	Table 52	Unlock Bypass Erase Suspend Request
UBESPG	Table 54	Unlock Bypass Erase Suspended - Program
UBESPG1	Table 54	Unlock Bypass Erase Suspended - Word Program
UBESPS	Table 55	Unlock Bypass Erase Suspended - Program Suspended
UBESPSR	Table 54	Unlock Bypass Erase Suspended - Program Suspend
UBES_WB	Table 54	Unlock Bypass Erase Suspended - Write to Buffer
UBES_WB_D	Table 54	Unlock Bypass Erase Suspended - Write to Buffer Data
UBPS	Table 57	Unlock Bypass Program Suspended
UBPSR	Table 56	Unlock Bypass Program Suspended Request
UBRST	Table 51	Unlock Bypass- Reset
UBSER	Table 52	Unlock Bypass - Sector Erase Start
UBWB	Table 56	Unlock Bypass - Write to Buffer
UBWB_D	Table 56	Unlock Bypass - Write to Buffer Write Data
UBPG1	Table 56	Unlock Bypass - Word Program
UBPG	Table 56	Unlock Bypass - Program
WB	Table 38	Write to Buffer
WB_D	Table 38	Write to Buffer Write Data

12 Electrical specifications

12.1 Absolute maximum ratings

Table 59 Absolute maximum ratings

Parameter		Rating
Storage temperature, plastic packages		–65°C to +150°C
Ambient temperature with power applied		–65°C to +125°C
Voltage with respect to ground	V_{CC} [166]	–0.5 V to +4.0 V
	V_{IO} [166]	–0.5 V to +4.0 V
	A9 and ACC [167]	–0.5 V to +12.5 V
	All other pins [166]	–0.5 V to V_{IO} + 0.5 V
Output short circuit current [168]		200 mA

12.2 Latch-up characteristics

This product complies with JEDEC standard JESD78C latch-up testing requirements.

12.3 Thermal resistance

Table 60 Thermal resistance

Parameter	Description	Test condition	TS056	TS048	LAE064	LAA064	VBK048	Unit
Theta JA	Thermal resistance (Junction to ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance in accordance with EIA/JESD51. with Still Air (0 m/s).	52.5	45.8	38.0	28.5	33.7	°C/W
Theta JB	Thermal resistance (Junction to board)		50	25.2	19.8	20.9	19.7	°C/W
Theta JC	Thermal resistance (Junction to case)		20	8.5	13.2	12.8	14.2	°C/W

Notes

166. Minimum DC voltage on input or I/Os is –0.5 V. During voltage transitions, inputs or I/Os may overshoot V_{SS} to –2.0 V for periods of up to 20 ns. See **Figure 17**. Maximum DC voltage on input or I/Os is V_{CC} + 0.5 V. During voltage transitions, input or I/O pins may overshoot to V_{CC} + 2.0 V for periods up to 20 ns. See **Figure 18**.
167. Minimum DC input voltage on pins A9 and ACC is –0.5 V. During voltage transitions, A9 and ACC may overshoot V_{SS} to –2.0V for periods of up to 20 ns. See **Figure 17**. Maximum DC input voltage on pin A9 and ACC is +12.5 V which may overshoot to +14.0 V for periods up to 20 ns.
168. No more than one output may be shorted to ground at a time. Duration of the short circuit should not be greater than one second.
169. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational sections of this data sheet is not implied. Exposure of the device to absolute maximum rating conditions for extended periods may affect device reliability.

12.4 Operating ranges

Operating ranges define those limits between which the functionality of the device is guaranteed.

12.4.1 Temperature ranges

Table 61 Temperature ranges

Description	Parameter	Device	Spec		Unit
			Min	Max	
Ambient temperature	T_A	Industrial (I)	–40	+85	°C
		Industrial Plus (V)	–40	+105	
		Extended (N)	–40	+125	

12.4.2 Power supply voltages

V_{CC}	2.7 V to 3.6 V
V_{IO}	1.65 V to V_{CC} + 200 mV

12.4.3 Power-up and power-down

During power-up or power-down V_{CC} must always be greater than or equal to V_{IO} ($V_{CC} \geq V_{IO}$).

The device ignores all inputs until a time delay of t_{VCS} has elapsed after the moment that V_{CC} and V_{IO} both rise above, and stay above, the minimum V_{CC} and V_{IO} thresholds. During t_{VCS} the device is performing power on reset operations.

During power-down or voltage drops below V_{CC} Lockout maximum (V_{LKO}), the V_{CC} and V_{IO} voltages must drop below V_{CC} Reset (V_{RST}) minimum for a period of t_{PD} for the part to initialize correctly when V_{CC} and V_{IO} again rise to their operating ranges. See **Figure 16**. If during a voltage drop the V_{CC} stays above V_{LKO} maximum the part will stay initialized and will work correctly when V_{CC} is again above V_{CC} minimum. If the part locks up from improper initialization, a hardware reset can be used to initialize the part correctly.

Normal precautions must be taken for supply decoupling to stabilize the V_{CC} and V_{IO} power supplies. Each device in a system should have the V_{CC} and V_{IO} power supplies decoupled by a suitable capacitor close to the package connections (this capacitor is generally on the order of 0.1 µF). At no time should V_{IO} be greater then 200 mV above V_{CC} ($V_{CC} \geq V_{IO}$ – 200 mV).

Table 62 Power-up / power-down voltage and timing

Parameter	Parameter	Min	Max	Unit
V_{CC}	V_{CC} Power Supply	2.7	3.6	V
V_{LKO}	V_{CC} level below which re-initialization is required [170]	–	2.5	V
V_{RST}	V_{CC} and V_{IO} Low voltage needed to ensure initialization will occur [170]	1.0	–	V
t_{PD}	Duration of $V_{CC} \leq V_{RST}$(min) [170]	15	–	µs

Note
170.Not 100% tested.

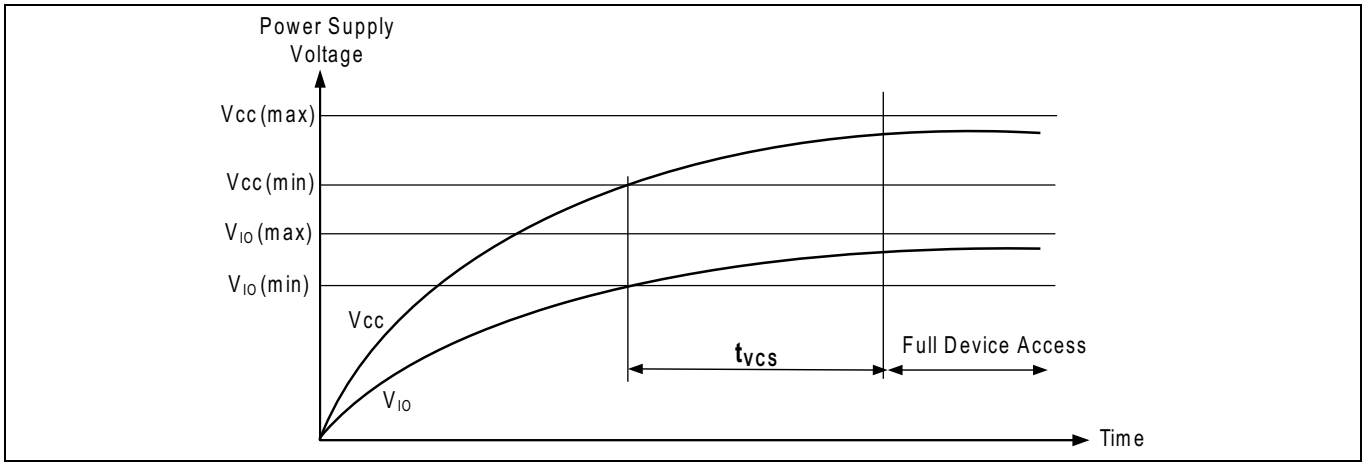


Figure 15 Power-up

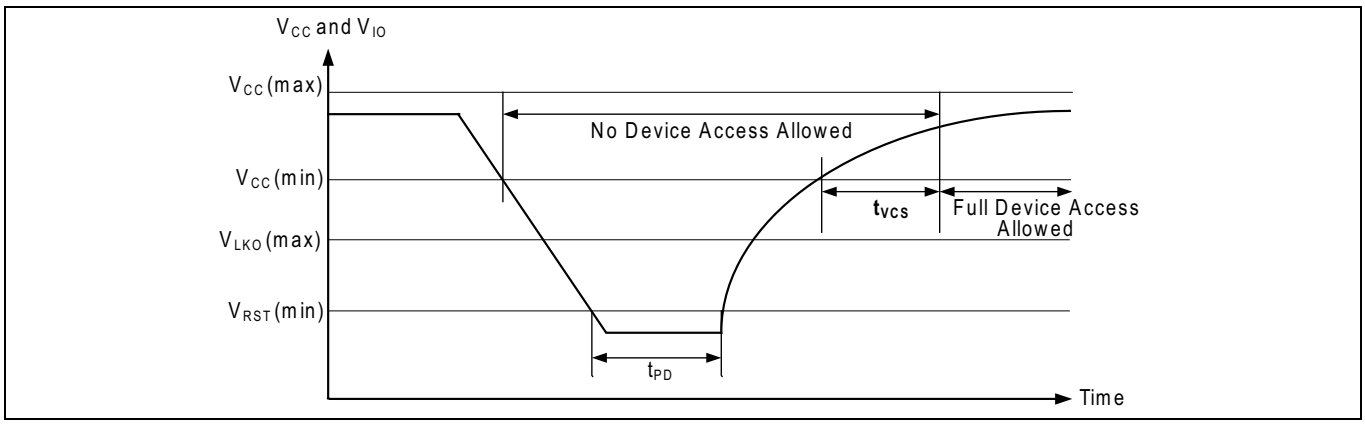


Figure 16 Power-down and voltage drop

12.4.4 Input signal overshoot

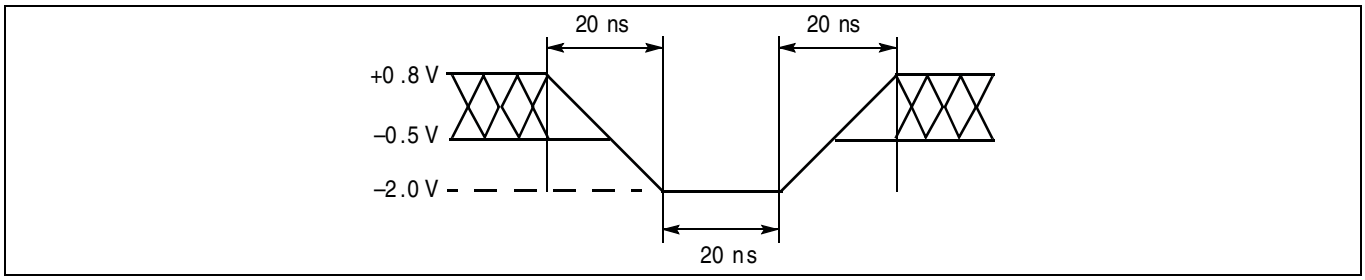


Figure 17 Maximum negative overshoot waveform

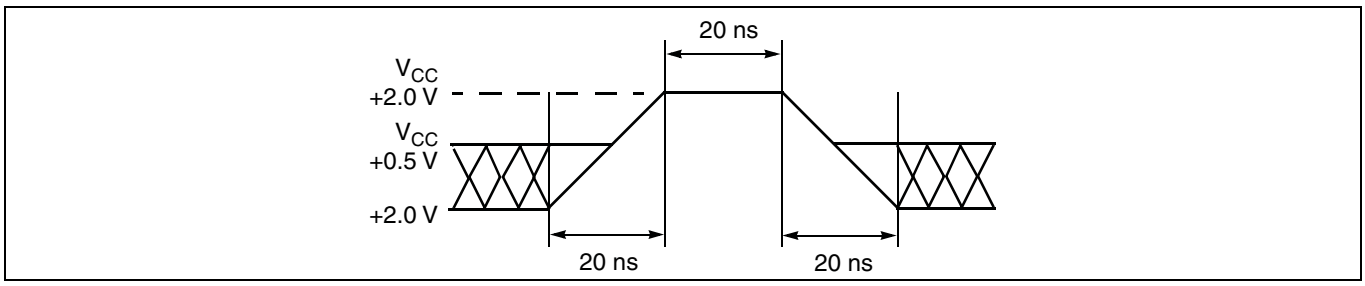


Figure 18 Maximum positive overshoot waveform

13 DC characteristics

Table 63 DC characteristics

Parameter	Description	Test conditions		Min	Typ [171]	Max	Unit
I_{LI}	Input load current [172]	$V_{IN} = V_{SS}$ to V_{IO}, $V_{CC} = V_{CC\ max}$	ACC	–	–	±2.0	µA
			Others	–	–	±1.0	
I_{LIT}	A9 input load current	$V_{CC} = V_{CC\ max}$, A9 = 12.5 V		–	–	35	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ to V_{IO}, $V_{CC} = V_{CC\ max}$		–	±0.02	±1.0	µA
I_{CC1}	V_{CC} initial read current [172]	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, Address switching @ 1 MHz		–	6.0	10	mA
		CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, Address switching @ 5 MHz		–	25	30	
		CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, Address switching @ 10 MHz		–	45	50	
I_{IO2}	V_{IO} non-active output	CE# = V_{IL}, OE# = V_{IH}		–	0.2	10	mA
I_{CC2}	V_{CC} intra-page read current [172]	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, Address switching @ 33 MHz		–	7.5	20	mA
I_{CC3}	V_{CC} active erase / program current [173, 174]	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$		–	50	60	mA
I_{CC4}	V_{CC} standby current	CE#, RESET# = V_{IH}, OE# = V_{IH}, $V_{IL} = V_{SS}$, $V_{IH} = V_{IO}$, $V_{CC} = V_{CC\ max}$		–	40	100	µA
I_{CC5}	V_{CC} reset current [174, 175]	RESET# = V_{IH}, $V_{IL} = V_{SS}$, $V_{IH} = V_{IO}$, $V_{CC} = V_{CC\ max}$		–	10	20	mA
I_{CC6}	Automatic sleep mode [176]	ACC = V_{IH}, $V_{IL} = V_{SS}$, $V_{IH} = V_{IO}$, $V_{CC} = V_{CC\ max}$, t_{ACC} + 30 ns		–	3	6	mA
		ACC = V_{IH}, $V_{IL} = V_{SS}$, $V_{IH} = V_{IO}$, $V_{CC} = V_{CC\ max}$, t_{ASSB}		–	40	100	µA
I_{CC7}	V_{CC} current during power-up [174, 177]	RESET# = V_{IO}, CE# = V_{IO}, OE# = V_{IO}, $V_{CC} = V_{CC}$max		–	53	80	mA
I_{ACC}	ACC accelerated program current	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC}$max, ACC = V_{HH}	ACC	–	10	20	mA
			V_{CC}	–	50	60	mA
V_{IL}	Input low voltage [178]			–0.5	–	0.3 × V_{IO}	V
V_{IH}	Input high voltage [178]			0.7 × V_{IO}	–	V_{IO} + 0.4	V
V_{HH}	Voltage for ACC program acceleration	V_{CC} = 2.7 V–3.6 V		11.5	–	12.5	V
V_{ID}	Voltage for autoselect	V_{CC} = 2.7 V–3.6 V		11.5	–	12.5	V
V_{OL}	Output low voltage [178, 180]	I_{OL} = 100 µA for DQ15–DQ0 I_{OL} = 2 mA for RY/BY#		–	–	0.15 × V_{IO}	V
V_{OH}	Output High Voltage [178]	I_{OH} = –100 µA		0.85 × V_{IO}	–	–	V
V_{LKO}	Low V_{CC} Lock-Out Voltage [174]			2.3	–	2.5	V
V_{RST}	Low V_{CC} Power on Reset Voltage [174]			–	1.0	–	V

Notes

171. Temperature = +25°C, V_{CC} = 3 V.
172. I_{CC} current listed is typically less than 2 mA / MHz, with OE# at V_{IH}.
173. I_{CC} active while Embedded Erase, Embedded Program, or Write Buffer Programming is in progress.
174. Not 100% tested.
175. If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC5} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to standby mode until the next read or write.
176. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.
177. During power-up there are spikes of current demand, the system needs to be able to supply this current to insure the part initializes correctly.
178. V_{IO} = 1.65 V–V_{CC} or 2.7 V–V_{CC}.
179. V_{CC} = 3 V and V_{IO} = 3 V or 1.8 V. When V_{IO} is at 1.8 V, I/Os cannot operate at 3 V.
180. The recommended pull-up resistor for RY/BY# output is 5k to 10k Ohms.

Table 64 DC characteristics, CMOS compatible in cabin temperature (–40°C to +105°C)

Parameter	Description	Test conditions		Min	Typ [181]	Max	Unit
I_{LI}	Input load current [182]	$V_{IN} = V_{SS}$ to V_{IO}, $V_{CC} = V_{CC\ max}$	ACC	–	–	±2.0	µA
			Others	–	–	±1.0	
I_{LIT}	A9 input load current	$V_{CC} = V_{CC\ max}$, A9 = 12.5 V		–	–	35	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ to V_{IO}, $V_{CC} = V_{CC\ max}$		–	±0.02	±1.0	µA
I_{CC1}	V_{CC} initial read current [182]	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, Address switching @ 1 MHz		–	6.0	10	mA
		CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, Address switching @ 5 MHz		–	25	30	
		CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, Address switching @ 10 MHz		–	45	50	
I_{IO2}	V_{IO} non-active output	CE# = V_{IL}, OE# = V_{IH}		–	0.2	10	mA
I_{CC2}	V_{CC} intra-page read current [182]	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$, Address switching @ 33 MHz		–	7.5	20	mA
I_{CC3}	V_{CC} active erase / program current [183, 184]	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC\ max}$		–	50	60	mA
I_{CC4}	V_{CC} standby current	CE#, RESET# = V_{IH}, OE# = V_{IH}, $V_{IL} = V_{SS}$, $V_{IH} = V_{IO}$, $V_{CC} = V_{CC\ max}$		–	40	<200	µA
I_{CC5}	V_{CC} reset current [184, 185]	RESET# = V_{IH}, $V_{IL} = V_{SS}$, $V_{IH} = V_{IO}$, $V_{CC} = V_{CC\ max}$		–	10	20	mA
I_{CC6}	Automatic sleep mode [186]	ACC = V_{IH}, $V_{IL} = V_{SS}$, $V_{IH} = V_{IO}$, $V_{CC} = V_{CC\ max}$, t_{ACC} + 30 ns		–	3	6	mA
		ACC = V_{IH}, $V_{IL} = V_{SS}$, $V_{IH} = V_{IO}$, $V_{CC} = V_{CC\ max}$, t_{ASSB}		–	40	<200	µA
I_{CC7}	V_{CC} current during power-up [184, 187]	RESET# = V_{IO}, CE# = V_{IO}, OE# = V_{IO}, $V_{CC} = V_{CC}$max		–	53	80	mA
I_{ACC}	ACC accelerated program current	CE# = V_{IL}, OE# = V_{IH}, $V_{CC} = V_{CC}$max, ACC = V_{HH}	ACC	–	10	20	mA
			V_{CC}	–	50	60	mA
V_{IL}	Input low voltage [188]			–0.5	–	0.3 × V_{IO}	V
V_{IH}	Input high voltage [188]			0.7 × V_{IO}	–	V_{IO} + 0.4	V
V_{HH}	Voltage for ACC program acceleration	V_{CC} = 2.7 V–3.6 V		11.5	–	12.5	V
V_{ID}	Voltage for autoselect	V_{CC} = 2.7 V–3.6 V		11.5	–	12.5	V
V_{OL}	Output low voltage [189, 190]	I_{OL} = 100 µA for DQ15–DQ0 I_{OL} = 2 mA for RY/BY#		–	–	0.15 × V_{IO}	V
V_{OH}	Output High Voltage [188]	I_{OH} = –100 µA		0.85 × V_{IO}	–	–	V
V_{LKO}	Low V_{CC} Lock-Out Voltage [184]			2.3	–	2.5	V
V_{RST}	Low V_{CC} Power on Reset Voltage [184]			–	1.0	–	V

Notes

181. Temperature = +25°C, V_{CC} = 3 V.
182. I_{CC} current listed is typically less than 2 mA / MHz, with OE# at V_{IH}.
183. I_{CC} active while Embedded Erase, Embedded Program, or Write Buffer Programming is in progress.
184. Not 100% tested.
185. If an embedded operation is in progress at the start of reset, the current consumption will remain at the embedded operation specification until the embedded operation is stopped by the reset. If no embedded operation is in progress when reset is started, or following the stopping of an embedded operation, I_{CC5} will be drawn during the remainder of t_{RPH}. After the end of t_{RPH} the device will go to standby mode until the next read or write.
186. Automatic sleep mode enables the low power mode when addresses remain stable for t_{ACC} + 30 ns.
187. During power-up there are spikes of current demand, the system needs to be able to supply this current to insure the part initializes correctly.
188. V_{IO} = 1.65 V–V_{CC} or 2.7 V–V_{CC}.
189. V_{CC} = 3 V and V_{IO} = 3 V or 1.8 V. When V_{IO} is at 1.8 V, I/Os cannot operate at 3 V.
190. The recommended pull-up resistor for RY/BY# output is 5k to 10k Ohms.

13.1 Capacitance characteristics

Table 65 Connector capacitance for FBGA (LAA) package

Parameter	Description	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$	4	7	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$	4	7	pF
C_{IN2}	Control pin capacitance	$V_{IN} = 0$	6	8	pF
C_{IN3}	ACC or WP#/ACC pin capacitance	$V_{IN} = 0$	4	8	pF
RY/BY#	Output capacitance	$V_{OUT} = 0$	3	5	pF

Table 66 Connector capacitance for FBGA (LAE) package

Parameter	Description	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$	4	6	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$	4	6	pF
C_{IN2}	Control pin capacitance	$V_{IN} = 0$	6	7	pF
C_{IN3}	ACC or WP#/ACC pin capacitance	$V_{IN} = 0$	4	8	pF
RY/BY#	Output capacitance	$V_{OUT} = 0$	3	4	pF

Table 67 Connector capacitance for FBGA (VBK) package

Parameter	Description	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$	4	6	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$	4	6	pF
C_{IN2}	Control pin capacitance	$V_{IN} = 0$	6	7	pF
C_{IN3}	ACC or WP#/ACC pin capacitance	$V_{IN} = 0$	4	8	pF
RY/BY#	Output capacitance	$V_{OUT} = 0$	3	4	pF

Table 68 Connector capacitance for 56-pin TSOP and 48-pin packages

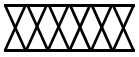
Parameter	Description	Test setup	Typ	Max	Unit
C_{IN}	Input capacitance	$V_{IN} = 0$	4	7	pF
C_{OUT}	Output capacitance	$V_{OUT} = 0$	4	7	pF
C_{IN2}	Control pin capacitance	$V_{IN} = 0$	6	8	pF
C_{IN3}	ACC or WP#/ACC pin capacitance	$V_{IN} = 0$	4	8	pF
RY/BY#	Output capacitance	$V_{OUT} = 0$	3	5	pF

Notes
191.Sampled, not 100% tested.
192.Test conditions $T_A = 25°C$, f = 1.0 MHz.

14 Test specifications

14.1 Key to switching waveforms

Table 69 Waveform details

Waveform	Inputs	Outputs
	Steady	
	Changing from H to L	
	Changing from L to H	
	Don't care, any change permitted	Changing, state unknown
	Does not apply	Center line is high impedance state (High-Z)

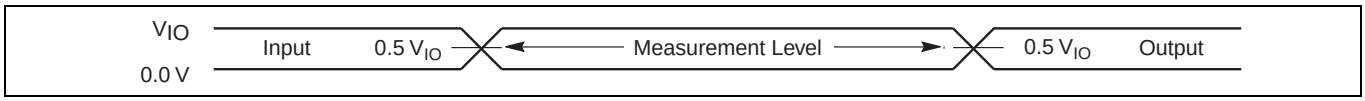


Figure 19 Input waveforms and measurement levels

14.2 AC test conditions

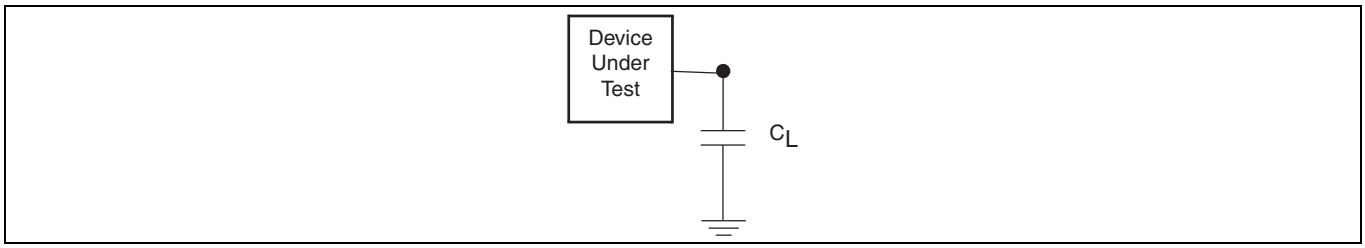


Figure 20 Test setup

Table 70 Test specifications

Test condition	All speeds	Unit
Output load capacitance, C_L (including jig capacitance)	30	pF
Input rise and fall times [193]	1.5	ns
Input Pulse Levels	0.0 or V_{IO}	V
Input timing measurement reference levels	0.5 × V_{IO}	V
Output timing measurement reference levels	0.5 × V_{IO}	V

Note
193.Measured between V_{IL} max and V_{IH} min.

14.3 Power-on reset (POR) and warm reset

Normal precautions must be taken for supply decoupling to stabilize the V_{CC} and V_{IO} power supplies. Each device in a system should have the V_{CC} and V_{IO} power supplies decoupled by a suitable capacitor close to the package connections (this capacitor is generally on the order of 0.1 µF).

Table 71 POR parameters

Parameter	Description	Limit	Value	Unit
t_{VCS}	V_{CC} setup time to first access [194, 195]	Min	50	µs
t_{VIOS}	V_{IO} setup time to first access [194, 195]	Min	50	µs
t_{RPH}	RESET# LOW to CE# LOW	Min	50	µs
t_{RP}	RESET# pulse width	Min	200	ns
t_{RH}	Time between RESET# (HIGH) and CE# (LOW)	Min	50	ns
t_{RB}	RY/BY# output HIGH to CE#, OE# pin LOW or address transition	Min	0	ns
t_{CEH}	CE# Pulse Width HIGH	Min	20	ns

Notes

194. Not 100% tested.
195. Timing measured from V_{CC} reaching V_{CC} minimum and V_{IO} reaching V_{IO} minimum to V_{IH} on Reset and V_{IL} on CE#.
196. RESET# LOW is optional during POR. If RESET is asserted during POR, the later of t_{RPH}, t_{VIOS}, or t_{VCS} will determine when CE# may go LOW. If RESET# remains LOW after t_{VIOS}, or t_{VCS} is satisfied, t_{RPH} is measured from the end of t_{VIOS}, or t_{VCS}. RESET must also be HIGH t_{RH} before CE# goes LOW.
197. $V_{CC} \geq V_{IO} - 200$ mV during power-up.
198. V_{CC} and V_{IO} ramp rate can be non-linear.
199. Sum of t_{RP} and t_{RH} must be equal to or greater than t_{RPH}.

14.3.1 Power-on (Cold) reset (POR)

During the rise of power supplies the V_{IO} supply voltage must remain less than or equal to the V_{CC} supply voltage. V_{IH} also must remain less than or equal to the V_{IO} supply.

The cold reset embedded algorithm requires a relatively long, hundreds of µs, period (t_{VCS}) to load all of the EAC algorithms and default state from non-volatile memory. During the cold reset period all control signals including CE# and RESET# are ignored. If CE# is LOW during t_{VCS} the device may draw higher than normal POR current during t_{VCS} but the level of CE# will not affect the cold reset EA. CE# or OE# must transition from HIGH to LOW or there must be an address transition after t_{VCS} for a valid read operation (t_{ACC} or t_{CE} is required after t_{RH}). RESET# may be HIGH or LOW during t_{VCS}. If RESET# is LOW during t_{VCS} it may remain LOW at the end of t_{VCS} to hold the device in the hardware reset state. If RESET# is HIGH at the end of t_{VCS} the device will go to the standby state.

When power is first applied, with supply voltage below V_{RST} then rising to reach operating range minimum, internal device configuration and warm reset activities are initiated. CE# is ignored for the duration of the POR operation (t_{VCS} or t_{VIOS}). RESET# LOW during this POR period is optional. If RESET# is driven LOW during POR it must satisfy the hardware reset parameters t_{RP} and t_{RPH}. In which case the reset operations will be completed at the later of t_{VCS} or t_{VIOS} or t_{RPH}.

During cold reset the device will draw I_{CC7} current.

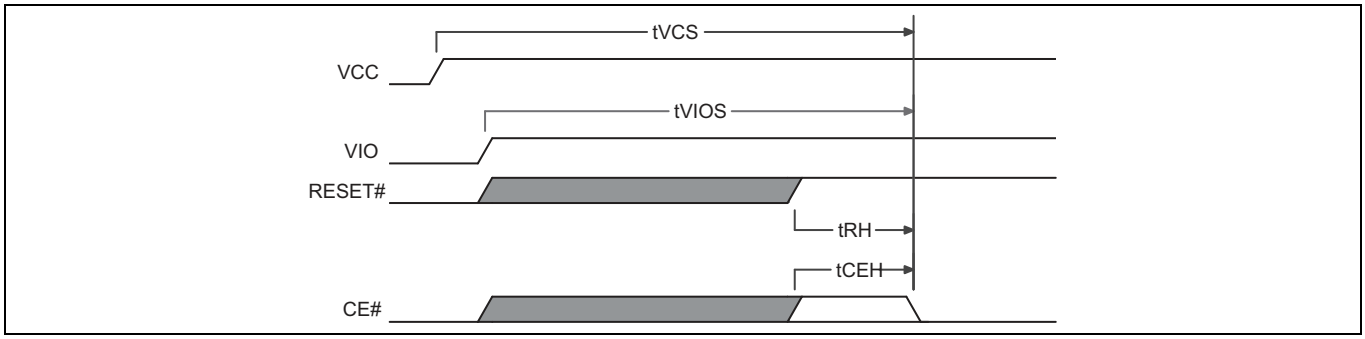


Figure 21 Power-up diagram

14.3.2 Hardware (warm) reset

During hardware reset (t_{RPH}) the device will draw I_{CC5} current.

When RESET# continues to be held at V_{SS}, the device draws CMOS standby current (I_{CC4}). If RESET# is held at V_{IL}, but not at V_{SS}, the standby current is greater.

If a cold reset has not been completed by the device when RESET# is asserted LOW after t_{VCS}, the Cold Reset# EA will be performed instead of the Warm RESET#, requiring t_{VCS} time to complete. See **Figure 22**.

After the device has completed POR and entered the standby state, any later transition to the hardware reset state will initiate the warm reset embedded algorithm. A warm reset is much shorter than a cold reset, taking tens of µs (t_{RPH}) to complete. During the warm reset EA, any in progress Embedded Algorithm is stopped and the EAC is returned to its POR state without reloading EAC algorithms from non-volatile memory. After the warm reset EA completes, the interface will remain in the hardware reset state if RESET# remains LOW. When RESET# returns HIGH the interface will transit to the standby state. If RESET# is HIGH at the end of the warm reset EA, the interface will directly transit to the standby state. CE# or OE# must transition from HIGH to LOW or there must be an address transition after t_{VCS} for a valid read operation (t_{ACC} or t_{CE} is required).

If POR has not been properly completed by the end of t_{VCS}, a later transition to the hardware reset state will cause a transition to the power-on reset interface state and initiate the cold reset embedded algorithm. This ensures the device can complete a cold reset even if some aspect of the system power-on voltage ramp-up causes the POR to not initiate or complete correctly. The RY/BY# pin is LOW during cold or warm reset as an indication that the device is busy performing reset operations.

Hardware reset is initiated by the RESET# signal going to V_{IL}.

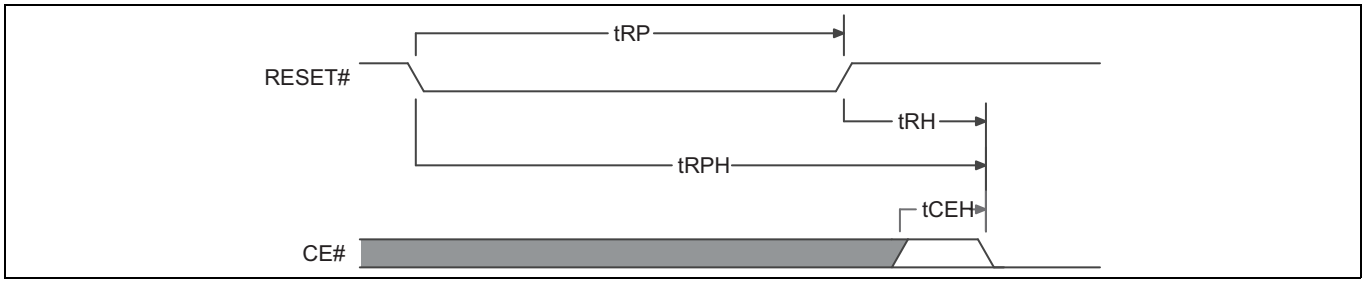


Figure 22 Hardware reset

15 AC characteristics

15.1 Read-only operations

Table 72 Read-only operations Industrial Temperature (–40°C to +85°C)

Parameter		Description		Test setup		Speed options		Unit
JEDEC	Std.					70	80	
t_{AVAV}	t_{RC}	Read cycle time [200]		V_{IO} = 2.7 V to V_{CC}	Min	70	–	ns
				V_{IO} = 1.65 V to V_{CC}		–	80	
t_{AVQV}	t_{ACC}	Address to output delay	CE#, OE# = V_{IL}	V_{IO} = 2.7 V to V_{CC}	Max	70	–	ns
				V_{IO} = 1.65 V to V_{CC}		–	80	
t_{ELQV}	t_{CE}	Chip Enable to output delay	OE# = V_{IL}	V_{IO} = 2.7 V to V_{CC}	Max	70	–	ns
				V_{IO} = 1.65 V to V_{CC}		–	80	
	t_{PACC}	Page access time		V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		25		
t_{GLQV}	t_{OE}	Output Enable to output delay	Read	V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		25		
			Poll	V_{IO} = 2.7 V to V_{CC}		25		
				V_{IO} = 1.65 V to V_{CC}		35		
	t_{ASO}	Address setup time	Poll	–	Min	15		ns
	t_{AHT}	Address hold time	Poll	–	Min	0		ns
	t_{CEPH}	CE# HIGH	Poll	–	Min	20		ns
	t_{OEP}	OE# LOW	Poll	–	Min	25		ns
	t_{OEPH}	OE# HIGH	Poll	–	Min	20		ns
	t_{OEC}	OE# cycle time	Poll	–	Min	60		ns
t_{EHQZ}	t_{DF}	Chip Enable to output High-Z [200]		V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		20		ns
t_{GHQZ}	t_{DF}	Output Enable to output High-Z [200]		V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		20		ns
t_{AXQX}	t_{OH}	Output hold time from addresses, CE# or OE#, whichever occurs first		–	Min	0		ns
	t_{OEH}	Output Enable hold time [200]	Read	–	Min	0		ns
			Toggle and Data# Polling	–	Min	10		ns
	t_{ASSB}	Automatic sleep to standby time [200]		CE# = V_{IL}, Address stable	Typ	5		µs
					Max	8		µs
t_{BLEL}	t_{FLEL}	BYTE# LOW to CE#		–	Max	10		ns
t_{BHEL}	t_{FHEL}	BYTE# HIGH to CE#		–	Max	10		ns
t_{BLQV}	t_{FLQV}	BYTE# LOW to output High-Z [200]		–	Max	10		ns
t_{BHQV}	t_{FHQV}	BYTE# HIGH to output delay		–	Max	10		ns

Notes
200.Not 100% tested.
201.See **Figure 20** and **Table 70** for test specifications.

Table 73 Read-only operations Industrial Plus Temperature (–40°C to +105°C)

Parameter		Description		Test setup		Speed options		Unit
JEDEC	Std.					80	90	
t_{AVAV}	t_{RC}	Read cycle time [202]		V_{IO} = 2.7 V to V_{CC}	Min	80	–	ns
				V_{IO} = 1.65 V to V_{CC}		–	90	
t_{AVQV}	t_{ACC}	Address to output delay	CE#, OE# = V_{IL}	V_{IO} = 2.7 V to V_{CC}	Max	80	–	ns
				V_{IO} = 1.65 V to V_{CC}		–	90	
t_{ELQV}	t_{CE}	Chip Enable to output delay	OE# = V_{IL}	V_{IO} = 2.7 V to V_{CC}	Max	80	–	ns
				V_{IO} = 1.65 V to V_{CC}		–	90	
	t_{PACC}	Page access time		V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		25		
t_{GLQV}	t_{OE}	Output Enable to output delay	Read	V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		25		
			Poll	V_{IO} = 2.7 V to V_{CC}		25		
				V_{IO} = 1.65 V to V_{CC}		35		
	t_{ASO}	Address setup time	Poll	–	Min	15		ns
	t_{AHT}	Address hold time	Poll	–	Min	0		ns
	t_{CEPH}	CE# HIGH	Poll	–	Min	20		ns
	t_{OEP}	OE# LOW	Poll	–	Min	25		ns
	t_{OEPH}	OE# HIGH	Poll	–	Min	20		ns
	t_{OEC}	OE# cycle time	Poll	–	Min	60		ns
t_{EHQZ}	t_{DF}	Chip Enable to output High-Z [202]		V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		20		ns
t_{GHQZ}	t_{DF}	Output Enable to output High-Z [202]		V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		20		ns
t_{AXQX}	t_{OH}	Output hold time from addresses, CE# or OE#, whichever occurs first		–	Min	0		ns
	t_{OEH}	Output Enable hold time [202]	Read	–	Min	0		ns
			Toggle and Data# Polling	–	Min	10		ns
	t_{ASSB}	Automatic sleep to standby time [202]		CE# = V_{IL}, Address stable	Typ	5		µs
					Max	8		µs
t_{BLEL}	t_{FLEL}	BYTE# LOW to CE#		–	Max	10		ns
t_{BHEL}	t_{FHEL}	BYTE# HIGH to CE#		–	Max	10		ns
t_{BLQV}	t_{FLQV}	BYTE# LOW to output High-Z [202]		–	Max	10		ns
t_{BHQV}	t_{FHQV}	BYTE# HIGH to output delay		–	Max	10		ns

Notes
202.Not 100% tested.
203.See **Figure 20** and **Table 70** for test specifications.

Table 74 Read-only operations Extended Temperature (–40°C to +125°C)

Parameter		Description		Test setup		Speed options		Unit
JEDEC	Std.					80	90	
t_{AVAV}	t_{RC}	Read cycle time [204]		V_{IO} = 2.7 V to V_{CC}	Min	80	–	ns
				V_{IO} = 1.65 V to V_{CC}		–	90	
t_{AVQV}	t_{ACC}	Address to output delay	CE#, OE# = V_{IL}	V_{IO} = 2.7 V to V_{CC}	Max	80	–	ns
				V_{IO} = 1.65 V to V_{CC}		–	90	
t_{ELQV}	t_{CE}	Chip Enable to output delay	OE# = V_{IL}	V_{IO} = 2.7 V to V_{CC}	Max	80	–	ns
				V_{IO} = 1.65 V to V_{CC}		–	90	
	t_{PACC}	Page access time		V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		25		
t_{GLQV}	t_{OE}	Output Enable to output delay	Read	V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		25		
			Poll	V_{IO} = 2.7 V to V_{CC}		25		
				V_{IO} = 1.65 V to V_{CC}		35		
	t_{ASO}	Address setup time	Poll	–	Min	15		ns
	t_{AHT}	Address hold time	Poll	–	Min	0		ns
	t_{CEPH}	CE# HIGH	Poll	–	Min	20		ns
	t_{OEP}	OE# LOW	Poll	–	Min	25		ns
	t_{OEPH}	OE# HIGH	Poll	–	Min	20		ns
	t_{OEC}	OE# cycle time	Poll	–	Min	60		ns
t_{EHQZ}	t_{DF}	Chip Enable to output High-Z [204]		V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		20		ns
t_{GHQZ}	t_{DF}	Output Enable to output High-Z [204]		V_{IO} = 2.7 V to V_{CC}	Max	15		ns
				V_{IO} = 1.65 V to V_{CC}		20		ns
t_{AXQX}	t_{OH}	Output hold time from addresses, CE# or OE#, whichever occurs first		–	Min	0		ns
	t_{OEH}	Output Enable hold time [204]	Read	–	Min	0		ns
			Toggle and Data# Polling	–	Min	10		ns
	t_{ASSB}	Automatic sleep to standby time [204]		CE# = V_{IL}, Address stable	Typ	5		µs
					Max	8		µs
t_{BLEL}	t_{FLEL}	BYTE# LOW to CE#		–	Max	10		ns
t_{BHEL}	t_{FHEL}	BYTE# HIGH to CE#		–	Max	10		ns
t_{BLQV}	t_{FLQV}	BYTE# LOW to output High-Z [204]		–	Max	10		ns
t_{BHQV}	t_{FHQV}	BYTE# HIGH to output delay		–	Max	10		ns

Notes
204.Not 100% tested.
205.See **Figure 20** and **Table 70** for test specifications.

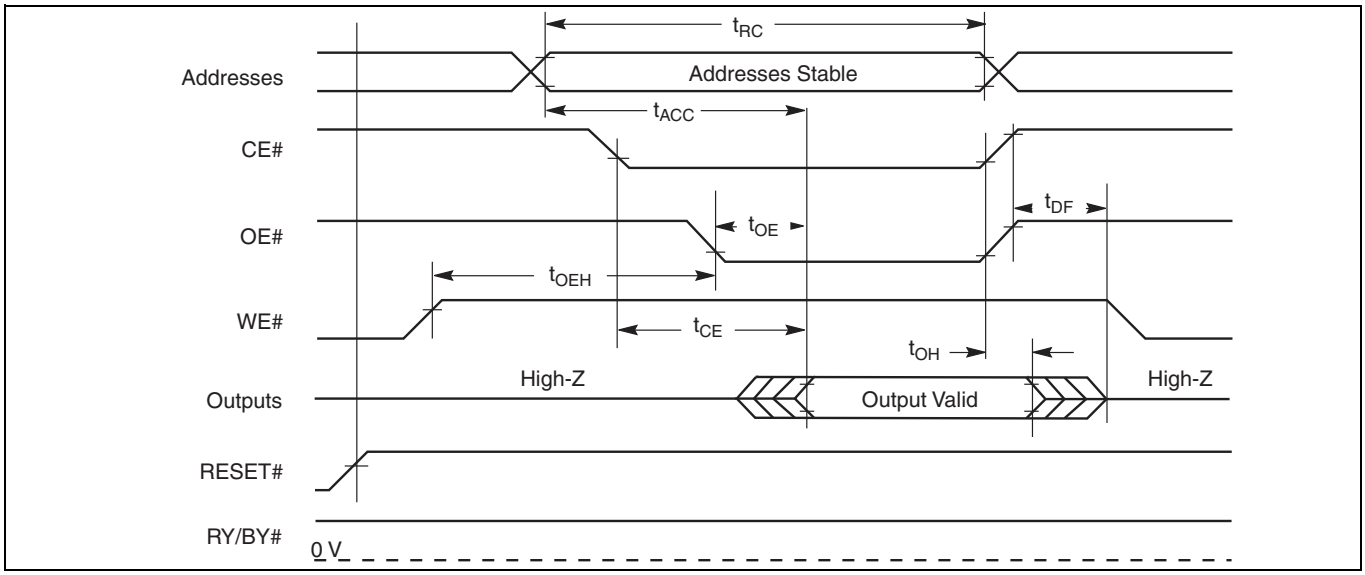


Figure 23 Read operation timings

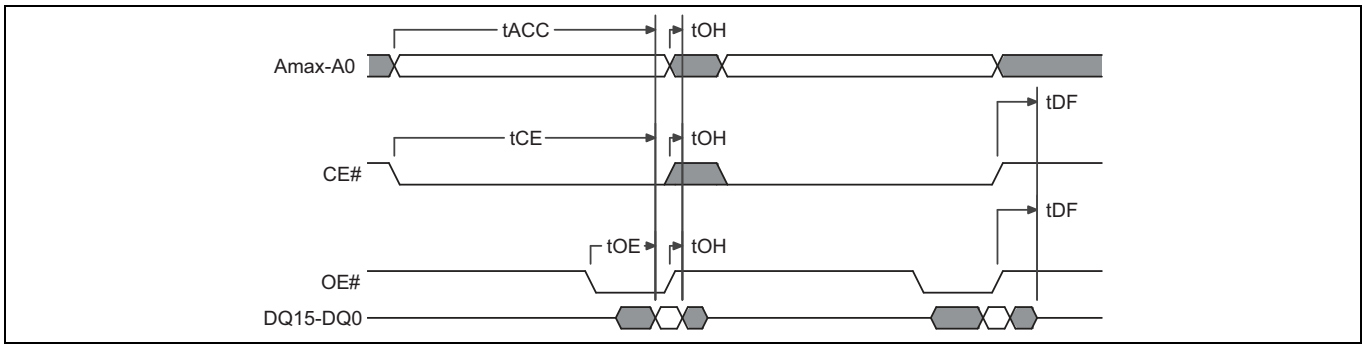


Figure 24 Back to Back Read (t_{ACC}) operation timing diagram

Notes
206.Word Configuration: Toggle A0, A1, and A2.
207.Byte Configuration: Toggle A1, A0, A2, and A3.

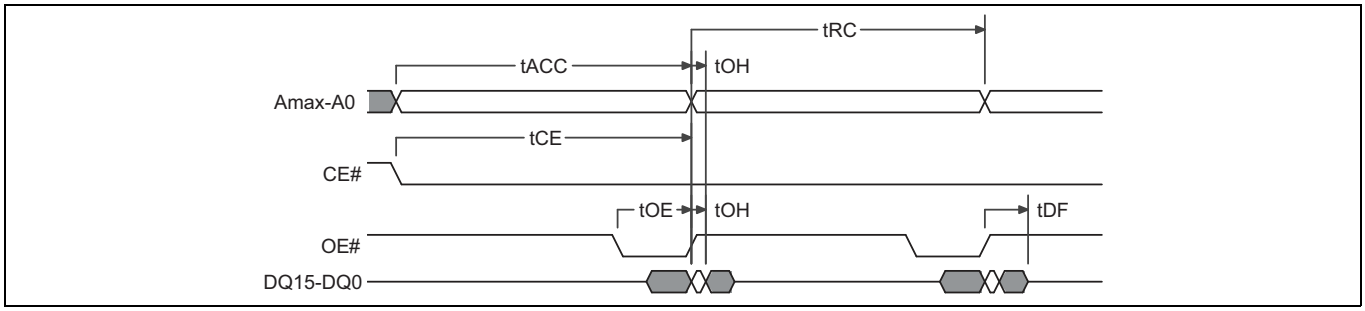


Figure 25 Back to Back Read operation (t_{RC}) timing diagram

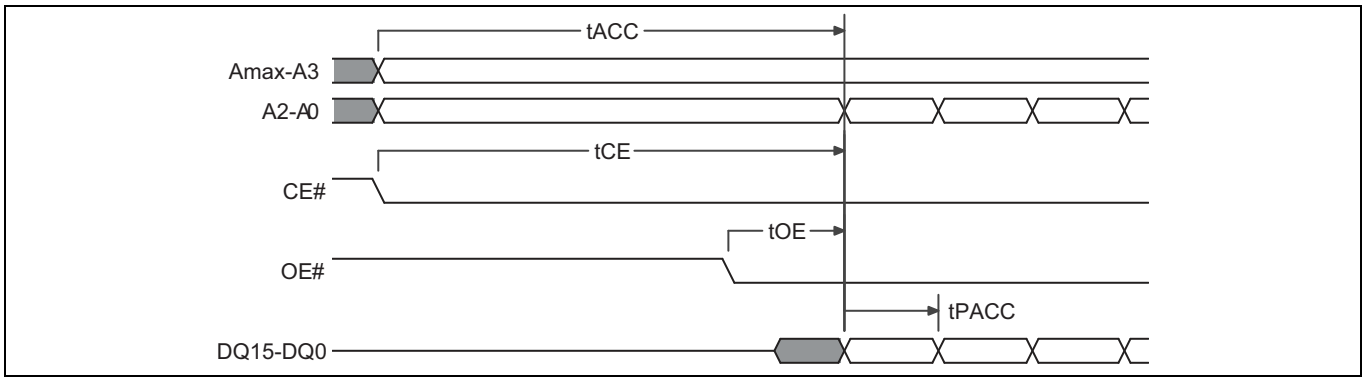


Figure 26 Page Read timing diagram

Notes
208.Word Configuration: Toggle A0, A1, and A2.
209.Byte Configuration: Toggle A1, A0, A2, and A3.
210.Back to Back operations, in which CE# remains Low between accesses, requires an address change to initiate the second access.
211.Word Configuration: Toggle A0, A1, and A2.
212.Byte Configuration: Toggle A1, A0, A2, and A3.

15.2 Asynchronous write operations

Table 75 Write operations

Parameter		Description		V_{IO} = 2.7 V to V_{CC}	V_{IO} = 1.65 V to V_{CC}	Unit
JEDEC	Std.					
t_{AVAV}	t_{WC}	Write cycle time [200]	Min	60		ns
t_{AVWL}	t_{AS}	Address setup time	Min	0		ns
t_{WLAX}	t_{AH}	Address hold time	Min	45		ns
t_{DVWH}	t_{DS}	Data setup time	Min	30		ns
t_{WHDX}	t_{DH}	Data hold time	Min	0		ns
t_{GHWL}	t_{GHWL}	Read recovery time before write (OE# HIGH to WE# LOW)	Min	0		ns
t_{ELWL}	t_{CS}	CE# setup time	Min	0		ns
t_{WHEH}	t_{CH}	CE# hold time	Min	0		ns
t_{WLWH}	t_{WP}	Write pulse width	Min	25		ns
t_{WHDL}	t_{WPH}	Write pulse width HIGH	Min	20		ns
	t_{SEA}	Sector erase time-out	Min	50		µs

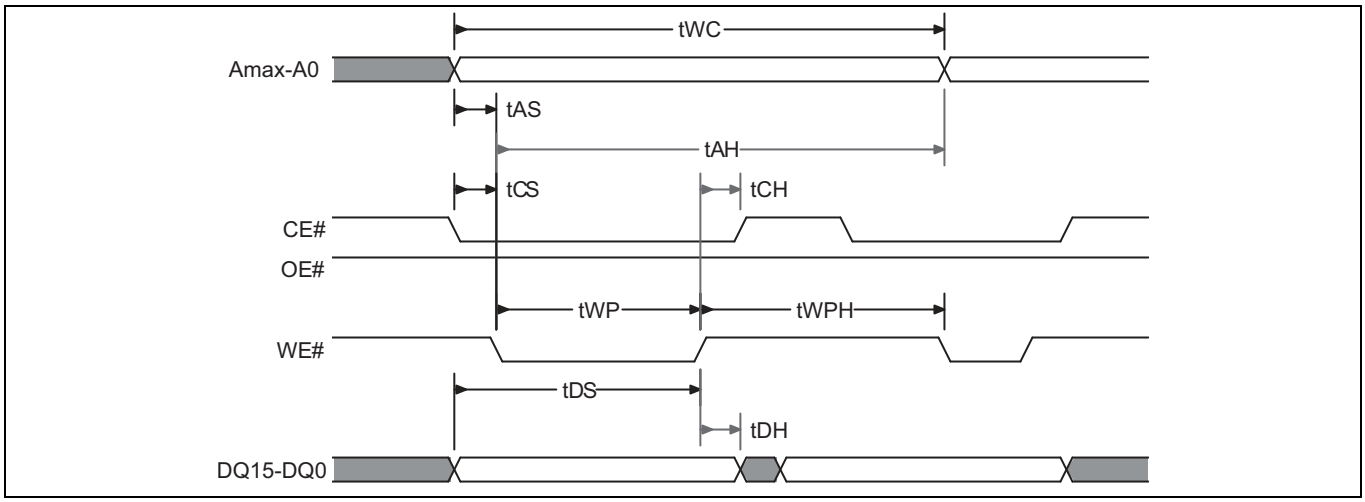


Figure 27 Back to Back Write operation timing diagram

Notes
213.Not 100% tested.
214.See the **"Erase and programming performance"** on page 104 for more information.
215.Word Configuration: Toggle A0, A1, and A2.
216.Byte Configuration: Toggle A1, A0, A2, and A3.

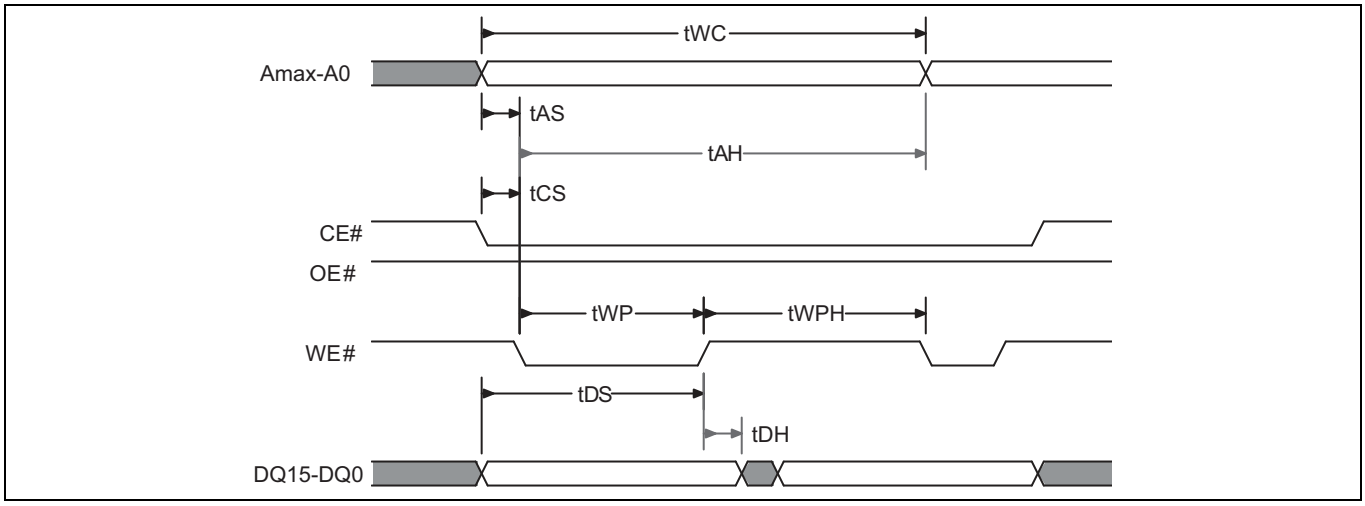


Figure 28 Back to Back (CE# V_{IL}) Write operation timing diagram

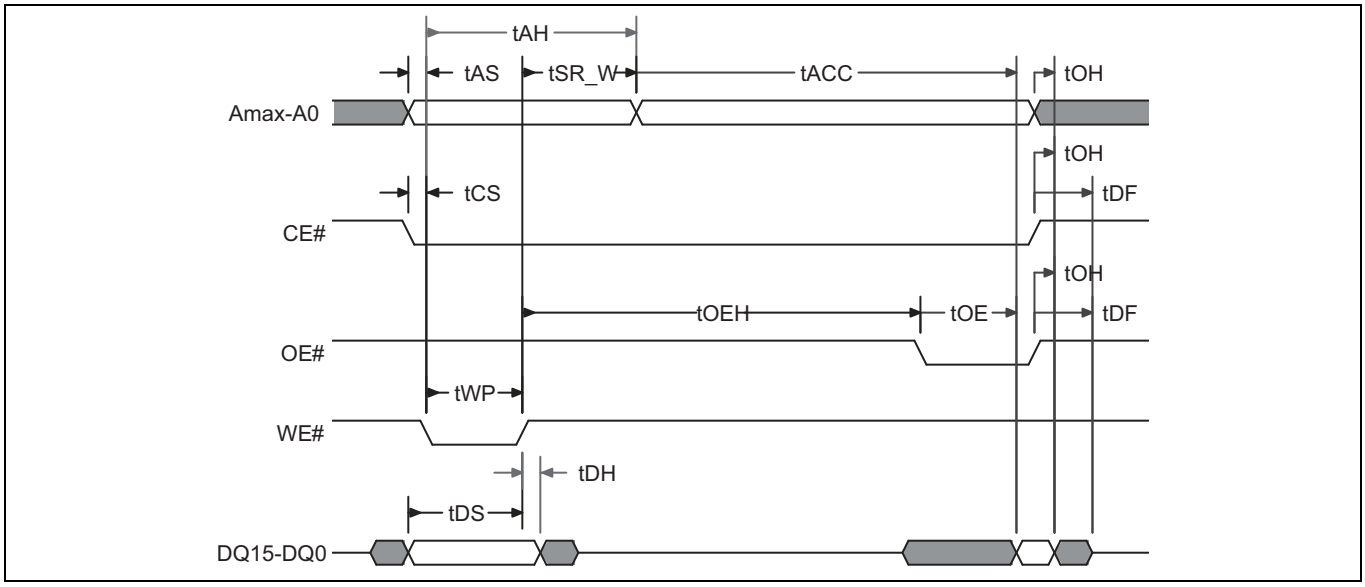


Figure 29 Write to Read (t_{ACC}) operation timing diagram

Notes
217.Word Configuration: Toggle A0, A1, and A2.
218.Byte Configuration: Toggle A1, A0, A2, and A3.
219.Word Configuration: Toggle A0, A1, and A2.
220.Byte Configuration: Toggle A1, A0, A2, and A3.

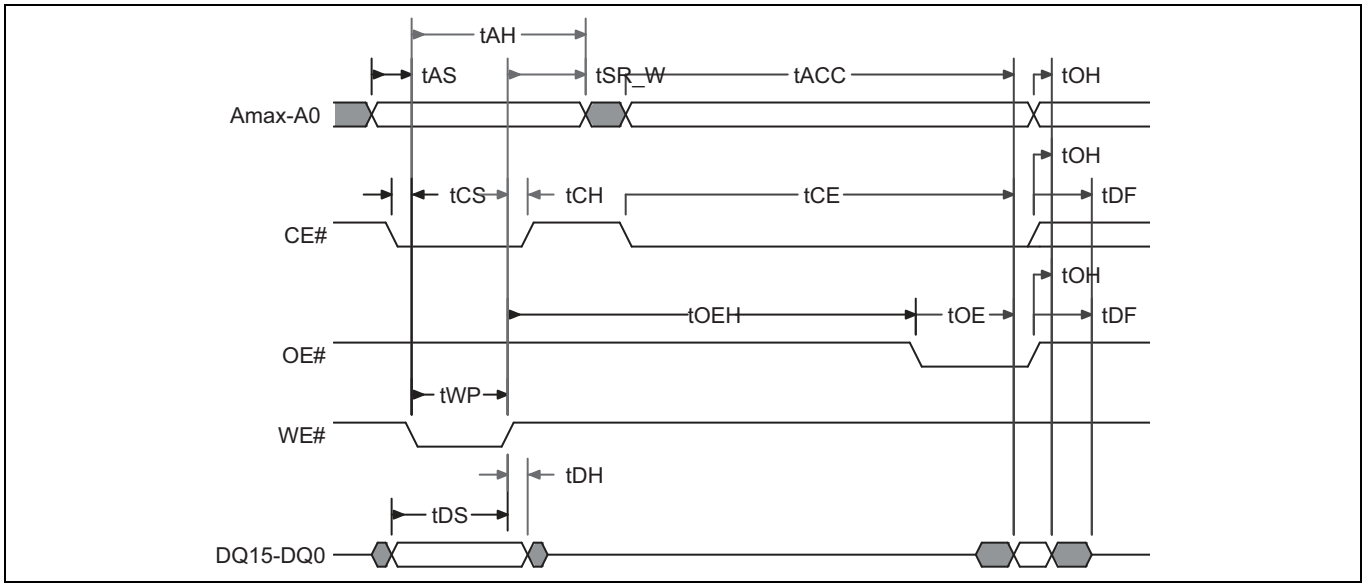


Figure 30 Write to Read (t_{CE}) operation timing diagram

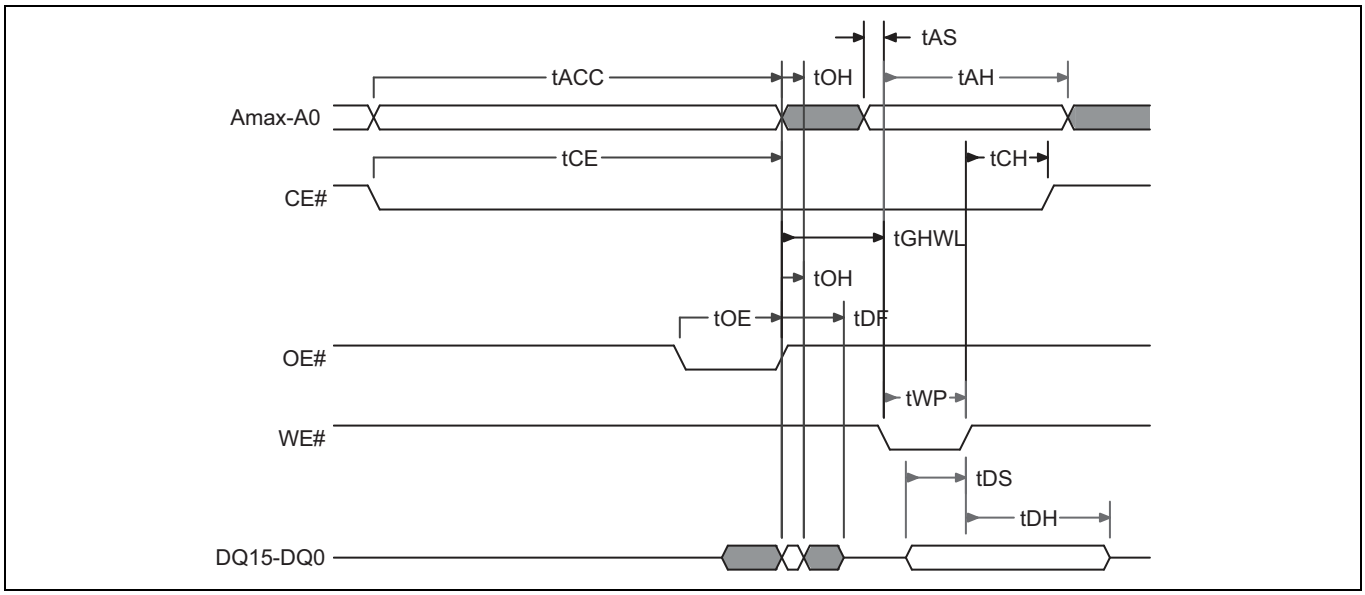


Figure 31 Read to Write (CE# V_{IL}) operation timing diagram

Notes
221.Word Configuration: Toggle A0, A1, and A2.
222.Byte Configuration: Toggle A1, A0, A2, and A3.
223.Word Configuration: Toggle A0, A1, and A2.
224.Byte Configuration: Toggle A1, A0, A2, and A3.

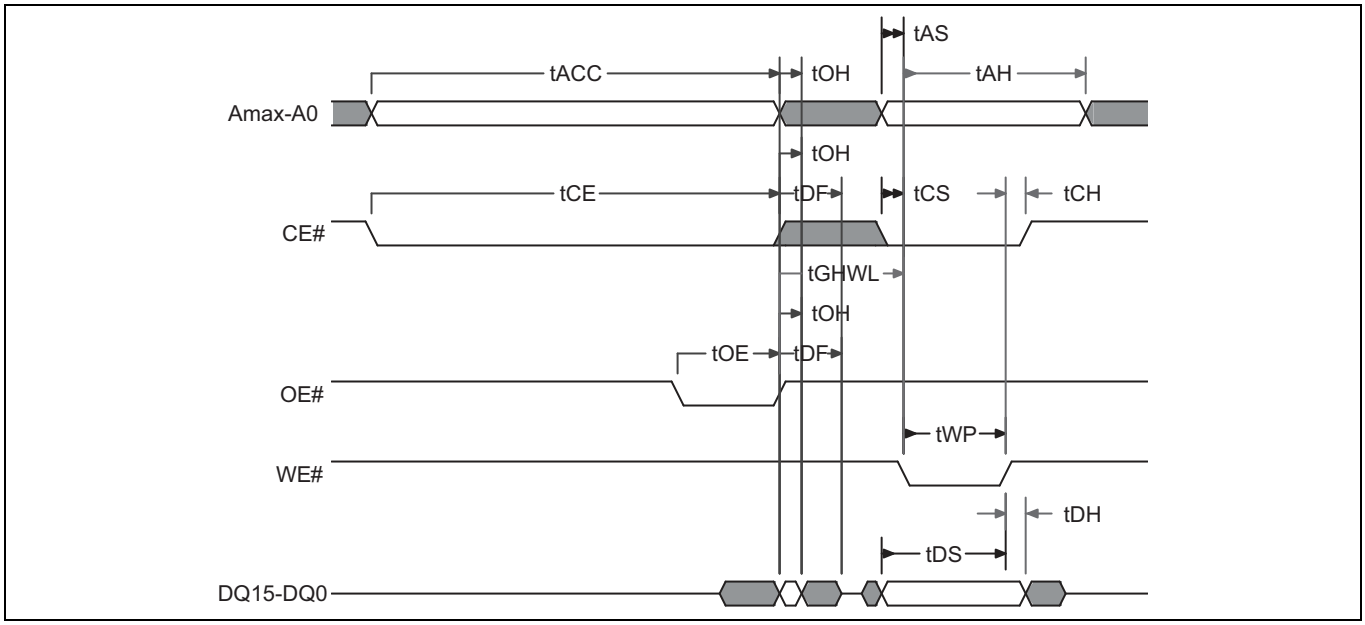


Figure 32 Read to Write (CE# Toggle) operation timing diagram

Notes
225.Word Configuration: Toggle A0, A1, and A2.
226.Byte Configuration: Toggle A1, A0, A2, and A3.

Table 76 Erase / program operations

Parameter		Description		V_{IO} = 2.7V to V_{CC}	V_{IO} = 1.65V to V_{CC}	Unit
JEDEC	Std					
t_{WHWH1}	t_{WHWH1}	Write buffer program operation	Typ	Note 227		µs
		Effective write buffer program operation per word	Typ	Note 227		µs
		Program operation per word or page	Typ	Note 227		µs
t_{WHWH2}	t_{WHWH2}	Sector erase operation [228]	Typ	Note 227		ms
	t_{BUSY}	Erase / Program Valid to RY/BY# Delay	Max	80		ns
	$t_{SR/W}$	Latency between Read and Write operations [229]	Min	10		ns
	t_{ESL}	Erase Suspend Latency	Max	Note 227		µs
	t_{PSL}	Program Suspend Latency	Max	Note 227		µs
	t_{RB}	RY/BY# Recovery Time	Min	0		µs
	t_{PPB}	PPB LOCK Unlock	Min	80		µs
			Max	120		
	t_{DP}	Data Polling to Protected Sector (Program)	Min	1		µs
		Data Polling to Protected Sector (Erase)	Min	100		µs
	t_{TOR}	Exceeded Timing Cleared (DQ5)	Max	2		µs
	t_{VHH}	V_{HH} Rise and Fall Time [228]	Min	250		ns

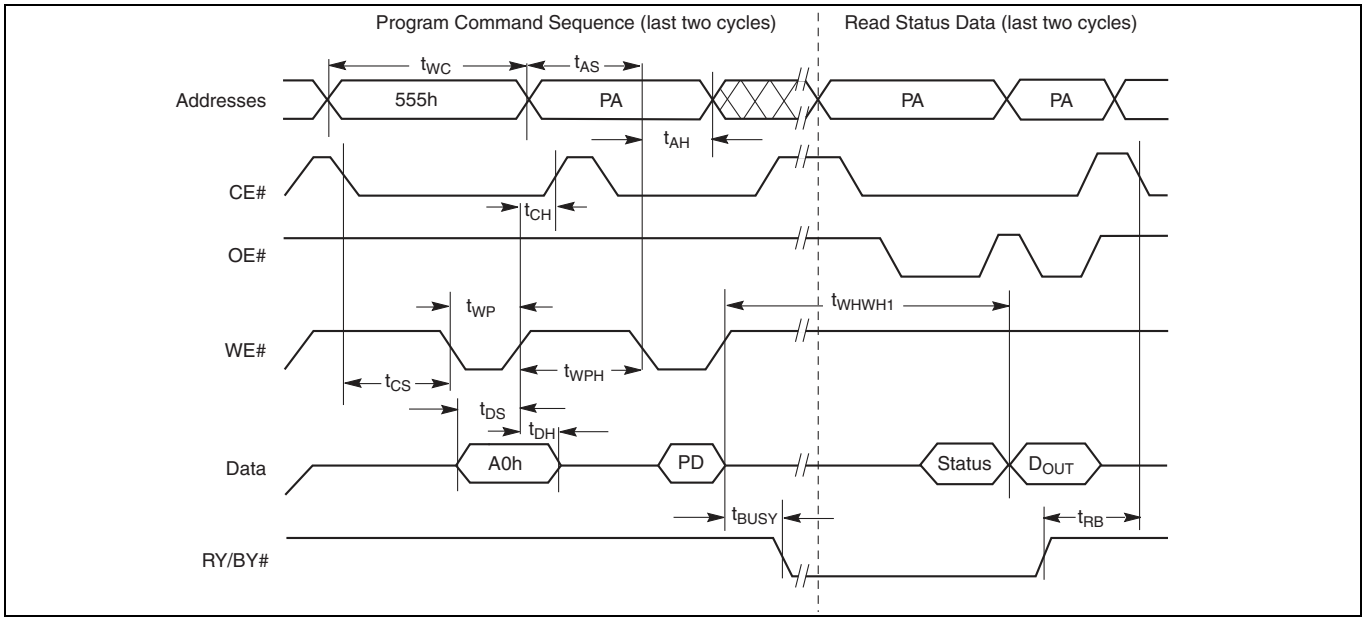


Figure 33 Program operation timings

Notes
227.See **Table 78** and **Table 79** for specific values.
228.Not 100% tested.
229.Upon the rising edge of WE#, must wait $t_{SR/W}$ before switching to another address.
230.PA = program address, PD = program data, D_{OUT} is the true data at the program address.
231.Illustration shows device in word mode.

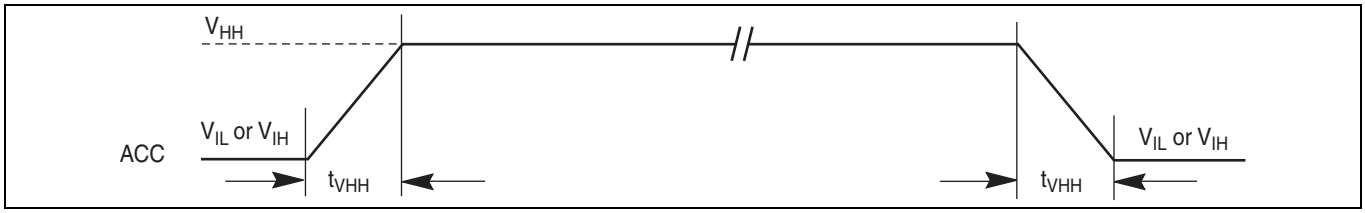


Figure 34 Accelerated program timing diagram

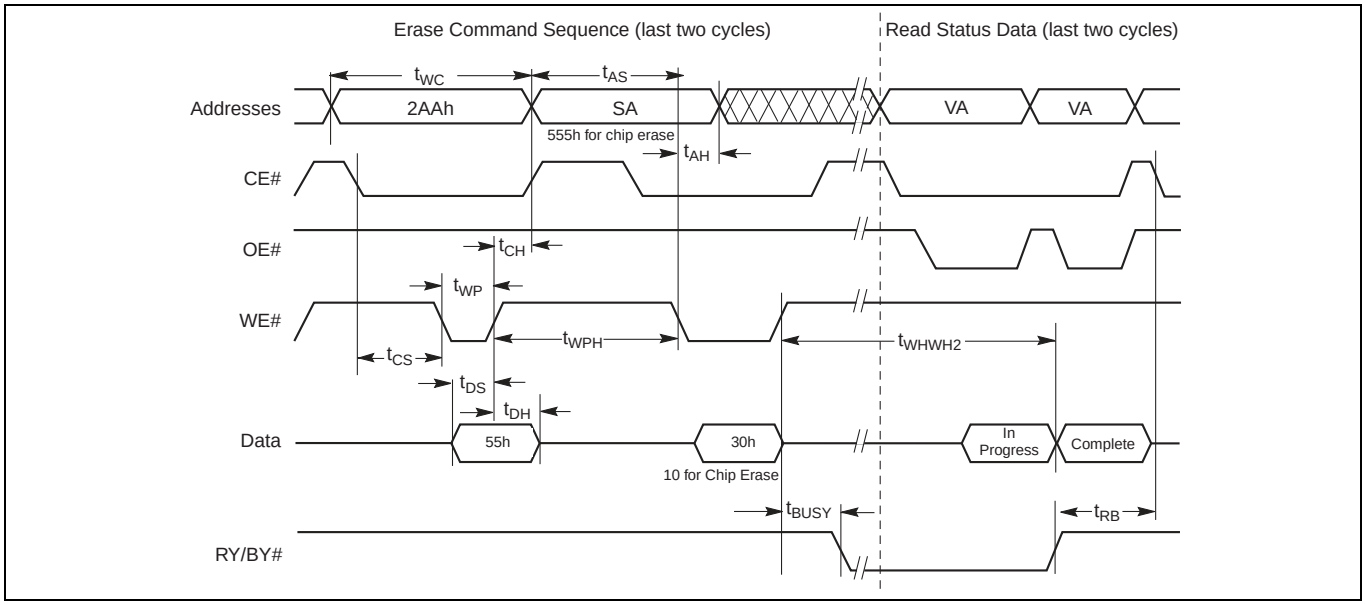


Figure 35 Chip / sector erase operation timings

Notes

232. SA = sector address (for Sector Erase), VA = Valid Address for reading status data (see **"Write Operation status"** on page 56.)
233. Illustration shows device in word mode.

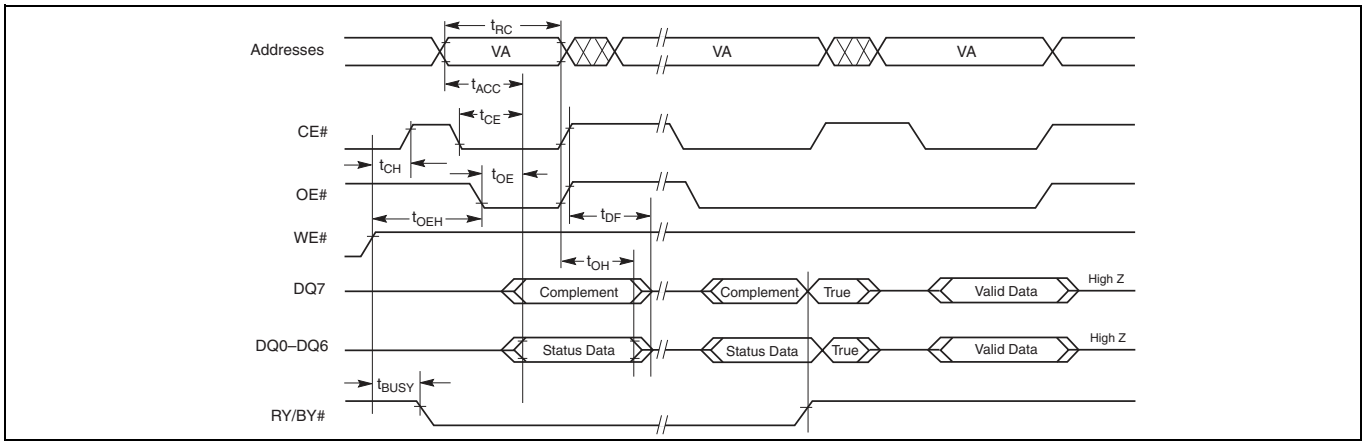


Figure 36 Data# polling timings (During embedded algorithms)

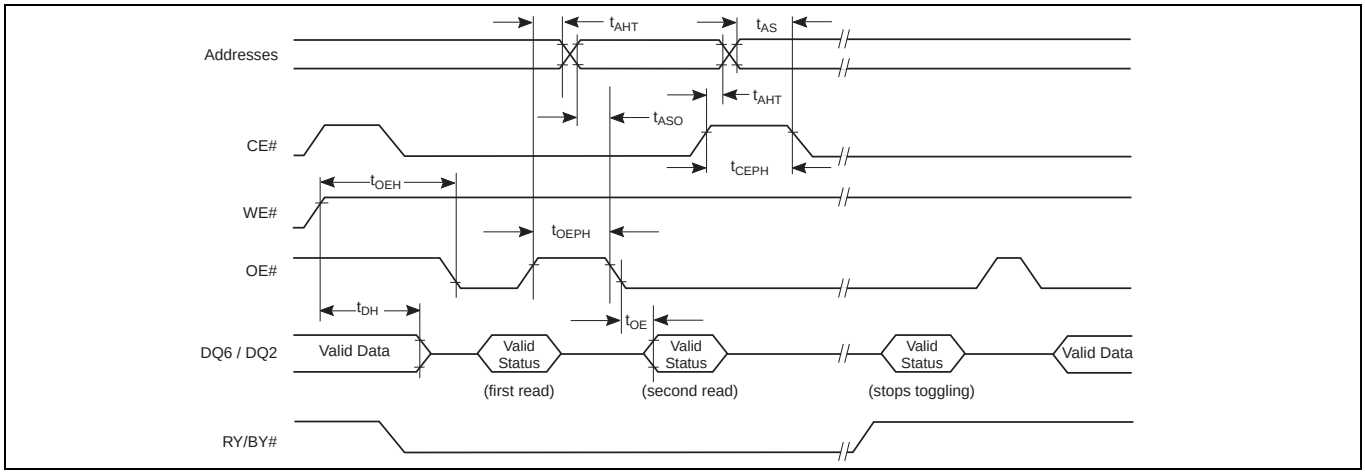


Figure 37 Toggle bit timings (During embedded algorithms)

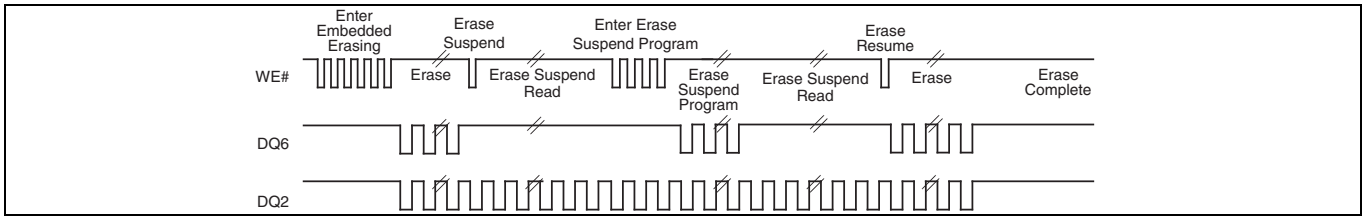


Figure 38 DQ2 vs. DQ6

Notes

234.VA = Valid address. Illustration shows first status cycle after command sequence, last status read cycle, and array data read cycle.

235.VA = Valid address; not required for DQ6. Illustration shows first two status cycle after command sequence, last status read cycle, and array data read cycle.

236.CE# does not need to go HIGH between status bit reads.

237.DQ2 toggles only when read at an address within an erase-suspended sector. The system may use OE# or CE# to toggle DQ2 and DQ6.

15.3 Alternative CE# controlled write operations

Table 77 Alternate CE# controlled erase and program operations

Parameter		Description		V_{IO} = 2.7 V to V_{CC}	V_{IO} = 1.65 V to V_{CC}	Unit
JEDEC	Std.					
t_{AVAV}	t_{WC}	Write Cycle time [213]	Min	60		ns
t_{AVWL}	t_{AS}	Address setup time	Min	0		ns
t_{ELAX}	t_{AH}	Address hold time	Min	45		ns
t_{DVEH}	t_{DS}	Data setup time	Min	30		ns
t_{EHDX}	t_{DH}	Data hold time	Min	0		ns
t_{GHEL}	t_{GHEL}	Read recovery time before write (OE# HIGH to CE# LOW)	Min	0		ns
t_{WLEL}	t_{WS}	WE# setup time	Min	0		ns
t_{EHWH}	t_{WH}	WE# hold time	Min	0		ns
t_{ELEH}	t_{CP}	CE# pulse width	Min	25		ns
t_{EHEL}	t_{CPH}	CE# pulse width HIGH	Min	20		ns
	t_{SEA}	Sector erase time-out	Min	50		µs

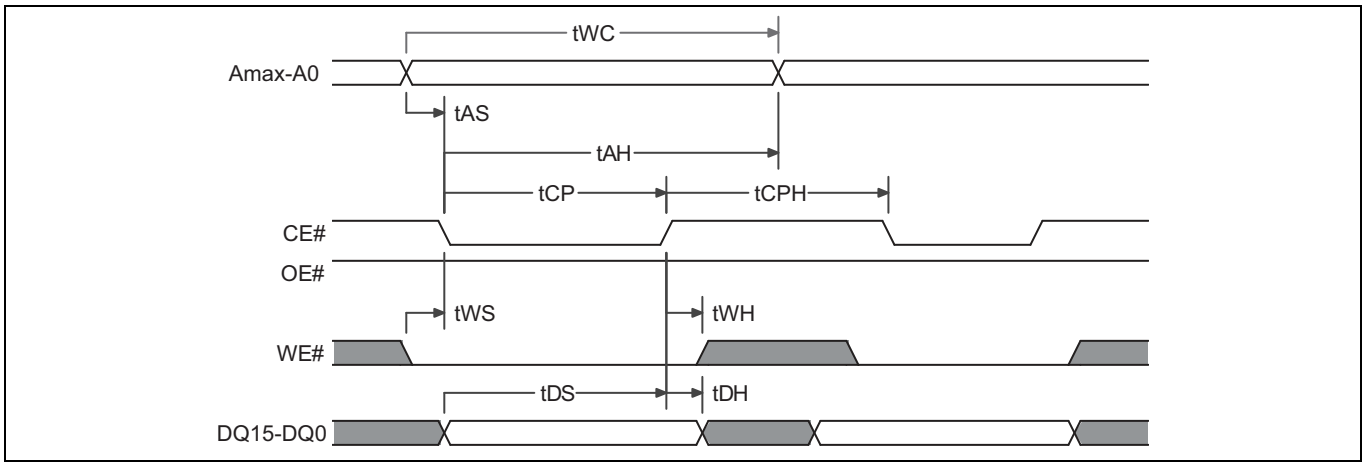


Figure 39 Back to Back (CE#) Write operation timing diagram

Notes
238.Not 100% tested.
239.See the **"Erase and programming performance"** on page 104 for more information.
240.Word Configuration: Toggle A0, A1, and A2.
241.Byte Configuration: Toggle A1, A0, A2, and A3.

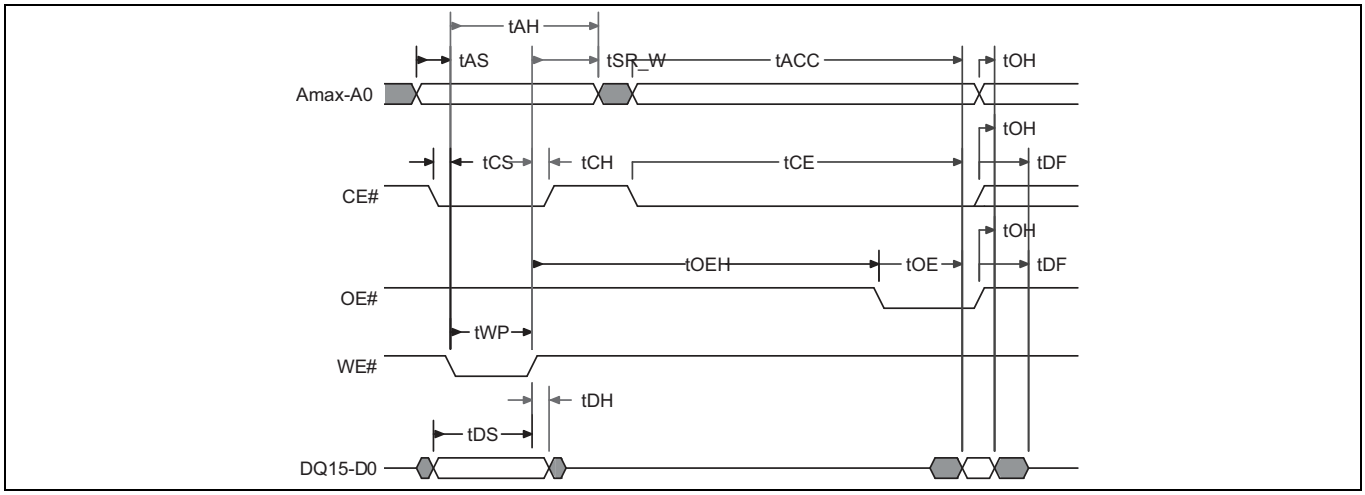


Figure 40 (CE#) Write to Read operation timing diagram

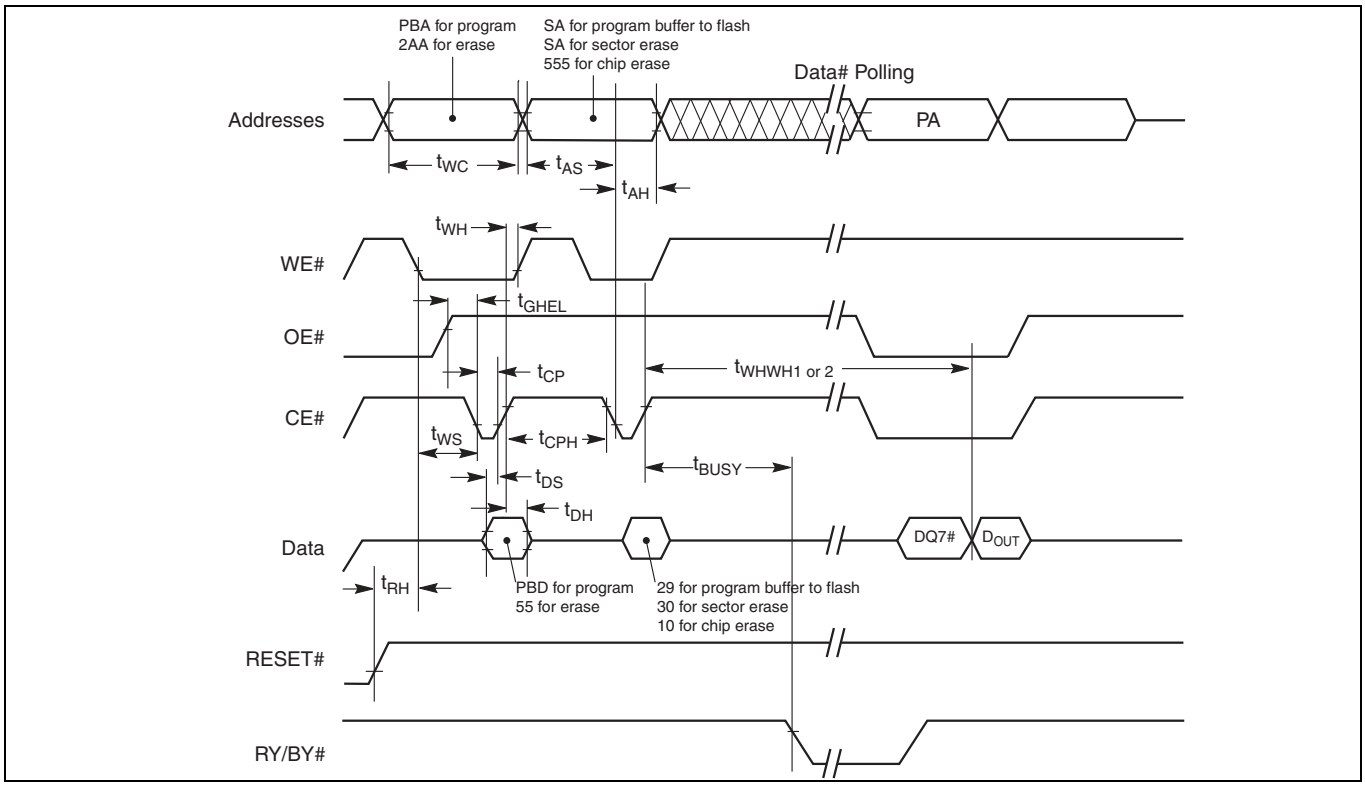


Figure 41 Alternate CE# Controlled Write (Erase / Program) operation timings

Notes
242.Word Configuration: Toggle A0, A1, and A2.
243.Byte Configuration: Toggle A1, A0, A2, and A3.
244.Figure indicates last two bus cycles of a program or erase operation.
245.PA = program address, SA = sector address, PD = program data.
246.DQ7# is the complement of the data written to the device. D_{OUT} is the data written to the device.
247.Illustration shows device in word mode.

16 Erase and programming performance

The Joint Electron Device Engineering Council (JEDEC) standard JESD22-A117 defines the procedural requirements for performing valid endurance and retention tests based on a qualification specification. This methodology is intended to determine the ability of a flash device to sustain repeated data changes without failure (program / erase endurance) and to retain data for the expected life (data retention). Endurance and retention qualification specifications are specified in JESD47 or may be developed using knowledge-based methods as in JESD94.

Table 78 Erase and programming performance for industrial temperature (–40°C to +85°C)

Parameter		Min	Typ [248]	Max [249]	Unit	Comments
Sector erase time	8 KB	–	235	1000	ms	Includes 00h programming prior to erasure [251]
	64 KB	–	300	1000		
Chip erase time [250]		–	38.4	65.4	s	
Single word programming time [250]		–	150	1200	µs	
Buffer program time [252]	2 byte [250]	–	150	1200	µs	Excludes system level overhead [253]
	32 byte [250]	–	200	1200		
	64 byte [250]	–	220	1200		
	128 byte [250]	–	300	1200		
	256 byte	–	400	1200		
Effective write buffer program operation per word	256 byte	–	3.125	–	µs	
Total accelerated effective write buffer program time	32 byte [250]	–	200	1200	µs	
	64 byte	–	220	1200		
Effective accelerated write buffer program operation per word	64 byte	–	6.9	–	µs	
Chip program time for a 128-word / 256-byte write buffer operation [250]		–	13.11	–	s	
Erase Suspend / Erase Resume (t_{ESL})		–	–	30	µs	
Program Suspend / Program Resume (t_{PSL})		–	–	23.5	µs	
Erase Resume to next Erase Suspend (t_{ERS})		–	100	–	µs	Minimum of 60 ns but ≥ typical periods are needed for erase to progress to completion.
Program Resume to next Program Suspend (t_{PRS})		–	100	–	µs	Minimum of 60 ns but ≥ typical periods are needed for program to progress to completion.
Evaluate Erase Status (t_{EES})		–	25	30	µs	

Notes

248. Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0V, 10,000 cycles; random data pattern.
249. Under worst case conditions of 90°C; Worst case V_{CC}, 100,000 cycles, random pattern.
250. Not 100% tested.
251. In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.
252. Write buffer Programming time is calculated on a per-word / per-byte basis for a 128-word / 256-byte write buffer operation.
253. System-level overhead is the time required to execute the command sequence(s) for the program command. See **Table 23** and **Table 25** for further information on command definitions.

Table 79 Erase and programming performance for industrial plus temperature (–40°C to +105°C)

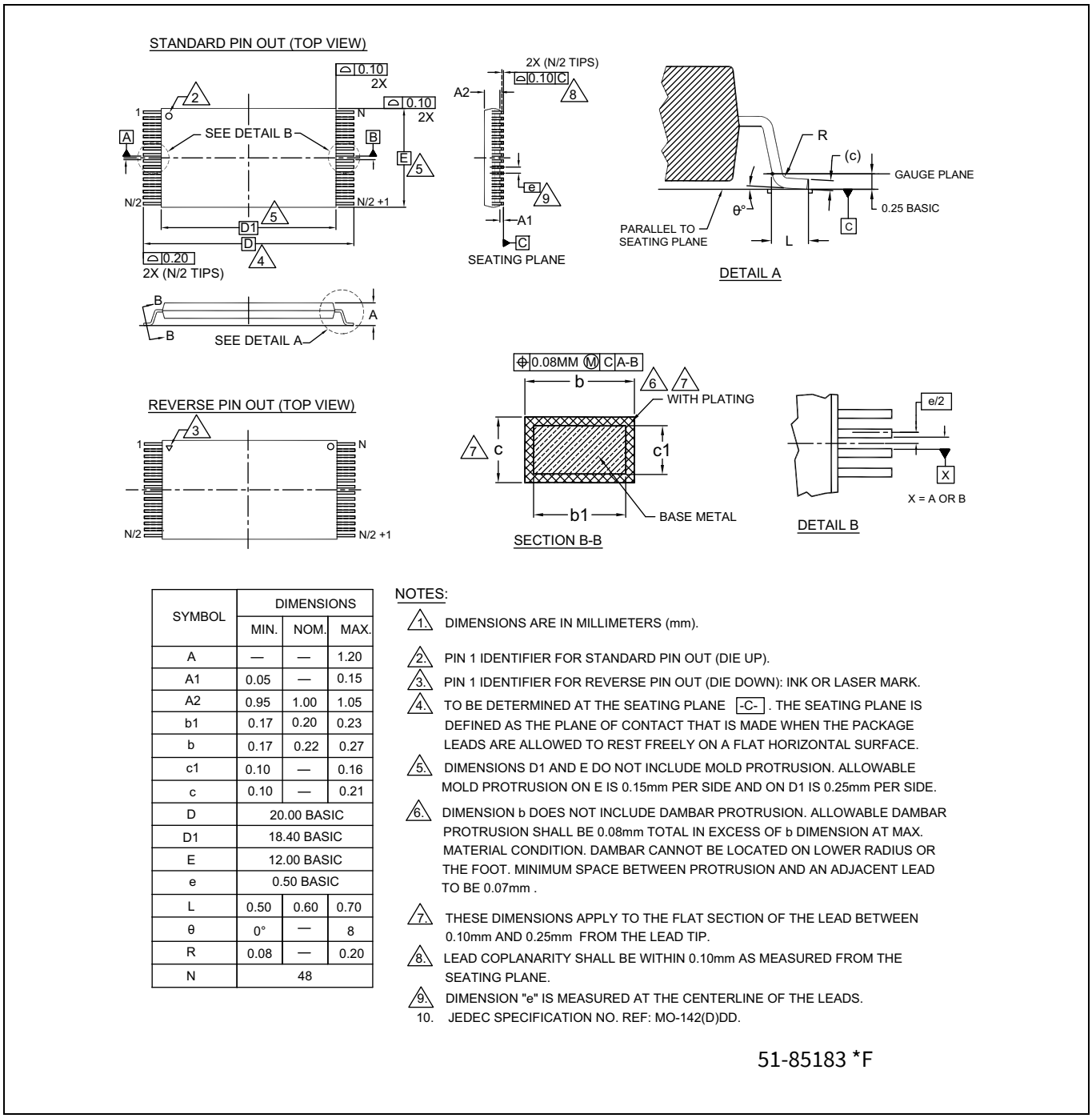
Parameter		Min	Typ [254]	Max [255]	Unit	Comments
Sector erase time	8 KB	–	235	1000	ms	Includes 00h programming prior to erasure [257]
	64 KB	–	300	1000		
Chip erase time [256]		–	38.4	65.4	s	
Single word programming time [256]		–	150	1200	µs	
Buffer program time [258]	2 byte [256]	–	150	1200	µs	Excludes system level overhead [259]
	32 byte [256]	–	200	1200		
	64 byte [256]	–	220	1200		
	128 byte [256]	–	300	1200		
	256 byte [256]	–	400	1200		
Effective write buffer program operation per word	256 byte	–	3.125	–	µs	
Total accelerated effective write buffer program time	32 byte [256]	–	200	1200	µs	
	64 byte	–	220	1200		
Effective accelerated write buffer program operation per word	64 byte	–	6.9	–	µs	
Chip program time for a 128-word / 256-byte write buffer operation [256]		–	13.11	–	s	
Erase Suspend / Erase Resume (t_{ESL})		–	–	30	µs	
Program Suspend / Program Resume (t_{PSL})		–	–	23.5	µs	
Erase Resume to next Erase Suspend (t_{ERS})		–	100	–	µs	Minimum of 60 ns but ≥ typical periods are needed for erase to progress to completion.
Program Resume to next Program Suspend (t_{PRS})		–	100	–	µs	Minimum of 60 ns but ≥ typical periods are needed for program to progress to completion.
Evaluate Erase Status (t_{EES})		–	25	30	µs	

Notes

254. Typical program and erase times assume the following conditions: 25°C, V_{CC} = 3.0 V, 10,000 cycles; random data pattern.
255. Under worst case conditions of 110°C; Worst case V_{CC}, 100,000 cycles, random pattern.
256. Not 100% tested.
257. In the pre-programming step of the Embedded Erase algorithm, all bits are programmed to 00h before erasure.
258. Write buffer Programming time is calculated on a per-word / per-byte basis for a 128-word / 256-byte write buffer operation.
259. System-level overhead is the time required to execute the command sequence(s) for the program command. See **Table 23** and **Table 25** for further information on command definitions.

17 Package diagrams

17.1 TS048 — 48-pin standard thin small outline package (TSOP)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	12.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	48		

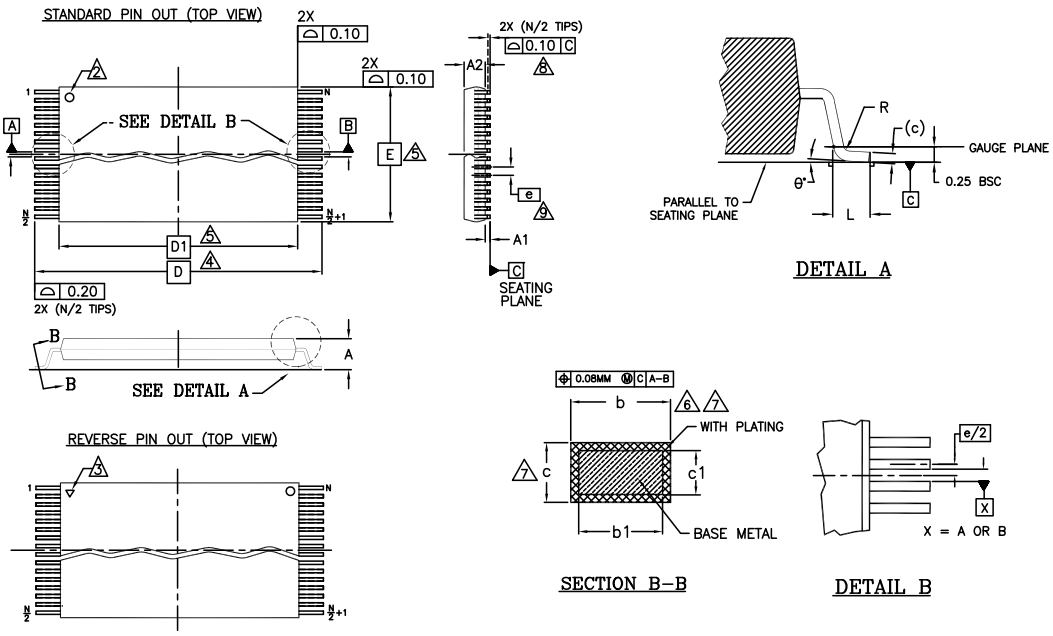
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)DD.

51-85183 *F

Figure 42 48-pin TSOP (18.4 × 12.0 × 1.2 mm) package outline, 51-85183

17.2 TS056 — 56-pin standard thin small outline package (TSOP)



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.05	—	0.15
A2	0.95	1.00	1.05
b1	0.17	0.20	0.23
b	0.17	0.22	0.27
c1	0.10	—	0.16
c	0.10	—	0.21
D	20.00 BASIC		
D1	18.40 BASIC		
E	14.00 BASIC		
e	0.50 BASIC		
L	0.50	0.60	0.70
θ	0°	—	8
R	0.08	—	0.20
N	56		

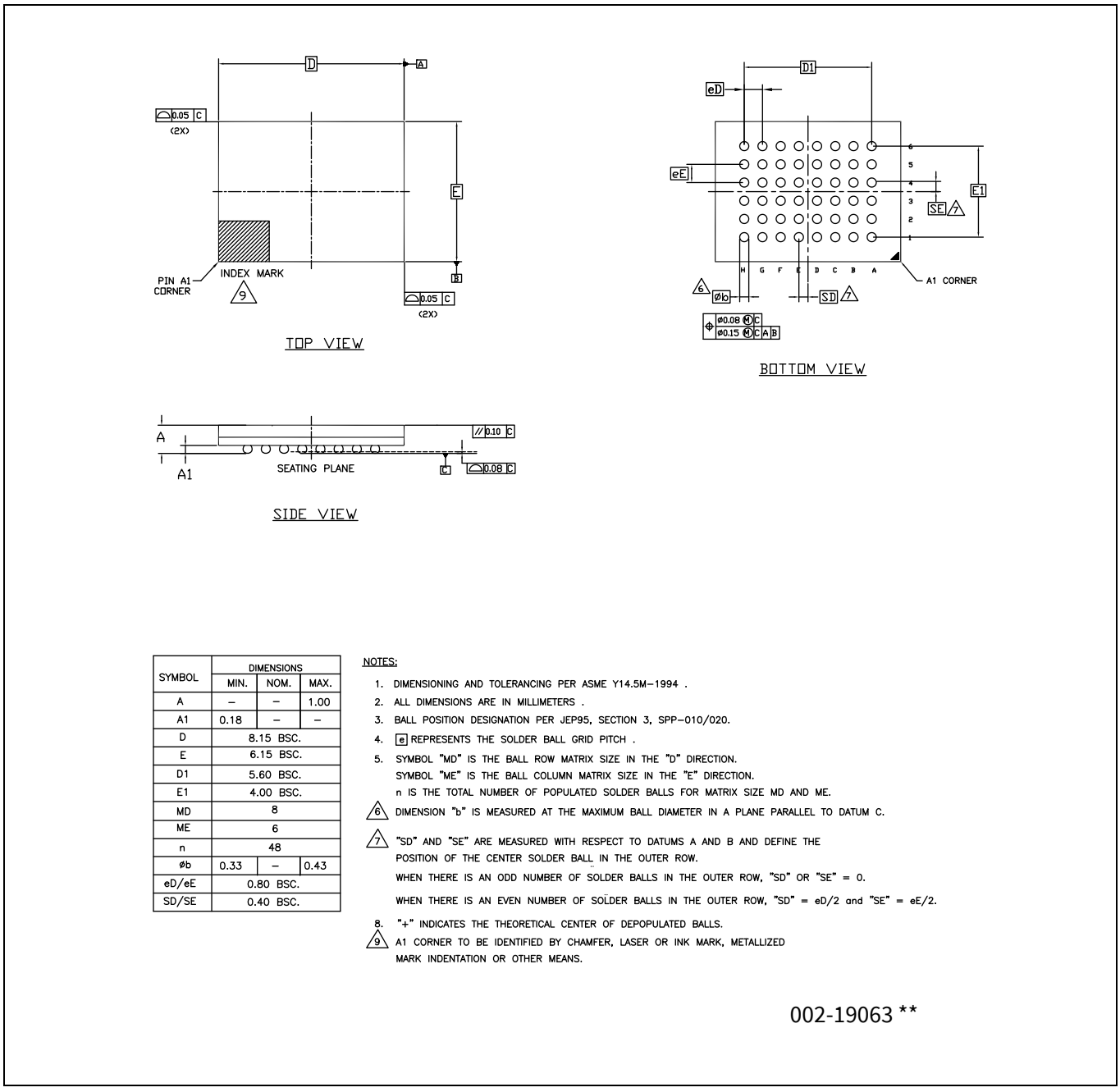
NOTES:

1. DIMENSIONS ARE IN MILLIMETERS (mm).
2. PIN 1 IDENTIFIER FOR STANDARD PIN OUT (DIE UP).
3. PIN 1 IDENTIFIER FOR REVERSE PIN OUT (DIE DOWN): INK OR LASER MARK.
4. TO BE DETERMINED AT THE SEATING PLANE -C- . THE SEATING PLANE IS DEFINED AS THE PLANE OF CONTACT THAT IS MADE WHEN THE PACKAGE LEADS ARE ALLOWED TO REST FREELY ON A FLAT HORIZONTAL SURFACE.
5. DIMENSIONS D1 AND E DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE MOLD PROTRUSION ON E IS 0.15mm PER SIDE AND ON D1 IS 0.25mm PER SIDE.
6. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08mm TOTAL IN EXCESS OF b DIMENSION AT MAX. MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND AN ADJACENT LEAD TO BE 0.07mm .
7. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10mm AND 0.25mm FROM THE LEAD TIP.
8. LEAD COPLANARITY SHALL BE WITHIN 0.10mm AS MEASURED FROM THE SEATING PLANE.
9. DIMENSION "e" IS MEASURED AT THE CENTERLINE OF THE LEADS.
10. JEDEC SPECIFICATION NO. REF: MO-142(D)EC.

002-15549 *B

Figure 43 56-pin TSOP (18.4 × 14.0 × 1.2 mm) package outline, 002-15549

17.3 VBK048 — 48-ball fine-pitch ball grid array (BGA) 8.15 × 6.15 mm package



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	–	–	1.00
A1	0.18	–	–
D	8.15 BSC.		
E	6.15 BSC.		
D1	5.60 BSC.		
E1	4.00 BSC.		
MD	8		
ME	6		
n	48		
øb	0.33	–	0.43
eD/eE	0.80 BSC.		
SD/SE	0.40 BSC.		

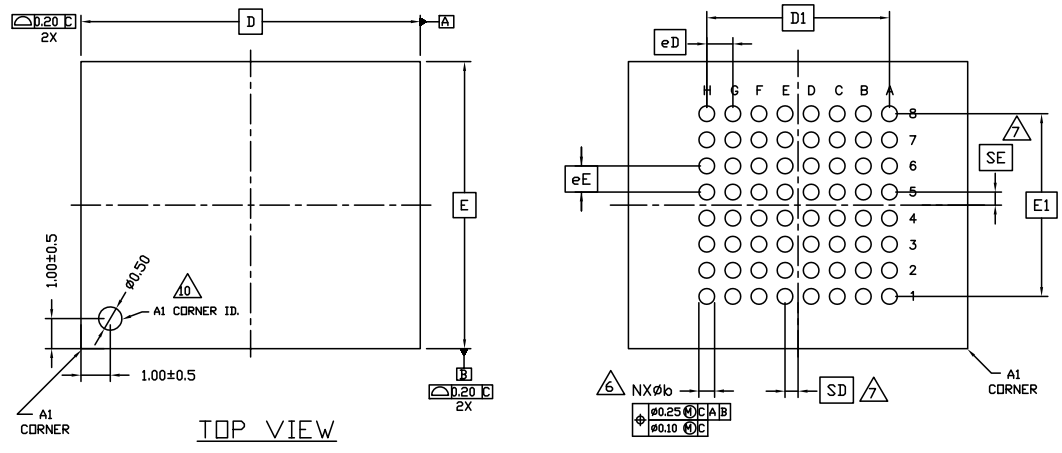
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JEP95, SECTION 3, SPP–010/020.
4. [e] REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   n IS THE TOTAL NUMBER OF POPULATED SOLDER BALLS FOR MATRIX SIZE MD AND ME.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 and "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-19063 **

Figure 44 48-ball VFBGA (8.15 × 6.15 × 1.00 mm) package outline, 002-19063

17.4 LAA064 — 64-ball fortified ball grid array (BGA) 13 × 11 mm package



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.40
A1	0.40	-	-
A2	0.60	-	-
D	13.00 BSC.		
E	11.00 BSC.		
D1	7.00 BSC.		
E1	7.00 BSC.		
MD	8		
ME	8		
N	64		
Øb	0.50	0.60	0.70
eD	1.00 BSC.		
eE	1.00 BSC.		
SD/SE	0.50 BSC.		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JEP95 SECTION 3, SPP-020 (RECTANGULAR) OR SPP-010 (SQUARE).
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE TOTAL NUMBER OF SOLDER BALLS.

6 DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C .

7 "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.

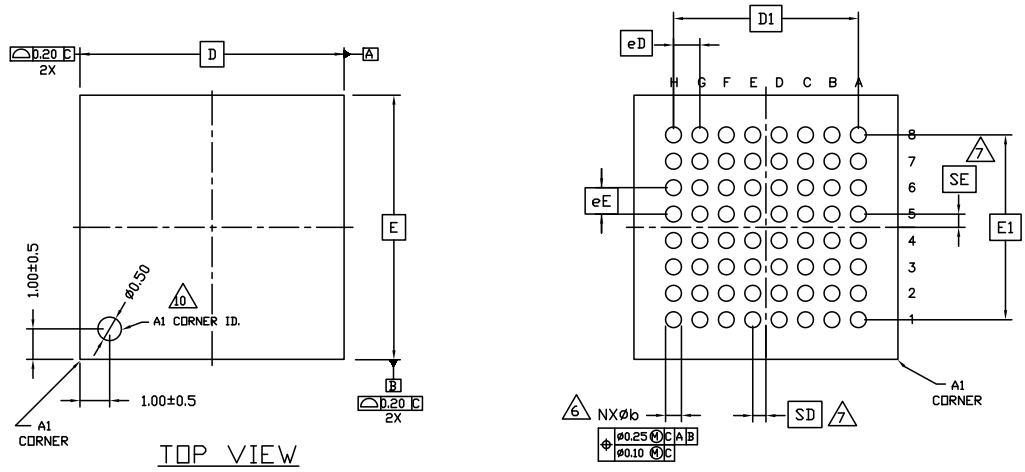
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.

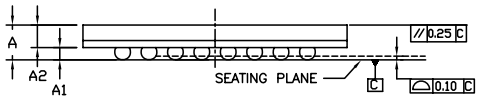
9 A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

002-15536 **

Figure 45 64-ball FBGA (13.0 × 11.0 × 1.4 mm) package outline, 002-15536

17.5 LAE064 — 64-ball fortified ball grid array (BGA) 9 × 9 mm package





SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	-	-	1.40
A1	0.40	-	-
A2	0.60	-	-
D	9.00 BSC.		
E	9.00 BSC.		
D1	7.00 BSC.		
E1	7.00 BSC.		
MD	8		
ME	8		
N	64		
Øb	0.50	0.60	0.70
eD	1.00 BSC.		
eE	1.00 BSC.		
SD/SE	0.50 BSC.		

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994 .
2. ALL DIMENSIONS ARE IN MILLIMETERS .
3. BALL POSITION DESIGNATION PER JEP95 SECTION 3, SPP-020 (RECTANGULAR) OR SPP-010 (SQUARE).
4. e REPRESENTS THE SOLDER BALL GRID PITCH .
5. SYMBOL "MD" IS THE BALL ROW MATRIX SIZE IN THE "D" DIRECTION.
   SYMBOL "ME" IS THE BALL COLUMN MATRIX SIZE IN THE "E" DIRECTION.
   N IS THE TOTAL NUMBER OF SOLDER BALLS.
6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C .
7. "SD" AND "SE" ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.
   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" OR "SE" = 0.
   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, "SD" = eD/2 AND "SE" = eE/2.
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.
10. JEDEC SPECIFICATION NO. REF : N/A

002-15537 *A

Figure 46 64-ball FBGA (9.0 × 9.0 × 1.4 mm) package outline, 002-15537

18 Ordering information

Standard products are available in several packages and operating ranges. The order number (valid combination) is formed by a combination of the following:

S29GL064S 70 T F I 01 0

Packing type
0 = Tray
3 = 13-inch tape and reel

Model number
01 = ×8/×16, V_{CC} = V_{IO} = 2.7 V–3.6 V, uniform sector, WP#/ACC = V_{IL} protects highest addressed sector
02 = ×8/×16, V_{CC} = V_{IO} = 2.7 V–3.6 V, uniform sector, WP#/ACC = V_{IL} protects lowest addressed sector
03 = ×8/×16, V_{CC} = V_{IO} = 2.7 V–3.6 V, top boot sector, WP#/ACC = V_{IL} protects top two addressed sectors[260]
04 = ×8/×16, V_{CC} = V_{IO} = 2.7 V–3.6 V, bottom boot sector, WP#/ACC = V_{IL} protects bottom two addressed sectors[260]
06 = ×16, V_{CC} = V_{IO} = 2.7 V–3.6 V, uniform sector, WP# = V_{IL} protects highest addressed sector
07 = ×16, V_{CC} = V_{IO} = 2.7 V–3.6 V, uniform sector, WP# = V_{IL} protects lowest addressed sector
V1 = ×8/×16, V_{CC} = 2.7 V–3.6 V, V_{IO} = 1.65 V–3.6 V, uniform sector, WP#/ACC = V_{IL} protects highest addressed sector
V2 = ×8/×16, V_{CC} = 2.7 V–3.6 V, V_{IO} = 1.65 V–3.6 V, uniform sector, WP#/ACC = V_{IL} protects lowest addressed sector
V6 = ×16, V_{CC} = 2.7 V–3.6 V, V_{IO} = 1.65 V–3.6 V, uniform sector, WP# = V_{IL} protects highest addressed sector
V7 = ×16, V_{CC} = 2.7 V–3.6 V, V_{IO} = 1.65 V–3.6 V, uniform sector, WP# = V_{IL} protects lowest addressed sector

Temperature range
I = Industrial (–40°C to +85°C)
V = Industrial Plus (–40°C to +105°C)
A = Automotive, AEC-Q100 grade 3 (–40°C to +85°C)
B = Automotive, AEC-Q100 grade 2 (–40°C to +105°C)

Package material set
F = Halogen-free, lead (Pb)-free[261]
H = Halogen-free, lead (Pb)-free[261]

Package type
B = Fine-pitch ball-grid array package (VBK048), 8.15 mm × 6.16 mm
D = Fortified ball-grid array package (LAE064), 9 mm × 9 mm
F = Fortified ball-grid array package (LAA064), 13 mm × 11 mm
T = Thin small outline package (TSOP) standard pinout

Speed option
See product selector guide and valid combinations (70 = 70 ns, 80 = 80 ns, 90 = 90 ns)

Device number / description
S29GL064S, 64-Mb Page-Mode flash memory
Manufactured using 65-nm MIRRORBIT™ Process Technology, 3.0 Volt-Only Read, Program, and Erase

Notes
260.V_{IO} is tied internally to V_{CC}.
261.Halogen-free definition is in accordance with IEC 61249-2-21 specification.

18.1 Valid combinations

Valid combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations. **Table 80** and **Table 81** list configurations that are standard units and automotive grade / AEC-Q100 qualified units.

Production part approval process (PPAP) support is only provided for AEC-Q100 grade products.

Products to be used in end-use applications that require ISO/TS-16949 compliance must be AEC-Q100 grade products in combination with PPAP. Non–AEC-Q100 grade products are not manufactured or documented in full compliance with ISO/TS-16949 requirements. AEC-Q100 grade products are also offered without PPAP support for end-use applications that do not require ISO/TS-16949 compliance.

Table 80 S29GL064S valid combinations - Industrial (–40°C to +85°C)

Device number	Speed option	Package, material, and temperature range	Model number	Packing type	Package description	
S29GL064S	70	TFI, TFA	03, 04, 06, 07	0, 3 [262]	TS048 [263]	TSOP
	80		V6, V7			
	70		01, 02		TS056 [263]	
	80		V1, V2			
	70	BHI, BHA	03, 04		VBK048 [264]	Fine-pitch BGA
	70	FHI, FHA	01, 02, 03, 04		LAA064 [264]	Fortified BGA
	80		V1, V2			
	70	DHI, FHA	01, 02, 03, 04		LAE064 [264]	
	80		V1, V2			

Table 81 S29GL064S valid combinations - Industrial Plus (–40°C to +105°C)

Device number	Speed option	Package, material, and temperature range	Model number	Packing type	Package description	
S29GL064S	80	TFV, TFB	03, 04, 06, 07	0, 3 [262]	TS048 [263]	TSOP
	90		V6, V7			
	80		01, 02		TS056 [263]	
	90		V1, V2			
	80	BHV, BHB	03, 04		VBK048 [264]	Fine-pitch BGA
	80	FHV, FHB	01, 02, 03, 04		LAA064 [264]	Fortified BGA
	90		V1, V2			
	80	DHV, DHB	01, 02, 03, 04		LAE064 [264]	
	90		V1, V2			

Notes

262.Type 0 is standard. Specify others as required.
263.TSOP package marking omits packing type designator from ordering part number.
264.BGA package marking omits leading S29 and packing type designator from ordering part number.

Revision history

Document revision	Date	Description of changes
**	2013-12-11	Initial release.
*A	2014-03-11	**Global:** Changed data sheet status from *Advance Information* to *Preliminary*
*B	2014-04-16	**Common Flash Memory Interface (CFI):** Corrected values for Addresses (x16) 22h, 26h, 2Ah, 45h Clarified values for Addresses (x16) 4Eh and 2Eh
*C	2014-11-26	**Global:** Changed 'Automotive In-Cabin' Temperature Range to 'Industrial Plus' Temperature Range. **Common Flash Memory Interface (CFI):** System Interface String table: updated values for Addresses (x16) 21h, 22h, 25h, 26h **Command Definitions:** Sector Protection Commands (x16) table: corrected 'Password Protection' Addr value to '00' **Power-On Reset (POR) and Warm Reset:** Power-On and Reset Parameters table: corrected Value for T_{RPH} **Erase and Programming Performance:** Erase and Programming Performance for Industrial Temperature (-40°C to +85°C) table: updated Erase Times Erase and Programming Performance for In Cabin Temperature (-40°C to +105°C) table: updated Erase Times **AC Characteristics:** Added Notes to Figures 15.1 - 15.3, 15.5 - 15.10, 15.17 - 15.19
*D	2015-08-13	Updated to Cypress template.
*E	2017-01-04	Changed status from Preliminary to Final. Added ECC related information in all instances across the document. Added "Automotive AEC-Q100 Grade 3" and "Automotive AEC-Q100 Grade 2" Temperature Range related information in all instances across the document. Updated **Ordering information**: Added Automotive AEC-Q100 Grade 2 and Automotive AEC-Q100 Grade 3 Temperature Range details. Updated **Valid combinations**: Added Automotive AEC-Q100 Grade 2 and Automotive AEC-Q100 Grade 3 Temperature Range details. Added "Other resources". Updated **Device bus operations**: Added **Automatic ECC**. Updated **Command definitions**: Added **ECC Status ASO**. Added **Data integrity**. Updated **Electrical specifications**: Added **Thermal resistance**. Updated **Erase and programming performance**: Updated **Table 78**. Updated **Table 79**. Completing Sunset Review.
*F	2017-06-08	Updated Cypress Logo and Copyright.

Revision history

Document revision	Date	Description of changes
*G	2017-10-30	Updated **Device bus operations**: Updated **Automatic ECC**: Updated **Write buffer programming**: Updated description. Updated to new template. Completing Sunset Review.
*H	2018-08-03	Updated **Ordering information**: Updated details corresponding to “F” and “H” under “Package Materials Set” in the diagram. Added a note “Halogen free definition is in accordance with IEC 61249-2-21 specification” and referred the same note in “F” and “H”. Updated **Command definitions**: Updated **Command definitions**: Updated **Table 25**: Updated Note 65. Updated to new template.
*I	2022-07-28	Removed “Other resources”. Updated **Data integrity**: Updated **Data retention**: Updated description. Updated **Electrical specifications**: Updated **Thermal resistance**: Updated **Table 60**. Updated **Package diagrams**: Replaced “Physical dimensions” with “Package diagrams” in heading. Updated **TS048 — 48-pin standard thin small outline package (TSOP)**: Replaced existing diagram with spec 51-85183 *F. Updated **TS056 — 56-pin standard thin small outline package (TSOP)**: Replaced existing diagram with spec 002-15549 *B. Updated **VBK048 — 48-ball fine-pitch ball grid array (BGA) 8.15 × 6.15 mm package**: Replaced existing diagram with spec 002-19063 **. Updated **LAA064 — 64-ball fortified ball grid array (BGA) 13 × 11 mm package**: Replaced existing diagram with spec 002-15536 **. Updated **LAE064 — 64-ball fortified ball grid array (BGA) 9 × 9 mm package**: Replaced existing diagram with spec 002-15537 *A. Migrated to Infineon template.

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