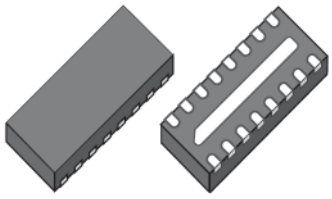
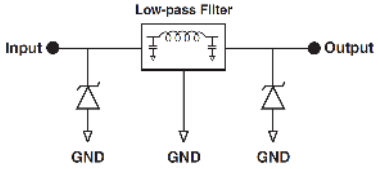
EMIF08-LCD04M16

Datasheet

8-line L-C IPAD EMI filter and ESD protection in micro QFN package



Micro QFN
3.3 x 1.35 16L



Product status
EMIF08-LCD04M16

Features

- High cut off frequency low-pass filter: F_C = 400 MHz at -6 dB
- High efficiency in EMI filtering: better than -35 dB from 900 MHz to 2 GHz
- Very low PCB space consuming with plastic micro-package 3.3 x 1.35 mm
- Very thin package: 0.55 mm max.
- High efficiency in ESD (IEC 61000-4-2 level 4)
- High reliability offered by monolithic integration
- High reduction of parasitic elements through integration and µQFN packaging
- ECOPACK2 compliant

Complies with the following standards

- IEC 61000-4-2, level 4 on external pins:
  - ±15 kV (air discharge)
  - ±8 kV (contact discharge)

Applications

Where EMI filtering in ESD sensitive equipment is required:

- Mobile POS
- Human machine interface (HMI): STEVAL-PLC001V1
- Home automation HMI

Description

The EMIF08-LCD04M16 is an 8-line inductor capacitor (LC) EMI filter designed to suppress EMI/RFI noise in all systems subjected to electromagnetic interferences requiring a large bandwidth.

This filter includes an ESD protection circuitry, which prevents damage to the application when subjected to ESD surges up 15 kV contact discharge.

1 Characteristics

Figure 1. Pin configuration

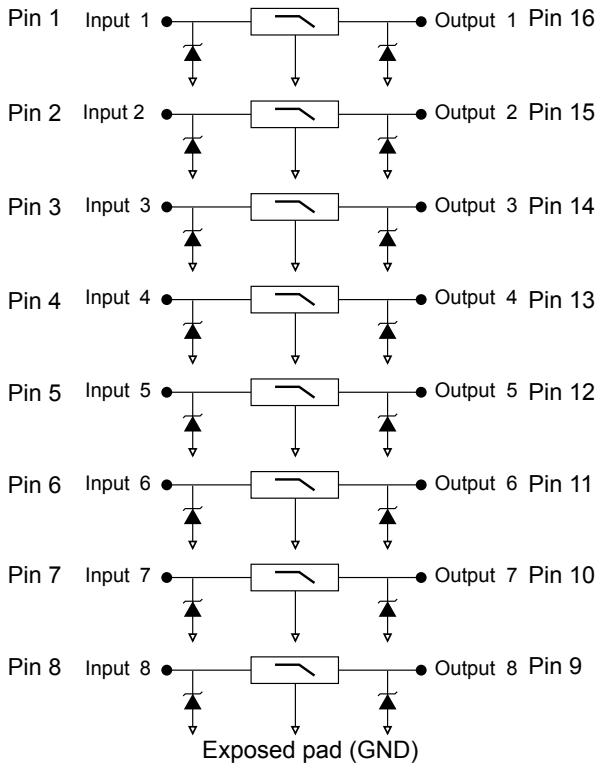


Table 1. Absolute maximum ratings (T_{amb} = 25 °C)

Symbol	Parameter	Value	Unit
V_{PP}	ESD IEC 61000-4-2, contact discharge:	±15	kV
T_j	Maximum junction temperature	125	°C
T_{op}	Operating temperature range	- 40 to + 85	°C
T_{stg}	Storage temperature range	- 55 to + 150	°C

Figure 2. Electrical characteristics (definitions)

Symbol	Parameter
V_{BR}	Breakdown voltage
I_{RM}	Leakage current at VRM
V_{RM}	Stand-off voltage
V_{CL}	Clamping voltage
R_d	Dynamic resistance
I_{PP}	Peak pulse current
$R_{I/O}$	Series resistance between Input and Output
C_{line}	Input capacitance per line

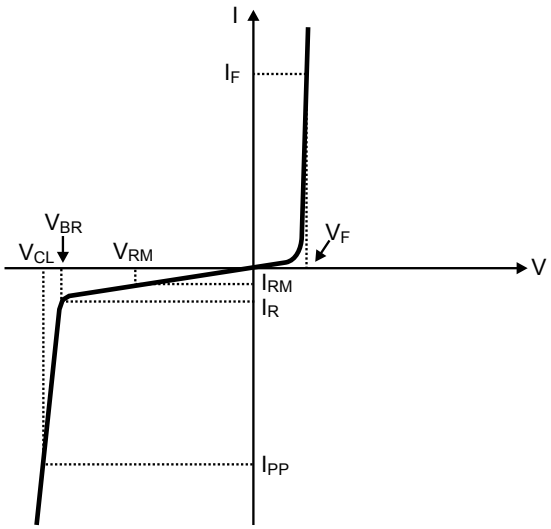


Table 2. Electrical characteristics (T_{amb} = 25 °C)

Symbol	Test conditions	Min.	Typ.	Max.	Unit
V_{BR}	I_R = 1 mA	6			V
I_{RM}	V_{RM} = 3 V per line			100	nA
L	Inductance		12		nH
R	Parasitic resistance of the inductance	9	12.5	20	Ω
F_C	50 Ω source and 50 Ω load termination at -6 dB		400		MHz
C_{line}	V_R = 3 V dc, V_{OSC} = 30 mV, F = 1 MHz	17	18	19	pF

1.1 Characteristics (curves)

Figure 3. S21 attenuation measurements

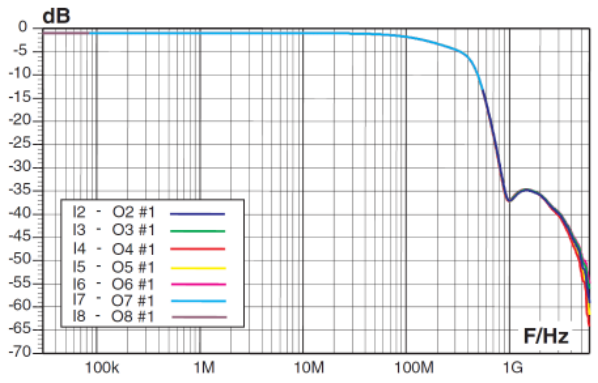


Figure 4. Analog cross talk measurements

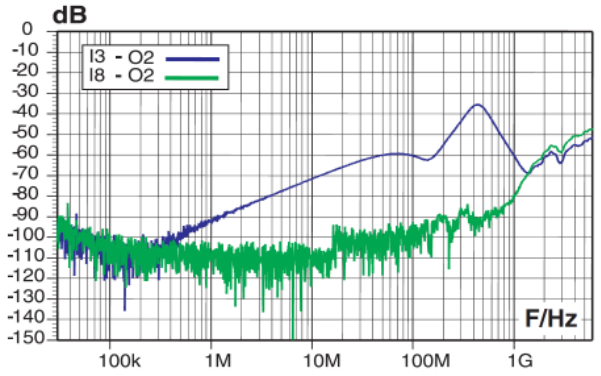


Figure 5. ESD response to IEC 61000-4-2 (+15 kV air discharge)

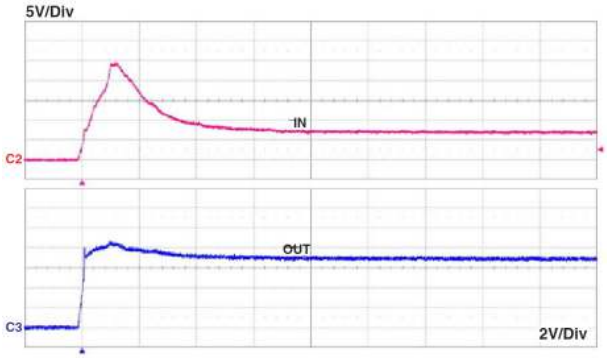


Figure 6. ESD response to IEC 61000-4-2 (-15 kV air discharge)

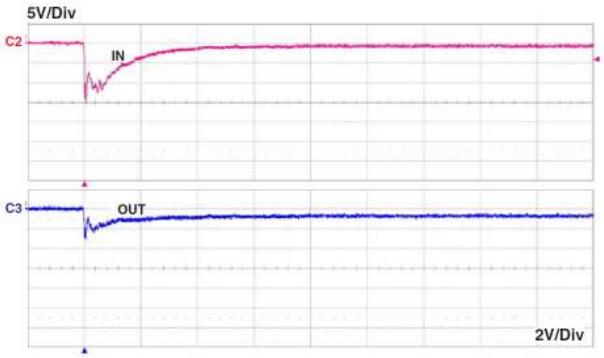
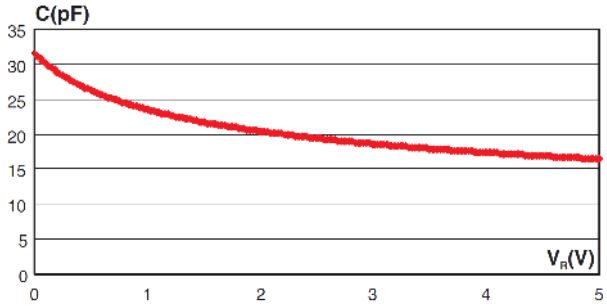


Figure 7. Line capacitance versus applied voltage



2 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

2.1 Micro QFN-16L 3.5x1.35 mm package information

- Epoxy meets UL94, V0
- Lead-free package

Figure 8. Micro QFN-16L 3.5x1.35 mm package outline

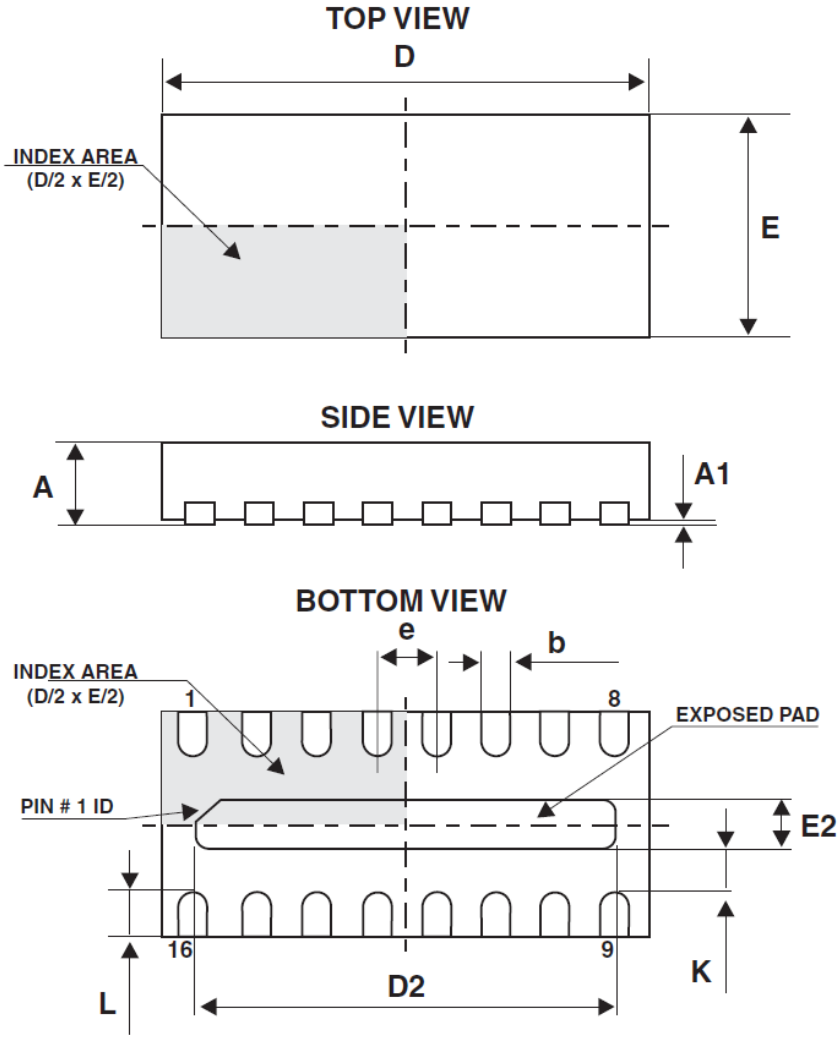


Table 3. Micro QFN-16L 3.5x1.35 mm mechanical data

Ref.	Dimensions					
	Millimeters					
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	0.45	0.50	0.55	0.018	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.0008	0.002
b	0.15	0.20	0.25	0.006	0.008	0.10
D		3.30			0.13	
D2	2.65	2.80	2.90	0.104	0.110	0.114
E		1.35			0.053	
E2	0.25	0.40	0.50	0.010	0.016	0.020
e		0.40			0.016	
k	0.20			0.008		
L	0.15	0.25	0.35	0.006	0.010	0.014

Figure 9. Footprint (dimensions in mm)

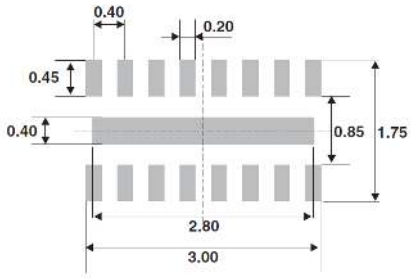
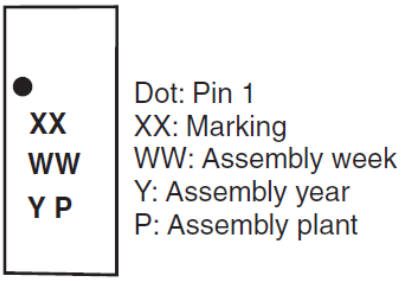


Figure 10. Marking



Note: Product marking may be rotated by 90° for assembly plant differentiation. In no case should this product marking be used to orient the component for its placement on a PCB. Only pin 1 mark is to be used for this purpose.

3 Recommendation on PCB assembly

3.1 Stencil opening design

1. General recommendation on stencil opening design
   a. Stencil opening dimensions: L (Length), W (Width), T (Thickness).
2. General design rule
   a. Stencil thickness (T) = 75 ~ 125 µm
   b. Aspect ratio = $\frac{W}{T} \geq 1.5$
   c. Aspect area = $\frac{L \times W}{2T(L + W)} \geq 0.66$
3. Reference design
   a. Stencil opening thickness: 100 µm
   b. Stencil opening for central exposed pad: Opening to footprint ratio is 50%.
   c. Stencil opening for leads: Opening to footprint ratio is 90%

Figure 11. Stencil opening dimensions

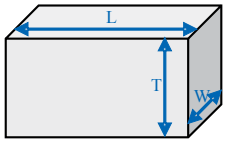
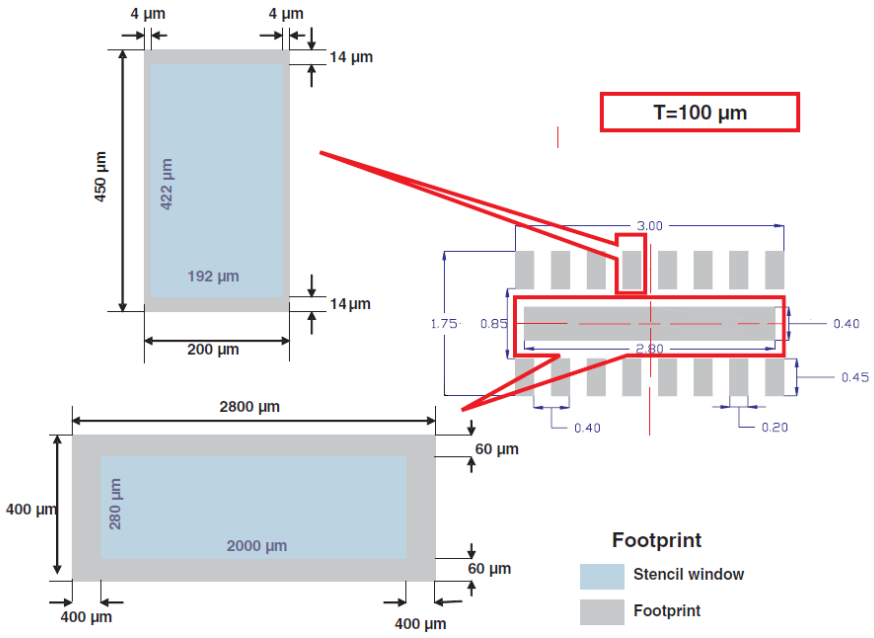


Figure 12. Recommended stencil window position



3.2 Solder paste

1. Halide-free flux qualification ROL0 according to ANSI/J-STD-004.
2. “No clean” solder paste is recommended.
3. Offers a high tack force to resist component movement during high speed.
4. Solder paste with fine particles: powder particle size is 20-45 µm.

3.3 Placement

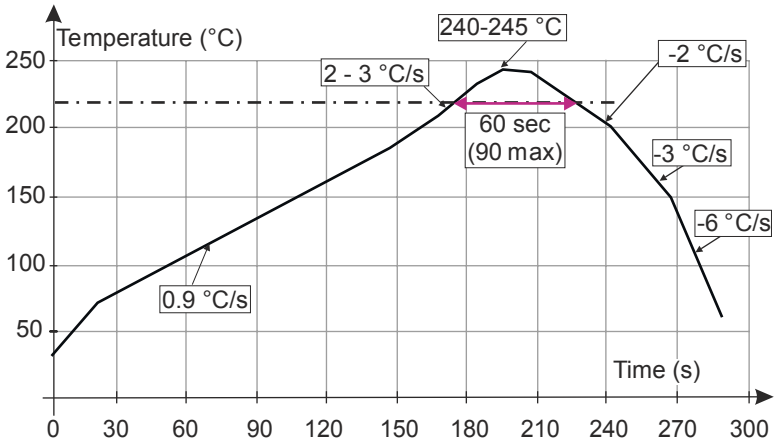
1. Manual positioning is not recommended.
2. It is recommended to use the lead recognition capabilities of the placement system, not the outline centering
3. Standard tolerance of ±0.05 mm is recommended.
4. 3.5 N placement force is recommended. Too much placement force can lead to squeezed out solder paste and cause solder joints to short. Too low placement force can lead to insufficient contact between package and solder paste that could cause open solder joints or badly centered packages.
5. To improve the package placement accuracy, a bottom side optical control should be performed with a high resolution tool.
6. For assembly, a perfect supporting of the PCB (all the more on flexible PCB) is recommended during solder paste printing, pick and place and reflow soldering by using optimized tools.

3.4 PCB design preference

1. To control the solder paste amount, the closed via is recommended instead of open vias.
2. The position of tracks and open vias in the solder area should be well balanced. A symmetrical layout is recommended, to avoid any tilt phenomena caused by asymmetrical solder paste due to solder flow away.

3.5 Reflow profile

Figure 13. ST ECOPACK recommended soldering reflow profile for PCB mounting



Note: Minimize air convection currents in the reflow oven to avoid component movement.

4 Ordering information

Figure 14. **Ordering information scheme**

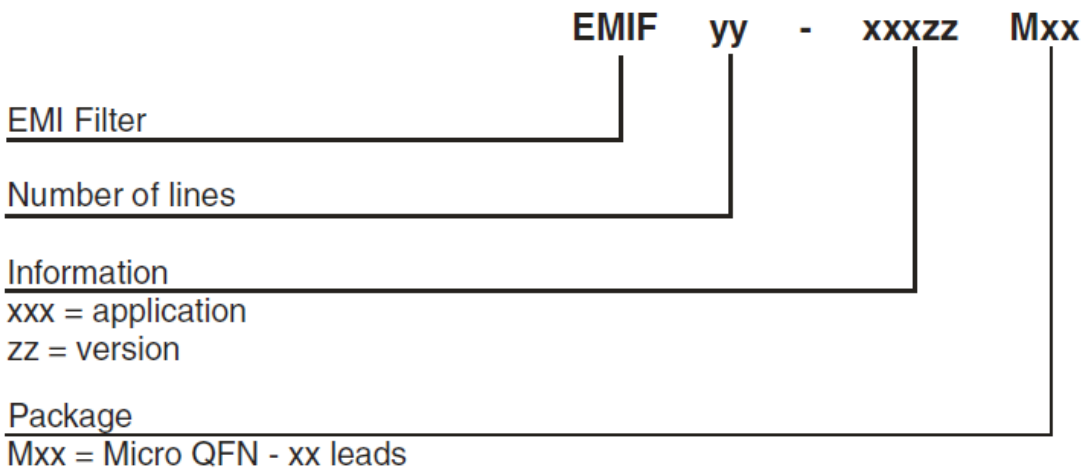


Table 4. **Ordering information**

Part number	Marking	Package	Weight	Base qty.	Delivery mode
EMIF08-LCD04M16	JA(1)	Micro QFN	6.74 mg	3000	Tape and reel

1. *The marking can be rotated by 90° to differentiate assembly location*

Revision history

Table 5. **Document revision history**

Date	Revision	Changes
20-May-2009	1	Initial release.
10-Nov-2009	2	Updated Features on page 1. Added Figure 2 on page 2.
14-Sep-2022	3	Added Figure 1. Pin configuration. Minor text changes.