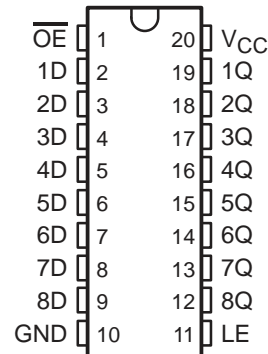


# CD74FCT573, CD74FCT573AT BiCMOS OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

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- BiCMOS Technology With Low Quiescent Power
- Buffered Inputs
- Input/Output Isolation From  $V_{CC}$
- Controlled Output Edge Rates
- 48-mA Output Sink Current
- Output Voltage Swing Limited to 3.7 V
- SCR Latch-Up-Resistant BiCMOS Process and Circuit Design
- 3-State Outputs Directly Drive Bus Lines
- Package Options Include Plastic Small-Outline (M) and Shrink Small-Outline (SM) Packages and Standard Plastic (E) DIP

CD74FCT573 . . . M OR SM PACKAGE  
CD74FCT573AT . . . E PACKAGE  
(TOP VIEW)



## description

The CD74FCT573 and CD74FCT573AT are octal, transparent, D-type latches, designed using a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output high level to two diode drops below  $V_{CC}$ . This resultant lowering of output swing (0 V to 3.7 V) reduces power-bus ringing [a source of electromagnetic interference (EMI)] and minimizes  $V_{CC}$  bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 48 mA.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ( $\overline{OE}$ ) input can be used to place the eight outputs in either a normal logic state (high or low) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

$\overline{OE}$  does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

The CD74FCT573 and CD74FCT573AT are characterized for operation from 0°C to 70°C.

**FUNCTION TABLE**  
(each latch)

INPUTS			OUTPUT
$\overline{OE}$	LE	D	Q
L	H	H	H
L	H	L	L
L	L	X	$Q_0$
H	X	X	Z



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**TEXAS  
INSTRUMENTS**

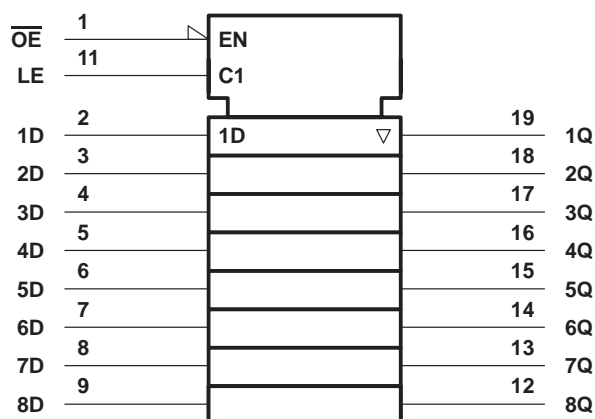
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# CD74FCT573, CD74FCT573AT BiCMOS OCTAL TRANSPARENT D-TYPE LATCHES WITH 3-STATE OUTPUTS

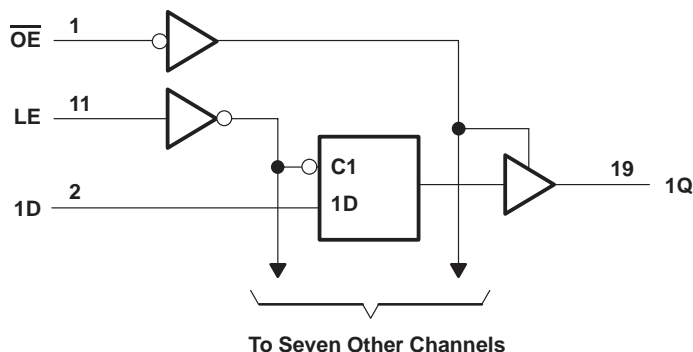
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## logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

## logic diagram (positive logic)



## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

DC supply voltage range, $V_{CC}$	.....	-0.5 V to 6 V
DC input clamp current, $I_{IK}$ ( $V_I < -0.5$ V)	.....	-20 mA
DC output clamp current, $I_{OK}$ ( $V_O < -0.5$ V)	.....	-50 mA
DC output sink current per output pin, $I_{OL}$	.....	70 mA
DC output source current per output pin, $I_{OH}$	.....	-30 mA
Continuous current through $V_{CC}$ , $I_{CC}$	.....	140 mA
Continuous current through GND	.....	400 mA
Package thermal impedance, $\theta_{JA}$ (see Note 1): E package	.....	69°C/W
M package	.....	58°C/W
SM package	.....	70°C/W
Storage temperature range, $T_{stg}$	.....	-65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The package thermal impedance is calculated in accordance with JESD 51.



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**CD74FCT573, CD74FCT573AT**  
**BiCMOS OCTAL TRANSPARENT D-TYPE LATCHES**  
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**recommended operating conditions (see Note 2)**

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	4.75	5.25	V
V <sub>IH</sub>	High-level input voltage	2		V
V <sub>IL</sub>	Low-level input voltage		0.8	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current		-15	mA
I <sub>OL</sub>	Low-level output current		48	mA
Δt/Δv	Input transition rise or fall rate	0	10	ns/V
T <sub>A</sub>	Operating free-air temperature	0	70	°C

NOTE 2: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)**

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
V <sub>IK</sub>	I <sub>I</sub> = -18 mA	4.75 V		-1.2		-1.2	V
V <sub>OH</sub>	I <sub>OH</sub> = -15 mA	4.75 V	2.4		2.4		V
V <sub>OL</sub>	I <sub>OL</sub> = 48 mA	4.75 V		0.55		0.55	V
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	5.25 V		±0.1		±1	μA
I <sub>OZ</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND	5.25 V		±0.5		±10	μA
I <sub>OS</sub> <sup>†</sup>	V <sub>I</sub> = V <sub>CC</sub> or GND, V <sub>O</sub> = 0	5.25 V		-60		-60	mA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.25 V		8		80	μA
ΔI <sub>CC</sub> <sup>‡</sup>	One input at 3.4 V, Other inputs at V <sub>CC</sub> or GND	5.25 V		1.6		1.6	mA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND			10		10	pF
C <sub>o</sub>	V <sub>O</sub> = V <sub>CC</sub> or GND			15		15	pF

<sup>†</sup> Not more than one output should be tested at a time, and the duration of the test should not exceed 100 ms.

<sup>‡</sup> This is the increase in supply current for each input at one of the specified TTL voltage levels rather than 0 V or V<sub>CC</sub>.

**timing requirements over recommended operating temperature conditions (unless otherwise noted) (see Figure 1)**

			CD74FCT573		CD74FCT573AT		UNIT
			MIN	MAX	MIN	MAX	
t <sub>w</sub>	Pulse duration	LE high	6		5		ns
t <sub>su</sub>	Setup time	Data before LE↓	2		2		ns
t <sub>h</sub>	Hold time	Data after LE↓	1.5		1.5		ns



**CD74FCT573, CD74FCT573AT**  
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**WITH 3-STATE OUTPUTS**

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switching characteristics over recommended operating conditions,  $T_A = 25^\circ\text{C}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	CD74FCT573			CD74FCT573AT			UNIT
			$T_A = 25^\circ\text{C}$			$T_A = 25^\circ\text{C}$			
			TYP	MIN	MAX	TYP	MIN	MAX	
$t_{pd}$	D	Q	5	1.5	8	3.9	1.5	5.7	ns
	LE		9	2	13	4.4	2	7	
$t_{en}$	$\overline{OE}$	Q	7	1.5	12	6	1.5	8	ns
$t_{dis}$	$\overline{OE}$	Q	6	1.5	7.5	4	1.5	5.8	ns

noise characteristics,  $V_{CC} = 5\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$

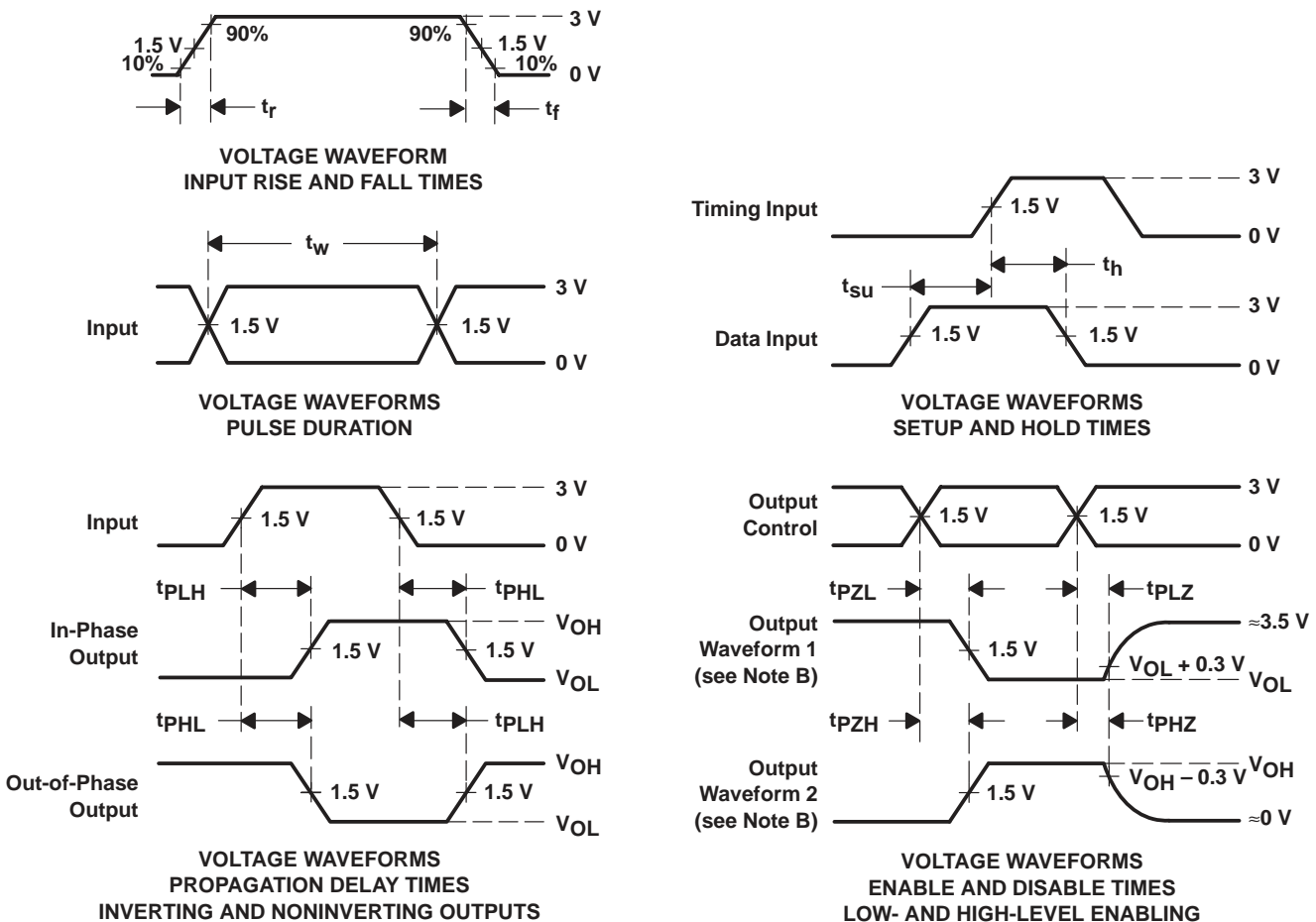
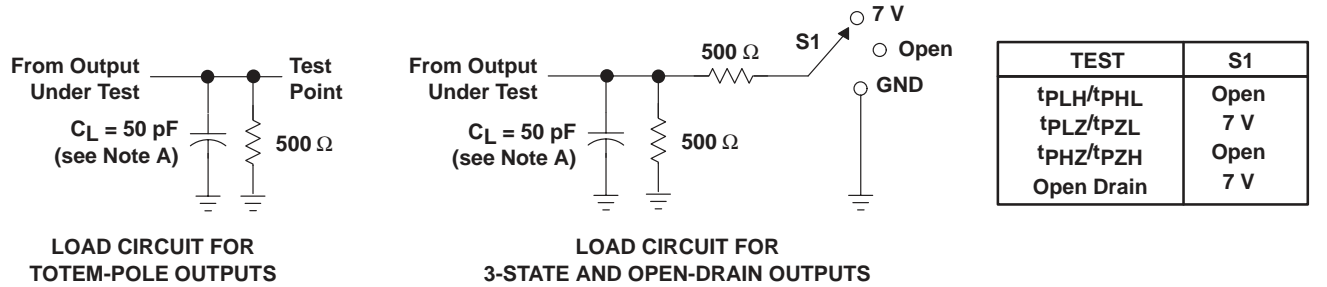
PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		1		V
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		0.5		V
$V_{IH(D)}$	High-level dynamic input voltage		2		V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

operating characteristics,  $V_{CC} = 5\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	No load, $f = 1\text{ MHz}$	34	pF



PARAMETER MEASUREMENT INFORMATION



- NOTES: A.  $C_L$  includes probe and jig capacitance.  
 B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.  
 C. All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r$  and  $t_f = 2.5 \text{ ns}$ .  
 D. The outputs are measured one at a time with one input transition per measurement.  
 E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .  
 F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .  
 G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
CD74FCT573ATE	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
CD74FCT573E	OBSOLETE	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
CD74FCT573M	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
CD74FCT573M96	OBSOLETE	SOIC	DW	20		TBD	Call TI	Call TI	0 to 70		
CD74FCT573SM	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	0 to 70		
CD74FCT573SM96	OBSOLETE	SSOP	DB	20		TBD	Call TI	Call TI	0 to 70		

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.

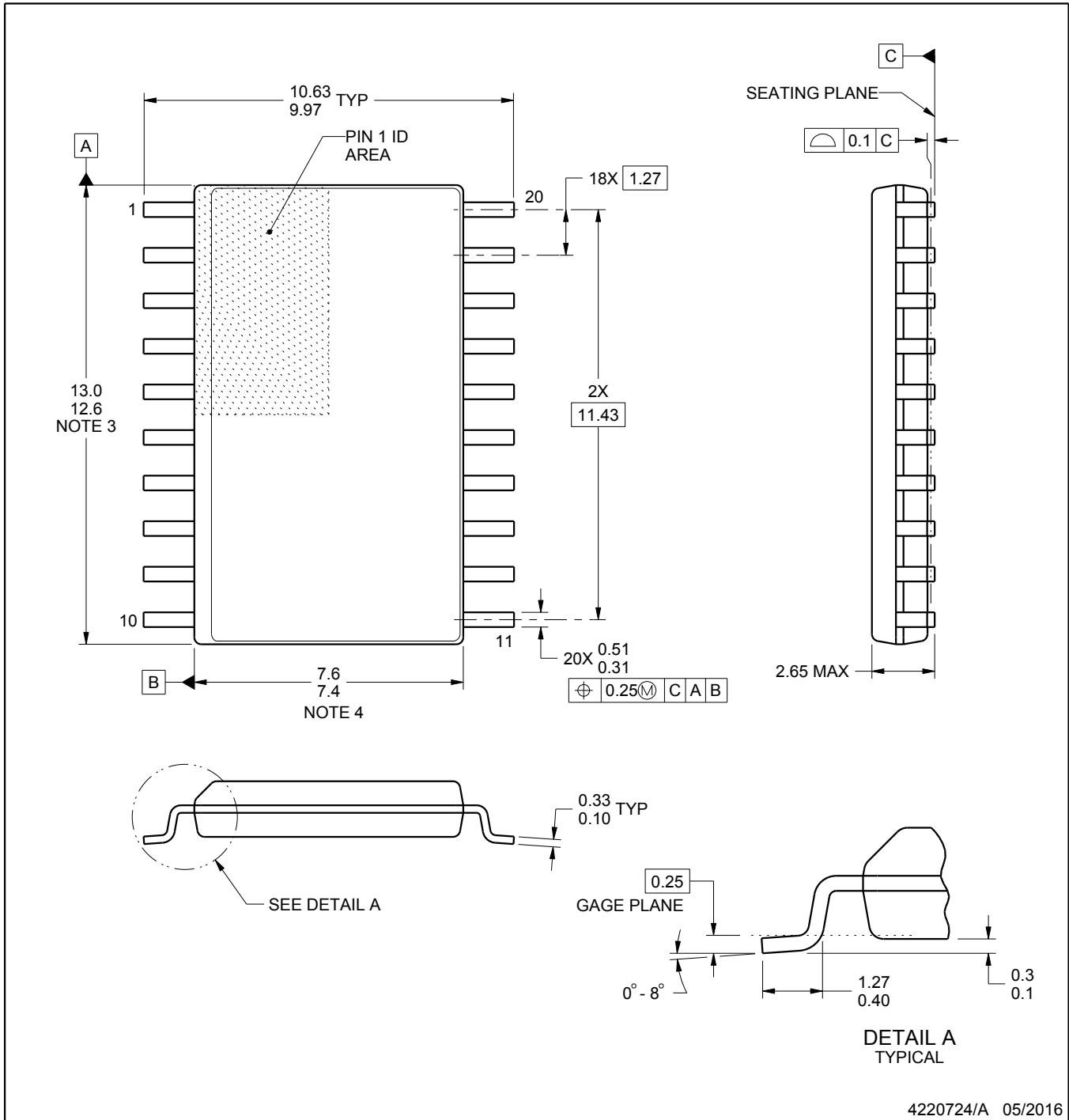
# DW0020A



# PACKAGE OUTLINE

## SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

**NOTES:**

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.



# EXAMPLE BOARD LAYOUT

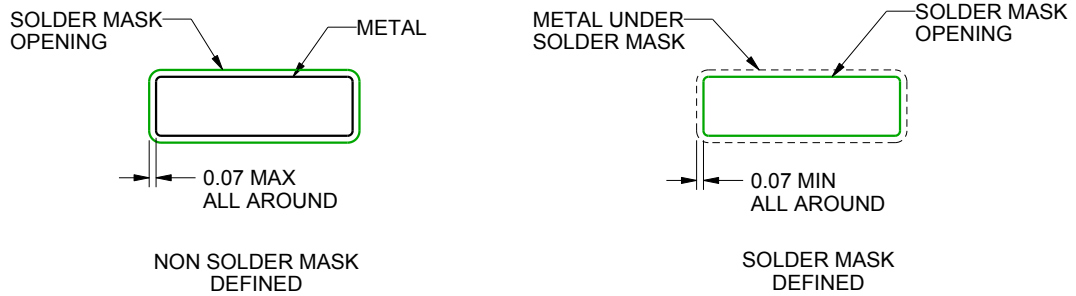
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE  
SCALE:6X



SOLDER MASK DETAILS

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NOTES: (continued)

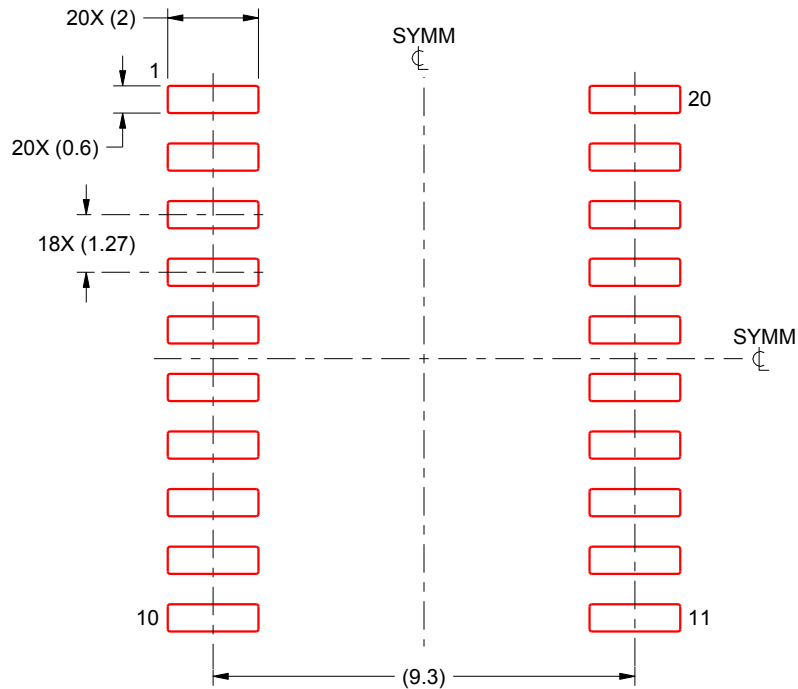
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:6X

4220724/A 05/2016

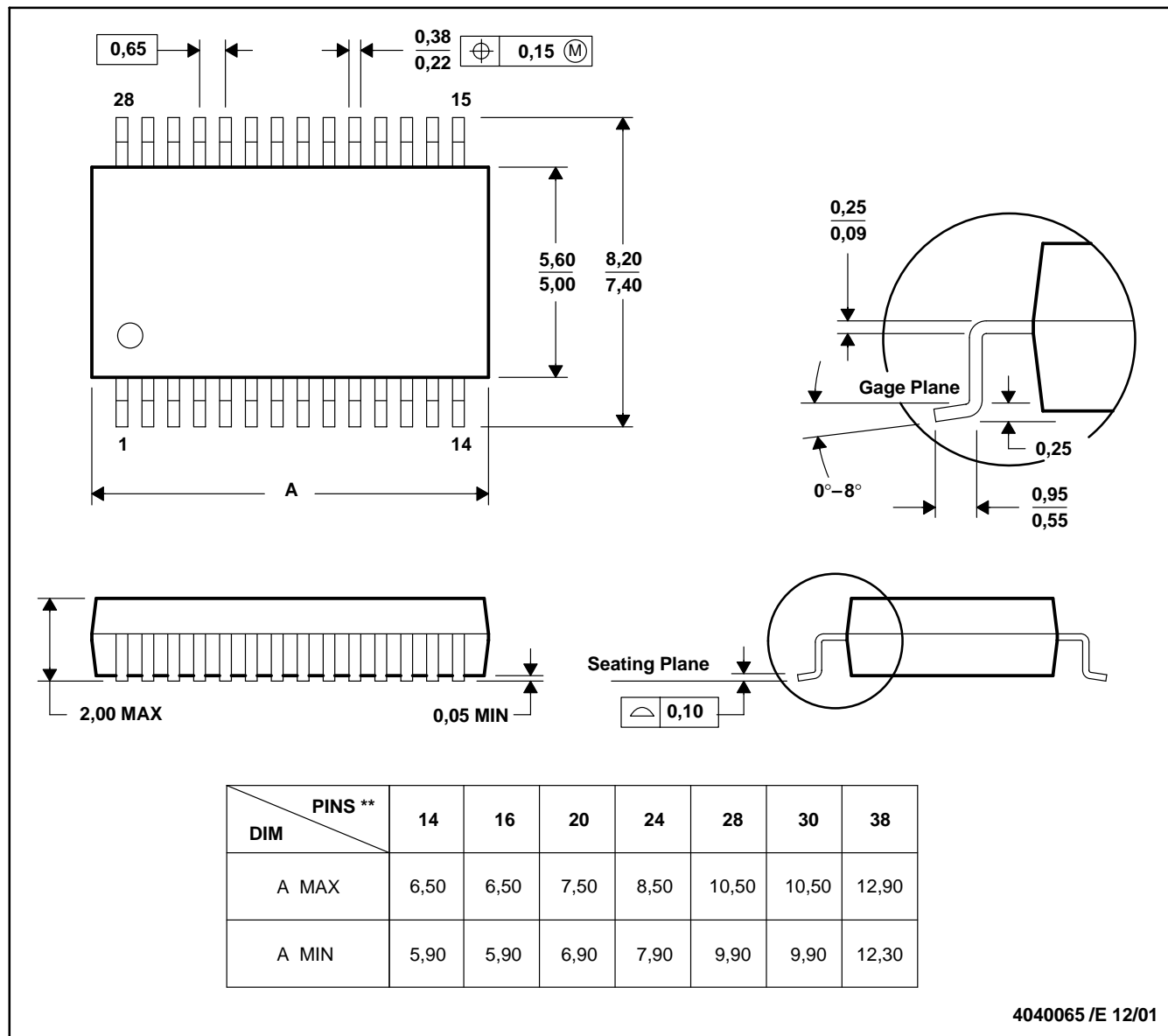
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

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