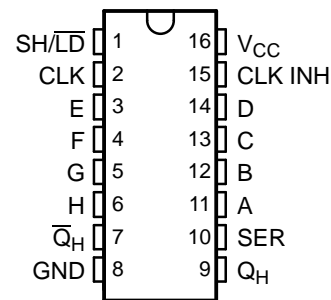


## FEATURES

- **Controlled Baseline**
  - One Assembly/Test Site, One Fabrication Site
- **Extended Temperature Performance of –55°C to 125°C**
- **Enhanced Diminishing Manufacturing Sources (DMS) Support**
- **Enhanced Product-Change Notification**
- **Qualification Pedigree <sup>(1)</sup>**
- **2-V to 5.5-V  $V_{CC}$  Operation**
- **Max  $t_{pd}$  of 10.5 ns at 5 V**
- **Supports Mixed-Mode Voltage Operation on All Ports**
- **$I_{off}$  Supports Partial-Power-Down Mode Operation**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

PW PACKAGE  
(TOP VIEW)



- (1) Component qualification in accordance with JEDEC and industry standards to ensure reliable operation over an extended temperature range. This includes, but is not limited to, Highly Accelerated Stress Test (HAST) or biased 85/85, temperature cycle, autoclave or unbiased HAST, electromigration, bond intermetallic life, and mold compound life. Such qualification testing should not be viewed as justifying use of this component beyond specified performance and environmental limits.

## DESCRIPTION

The SN74LV165A-EP is a parallel-load, 8-bit shift register designed for 2-V to 5.5-V  $V_{CC}$  operation.

When the device is clocked, data is shifted toward the serial output  $Q_H$ . Parallel-in access to each stage is provided by eight individual direct data inputs that are enabled by a low level at the shift/load ( $SH/\overline{LD}$ ) input. The SN74LV165A-EP features a clock-inhibit function and a complemented serial output,  $Q_H$ .

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while  $SH/\overline{LD}$  is held high and clock inhibit (CLK INH) is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH accomplishes clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when  $SH/\overline{LD}$  is held high. The parallel inputs to the register are enabled while  $SH/\overline{LD}$  is held low, independently of the levels of CLK, CLK INH, or SER.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

## ORDERING INFORMATION

$T_A$	PACKAGE <sup>(1)</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–55°C to 125°C	TSSOP – PW	Reel of 2000	SN74LV165AMPWREP	LV165EP

- (1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

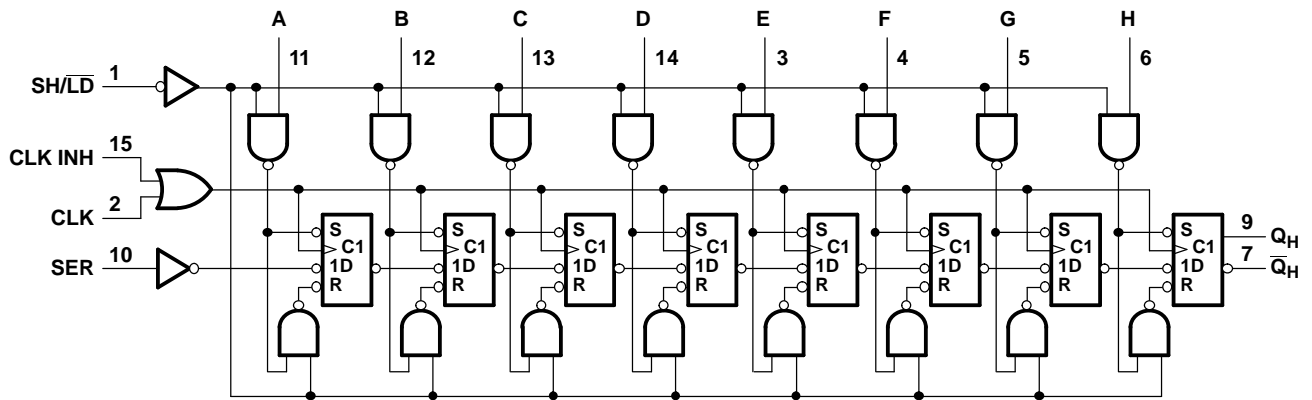
**SN74LV165A-EP**  
**PARALLEL-LOAD 8-BIT SHIFT REGISTER**

SCLS694—JANUARY 2006

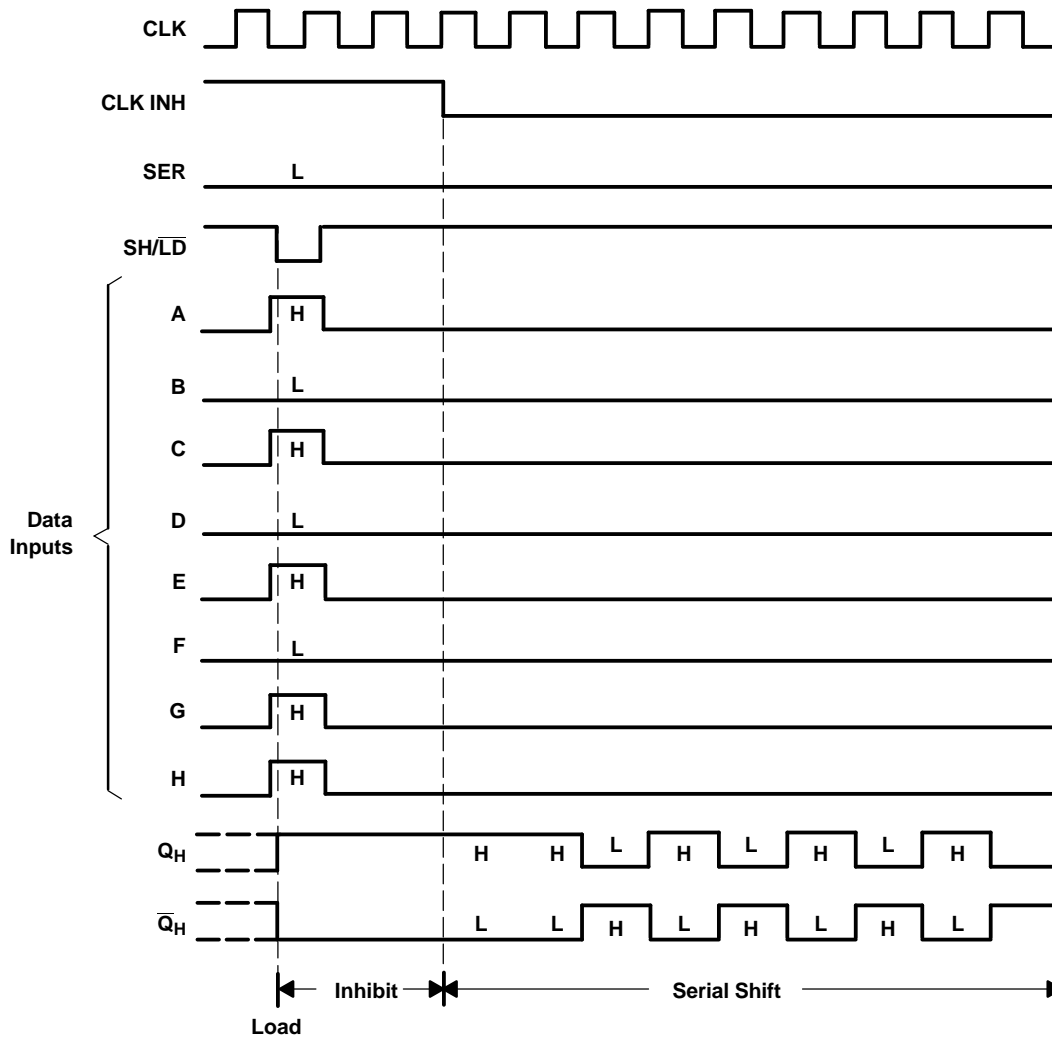
**FUNCTION TABLE**

INPUTS			OPERATION
SH/ $\overline{\text{LD}}$	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	$Q_0$
H	X	H	$Q_0$
H	L	$\uparrow$	Shift
H	$\uparrow$	L	Shift

**LOGIC DIAGRAM (POSITIVE LOGIC)**



**TYPICAL SHIFT, LOAD, AND INHIBIT SEQUENCES**



# SN74LV165A-EP PARALLEL-LOAD 8-BIT SHIFT REGISTER

SCLS694–JANUARY 2006

## Absolute Maximum Ratings<sup>(1)</sup>

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage range	-0.5	7	V
$V_I$	Input voltage range <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage range applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
$V_O$	Output voltage range <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$	V
$I_{IK}$	Input clamp current	$V_I < 0$	-20	mA
$I_{OK}$	Output clamp current	$V_O < 0$	-50	mA
$I_O$	Continuous output current	$V_O = 0$ to $V_{CC}$	$\pm 25$	mA
	Continuous current through $V_{CC}$ or GND		$\pm 50$	mA
$\theta_{JA}$	Package thermal impedance <sup>(4)</sup>		108	°C/W
$T_{stg}$	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

## Recommended Operating Conditions<sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	2	5.5	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2$ V	1.5	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.7$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.7$	
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.7$	
$V_{IL}$	Low-level input voltage	$V_{CC} = 2$ V	0.5	V
		$V_{CC} = 2.3$ V to 2.7 V	$V_{CC} \times 0.3$	
		$V_{CC} = 3$ V to 3.6 V	$V_{CC} \times 0.3$	
		$V_{CC} = 4.5$ V to 5.5 V	$V_{CC} \times 0.3$	
$V_I$	Input voltage	0	5.5	V
$V_O$	Output voltage	0	$V_{CC}$	V
$I_{OH}$	High-level output current	$V_{CC} = 2$ V	-50	$\mu$ A
		$V_{CC} = 2.3$ V to 2.7 V	-2	
		$V_{CC} = 3$ V to 3.6 V	-6	
		$V_{CC} = 4.5$ V to 5.5 V	-12	
$I_{OL}$	Low-level output current	$V_{CC} = 2$ V	50	$\mu$ A
		$V_{CC} = 2.3$ V to 2.7 V	2	
		$V_{CC} = 3$ V to 3.6 V	6	
		$V_{CC} = 4.5$ V to 5.5 V	12	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 2.3$ V to 2.7 V	200	ns/V
		$V_{CC} = 3$ V to 3.6 V	100	
		$V_{CC} = 4.5$ V to 5.5 V	20	
$T_A$	Operating free-air temperature	-55	125	°C

- (1) All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	MIN	TYP	MAX	UNIT
V <sub>OH</sub>	I <sub>OH</sub> = -50 μA	2 V to 5.5 V	V <sub>CC</sub> - 0.1			V
	I <sub>OH</sub> = -2 mA	2.3 V	2			
	I <sub>OH</sub> = -6 mA	3 V	2.48			
	I <sub>OH</sub> = -12 mA	4.5 V	3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 V to 5.5 V			0.1	V
	I <sub>OL</sub> = 2 mA	2.3 V			0.4	
	I <sub>OL</sub> = 6 mA	3 V			0.44	
	I <sub>OL</sub> = 12 mA	4.5 V			0.55	
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V			±1	μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V			20	μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0			5	μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V		1.7		pF

## Timing Requirements

over recommended operating free-air temperature range, V<sub>CC</sub> = 2.5 V ± 0.2 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration	CLK high or low	8.5	9		ns
		SH/ $\overline{\text{LD}}$ low	11	13		
t <sub>su</sub>	Setup time	SH/ $\overline{\text{LD}}$ high before CLK↑	7	8.5		ns
		SER before CLK↑	8.5	9.5		
		CLK INH before CLK↑	7	7		
		Data before SH/ $\overline{\text{LD}}$ ↑	11.5	12		
t <sub>h</sub>	Hold time	SER data after CLK↑	-1	0		ns
		Parallel data after SH/ $\overline{\text{LD}}$ ↑	0	0.5		
		SH/ $\overline{\text{LD}}$ high after CLK↑	0	0		

## Timing Requirements

over recommended operating free-air temperature range, V<sub>CC</sub> = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T <sub>A</sub> = 25°C		MIN	MAX	UNIT
		MIN	MAX			
t <sub>w</sub>	Pulse duration	CLK high or low	6	7		ns
		SH/ $\overline{\text{LD}}$ low	7.5	9		
t <sub>su</sub>	Setup time	SH/ $\overline{\text{LD}}$ high before CLK↑	5	6		ns
		SER before CLK↑	5	6		
		CLK INH before CLK↑	5	5		
		Data before SH/ $\overline{\text{LD}}$ ↑	7.5	8.5		
t <sub>h</sub>	Hold time	SER data after CLK↑	0	0		ns
		Parallel data after SH/ $\overline{\text{LD}}$ ↑	0.5	0.5		
		SH/ $\overline{\text{LD}}$ high after CLK↑	0	0		

# SN74LV165A-EP PARALLEL-LOAD 8-BIT SHIFT REGISTER

SCLS694–JANUARY 2006

## Timing Requirements

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

			$T_A = 25^\circ\text{C}$		MIN	MAX	UNIT
			MIN	MAX			
$t_w$	Pulse duration	CLK high or low	4		6.5		ns
		SH/ $\overline{\text{LD}}$ low	5		6.5		
$t_{su}$	Setup time	SH/ $\overline{\text{LD}}$ high before CLK $\uparrow$	4		4		ns
		SER before CLK $\uparrow$	4		4		
		CLK INH before CLK $\uparrow$	3.5		4.5		
		Data before SH/ $\overline{\text{LD}}$ $\uparrow$	5		5		
$t_h$	Hold time	SER data after CLK $\uparrow$	0.5		0.5		ns
		Parallel data after SH/ $\overline{\text{LD}}$ $\uparrow$	1		1		
		SH/ $\overline{\text{LD}}$ high after CLK $\uparrow$	0.5		0.5		

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{max}$			$C_L = 50\text{ pF}$	40	65		35		MHz
$t_{pd}$	CLK	$Q_H$ or $\overline{Q}_H$	$C_L = 50\text{ pF}$		15.3	23.3	1	26	ns
	SH/ $\overline{\text{LD}}$				16.1	25.1	1	28	
	H				15.9	25.3	1	28	

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{max}$			$C_L = 50\text{ pF}$	60	90		50		MHz
$t_{pd}$	CLK	$Q_H$ or $\overline{Q}_H$	$C_L = 50\text{ pF}$		10.9	14.9	1	16.9	ns
	SH/ $\overline{\text{LD}}$				11.3	19.3	1	22	
	H				11.1	17.6	1	20	

## Switching Characteristics

over recommended operating free-air temperature range,  $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$  (unless otherwise noted) (see [Figure 1](#))

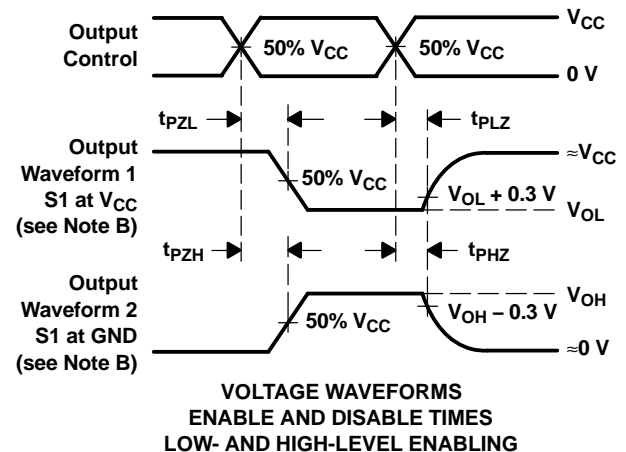
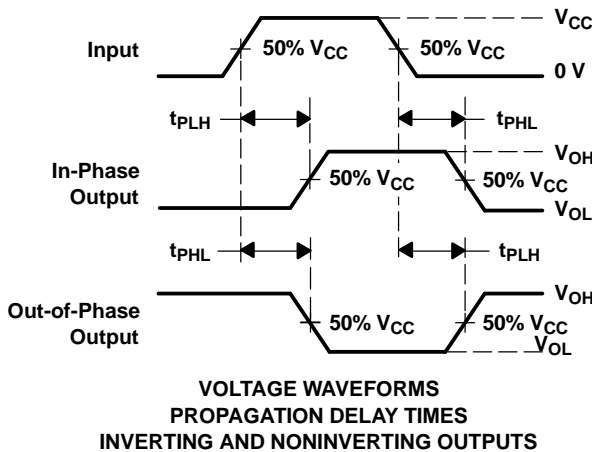
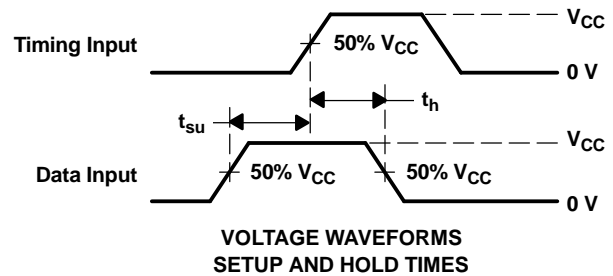
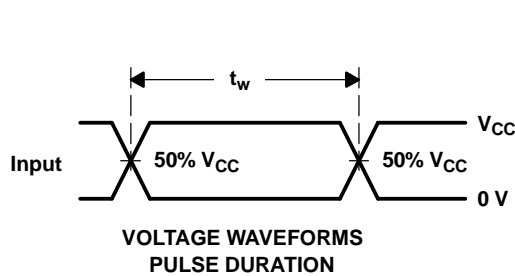
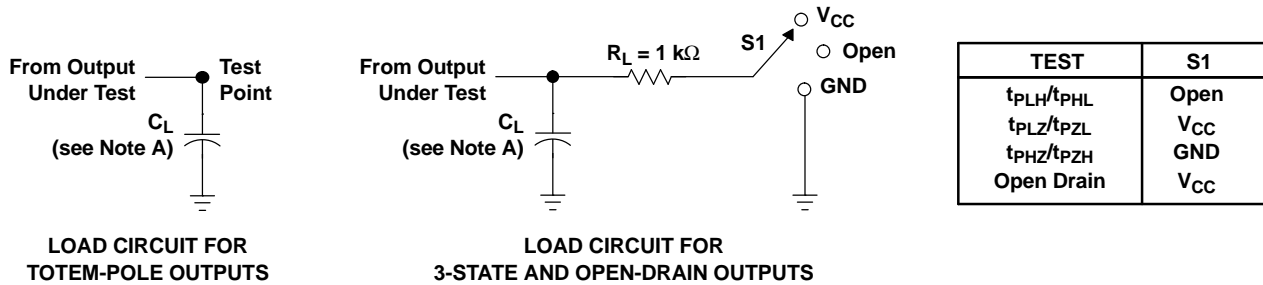
PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
$f_{max}$			$C_L = 50\text{ pF}$	75	85		75		MHz
$t_{pd}$	CLK	$Q_H$ or $\overline{Q}_H$	$C_L = 50\text{ pF}$		7.7	11.9	1	13.5	ns
	SH/ $\overline{\text{LD}}$				7.7	11.9	1	13.5	
	H				7.6	11	1	12.5	

## Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	$V_{CC}$	TYP	UNIT	
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}, f = 10\text{ MHz}$	3.3 V	36.1	pF
			5 V	37.5	

PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and jig capacitance.
  - B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
  - C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
  - D. The outputs are measured one at a time, with one input transition per measurement.
  - E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
  - F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
  - G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
  - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuits and Voltage Waveforms

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV165AMPWREP	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV165EP	<a href="#">Samples</a>
V62/06603-01XE	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	LV165EP	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74LV165A-EP :**

- Catalog: [SN74LV165A](#)

## NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV165AMPWREP	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV165AMPWREP	TSSOP	PW	16	2000	356.0	356.0	35.0

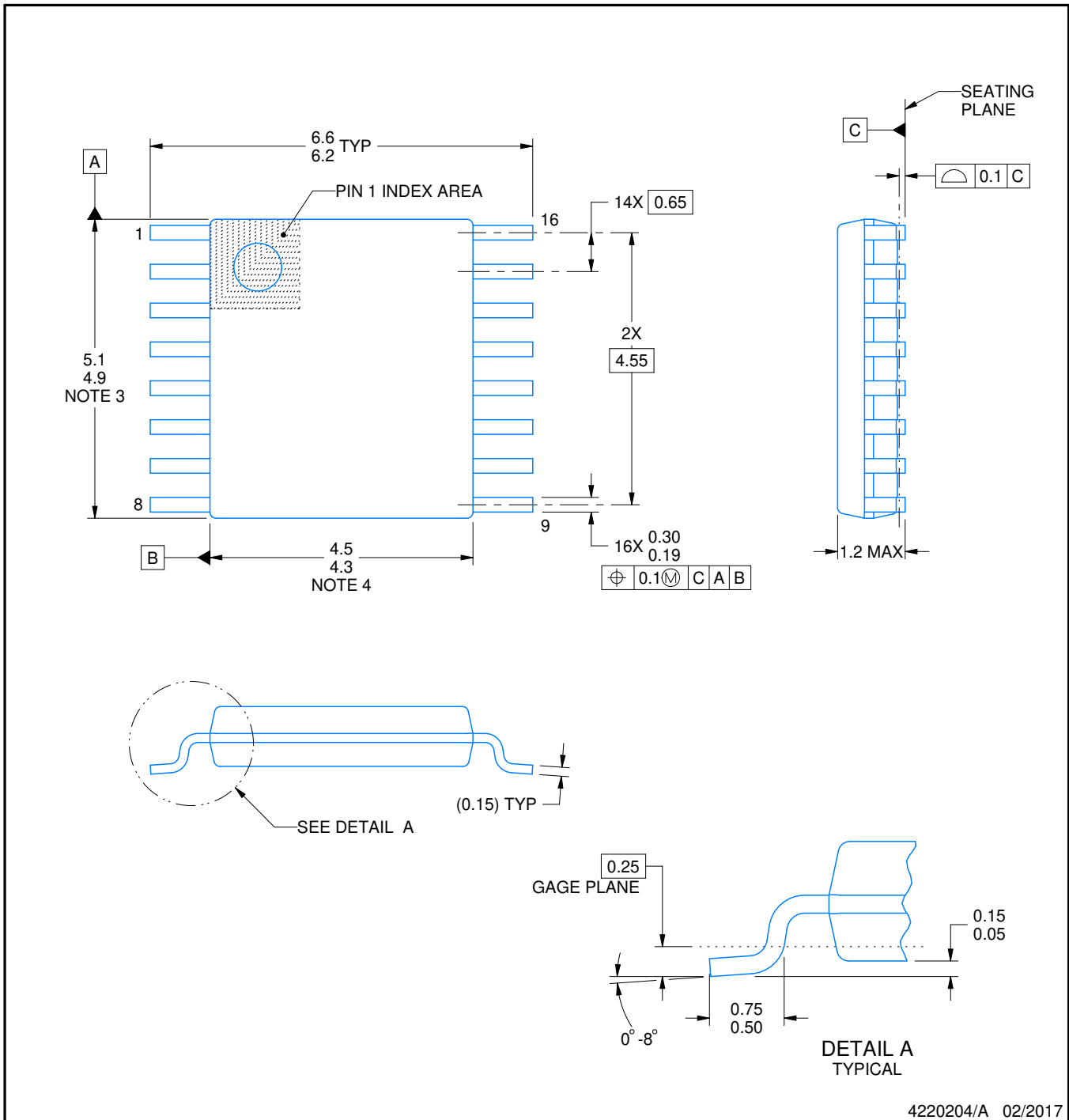
# PW0016A



# PACKAGE OUTLINE

## TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



4220204/A 02/2017

### NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

# EXAMPLE BOARD LAYOUT

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 10X



SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

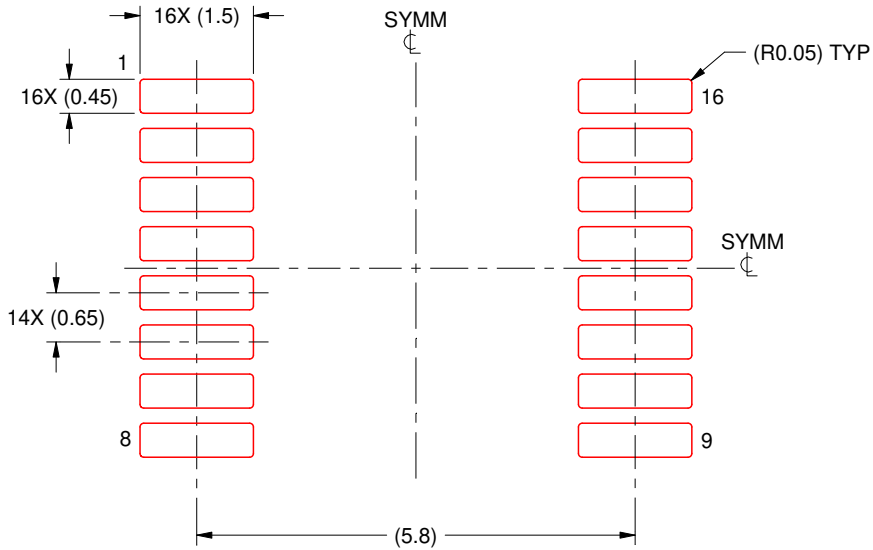
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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