

## Quad Class D Spatial Array

### General Description

The LM48901 is a quad Class D amplifier that utilizes Texas Instruments' proprietary spatial sound processor to create an enhanced sound stage for portable multimedia devices. The Class D output stages feature Texas Instruments' edge rate control (ERC) PWM architecture that significantly reduces RF emissions while preserving audio quality and efficiency.

The LM48901's flexible I<sup>2</sup>S interface is compatible with standard serial audio interfaces. A stereo differential-input ADC gives the device the ability to process analog stereo audio signals.

The LM48901 is configured through an I<sup>2</sup>C compatible interface and is capable of delivering 2.8W/channel of continuous output power into an 4Ω load with less than 10% THD+N. A 2.1 mode pairs two output drivers in parallel, increasing current drive for 4Ω loads.

Output short circuit and thermal overload protection prevent the device from being damaged during fault conditions. Superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM48901 is available in space saving microSMD and LLP packages.

### Key Specifications

■ SNR (A-Weighted)	87dBA (typ)
■ Output Power/channel, $P_{V_{DD}} = 5V$	
$R_L = 8\Omega$ , THD+N ≤10%	1.7W (typ)
$R_L = 4\Omega$ , THD+N ≤10%	2.8W (typ)
■ THD+N	0.06% (typ)
■ Efficiency/Channel	89% (typ)
■ PSRR at 217Hz	71dB (typ)
■ Shutdown current	1μA (typ)

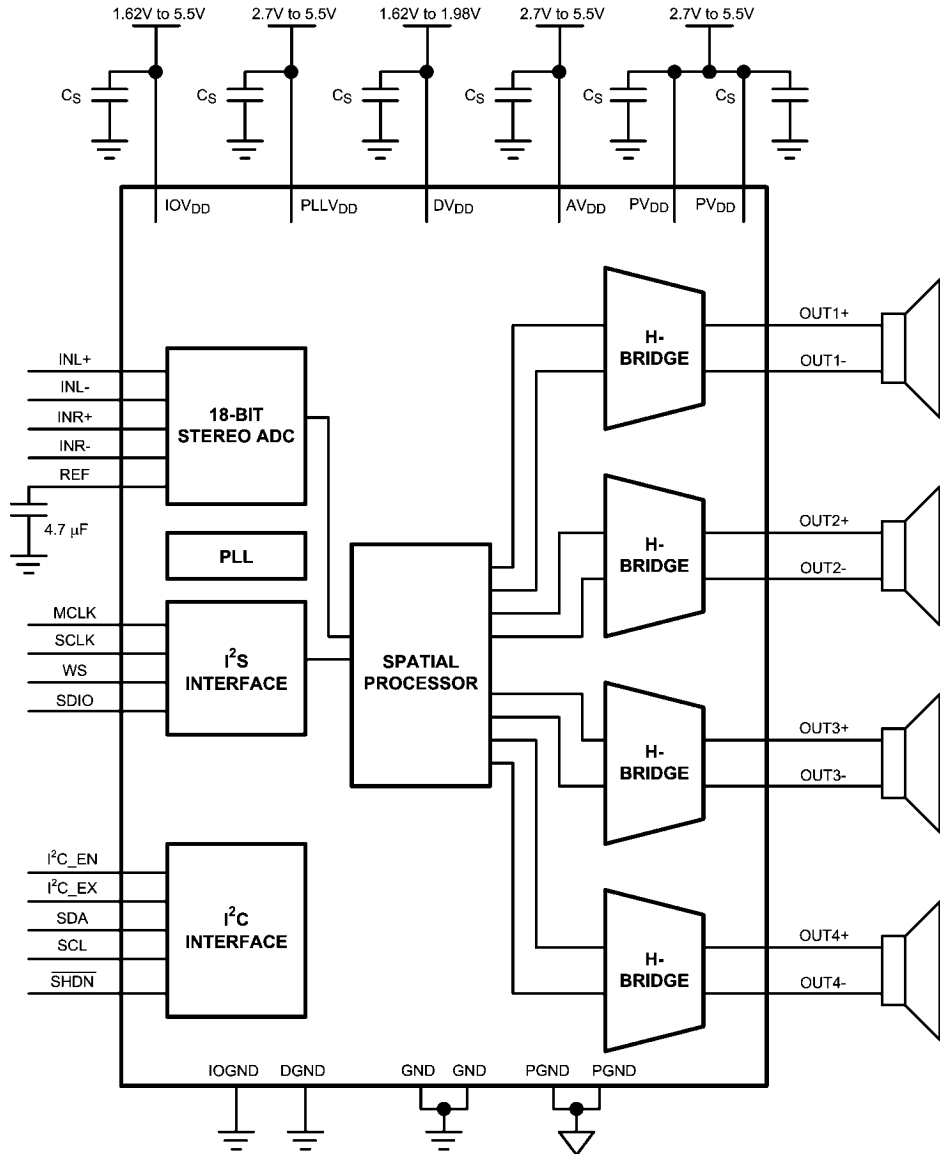
### Features

- Spatial Sound Processing
- I<sup>2</sup>S Compatible Input
- Differential-Input Stereo ADC
- Edge Rate Control Reduces EMI while Preserving Audio Quality and Efficiency
- Paralleled Output Mode
- Short Circuit and Thermal Overload Protection
- Minimum external components
- Click and Pop suppression
- Micro-power shutdown
- Available in space-saving micro SMD and LLP packages

### Applications

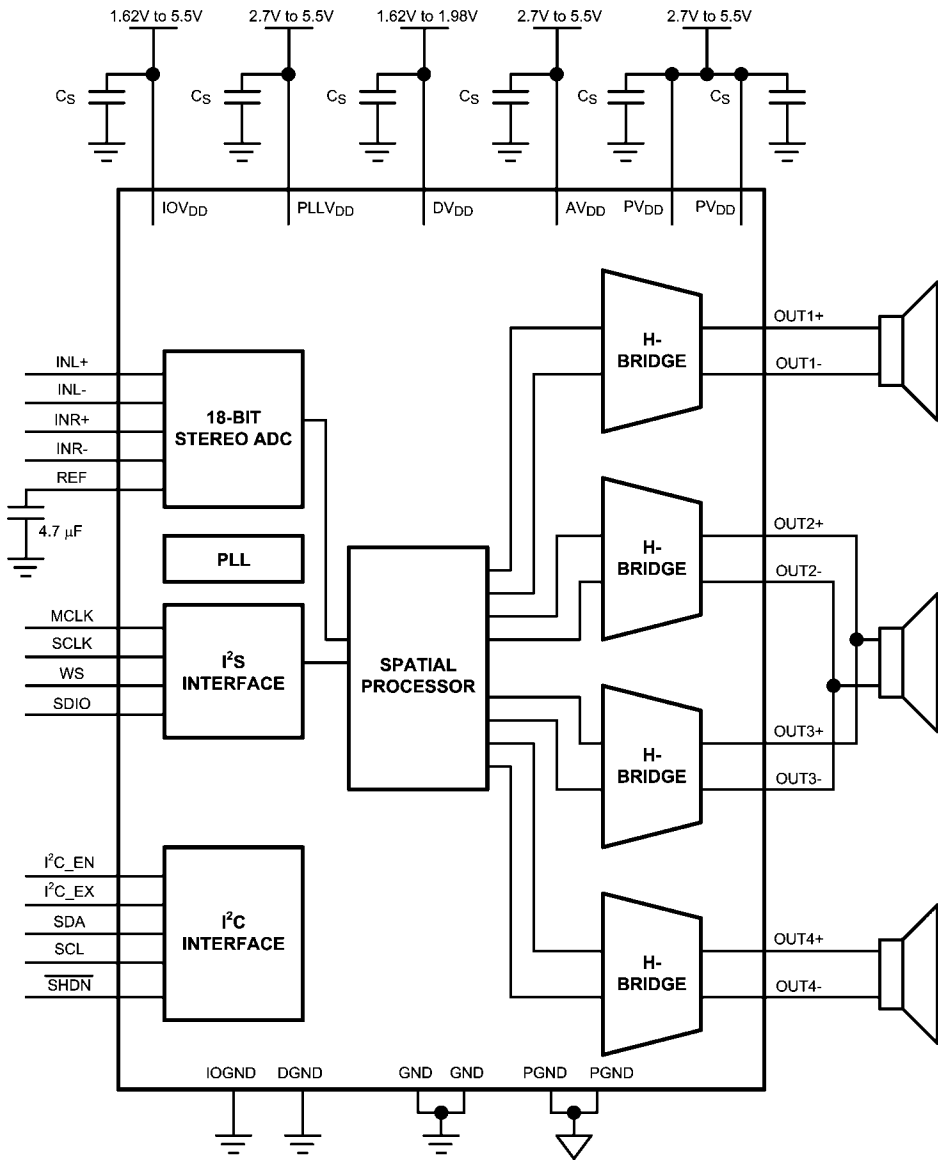
- Laptops
- Tablets
- Desktop Computers
- Sound Bars
- Multimedia Devices
- MP3 Player Accessories
- Docking Stations

# Typical Application



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FIGURE 1. Typical Audio Amplifier Application Circuit



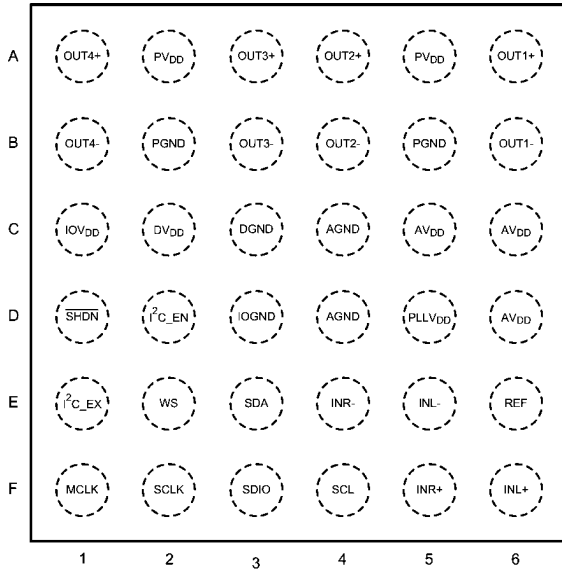
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**FIGURE 2. Channel Audio Amplifier Application Circuit**

Only OUT2 and OUT3 can be configured in parallel. OUT1 and OUT4 cannot be configured in parallel.

# Connection Diagrams

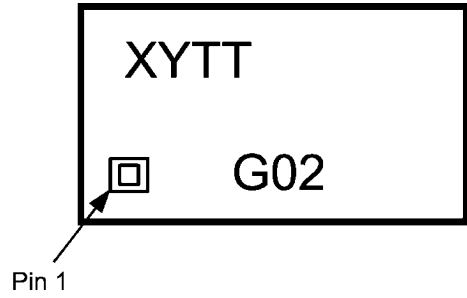
**micro SMD Package**



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**Top View**  
**Order Number LM48901RL**  
**See NS Package Number RLA36JSA**

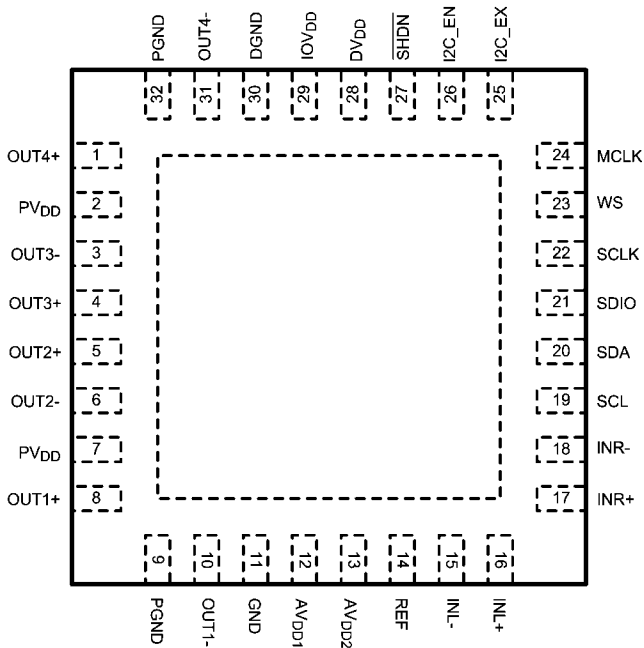
**36-Bump micro SMD Marking**



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**Top View**  
**XY = Date code**  
**TT = Die traceability**  
**G = Boomer Family**  
**02 = LM48901RL**

**SQ Package**



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**Top View**  
**Order Number LM48901SQ**  
**See NS Package Number SQA32A**

## Ordering Information

Ordering Information Table

Order Number	Package	Package Drawing Number	Transport Media	MSL Level	Green Status n
LM48901RL	36-bump microSMD	RLA36JSA	250 units on tape and reel	1	RoHS & no Sb/Br
LM48901RLX	36-bump microSMD	RLA36JSA	1000 units on tape and reel	1	RoHS & no Sb/Br
LM48901SQ	32-pin LLP	SQA32A	1000 units on tape and reel	1	RoHS & no Sb/Br
LM48901SQE	32-pin LLP	SQA32A	250 units on tape and reel	1	RoHS & no Sb/Br
LM48901SQX	32-pin LLP	SQA32A	4500 units on tape and reel	1	RoHS & no Sb/Br

TABLE 1. Pin Descriptions

BUMP	PIN	NAME	DESCRIPTION
A1	1	OUT4+	Channel 4 Non-Inverting Output
A2, A5	2, 7	PVDD	Class D Power Supply
A3	4	OUT3+	Channel 3 Non-Inverting Output. Connect to OUT2+ in Parallel Mode.
A4	5	OUT2+	Channel 2 Non-Inverting Output. Connect to OUT3+ in Parallel Mode.
A6	8	OUT1+	Channel 1 Non-Inverting Output
B1	31	OUT4-	Channel 4 Inverting Output
B2, B5	9, 32	PGND	Power Ground
B3	3	OUT3-	Channel 3 Inverting Output. Connect to OUT2- in Parallel Mode.
B4	6	OUT2-	Channel 2 Inverting Output. Connect to OUT3- in Parallel Mode.
B6	10	OUT1-	Channel 1 Inverting Output
C1	29	IOVDD	Digital Interface Power Supply
C2	28	DVDD	Digital Power Supply
C3	30	DGND	Digital Ground
C4	11	AGND1	Modulator Analog Ground
C5	—	AVDD3	ADC Reference Power Supply
C6	12	AVDD1	Modulator Analog Power Supply. Set to same voltage as $PV_{DD}$ for maximum headroom.
D1	27	$\overline{SHDN}$	Active Low Shutdown. Connect to $V_{DD}$ for normal operation.
D2	26	I <sup>2</sup> C_EN	I <sup>2</sup> C Enable Input
D3	30	IOGND	Digital Interface Ground
D4	—	AGND2	ADC Analog Ground
D5	—	PLL $V_{DD}$	PLL Power Supply
D6	13	AVDD2	ADC Analog Power Supply
E1	25	I <sup>2</sup> C_EX	I <sup>2</sup> C Enable Output
E2	23	WS	I <sup>2</sup> S Word Select Input
E3	20	SDA	I <sup>2</sup> C Serial Data Input
E4	18	INR-	Right Channel Inverting Analog Input
E5	15	INL-	Left Channel Inverting Analog Input
E6	14	REF	ADC Reference Bypass
F1	24	MCLK	Master Clock
F2	22	SCLK	Serial Clock Input
F3	21	SDIO	I <sup>2</sup> S Serial Data Input/Output
F4	19	SCL	I <sup>2</sup> C Clock Input
F5	17	INR+	Right Channel Non-Inverting Analog Input
F6	16	INL+	Left Channel Non-Inverting Analog Input

## Absolute Maximum Ratings (Note 1, Note 2)

If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.

### Supply Voltage

$AV_{DD}$ , $PV_{DD}$ , $PLV_{DD}$ , $IOV_{DD}$ <small>(Note 1)</small>	6.0V
Supply Voltage, $DV_{DD}$ <small>(Note 1)</small>	2.2V
Storage Temperature	-65°C to +150°C
Input Voltage	-0.3V to $V_{DD} + 0.3V$
Power Dissipation <small>(Note 3)</small>	Internally limited
ESD Susceptibility <small>(Note 4)</small>	2000V
ESD Susceptibility <small>(Note 5)</small>	150V
Junction Temperature	150°C

### Thermal Resistance

$\theta_{JA}$ (microSMD)	26°C/W
$\theta_{JA}$ (LLP)	26°C/W
$\theta_{JC}$ (LLP)	2.6°C/W

## Operating Ratings

### Temperature Range

$$T_{MIN} \leq T_A \leq T_{MAX} \quad -40^\circ\text{C} \leq T_A \leq +85^\circ\text{C}$$

### Supply Voltage

$AV_{DD}$	$2.7V \leq AV_{DD} \leq 5.5V$
$PV_{DD}$	$2.7V \leq PV_{DD} \leq 5.5V$
$PLL_{DD}$	$2.7V \leq PLL_{DD} \leq 5.5V$
$IOV_{DD}$	$1.62V \leq IOV_{DD} \leq 5.5V$
$DV_{DD}$	$1.62V \leq DV_{DD} \leq 1.98V$

## Electrical Characteristics $PV_{DD} = AV_{DD} = 5V$ , $IOV_{DD} = PLL_{DD} = 3.3V$ , $DV_{DD} = 1.8$ (Note 2, Note 8)

The following specifications apply for  $A_V = 0\text{dB}$ ,  $C_{REF} = 4.7\mu\text{F}$ ,  $R_L = 8\Omega$ ,  $f = 1\text{kHz}$ , unless otherwise specified. Limits apply for  $T_A = 25^\circ\text{C}$ .

Symbol	Parameter	Conditions	LM48901			Units (Limits)
			Min <small>(Note 8)</small>	Typ <small>(Note 7)</small>	Max <small>(Note 8)</small>	
$AV_{DD}$	Analog Supply Voltage Range	<small>(Note 9)</small>	2.7		5.5	V
$PV_{DD}$	Amplifier Supply Voltage Range	<small>(Note 9)</small>	2.7		5.5	V
$PLL_{DD}$	PLL Supply Voltage Range		2.7		5.5	V
$IOV_{DD}$	Interface Supply Voltage Range		1.62		5.5	V
$DV_{DD}$	Digital Supply Voltage Range		1.62		1.98	V
$AI_{DD}$	Analog Quiescent Supply Current	LM48901RL		17.5	21	mA
		LM48901SQ		19.2	22.3	mA
$PI_{DD}$	Amplifier Quiescent Supply Current	$R_L = 8\Omega$		5.25	8.25	mA
$PLLI_{DD}$	PLL Quiescent Supply Current	LM48901RL		1.5		mA
$DI_{DD}$	Quiescent Digital Power Supply Current			5.5	6.2	mA
$I_{SD}$	Shutdown Current (Analog, Amplifier and PLL Supplies)	Shutdown Enabled		1	5	$\mu\text{A}$
$DI_{STBY}$	Digital Standby Current			30		$\mu\text{A}$
$DI_{SD}$	Digital Shutdown Current	Shutdown Enabled		2		$\mu\text{A}$
$V_{OS}$	Differential Output Offset Voltage	$V_{IN} = 0$	-17	0	17	mV
$T_{WU}$	Wake-up Time	Power Up (Device Initialization)		150		ms
		From Shutdown		30		ms
$f_{SW}$	Switching Frequency	$f_S = 48\text{kHz}$		384		kHz

Symbol	Parameter	Conditions	LM48901			Units (Limits)
			Min (Note 8)	Typ (Note 7)	Max (Note 8)	
P <sub>O</sub>	Output Power/Channel	R <sub>L</sub> = 4Ω, THD+N = 10% f = 1kHz, 22kHz BW				
		V <sub>DD</sub> = 5V		2.8		W
		V <sub>DD</sub> = 3.6V		1.4		W
		R <sub>L</sub> = 4Ω, THD+N = 1% f = 1kHz, 22kHz BW				
		V <sub>DD</sub> = 5V		2.2		W
		V <sub>DD</sub> = 3.6V		1.2		W
		R <sub>L</sub> = 8Ω, THD+N = 10% f = 1kHz, 22kHz BW				
		V <sub>DD</sub> = 5V		1.7		W
		V <sub>DD</sub> = 3.6V		825		mW
		R <sub>L</sub> = 8Ω, THD+N = 1% f = 1kHz, 22kHz BW				
		V <sub>DD</sub> = 5V	1.0	1.3		W
		V <sub>DD</sub> = 3.6V		650		mW
P <sub>O</sub>	Output Power (Parallel Mode) (Note 10)	R <sub>L</sub> = 4Ω, THD+N = 10%, f = 1kHz, 22kHz BW				
		V <sub>DD</sub> = 5V		3.2		W
		V <sub>DD</sub> = 3.6V		1.6		W
		R <sub>L</sub> = 4Ω, THD+N = 1%, f = 1kHz, 22kHz BW				
		V <sub>DD</sub> = 5V		2.5		W
V <sub>DD</sub> = 3.6V		1.2		W		
THD+N	Total Harmonic Distortion + Noise	P <sub>O</sub> = 500mW, f = 1kHz, R <sub>L</sub> = 8Ω		0.06		%
PSRR	Power Supply Rejection Ratio (ADC Path)	V <sub>RIPPLE</sub> = 200mV <sub>P-P</sub> sine, Inputs AC GND, C <sub>IN</sub> = 1μF				
		f <sub>RIPPLE</sub> = 217Hz, Applied to PV <sub>DD</sub>		67		dB
		f <sub>RIPPLE</sub> = 217Hz, Applied to DV <sub>DD</sub>		54		dB
		f <sub>RIPPLE</sub> = 1kHz, Applied to PV <sub>DD</sub>		66		dB
		f <sub>RIPPLE</sub> = 1kHz, Applied to DV <sub>DD</sub>		54		dB
		f <sub>RIPPLE</sub> = 10kHz, Applied to PV <sub>DD</sub>		57		dB
		f <sub>RIPPLE</sub> = 10kHz, Applied to DV <sub>DD</sub>		52		dB
PSRR	Power Supply Rejection Ratio (I <sup>2</sup> S Path)	V <sub>RIPPLE</sub> = 200mV <sub>P-P</sub> sine, Inputs -120dBFS				
		f <sub>RIPPLE</sub> = 217Hz, Applied to PV <sub>DD</sub>		71		dB
		f <sub>RIPPLE</sub> = 217Hz, Applied to DV <sub>DD</sub>		58		dB
		f <sub>RIPPLE</sub> = 1kHz, Applied to PV <sub>DD</sub>		69		dB
		f <sub>RIPPLE</sub> = 1kHz, Applied to DV <sub>DD</sub>		57		dB
		f <sub>RIPPLE</sub> = 10kHz, Applied to PV <sub>DD</sub>		70		dB
		f <sub>RIPPLE</sub> = 10kHz, Applied to DV <sub>DD</sub>		55		dB
CMRR	Common Mode Rejection Ratio	V <sub>RIPPLE</sub> = 1V <sub>P-P</sub> , f <sub>RIPPLE</sub> = 217Hz, A <sub>V</sub> = 0dB		60		dB
η	Efficiency/Channel	V <sub>DD</sub> = 5V, P <sub>O</sub> = 1.1W		89		%
		V <sub>DD</sub> = 3.6V, P <sub>O</sub> = 400mW		87		%
η	Efficiency	V <sub>DD</sub> = 5V, P <sub>O</sub> = 1.1W		87		%
		V <sub>DD</sub> = 3.6V, P <sub>O</sub> = 400mW		86		%
SNR	Signal-to-Noise-Ratio	ADC Input, P <sub>O</sub> = 1W		85		dB
		I <sup>2</sup> S Input, P <sub>O</sub> = 1W		87		dB

Symbol	Parameter	Conditions	LM48901			Units (Limits)
			Min (Note 8)	Typ (Note 7)	Max (Note 8)	
CMVR	Common Mode Input Voltage Range			5		V
$\epsilon_{OS}$	Output Noise	Inputs AC GND, A-weighted, $A_V = 0dB$		130		$\mu V$
		I <sup>2</sup> S Input		72		$\mu V$
X <sub>TALK</sub>	Crosstalk			75		dB

## I<sup>2</sup>C Interface Characteristics (Note 1, Note 2)

The following specifications apply for  $R_{PU} = 1k\Omega$  to  $IOV_{DD}$ , unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	LM48901			Units
			Min (Note 7)	Typ (Note 6)	Max (Note 7)	
VIH	Logic Input High Threshold	SDA, SCL	$0.7 \cdot IOV_{DD}$			V
VIL	Logic Input Low Threshold	SDA, SCL		300		mV
VOL	Logic Output Low Threshold	SDA, ISDA = 3.6mA			0.35	V
IOH	Logic Output High Current	SDA, SCL			2	$\mu A$
	SCL Frequency				400	kHz
1	Hold Time (repeated START Condition)		0.6			$\mu s$
2	Clock Low Time		1.3			$\mu s$
3	Clock High Time		600			ns
4	Setup Time for Repeated START condition		600			ns
5	Data Hold Time	Output	300		900	ns
6	Data Setup Time		100			ns
7	SDA Rise Time				300	ns
8	SDA Fall Time				300	ns
9	Setup Time for STOP Condition		600			ns
10	Bus Free Time Between STOP and START Condition		1.3			$\mu s$

## I<sup>2</sup>S Timing Characteristics (Note 2, Note 8)

The following specifications apply for  $DV_{DD} = 1.8V$ , unless otherwise specified. Limits apply for  $T_A = 25^\circ C$ .

Symbol	Parameter	Conditions	LM48901			Units (Limits)
			Min (Note 7)	Typ (Note 6)	Max (Note 7)	
$t_{MCLKL}$	MCLK Pulse Width Low		16			ns
$t_{MCLKH}$	MCLK Pulse Width High		16			ns
$t_{MCLKY}$	MCLK Period		27			ns
$t_{BCLKR}$	SCLK rise time				3	ns
$t_{BCLKCF}$	SCLK fall time				3	ns
$t_{BCLKDS}$	SCLK Duty Cycle			50		%
$T_{DL}$	LRC Propagation Delay from SCLK falling edge				10	ns
$T_{DST}$	DATA Setup Time to SCLK Rising Edge		10			ns
$T_{DHT}$	DATA Hold Time from SCLK Rising Edge		10			ns



**Note 1:** "Absolute Maximum Ratings" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the Absolute Maximum Ratings or other conditions beyond those indicated in the Recommended Operating Conditions is not implied. The Recommended Operating Conditions indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.

**Note 2:** The Electrical Characteristics tables list guaranteed specifications under the listed Recommended Operating Conditions except as otherwise modified or specified by the Electrical Characteristics Conditions and/or Notes. Typical specifications are estimations only and are not guaranteed.

**Note 3:** The maximum power dissipation must be derated at elevated temperatures and is dictated by  $T_{JMAX}$ ,  $\theta_{JA}$ , and the ambient temperature,  $T_A$ . The maximum allowable power dissipation is  $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$  or the given in Absolute Maximum Ratings, whichever is lower.

**Note 4:** Human body model, applicable std. JESD22-A114C.

**Note 5:** Machine model, applicable std. JESD22-A115-A.

**Note 6:** Typical values represent most likely parametric norms at  $T_A = +25^\circ\text{C}$ , and at the Recommended Operation Conditions at the time of product characterization and are not guaranteed.

**Note 7:** Datasheet min/max specification limits are guaranteed by design, test, or statistical analysis.

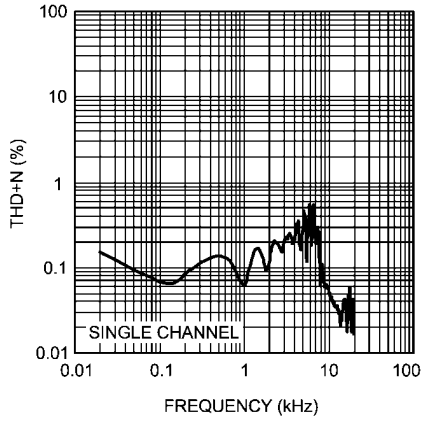
**Note 8:**  $R_L$  is a resistive load in series with two inductors to simulate an actual speaker load. For  $R_L = 8\Omega$ , the load is  $15\mu\text{H}+8\Omega+15\mu\text{H}$ . For  $R_L = 4\Omega$ , the load is  $15\mu\text{H}+4\Omega+15\mu\text{H}$ .

**Note 9:** Maintain  $PV_{DD}$  and  $AV_{DD}$  at the same voltage potential.

**Note 10:** Only OUT2 and OUT3 can be configured in Parallel Mode.

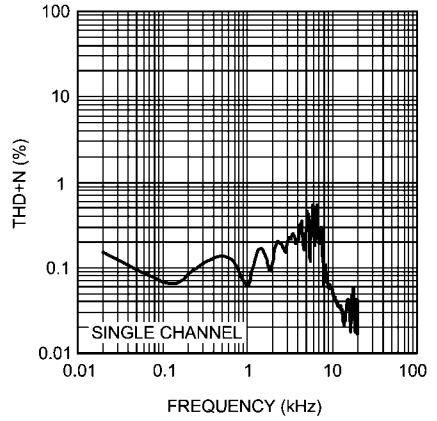
# Typical Performance Characteristics

**THD+N vs FREQUENCY**  
 $V_{DD} = 3.6V, P_{OUT} = 500mW,$   
 $R_L = 8\Omega, \text{ADC Input}$



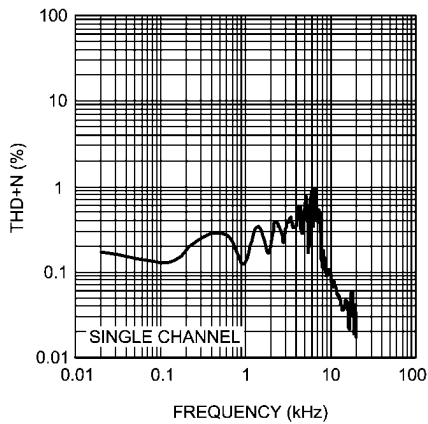
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**THD+N vs FREQUENCY**  
 $V_{DD} = 5V, P_{OUT} = 925 mW,$   
 $R_L = 8\Omega, \text{ADC Input}$



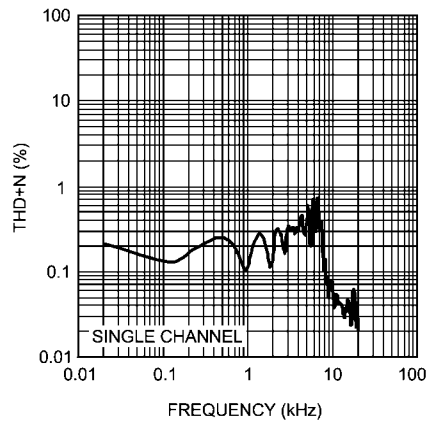
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**THD+N vs FREQUENCY**  
 $V_{DD} = 3.6V, P_{OUT} = 7505 mW,$   
 $R_L = 4\Omega, \text{ADC Input}$



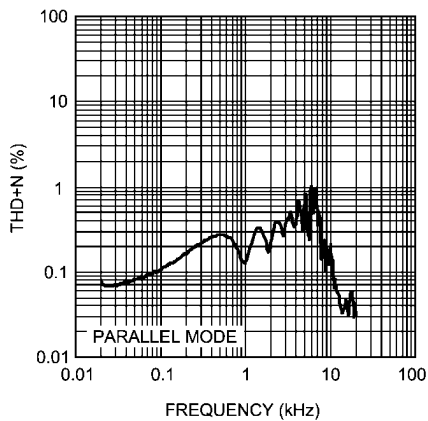
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**THD+N vs FREQUENCY**  
 $V_{DD} = 5V, P_{OUT} = 1.3W,$   
 $R_L = 4\Omega, \text{ADC Input}$



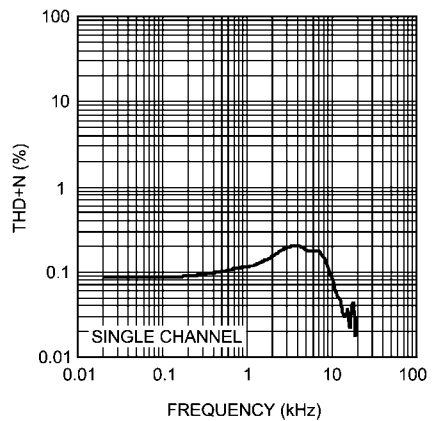
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**THD+N vs FREQUENCY**  
 $V_{DD} = 3.6V, P_{OUT} = 900mW,$   
 $R_L = 4\Omega, \text{ADC Input}$



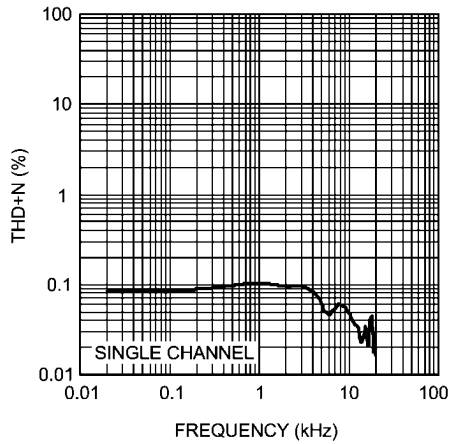
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**THD+N vs FREQUENCY**  
 $V_{DD} = 3.6V, P_{OUT} = 450mW,$   
 $R_L = 8\Omega, \text{I}^2\text{S Input}$



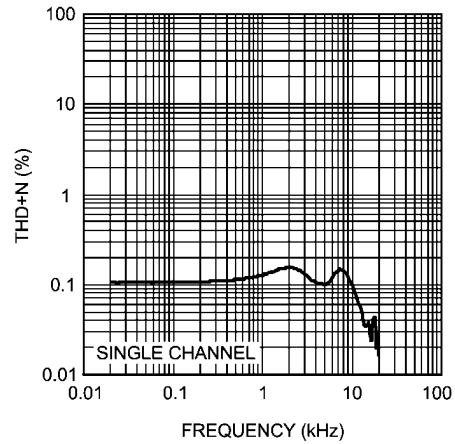
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**THD+N vs FREQUENCY**  
 $V_{DD} = 5V, P_{OUT} = 950mW,$   
 $R_L = 8\Omega, I^2S$  Input



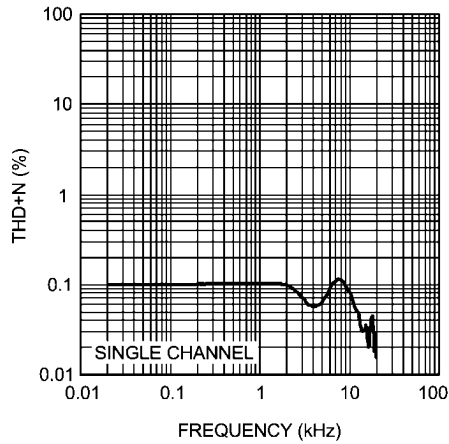
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**THD+N vs FREQUENCY**  
 $V_{DD} = 3.6V, P_{OUT} = 750mW,$   
 $R_L = 4\Omega, I^2S$  Input



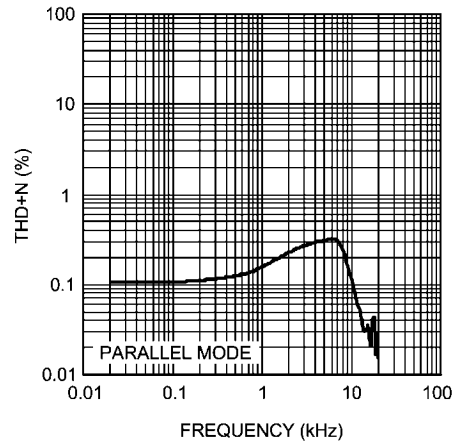
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**THD+N vs FREQUENCY**  
 $V_{DD} = 5V, P_{OUT} = 1.65W,$   
 $R_L = 4\Omega, I^2S$  Input



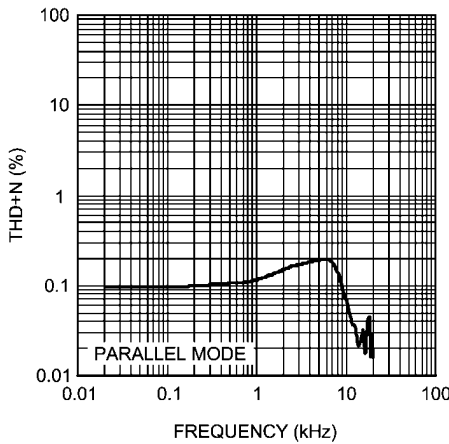
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**THD+N vs FREQUENCY**  
 $V_{DD} = 3.6V, P_{OUT} = 850mW,$   
 $R_L = 4\Omega, I^2S$  Input



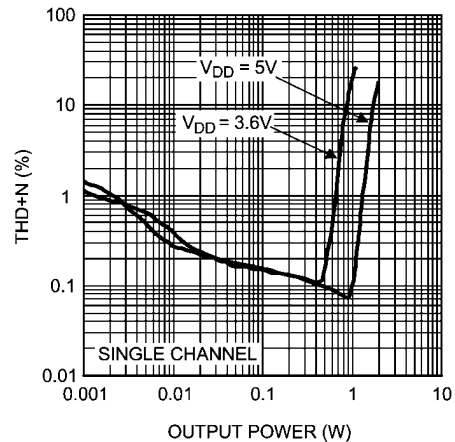
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**THD+N vs FREQUENCY**  
 $V_{DD} = 5V, P_{OUT} = 1.8W,$   
 $R_L = 4\Omega, I^2S$  Input



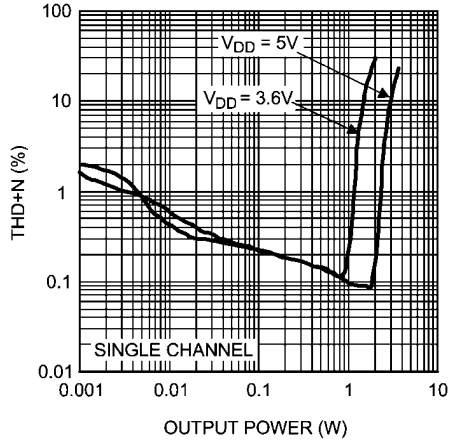
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**THD+N vs OUTPUT POWER**  
 $R_L = 8\Omega, f = 1kHz, ADC$  Input



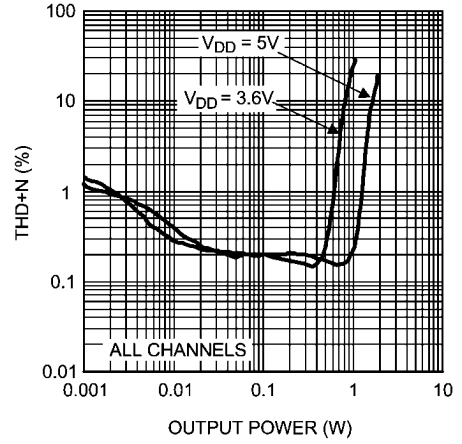
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**THD+N vs OUTPUT POWER**  
 $R_L = 4\Omega, f = 1\text{kHz}, \text{ADC Input, Single channel}$



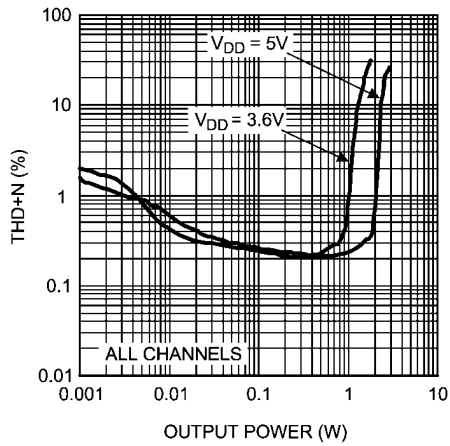
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**THD+N vs OUTPUT POWER**  
 $R_L = 8\Omega, f = 1\text{kHz}, \text{ADC Input}$



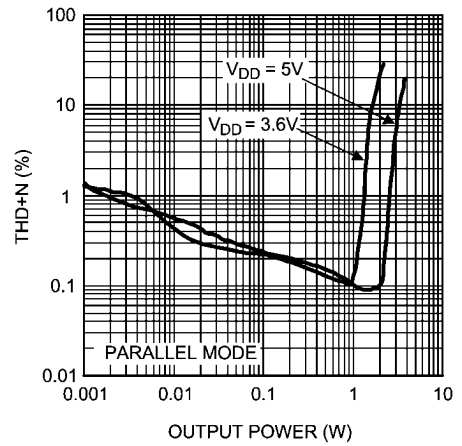
30169212

**THD+N vs OUTPUT POWER**  
 $R_L = 4\Omega, f = 1\text{kHz}, \text{ADC Input, All channels}$



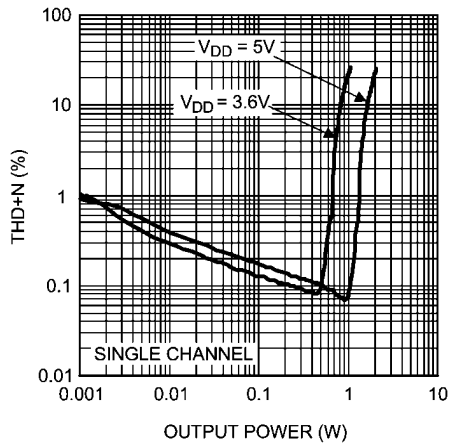
30169213

**THD+N vs OUTPUT POWER**  
 $R_L = 4\Omega, f = 1\text{kHz}, \text{ADC Input, Parallel mode}$



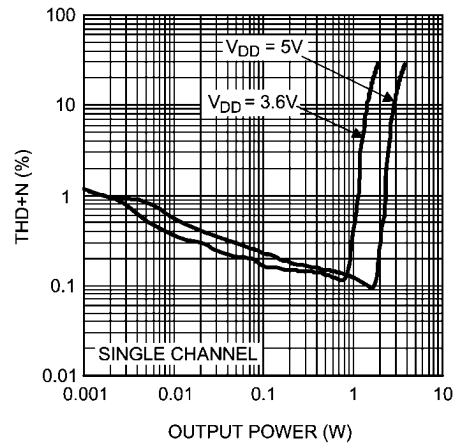
30169214

**THD+N vs OUTPUT POWER**  
 $R_L = 8\Omega, f = 1\text{kHz}, \text{I}^2\text{S Input, Single mode}$

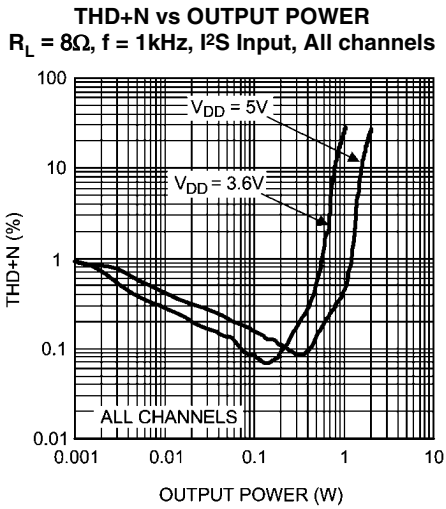


30169215

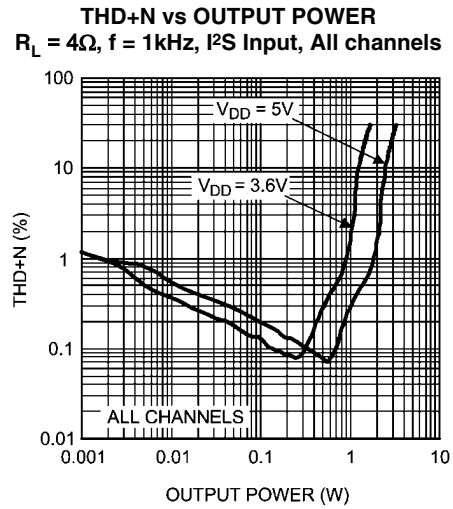
**THD+N vs OUTPUT POWER**  
 $R_L = 4\Omega, f = 1\text{kHz}, \text{I}^2\text{S Input, Single channel}$



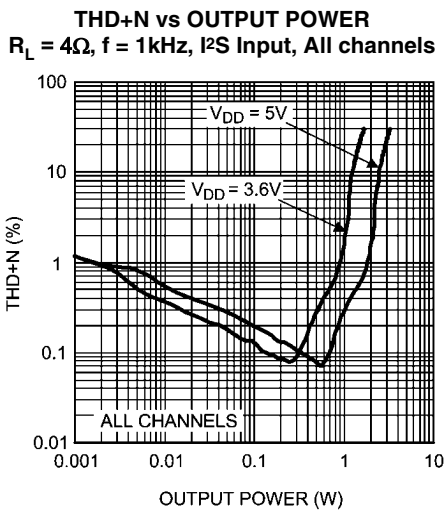
30169216



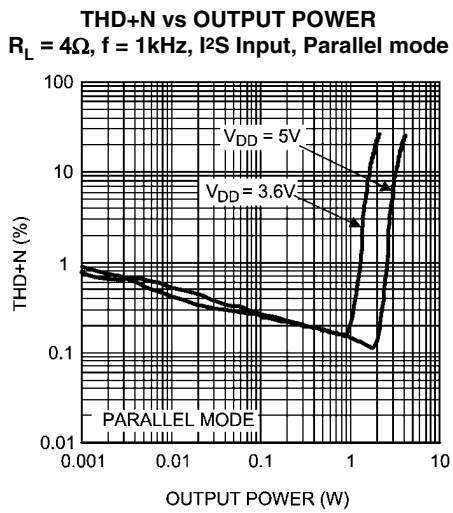
30169217



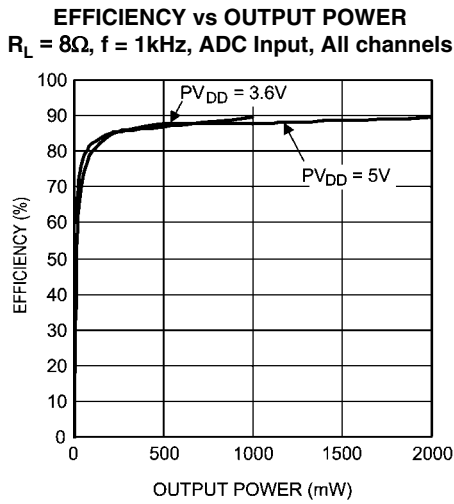
30169218



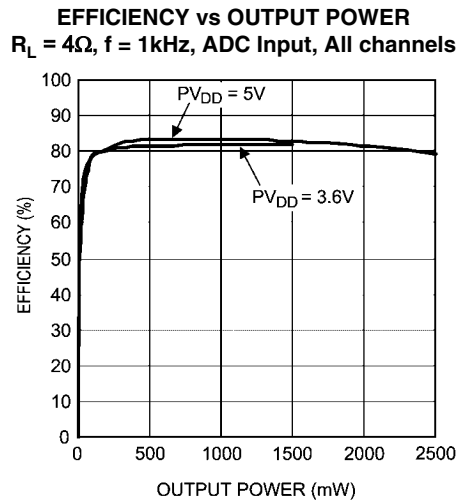
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30169219

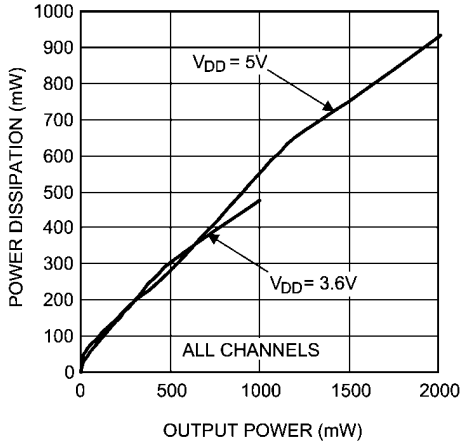


30169286



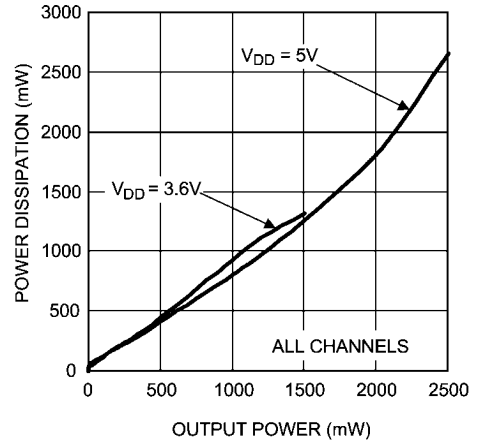
30169287

**POWER DISSIPATION vs OUTPUT POWER**  
 $R_L = 8\Omega, f = 1\text{kHz}, \text{ADC Input}$



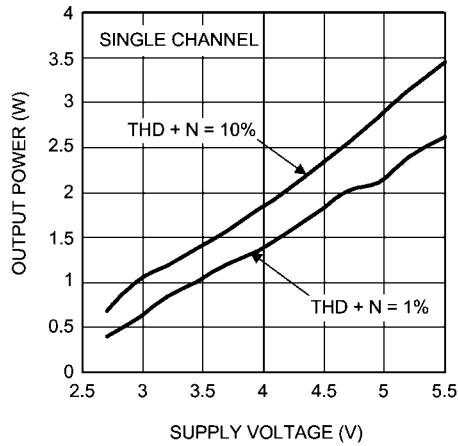
30169288

**POWER DISSIPATION vs OUTPUT POWER**  
 $R_L = 4\Omega, f = 1\text{kHz}, \text{ADC Input}$



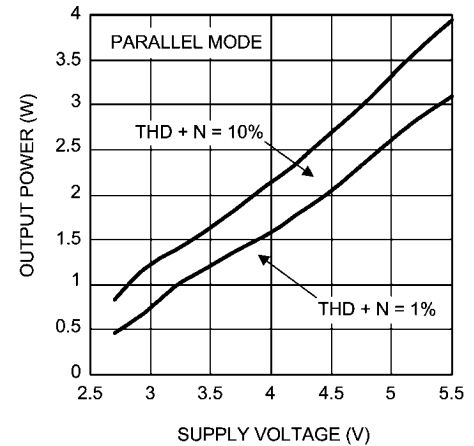
30169289

**OUTPUT POWER vs SUPPLY VOLTAGE**  
 $R_L = 4\Omega, f = 1\text{kHz}, \text{ADC Input, Single mode}$



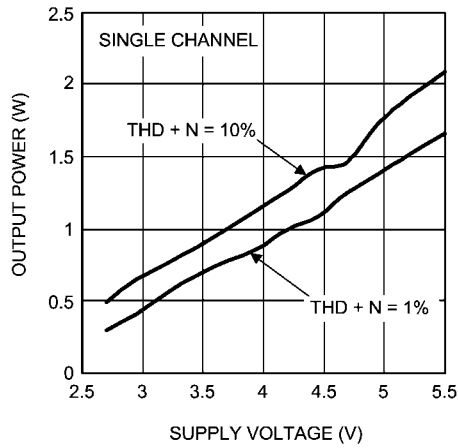
30169290

**OUTPUT POWER vs SUPPLY VOLTAGE**  
 $R_L = 4\Omega, f = 1\text{kHz}, \text{ADC Input, Parallel mode}$



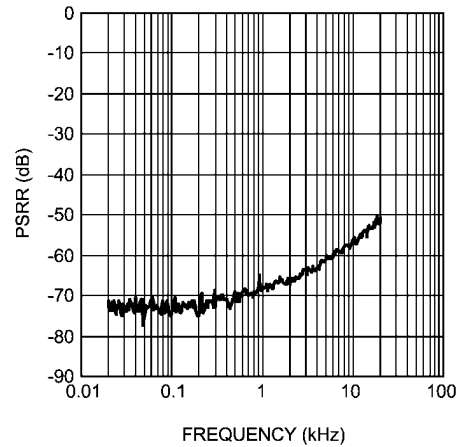
30169291

**OUTPUT POWER vs SUPPLY VOLTAGE**  
 $R_L = 8\Omega, f = 1\text{kHz}, \text{ADC Input, Single channel}$



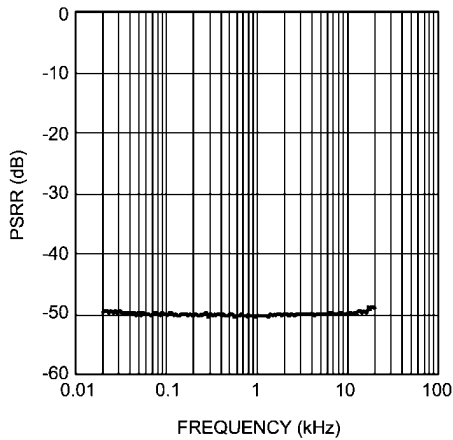
30169292

**PSRR vs FREQUENCY**  
 $P_{V_{DD}} = 5V, V_{RIPPLE} = 200\text{mV}_{P-P}, R_L = 8\Omega,$   
 $\text{ADC Mode, ADC input} = \text{AC GND}$



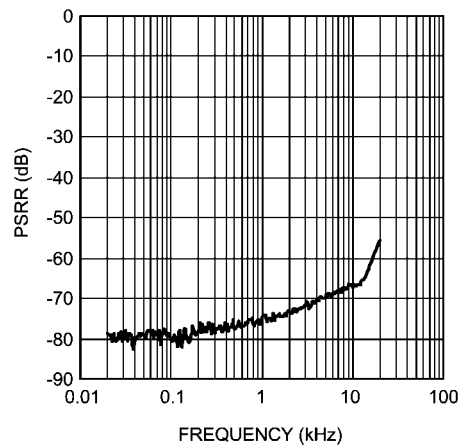
301692a8

**PSRR vs FREQUENCY**  
 $DV_{DD} = 1.8V$ ,  $V_{RIPPLE} = 200mV_{P-P}$ ,  $R_L = 8\Omega$ ,  
 ADC Mode, ADC input = AC GND



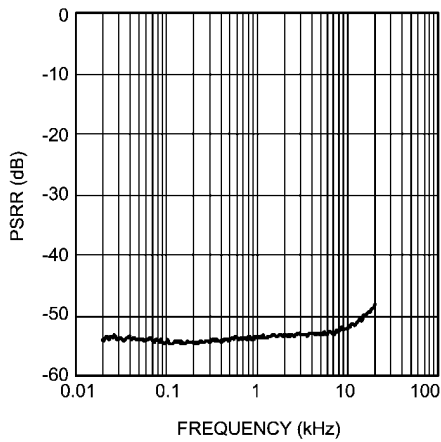
301692a9

**PSRR vs FREQUENCY**  
 $PV_{DD} = 5V$ ,  $V_{RIPPLE} = 200mV_{P-P}$ ,  $R_L = 8\Omega$ ,  
 $I_2S$  mode,  $I_2S$  input = -120dBFS



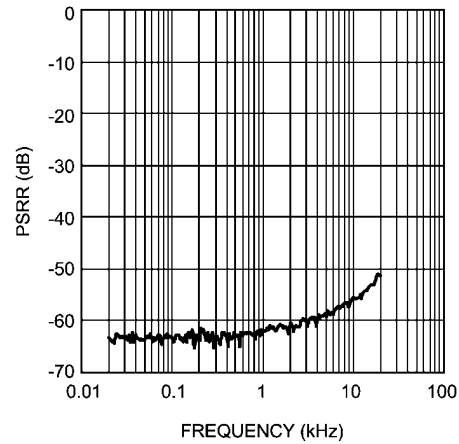
301692b0

**PSRR vs FREQUENCY**  
 $DV_{DD} = 1.8V$ ,  $V_{RIPPLE} = 200mV_{P-P}$ ,  $R_L = 8\Omega$ ,  
 $I_2S$  mode,  $I_2S$  input = -120dBFS



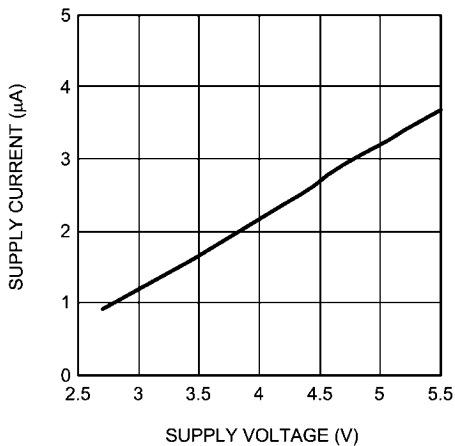
301692b1

**PSRR vs FREQUENCY**  
 $V_{RIPPLE} = 200mV_{P-P}$ ,  $R_L = 8\Omega$ ,  
 ADC mode



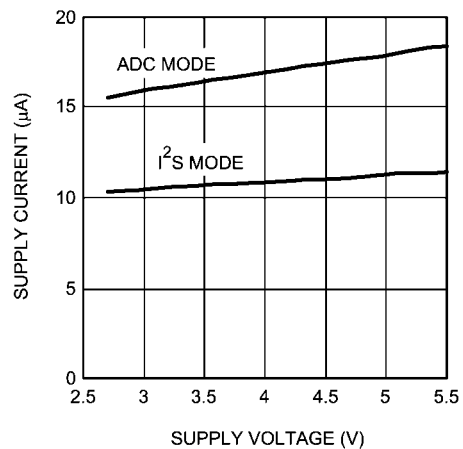
30169297

**SUPPLY CURRENT vs SUPPLY VOLTAGE ( $PV_{DD}$ )**  
 $R_L = \text{Open}$ , ADC mode,  
 All channels enabled



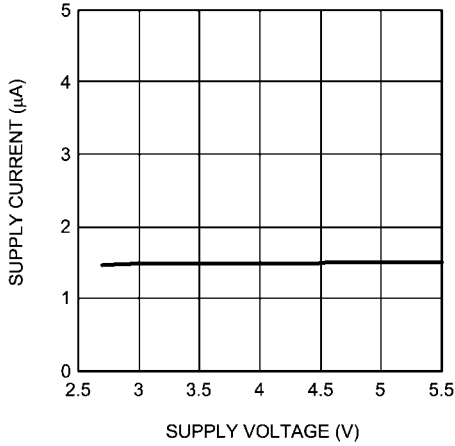
30169298

**SUPPLY CURRENT vs SUPPLY VOLTAGE ( $AV_{DD}$ )**  
 $R_L = \text{Open}$



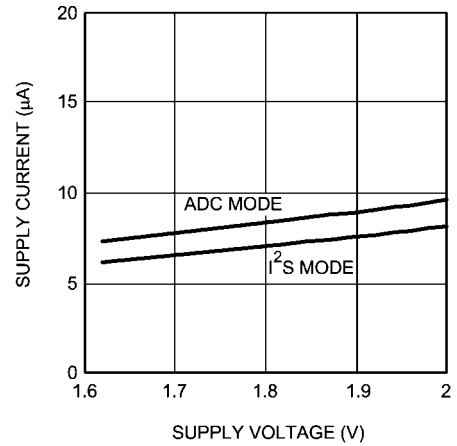
30169299

**SUPPLY CURRENT vs SUPPLY VOLTAGE (PLV<sub>DD</sub>)**  
**ADC mode, All channels enabled**



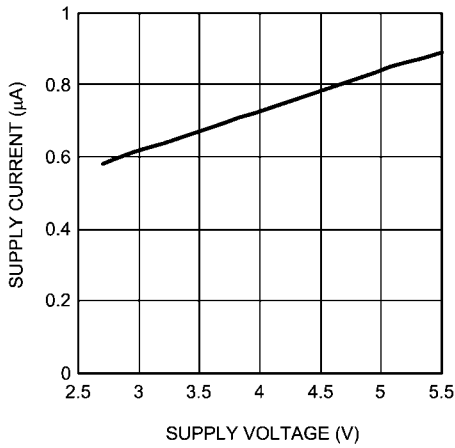
301692a0

**SUPPLY CURRENT vs SUPPLY VOLTAGE (DV<sub>DD</sub>)**  
**R<sub>L</sub> = Open**



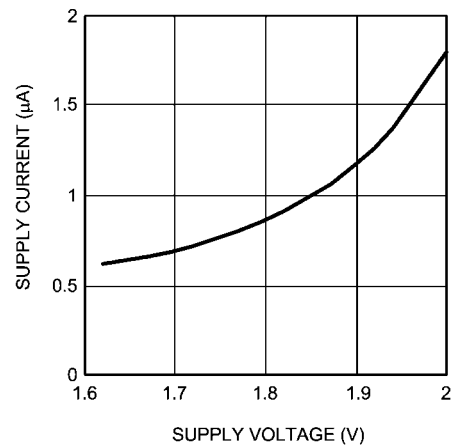
301692a1

**SHUTDOWN CURRENT vs SUPPLY VOLTAGE**



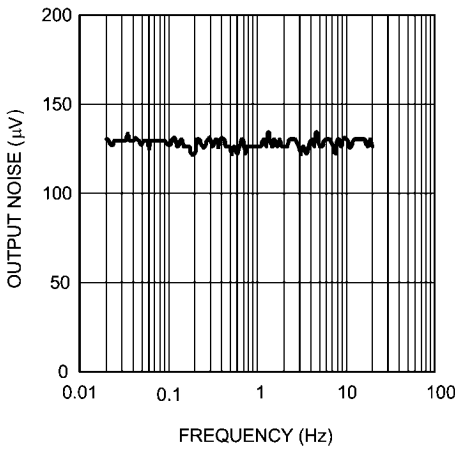
301692a2

**SHUTDOWN CURRENT vs SUPPLY VOLTAGE (DV<sub>DD</sub>)**



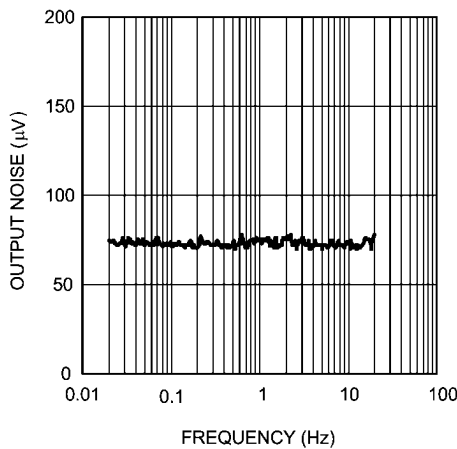
301692a3

**OUTPUT NOISE VS FREQUENCY**  
**PV<sub>DD</sub> = 5V, R<sub>L</sub> = 8Ω,**  
**ADC mode, ADC Input = AC GND**



301692b7

**OUTPUT NOISE VS FREQUENCY**  
**DV<sub>DD</sub> = 1.8V, R<sub>L</sub> = 8Ω,**  
**I<sup>2</sup>S mode, I<sup>2</sup>S Input = -120dBFS**



301692b8



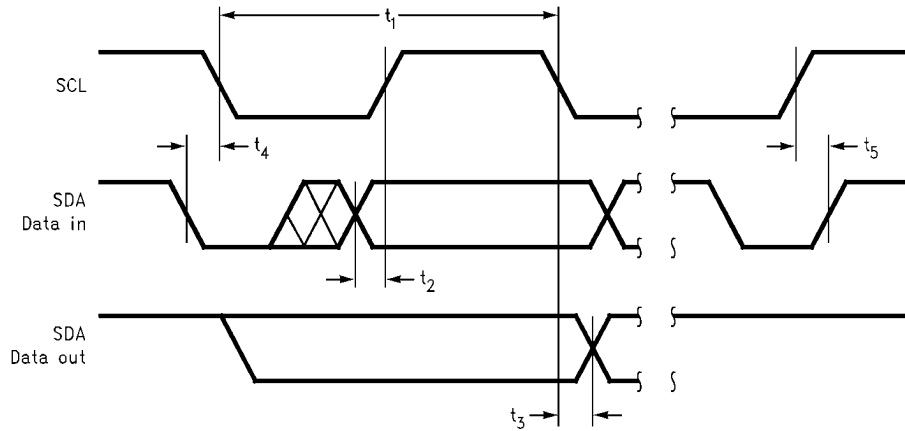
## Application Information

### I<sup>2</sup>C COMPATIBLE INTERFACE

The LM48901 is controlled through an I<sup>2</sup>C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock and data lines are bi-directional (open drain). The LM48901 can communicate at clock rates up to 400kHz. Figure 3 shows the I<sup>2</sup>C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48901 is a transmit/receive device, and can act

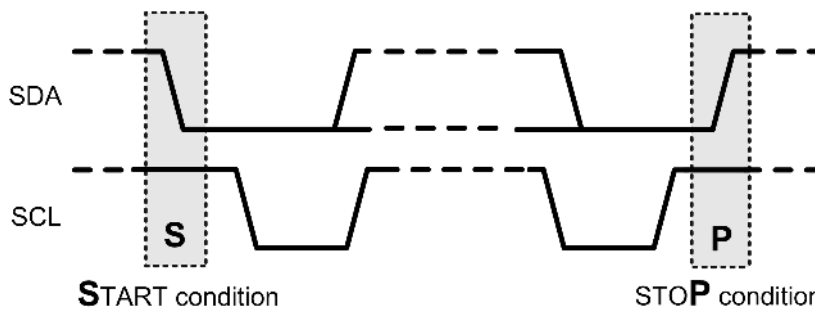
as the I<sup>2</sup>C master, generating the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition Figure 4.

Due to the number of data registers, the LM48901 employs a page mode scheme. Each data write consists of 7, 8 bit data bytes, device address (1 byte), 16 bit register address (2 bytes), and 32 bit register data (4 bytes). Each byte is followed by an acknowledge pulse Figure 5. Single byte read and write commands are ignored. The LM48901 device address is 0110000X.



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FIGURE 3. I<sup>2</sup>C Timing Diagram



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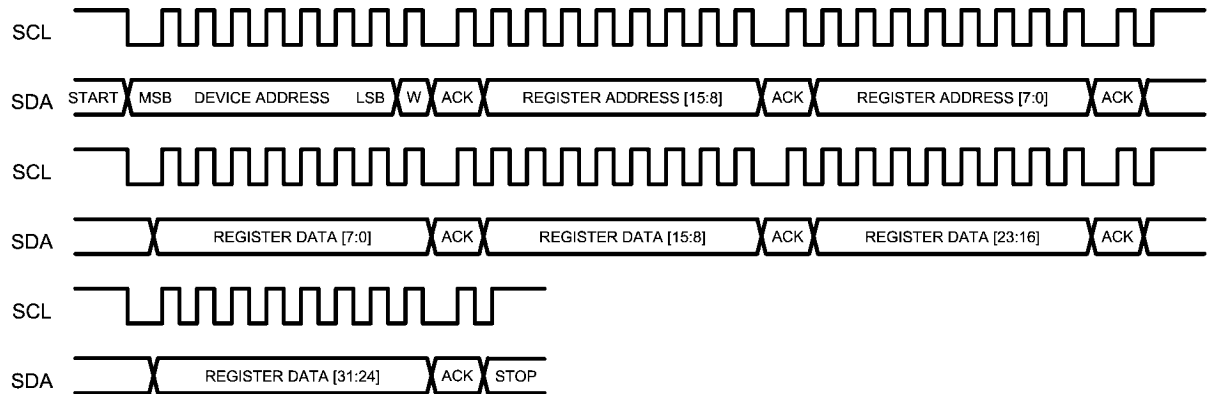
FIGURE 4. Start and Stop Diagram

## WRITE SEQUENCE

The example write sequence is shown in Figure 5. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the  $R/\bar{W}$  bit ( $R/\bar{W} = 0$  indicating the master is writing to the LM48901). The data is latched in on the rising edge of the clock. Each address bit must be stable while SDA is HIGH. After the  $R/\bar{W}$  bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48901 receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK).

Once the master device registers the ACK bit, the first 8-bit register address word is sent, MSB first [15:8]. Each data bit should be stable while SCL is HIGH. After the first 8-bit register address is sent, the LM48901 sends another ACK bit. Upon receipt of acknowledge, the second 8-bit register address word is sent [7:0], followed by another ACK bit. The register data is sent, 8-bits at a time, MSB first in the following order [7:0], [15:8], [23:16], [31:24]. Each 8-bit word is followed by an ACK, upon receipt of which the successive 8-bit word is sent. Following the acknowledgement of the last register data word [31:24], the master issues a STOP bit, allowing SDA to go high while SDA is high.



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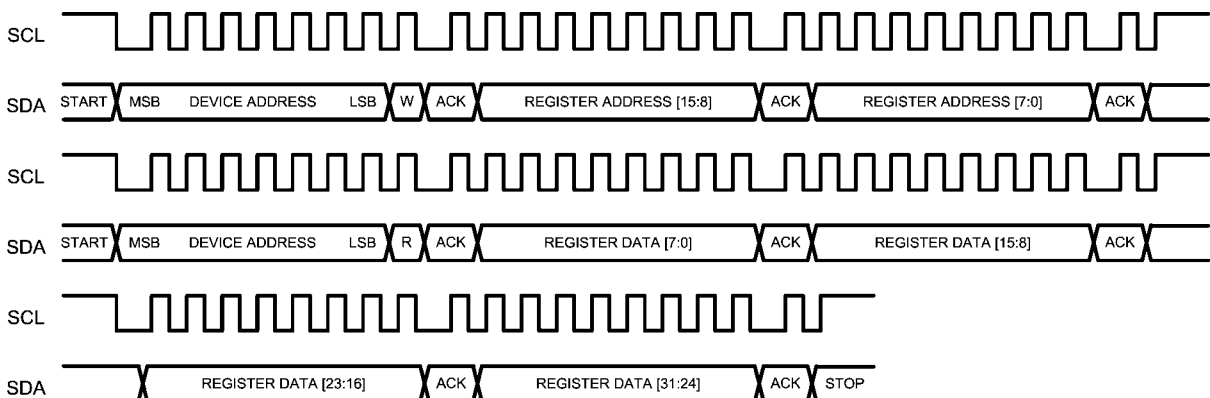
FIGURE 5. Example I<sup>2</sup>C Write Sequence

## READ SEQUENCE

The example read sequence is shown in Figure 6. The START signal, the transition of SDA from HIGH to LOW while SDA is HIGH, is generated, altering all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, followed by the  $R/\bar{W}$  bit ( $R/\bar{W} = 0$ ). After the  $R/\bar{W}$  bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48901 receives the correct address, the device pulls the SDA line low, generating and acknowledge bit (ACK). Once the master device registers the ACK bit, the first 8-bit register address word is sent, MSB first [15:8], followed by and ACK from the

LM48901. Upon receipt of the acknowledge, the second 8-bit register address word is sent [7:0], followed by another ACK bit. Following the acknowledgement of the last register address, the master initiates a REPEATED START, followed by the 7-bit device address, followed by  $R/\bar{W} = 1$  ( $R/\bar{W} = 1$  indicating the master wants to read data from the LM48901). The LM48901 sends an ACK, followed by the selected register data. The register data is sent, 8-bits at a time, MSB first in the following order [7:0], [15:8], [23:16], [31:24]. Each 8-bit word is followed by an ACK, upon receipt of which the successive 8-bit word is sent. Following the acknowledgement of the last register data word [31:24], the master issues a STOP bit, allowing SDA to go high while SDA is high.



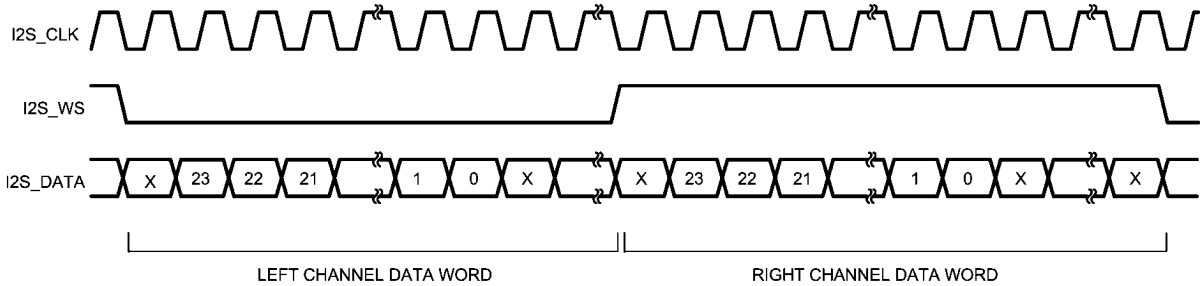
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FIGURE 6. Example I<sup>2</sup>C Read Sequence

**I<sup>2</sup>S DATA FORMAT**

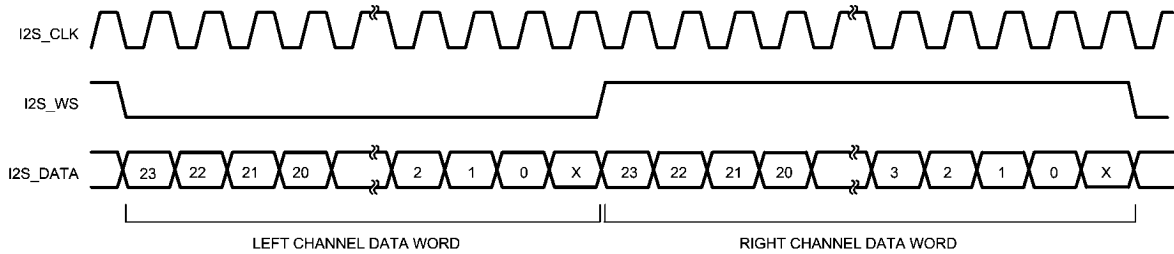
The LM48901 supports three I<sup>2</sup>S formats: Normal Mode [Figure 7](#), Left Justified Mode [Figure 8](#), and Right Justified Mode [Figure 9](#). In Normal Mode, the audio data is transmitted MSB first, with the unused bits following the LSB. In Left Justified

Mode, the audio data format is similar to the Normal Mode, without the delay between the LSB and the change in I<sup>2</sup>S\_WS. In Right Justified Mode, the audio data MSB is transmitted after a delay of a preset number of bits.



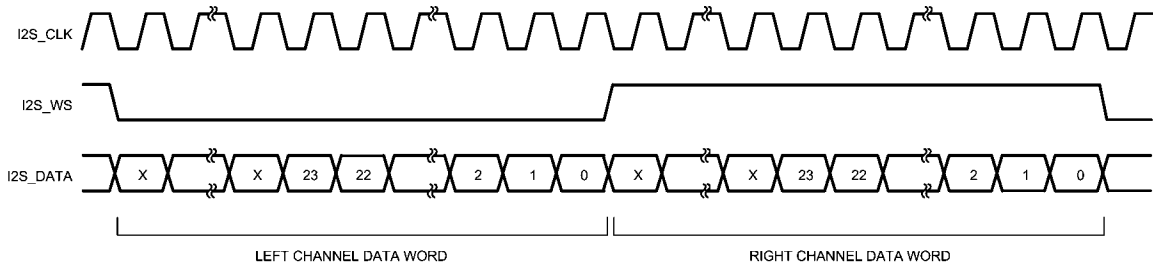
301692b4

**FIGURE 7. I<sup>2</sup>S Normal Input Format**



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**FIGURE 8. I<sup>2</sup>S Left Justified Input Format**



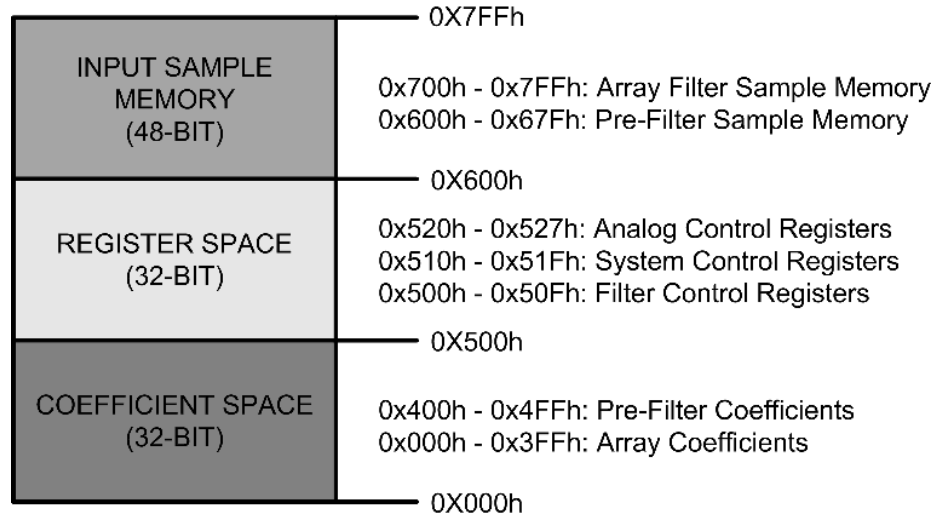
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**FIGURE 9. I<sup>2</sup>S Right Justified Input Format**

**MEMORY ORGANIZATION**

The LM48901 memory is organized into three main regions: a 32-bit wide Coefficient Space that holds the spatial coefficients, a 32-bit wide Register Space that holds the device

configuration settings, and a 48-bit wide Audio Sample Space that holds the current audio data sampled from either the AD-Cs or the I2S interface, organized as shown in [Figure 10](#).



30169207

**FIGURE 10. LM48901 Memory Organization****COEFFICIENT MEMORY**

The device must be in Debug mode in order to write to the Coefficient memory. Set Bit 7 (DBG\_ENABLE) in Filter Debug

Register 1 (0x504h) = 1 to enable Debug mode. The Coefficient Memory Space is organized as follows.

**TABLE 2. Coefficient Memory Space**

REGISTER ADDRESS	REGISTER CONTENTS	
	(31:16)	(15:0)
0x000h - 0x0FFh	256x16 bit Array Taps (Right Input to OUT4)	256x16 bit Array Taps (Left Input to OUT4)
0x100h - 0x1FFh	256x16 bit Array Taps (Right Input to OUT3)	256x16 bit Array Taps (Left Input to OUT3)
0x200h - 0x2FFh	256x16 bit Array Taps (Right Input to OUT2)	256x16 bit Array Taps (Left Input to OUT2)
0x300h - 0x3FFh	256x16 bit Array Taps (Right Input to OUT1)	256x16 bit Array Taps (Left Input to OUT1)
0x400h - 0x47Eh (EVEN)	C2 128x16 bit Prefilter Taps (Right to Right)	C0 128x16 bit Prefilter FIR Taps (Left to Left)
0x441h - 0x47Fh (ODD)	C3 128x16 bit Prefilter Taps (Right to Left)	C1 128x16 bit Prefilter FIR Taps (Left to Right)

## CONTROL REGISTERS

TABLE 3. Register Map

Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0
FILTER CONTROL	0x500h [7:0]	0xFFh	ARRAY_TAP							
	0x500h [15:8]	0xFFh	UNUSED	PRE_TAP						
	0x500h [23:16]	0xE4h	CH4_SEL		CH3_SEL		CH2_SEL		CH1_SEL	
	0x500h [31:24]	0x31h	ARRAY_ENABLE	PRE_ENABLE	ARRAY_BYPASS	PRE_BYPASS	UNUSED			
FILTER COMP1	0x501h [7:0]	0x00h	G1_GAIN			COMP_TH				
	0x501h [15:8]	0x00h	UNUSED	POST_GAIN			UNUSED	COMP_RATIO		
	0x501h [23:16]	0x00h	ARRAY_COMP_SELECT							
	0x501h [31:24]	0x00h	UNUSED							
FILTER COMP2	0x502h [7:0]	0x00h	G1_GAIN			COMP_TH				
	0x502h [15:8]	0x00h	UNUSED	POST_GAIN			UNUSED	COMP_RATIO		
	0x502h [23:16]	0x00h	G1_GAIN			COMP_TH				
	0x502h [31:24]	0x00h	UNUSED	POST_GAIN			UNUSED	COMP_RATIO		
FILTER DEBUG0	0x503h [7:0]	0xFFh	DBG_DATA [7:0]							
	0x503h [15:8]	0xFFh	DBG_DATA [15:8]							
	0x503h [23:16]	0xFFh	DBG_DATA [23:16]							
	0x503h [31:24]	0xFFh	DBG_STEP	UNUSED						
FILTER DEBUG1	0x504h [7:0]	0xFFh	DBG_ENABLE	STEP_ENABLE	UNUSE D	FILTER_SELECT	ACC_ADDR			
	0x504h [15:8]	0xFFh	UNUSED							
	0x504h [23:16]	0xFFh	UNUSED							
	0x504h [31:24]	0xFFh	UNUSED							
FILTER STATS	0x505h [7:0]	0x00h	COUNT1_MODE				CH_SEL			
	0x505h [15:8]	0x80h	CLEAR	UNUSED			COUNT2_MODE			
	0x505h [23:16]	0x00h	COUNT1_MODE				CH_SEL			
	0x505h [31:24]	0x80h	CLEAR	UNUSED			COUNT2_MODE			

Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0
FILTER TAP (READ-ONLY)	0x508h [7:0]	0x7Fh	TAP_LENGTH							
	0x508h [15:8]	0x00h	UNUSED							
	0x508h [23:16]	0x00h	UNUSED							
	0x508h [31:24]	0x00h	UNUSED							
ACCUML DEBUG (READ-ONLY)	0x509h [7:0]	0x00h	DBG_ACCL [7:0]							
	0x509h [15:8]	0x00h	DBG_ACCL [15:8]							
	0x509h [23:16]	0x00h	DBG_ACCL [23:16]							
	0x509h [31:24]	0x00h	DBG_ACCL [31:24]							
ACCUMH DEBUG (READ-ONLY)	0x50Ah [7:0]	0x00h	DBG_ACCH							
	0x50Ah [15:8]	0x00h	BDG_ACCH							
	0x50Ah [23:16]	0x00h	UNUSED							
	0x50Ah [31:24]	0x00h	UNUSED							
DBG SAT (READ-ONLY)	0x50Bh [7:0]	0x00h	DBG_SAT [7:0]							
	0x50Bh [15:8]	0x00h	DBG_SAT [15:8]							
	0x50Bh [23:16]	0x00h	DBG_SAT [23:16]							
	0x50Bh [31:24]	0x00h	UNUSED							
STAT PCNT1 (READ-ONLY)	0x50Ch [7:0]	0x00h	COUNT [7:0]							
	0x50Ch [15:8]	0x00h	COUNT [15:8]							
	0x50Ch [23:16]	0x00h	COUNT [23:16]							
	0x50Ch [31:24]	0x00h	OVF	COUNT [30:24]						
STAT PCNT2 (READ-ONLY)	0x50Dh [7:0]	0x00h	COUNT [7:0]							
	0x50Dh [15:8]	0x00h	COUNT [15:8]							
	0x50Dh [23:16]	0x00h	COUNT [23:16]							
	0x50Dh [31:24]	0x00h	OVF	COUNT [30:24]						

Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0
STAT ACNT1 (READ-ONLY)	0x50Eh [7:0]	0x00h	COUNT [7:0]							
	0x50Eh [15:8]	0x00h	COUNT [15:8]							
	0x50Eh [23:16]	0x00h	COUNT [23:16]							
	0x50Eh [31:24]	0x00h	OVF	COUNT [30:24]						
STAT ACNT2 (READ-ONLY)	0x50Fh [7:0]	0x00h	COUNT [7:0]							
	0x50Fh [15:8]	0x00h	COUNT [15:8]							
	0x50Fh [23:16]	0x00h	COUNT [23:16]							
	0x50Fh [31:24]	0x00h	OVF	COUNT [30:24]						
SYS CONFIG	0x530h [7:0]	0x30h	CONFIG_CLK_ENABLE	DEVICE_ID						
	0x530h [15:8]	0x00h	ALTID_ENABLE	ALT_DEVICE_ID						
	0x530h [23:16]	0x8Ch	CL_ENABLE	UNUSED	CL_PAGE			CL_W	CL_REQ	
	0x530h [31:24]	0x00h	UNUSED						MBIST1_ENABLE	MBIST0_ENABLE
CL REG0	0x531h [7:0]	0x00h	TRANS_LENGTH [7:0]							
	0x531h [15:8]	0x10h	TRANS_LENGTH [15:8]							
	0x531h [23:16]	0x00h	REG_START_ADDR [7:0]							
	0x531h [31:24]	0x00h	REG_START_ADDR [16:8]							
CL REG1	0x532h [7:0]	0x00h	E2_START_ADDR [7:0]							
	0x532h [15:8]	0x00h	E2_START_ADDR [15:8]							
	0x532h [23:16]	0x00h	UNUSED							
	0x532h [31:24]	0x00h	UNUSED							
E2_OFFSET	0x533h [7:0]	0x00h	UNUSED	E2_OFFSET						
	0x533h [15:8]	0x00h	UNUSED							
	0x533h [23:16]	0x00h	UNUSED							
	0x533h [31:24]	0x00h	UNUSED							

Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0	
I <sup>2</sup> C_EnXT	0x534h [7:0]	0x00h	I <sup>2</sup> C_EnXT	UNUSED	E2NXT_OFFSET						
	0x534h [15:8]	0x00h	UNUSED								
	0x534h [23:16]	0x00h	UNUSED								
	0x534h [31:24]	0x00h	UNUSED								
MBIST STAT (READ-ONLY)	0x538h [7:0]	0x7Fh	UNUSED		MBIST_EN		MBIST_GO		MBIST_DONE		
	0x538h [15:8]	0x80h	UNUSED								
	0x538h [23:16]	0x00h	UNUSED								
	0x538h [31:24]	0x80h	UNUSED								
DELAY	0x520h [7:0]	0x06h	POWER_UP_DELAY [7:0]								
	0x520h [15:8]	0x00h	POWER_UP_DELAY [15:8]								
	0x520h [23:16]	0x20h	DEGLITCH_DELAY								
	0x520h [31:24]	0x09h	STATE_DELAY								
ENABLE & CLOCKS	0x521h [7:0]	0x00h	UNUSED				VREF_DELAY	PULSE	FORCE	ENABLE	
	0x521h [15:8]	0x00h	UNUSED	QSA_CLK_STOP	HIFI	PCM_CLK_SEL	I <sup>2</sup> S_CLK	MCLK_RATE			
	0x521h [23:16]	0x00h	UNUSED							ADC_SYNC	
	0x521h [31:24]	0x00h	UNUSED								
DIGITAL MIXER	0x522h [7:0]	0x33h	ZERO_CROSS	MUTE	ADC_LVL						
	0x522h [15:8]	0x33h	UNUSED		I <sup>2</sup> S_LVL						
	0x522h [23:16]	0x00h	I <sup>2</sup> SB_ON	I <sup>2</sup> SA_ON	I <sup>2</sup> SB_TX_SEL		I <sup>2</sup> SA_TX_SEL		ADC_DSP	I <sup>2</sup> S_DSP	
	0x522h [31:24]	0x00h	OUT4_SEL		OUT3_SEL		OUT2_SEL		OUT1_SEL		
ANALOG	0x523h [7:0]	0x00h	BYPASS_MOD	AUTO_SD	ADC_TRIM	ZERO_DIG	ZERO_ANA	PARALLEL	ANA_LVL		
	0x523h [15:8]	0x00h	UNUSED			SE_MOD	PMC_TEST	TSD_DIS	SCKT_DIS	TST_SHT	
	0x523h [23:16]	0x00h	UNUSED								
	0x523h [31:24]	0x00h	UNUSED								



Register Name	Register Address	Default Value	7	6	5	4	3	2	1	0	
I2S PORT	0x524h [7:0]	0x01h	SYNC_ MODE	STEREO_ SYNC_ PHASE	CLOCK_ PHASE	SYNC_ MS	CLK_MS	TX_ ENABLE	RX_ ENABLE	STEREO	
	0x524h [15:8]	0x00h	UNUSED		HALF_CYCLE_DIVIDER						
	0x524h [23:14]	0x00h	UNUSED				SYNTH_ DENOM	SYNTH_NUM			
	0x524h [31:24]	0x00h	UNUSED		MONO_SYNC_WIDTH			SYNC_RATE			
	0x525h [7:0]	0x00h	TX_BIT		TX_WIDTH			RX_WIDTH			
	0x525h [15:8]	0x02h	RX_ A/ $\mu$ LAW	RX_ COMPAN D	RX_MSB_POSITION					RX_ MODE	
	0x525h [23:16]	0x02h	TX_ A/ $\mu$ LAW	TX_ COMPAN D	TX_MSB_POSITION					TX_ MODE	
	0x525h [31:24]	0x00h	UNUSED								
ADC TRIM CO-EFFICIENT	0x526h [7:0]	0x00h	ADC_COMP_COEFF_C0 [7:0]								
	0x526h [15:8]	0x00h	ADC_COMP_COEFF_C0 [15:8]								
	0x526h [23:14]	0x00h	ADC_COMP_COEFF_C1 [7:0]								
	0x526h [31:24]	0x00h	ADC_COMP_COEFF_C1 [15:8]								
	0x527h [7:0]	0x00h	ADC_COMP_COEFF_C2 [7:0]								
	0x527h [15:8]	0x00h	ADC_COMP_COEFF_C2 [15:8]								
READBACK (READ-ONLY)	0x528h [7:0]	0x00h	UNUSED		I2SL_ LVL CLIP	I2SR_ LVL CLIP	ADCL_ LVL CLIP	ADCR_ LVL CLIP	ADCL_ CLIP	ADCR_ CLIP	
	0x528h [15:8]	0x00h	UNUSED			THERMAL	SHORT4	SHORT3	SHORT2	SHORT1	
	0x528h [23:14]	0x00h	SPARE								
	0x528h [31:24]	0x00h	UNUSED								
READBACK (READ-ONLY)	0x529h [7:0]	0x00h	UNUSED				CE_STATE				
	0x529h [15:8]	0x00h	SPARE								
	0x529h [23:14]	0x00h	UNUSED								
	0x529h [31:24]	0x00h	UNUSED								

#### FILTER CONTROL REGISTER (0x500h)

Configures the LM48901 Array and Pre-Array filters (Spatial Engine). The Filter Control Register sets the length of the Array and Pre-Array filter taps, and selects the filter channel source for each audio output. Set PRE\_BYPASS and ARRAY\_BYPASS to 1 to bypass the Spatial Engine, disabling the spatial effect without modifying the coefficients. Set PRE\_ENABLE and ARRAY\_ENABLE

to 1 to enable the Spatial Engine. Set PRE\_ENABLE and ARRAY\_ENABLE to 0 to disable the spatial engine. Disabling the Spatial Engine does not affect the register contents. Disable the Spatial Engine during coefficient programming.

**TABLE 4. Filter Control Register**

BIT	NAME	VALUE	DESCRIPTION
7:0	ARRAY_TAP		Array Filter Tap Length
14:8	PRE_TAP		Pre-filter Tap Length. Pre-filter tap length should be less than or equal to the Array filter tap length
15	UNUSED		
17:16	CH1_SEL		Channel 1 Output Routing Selection
		00	Array Filter Channel 0 Output Select
		01	Array Filter Channel 1 Output Select
		10	Array Filter Channel 2 Output Select
		11	Array Filter Channel 3 Output Select
19:18	CH2_SEL		Channel 2 Output Routing Selection
		00	Array Filter Channel 0 Output Select
		01	Array Filter Channel 1 Output Select
		10	Array Filter Channel 2 Output Select
		11	Array Filter Channel 3 Output Select
21:20	CH3_SEL		Channel 3 Output Routing Selection
		00	Array Filter Channel 0 Output Select
		01	Array Filter Channel 1 Output Select
		10	Array Filter Channel 2 Output Select
		11	Array Filter Channel 3 Output Select
23:22	CH4_SEL		Channel 4 Output Routing Selection
		00	Array Filter Channel 0 Output Select
		01	Array Filter Channel 1 Output Select
		10	Array Filter Channel 2 Output Select
		11	Array Filter Channel 3 Output Select
27:24	UNUSED		
28	PRE_BYPASS	0	Pre-Array filter not bypassed
		1	Pre-Array filter bypassed
29	ARRAY_BYPASS	0	Array filter not bypassed
		1	Array filter bypassed
30	PRE_ENABLE	0	Pre-Array filter disabled. Disable the Pre-Array Filter during filter and coefficient programming. Disabling the Pre-Array Filter does not affect the device memory contents.
		1	Pre-Array filter enabled
31	ARRAY_ENABLE	0	Array filter disabled. Disable the Array Filter during filter and coefficient programming. Disabling the Array Filter does not affect the device memory contents.
		1	Array filter enabled

## COMPRESSOR CONTROL REGISTER 1 (FILTER COMP1) (0x501h)

TABLE 5. Compressor Control Register

BIT	NAME	VALUE	DESCRIPTION
4:0	COMP_TH		Pre-Filter Compressor Threshold
		00000	0
		00001	0.3125
		00010	0.0625
		-	-
		10000	0.5
		-	-
		11000	0.75
		-	-
		11111	0.96875
7:5	G1_GAIN		Pre-Compression Gain (V/V)
		000	2
		001	4
		010	8
		011	16
		100	32
		101	64
		110	128
		111	256
10:8	COMP_RATIO		Compression Ratio
		000	1:1
		001	2:1
		010	2.66:1
		011	4:1
		100	5.33:1
		101	8:1
		110	10.66:1
		111	16:1
11	UNUSED		
14:12	POST_GAIN		Post Compression Gain (V/V)
		000	1
		001	1.25
		010	1.5
		011	2
		100	2.5
		101	3
		110	4
		111	8
15	UNUSED		

BIT	NAME	VALUE	DESCRIPTION
23:16	ARRAY_COMP_SELECT		Array Filter Compression Control Register Select. The Array Filter has four channels, each channel can choose one of two Array Filter Compression Threshold, Pre-Compression Gain, Compression Ratio, and Post Compression Gain settings from the FILTER_COMP2 register Table 4.
		0000	Select Setting 0
		-	-
		1111	Select Setting 1
31:24	UNUSED		

**COMPRESSOR CONTROL REGISTER 2 (FILTER COMP2) (0x502h)**

**TABLE 6. Compressor Control Register 2**

BIT	NAME	VALUE	DESCRIPTION
4:0	COMP_TH		Array Filter Compressor Threshold (Setting 0)
		00000	0
		00001	0.03125
		00010	0.0325
		-	-
		10000	0.5
		-	-
		11000	0.75
		-	-
		11111	0.96875
7:5	G1_GAIN		Pre-Compression Gain (V/V) (Setting 0)
		000	2
		001	4
		010	8
		011	16
		100	32
		101	64
		110	128
		111	256
10:8	COMP_RATIO		Compression Ratio (Setting 0)
		000	1:1
		001	2:1
		010	2.66:1
		011	4:1
		100	5.33:1
		101	8:1
		110	10.66:1
111	16:1		
11	UNUSED		

BIT	NAME	VALUE	DESCRIPTION
14:12	POST_GAIN		Post Compression Gain (V/V) (Setting 0)
		000	1
		001	1.25
		010	1.5
		011	2
		100	2.5
		101	3
		110	4
111	8		
15	UNUSED		
20:16	COMP_TH		Pre-Filter Compressor Threshold (Setting 1)
		00000	0
		00001	0.03125
		00010	0.0325
		-	-
		10000	0.5
		-	-
		11000	0.75
-	-		
11111	0.96875		
23:21	G1_GAIN		Pre-Compression Gain (V/V) (Setting 1)
		000	2
		001	4
		010	8
		011	16
		100	32
		101	64
		110	128
111	256		
24:26	COMP_RATIO		Compression Ratio (Setting 1)
		000	1:1
		001	2:1
		010	2.66:1
		011	4:1
		100	5.33:1
		101	8:1
		110	10.66:1
111	16:1		
27	UNUSED		
30:28	POST_GAIN		Post Compression Gain (V/V) (Setting 1)
		000	1
		001	1.25
		010	1.5
		011	2
		100	2.5
		101	3
		110	4
111	8		
31	UNUSED		

**FILTER DEBUG REGISTER 1 (FILT\_DBG1) (0x504h)****TABLE 7. Filter Debug Register 1**

BIT	NAME	VALUE	DESCRIPTION
3:0	ACC_ADDR		Accumulator Address. Selects which accumulator is read during debug mode
4	FILTER_SELECT	0	Selects Pre-Filter Accumulators
		1	Selects Array Filter Accumulators
5	UNUSED		
6	STEP_ENABLE	0	Single Step Disabled
		1	Single Step Enabled
7	DBG_ENABLE	0	Debug Mode Disabled. Coefficient memory is inaccessible with Debug mode is disabled.
		1	Debug Mode Enabled. Coefficient memory is accessible when Debug mode is enabled.
31:8	UNUSED		

**FILTER STATISTICS CONTROL REGISTER (FILT\_STC) (0x505h)****TABLE 8. Filter Statistics Control Register**

BIT	NAME	VALUE	DESCRIPTION
PRE-FILTER Counter			
3:0	CH_SEL		Channel Select
		000	Channel 0
		001	Channel 1
		010	Channel 2
		011	Channel 3
		100	Channel 4
		101	Channel 5
		110	Channel 6
7:4	COUNT1_MODE		Counter 1 Mode Select. Specifies input of Counter 1
		0000	Sample Count Mode. Every audio sample is counted
		0001	Overflow. Overflow events counted
		0010	Frequency Error. Indicates input frequency not sufficient for given filter length
		1000	MAGN[7]
		1001	MAGN[7:6]
		1010	MAGN[7:5]
		1011	MAGN[7:4]
		1100	MAGN[7:3]
		1101	MAGN[7:2]
		1110	MAGN[7:1]
		1111	MAGN[7:0]

BIT	NAME	VALUE	DESCRIPTION
11:8	COUNT2_MODE		Counter 2 Mode Select. Specifies input of Counter 2
		0000	Sample Count Mode. Every audio sample is counted
		0001	Overflow. Overflow events counted
		0010	Frequency Error. Indicates input frequency not sufficient for given filter length
		1000	MAGN[7]
		1001	MAGN[7:6]
		1010	MAGN[7:5]
		1011	MAGN[7:4]
		1100	MAGN[7:3]
		1101	MAGN[7:2]
		1110	MAGN[7:1]
1111	MAGN[7:0]		
14:12	UNUSED		
15	CLEAR	0	Counter Enabled
		1	Counter Cleared
ARRAY-FILTER Counter			
19:16	CH_SEL		Channel Select
		000	Channel 0
		001	Channel 1
		010	Channel 2
		011	Channel 3
		100	Channel 4
		101	Channel 5
		110	Channel 6
		111	Channel 7
23:20	COUNT1_MODE		Counter 1 Mode Select. Specifies input of Counter 1
		0000	Sample Count Mode. Every audio sample is counted
		0001	Overflow. Overflow events counted
		0010	Frequency Error. Indicates input frequency not sufficient for given filter length
		1000	MAGN[7]
		1001	MAGN[7:6]
		1010	MAGN[7:5]
		1011	MAGN[7:4]
		1100	MAGN[7:3]
		1101	MAGN[7:2]
		1110	MAGN[7:1]
1111	MAGN[7:0]		

BIT	NAME	VALUE	DESCRIPTION
27:24	COUNT2_MODE		Counter 2 Mode Select. Specifies input of Counter 2
		0000	Sample Count Mode. Every audio sample is counted
		0001	Overflow. Overflow events counted
		0010	Frequency Error. Indicates input frequency not sufficient for given filter length
		1000	MAGN[7]
		1001	MAGN[7:6]
		1010	MAGN[7:5]
		1011	MAGN[7:4]
		1100	MAGN[7:3]
		1101	MAGN[7:2]
		1110	MAGN[7:1]
		1111	MAGN[7:0]
30:28	UNUSED		
31	CLEAR	0	Counter Enabled
		1	Counter Cleared

**DELAY REGISTER (DELAY) (0x520h)****TABLE 9. Delay Register**

BIT	NAME	VALUE	DESCRIPTION
15:0	POWER_UP_DELAY		Sets I2C Delay Time. Default 10ms delay.
23:16	DEGLITCH_DELAY		Sets ENABLE Bit Polling Timeout. Default 32ms delay
31:24	STATE_DELAY		Sets Delay Between Power Up/Down States

**ENABLE AND CLOCK CONFIGURATION REGISTER (ENABLE & CLOCKS) (0x521h)****TABLE 10. Enable and Clock Configuration Register**

BIT	NAME	VALUE	DESCRIPTION
0	ENABLE	0	Device Disabled in I <sup>2</sup> C Mode
		1	Device Enabled in I <sup>2</sup> C Mode
1	FORCE	0	Device Enabled Via SHDN <<overbar>> Pin
		1	Device Enabled Via I <sup>2</sup> C
2	PULSE	0	SHDN<<overbar>> Requires a Stable Logic Level
		1	SHDN<<overbar>> Accepts a Pulse Input
3	RELY_ON_VREF	0	Device waits for delay time determined by STATE_DELAY to enable.
		1	Device waits for stable VREF
7:4	UNUSED		
10:8	MCLK_RATE		Selects PLL Input Divider
		000	32fs (1.536MHz)
		001	64fs (3.072MHz)
		010	128fs (6.114MHz)
		011	256fs (12.288MHz)
		100	512fs (24.576MHz)
		101	UNUSED
		110	UNUSED
11	I2S_CLK	0	MCLK Input to PLL
		1	I <sup>2</sup> S_CLK Input to PLL



BIT	NAME	VALUE	DESCRIPTION
12	PMC_CLK_SEL	0	Oscillator Clock Input to Power Management Circuitry
		1	External Clock to Power Management Circuitry. Power management circuit uses MCLK or I <sup>2</sup> S_CLK. Clock source depends on the state of I <sup>2</sup> S_CLK. External Clock mode disables the internal oscillator.
13	HIFI	0	HiFi Mode Disabled
		1	HiFi Mode Enabled. PLL always produces a 4096fs clock.
14	QSA_CLK_STOP	0	QSA Clock Enabled
		1	QSA Clock Disabled Following Device Configuration
15	UNUSED		
16	ADC_SYNC_SEL	0	Normal Operation
		1	Reverse ADC SYNC Signal for additional timing margin at low supply voltages.
31:17	UNUSED		

#### DIGITAL MIXER CONTROL REGISTER (DIGITAL MIXER) (0x522h)

TABLE 11. Digital Mixer Control Register

BIT	NAME	VALUE	DESCRIPTION
5:0	ADC_LVL		Sets the Gain of the ADC Path (dB)
		000000	-76.5
		000001	-75
		-	1.5dB steps
		110010	-1.5
		110011	0
		110100	1.5
		-	1.5dB Steps
6	MUTE	0	Normal Operation
		1	Mute
7	ZXD_DISABLE	0	Zero Crossing Detection Enabled
		1	Zero Crossing Detection Disabled
13:8	I <sup>2</sup> S_LVL		Sets the Gain of the I <sup>2</sup> S Path (dB)
		000000	-76.5
		000001	-75
		-	1.5dB steps
		110010	-1.5
		110011	0 ( $V_{OUT} = 3.36V_{RMS}$ with 0dBFS input)
		110100	1.5
		-	1.5dB Steps
111111	18		
15:14	UNUSED		
16	I <sup>2</sup> S_DSP	0	I <sup>2</sup> S Data Not Passed to DSP
		1	I <sup>2</sup> S Data Passed to DSP
17	ADC_DSP	0	ADC Output Not Passed to DSP
		1	ADC Output Passed to DSP

BIT	NAME	VALUE	DESCRIPTION
19:18	ISA_TX_SEL		Selects Input of Primary I <sup>2</sup> S Transmitter
		00	None
		01	ADC
		10	DSP1/2
		11	DSP3/4
21:20	ISB_TX_SEL		Selects Input of Secondary I <sup>2</sup> S Transmitter
		00	None
		01	ADC
		10	DSP1/2
		11	DSP3/4
22	I <sup>2</sup> SA_ON	0	I <sup>2</sup> SA Data NOT Output on $\overline{\text{SHDN}}$
		1	I <sup>2</sup> SA Data Output on $\overline{\text{SHDN}}$
23	I <sup>2</sup> SB_ON	0	I <sup>2</sup> SB Data NOT Output on $\overline{\text{SHDN}}$
		1	I <sup>2</sup> SB Data Output on $\overline{\text{SHDN}}$
25:24	OUT1_SEL		Selects OUT1 Amplifier Input Source
		00	OUT1 Disabled
		01	DSP
		10	I <sup>2</sup> S
		11	ADC
27:26	OUT2_SEL		Selects OUT2 Amplifier Input Source
		00	OUT2 Disabled
		01	DSP
		10	I <sup>2</sup> S
		11	ADC
29:28	OUT3_SEL		Selects OUT3 Amplifier Input Source
		00	OUT3 Disabled
		01	DSP
		10	I <sup>2</sup> S
		11	ADC
31:30	OUT4_SEL		Selects OUT4 Amplifier Input Source
		00	OUT4 Disabled
		01	DSP
		10	I <sup>2</sup> S
		11	ADC

#### ANALOG CONFIGURATION REGISTER (ANALOG) (0x523h)

TABLE 12. Analog Configuration Register

BIT	NAME	VALUE	DESCRIPTION
1:0	ANA_LVL		Sets ADC Preamp Gain (dB)
		00	0
		01	2.4
		10	3.5
		11	6
2	PARALLEL	0	Normal Operation. OUT2 and OUT3 operate as separate amplifiers.
		1	Parallel Operation. OUT2 and OUT3 operate in parallel as a single amplifier.

BIT	NAME	VALUE	DESCRIPTION
3	ZERO_ANA	0	Normal Operation
		1	Auto-Shutdown Mode. Automatically disables the amplifiers when no analog input is detected.
4	ZERO_DIG	0	Normal Operation
		1	Auto-Shutdown Mode. Automatically disables the amplifiers when there is no I2S input.
5	ADCTRIM	0	ADC Trim Disabled
		1	ADC Trim Enabled. Use ADC_COMP_COEFF_C0-C2 to trim ADC.
6	AUTO_SD	0	Normal Operation
		1	Fault Conditions Disable the Amplifiers
7	BYPASS_MOD	0	Normal Operation
		1	Pulse Correction Bypass. Amplifier output stages act as a buffer, passing PWM signal without correction to output.
8	TST_SHT	0	Normal Operation
		1	Short Amplifier Inputs. Sets amplifier outputs to 50% duty cycle, minimizing click and pop during power up/down.
9	SCKT_DIS	0	Normal Operation
		1	Output Short Circuit Protection Disabled
10	TSD_DIS	0	Normal Operation
		1	Thermal Shutdown Disabled
11	PMC_TEST	0	Normal Operation
		1	PMC uses PLL Source Clock
12	SE_MOD	0	Normal Operation
		1	Single Edge Modulation Mode
31:13	UNUSED		

#### I<sup>2</sup>S PORT CONFIGURATION REGISTER (I<sup>2</sup>S PORT) (0x524h/0x525h)

TABLE 13.

BIT	NAME	VALUE	DESCRIPTION
<b>0x524h</b>			
0	STEREO	0	Mono Mode
		1	Stereo Mode
1	RX_ENABLE	0	Receive Mode Disabled
		1	Receive Mode Enabled
2	TX_ENABLE	0	Transmit Mode Disabled
		1	Transmit Mode Enabled
3	CLK_MS	0	I2S Clock Slave. Device requires an external SCLK for proper operation.
		1	I2S Clock Master. Device generates SCLK and transmits when either RX or TX mode are enabled.
4	SYNC_MS	0	I2S WS Slave. Device requires an external WS for proper operation.
		1	I2S WS Master. Device generates WS and transmits when either RX or TX mode are enabled.
5	CLOCK_PHASE	0	I2S Clock Phase. Transmit on falling edge, receive on rising edge.
		1	PCM Clock Phase. Transmit on rising edge, receive on falling edge.

BIT	NAME	VALUE	DESCRIPTION
6	STEREO_SYNC_PHASE	0	I2S Data Format: Left, Right
		1	I2S Data Format: Right, Left
7	SYNC_MODE	Mono	Rising edge indicates start of data word.
		0	SYNC low = Left, SYNC high = Right
		1	SYNC low = Right, SYNC high = left
13:8	HALF_CYCLE_DIVIDER		Configures the I2S port master clock half-cycle divider. Program the half-cycle divider by: (ReqDiv*2) 1
		000000	BYPASS
		000001	1
		000010	1.5
		000011	2
		-	-
		111101	31
		111110	31.5
111111	32		
15:14	UNUSED		
18:16	SYNTH_NUM		Sets the Clock Generator Numerator
		000	SYNTH_DENOM (1/)
		001	100/SYNTH_DENOM
		010	96/SYNTH_DENOM
		011	80/SYNTH_DENOM
		100	72/SYNTH_DENOM
		101	64/SYNTH_DENOM
		110	48/SYNTH_DENOM
111	0/SYNTH_DENOM		
19	SYNTH_DENOM	0	Clock Generator Denominator = 128
		1	Clock Generator Denominator = 125
23:20	UNUSED		
26:24	SYNC_RATE		Sets number of clock cycles before SYNC pattern repeats.
			MONO MODE
		000	8
		001	12
		010	16
		011	18
		100	20
		101	24
		110	25
		111	32
			STEREO MODE
		000	16
		01	24
		010	32
		011	36
		100	40
		101	48
		110	50
111	64		

BIT	NAME	VALUE	DESCRIPTION
29:27	MONO_SYNC_WIDTH		Sets SYNC symbol width in Mono Mode
		000	1
		001	2
		010	4
		011	7
		100	8
		101	11
		110	15
111	16		
31:30	UNUSED		
0x525h			
2:0	RX_WIDTH		Sets number of valid RECEIVE bits.
		000	24
		001	20
		010	18
		011	16
		100	14
		101	13
		110	12
111	8		
5:3	TX_WIDTH		Sets number of TRANSMIT bits.
		000	24
		001	20
		010	18
		011	16
		100	14
		101	13
		110	12
111	8		
7:6	TX_BIT		Sets number of pad bits after the valid Transmit bits.
		00	0
		01	1
		10	High-Z
		11	High-Z
8	RX_MODE	0	MSB Justified Receive Mode
		1	LSB Justified Receive Mode

BIT	NAME	VALUE	DESCRIPTION
13:9	RX_MSB_POSITION		MSB location from the frame start (MSB Justified) or LSB location from the frame end (LSB Justified)
		00000	0 (DSP/PCM LONG)
		00001	1 (I2S/PCM SHORT)
		00010	2
		00011	3
		00100	4
		00101	5
		00110	6
		00111	7
		01000	8
		01001	9
		01010	10
		01011	11
		01100	12
		01101	13
		01110	14
		01111	15
		10000	16
		10001	17
		10010	18
		10011	19
		10100	20
		10101	21
		10110	22
		10111	23
		11000	24
		11001	25
		11010	26
		11011	27
		11100	28
		11101	29
11110	30		
11111	31		
14	RX_COMPAND	0	Normal Operation
		1	Audio Data Companded
15	RX_A/μLAW	0	μLaw Compand Mode
		1	A-Law Compand Mode
16	TX_MODE	0	MSB Justified Transmit Mode
		1	LSB Justified Transmit Mode

BIT	NAME	VALUE	DESCRIPTION
21:17	TX_MSB_POSITION		MSB location from the frame start (MSB Justified) or LSB location from the frame end (LSB Justified)
		00000	0 (DSP/PCM LONG)
		00001	1 (I2S/PCM SHORT)
		00010	2
		00011	3
		00100	4
		00101	5
		00110	6
		00111	7
		01000	8
		01001	9
		01010	10
		01011	11
		01100	12
		01101	13
		01110	14
		01111	15
		10000	16
		10001	17
		10010	18
		10011	19
		10100	20
		10101	21
		10110	22
		10111	23
		11000	24
		11001	25
		11010	26
		11011	27
		11100	28
		11101	29
11110	30		
11111	31		
22	TX_COMPAND	0	Normal Operation
		1	Audio Data Companded
23	TX_A/ $\mu$ LAW	0	$\mu$ Law Compand Mode
		1	A-Law Compand Mode
31:24	UNUSED		

**ADC TRIM COEFFICIENT REGISTER (ADC\_TRIM) (0x526h/0x527)****TABLE 14. ADC Trim Coefficient Register**

BIT	NAME	VALUE	DESCRIPTION
<b>0x526h</b>			
15:0	ADC_COMP_COEFF_C0		Sets ADC Trim Coefficient C0
31:16	ADC_COMP_COEFF_C1		Sets ADC Trim Coefficient C1
<b>0x527h</b>			
15:0	ADC_COMP_COEFF_C2		Sets ADC Trim Coefficient C2

**READBACK REGISTER (READBACK) (0x528h) READ-ONLY****TABLE 15. Readback Register**

BIT	NAME	VALUE	DESCRIPTION
0	ADCR_CLIP	1	Right Channel ADC Input Clipped
1	ADCL_CLIP	1	Left Channel ADC Input Clipped
2	ADCR_LVLCLIP	1	Right Channel ADC Output Clipped
3	ADCL_LVLCLIP	1	Left Channel ADC Output Clipped
4	I2SR_LVLCLIP	1	Right Channel I2S Output Clipped
5	I2SL_LVLCLIP	1	Left Channel I2S Output Clipped
7:6	UNUSED		
8	SHORT1	1	OUT1 Output Short Circuit
9	SHORT2	1	OUT2 Output Short Circuit
10	SHORT3	1	OUT3 Output Short Circuit
11	SHORT4	1	OUT4 Output Short Circuit
12	THERMAL	1	Thermal Shutdown Threshold Exceeded
23:13	SPARE		
31:24	UNUSED		



## SYSTEM CONFIGURATION REGISTER (SYS\_CONFIG) (0x530h)

TABLE 16. System Configuration Register

BIT	NAME	VALUE	DESCRIPTION
6:0	DEVICE_ID		Sets LM48901 Device ID in slave mode
7	CONFIG_CLK_ENABLE	0	Configuration Loader Clock Disabled
		1	Configuration Loader Clock Enabled
14:8	ALT_DEVICE_ID		Sets Alternate Device ID in Slave Mode.
15	ALTIM_ENABLE	0	Selects DEVICE_ID
		1	Selects ALT_DEVICE_ID
16	CL_REQ	0	Configuration Loader Access not Requested
		1	Configuration Loader Access Requested. I2C Master Transaction Enabled
17	CL_W	0	Configuration Loader Set to READ-ONLY
		1	Configuration Loader Set to WRITE
20:18	CL_PAGE		Sets I2C Page Mode Length
		00	Single Byte
		01	4 Bytes
		10	8 Bytes
		11	16 Bytes
22:21	UNUSED		
23	CL_ENABLE	0	Device Configured as I2C Slave
		1	Device Configured as I2C Master
24	MBIST0_ENABLE	0	Memory BIST Controller 0 Disabled
		1	Memory BIST Control 0 Enabled.
25	MBIST1_ENABLE	0	Memory BIST Controller 1 Disabled
		1	Memory BIST Control 1 Enabled.
31:26	UNUSED		

I<sup>2</sup>C MASTER CONFIGURATION LOADER REGISTER 0 (CL\_REG0) (0x531h)

TABLE 17. Filter Debug Register 0

BIT	NAME	VALUE	DESCRIPTION
15:0	TRANS_LENGTH		Sets I2C Master Transaction Length
31:16	REG_START_ADDR		Starting Address of LM48901 Memory

I<sup>2</sup>C MASTER CONFIGURATION LOADER REGISTER 1 (CL\_REG1) (0x532h)

TABLE 18. Filter Debug Register 1

BIT	NAME	VALUE	DESCRIPTION
15:0	E2_START_ADDR		Sets EEPROM Address. Indicates EEPROM start address where data is stored
31:16	UNUSED		

## EEPROM ADDRESS OFFSET REGISTER (E2\_OFFSET) (0x533h)

TABLE 19. EEPROM Address Offset Register

BIT	NAME	VALUE	DESCRIPTION
5:0	E2_OFFSET		EEPROM Address Offset Value.
31:6	UNUSED		

**I<sup>2</sup>C EnXT REGISTER (I<sup>2</sup>CEnXT) (0x534h)****TABLE 20. I<sup>2</sup>C EnXT Register**

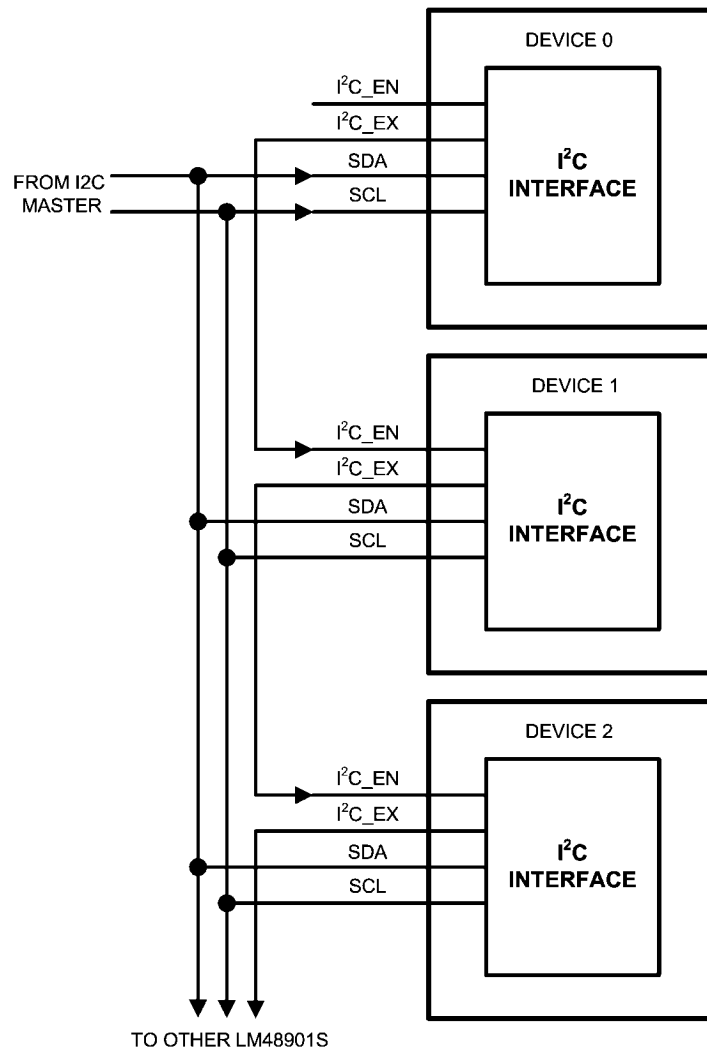
BIT	NAME	VALUE	DESCRIPTION
5:0	E2NXT_OFFSET		Sets EEPROM Address Offset for Following LM48901 when devices are Daisy Chained.
6	UNUSED		
7	I <sup>2</sup> C_EnXT	0	Next Device in Daisy Chain Disabled. I <sup>2</sup> C_EX driven Low.
		1	Next Device in Daisy Chain Enabled. I <sup>2</sup> C_EX driven HIGH.
31:8	UNUSED		

**READ-ONLY MBIST STATUS REGISTER (MBIST\_STAT) (0x538h)****TABLE 21. MBIST Status Register**

BIT	NAME	VALUE	DESCRIPTION
1:0	MBIST_DONE		Logic HIGH indicates memory test complete
3:2	BIST_GO		Logic Low indicates memory fault when MBIST_DONE is HIGH
5:4	MBIST_EN	0	MBIST Read-back Disabled
		1	MBIST Read-back Enabled
31:6	UNUSED		

**DAISY CHAINING****I<sup>2</sup>C\_EN/I<sup>2</sup>C\_EX**

The LM48901 supports daisy chaining up to 127 devices from a single I<sup>2</sup>C bus utilizing I<sup>2</sup>C\_EN and I<sup>2</sup>C\_EX in a chain enable scheme. I<sup>2</sup>C\_EX is a push/pull logic output that drives the I<sup>2</sup>C\_EN of the following device in the chain [Figure 11](#). At power up, I<sup>2</sup>C\_EnXT (bit 8, I<sup>2</sup>C\_EnXT Register [0x534h]) is set to 0, resulting in I<sup>2</sup>C\_EN driven low, disabling the I<sup>2</sup>C interface of the following device. Once device configuration is complete, and I<sup>2</sup>C\_EnXT is set to 1, I<sup>2</sup>C\_EN is driven high, enabling the I<sup>2</sup>C interface of the following device. Driving I<sup>2</sup>C\_EN high enables the device's I<sup>2</sup>C interface, driving I<sup>2</sup>C\_EN low disables the device's I<sup>2</sup>C interface.



30169208

FIGURE 11. I<sup>2</sup>C\_EN/I<sup>2</sup>C\_EX Daisy Chaining Example

### Device Address

The 0110000X is the default LM48901 I<sup>2</sup>C address hard coded into the device. Two alternate device addresses can be programmed, via the SYS CONFIG (0x530h) Register. Use the default address during initial device configuration.

## GENERAL AMPLIFIER FUNCTION

### Class D Amplifier

The LM48901 features four high-efficiency Class D audio power amplifiers that utilizes Texas Instruments' filterless modulation scheme external component count, conserving board space and reducing system cost. The Class D outputs transition from  $V_{DD}$  to GND with a 384kHz switching frequency. With no signal applied, the outputs switch with a 50% duty cycle, in phase, causing the two outputs to cancel. This cancellation results in no net voltage across the speaker, thus there is no current to the load in the idle state.

With the input signal applied, the duty cycle (pulse width) of the LM48901 outputs changes. For increasing output voltage, the duty cycle of OUT<sub>+</sub> increases while the duty cycle of OUT<sub>-</sub> decreases. For decreasing output voltages, the converse occurs. The difference between the two pulse widths yield the differential output voltage.

### Edge Rate Control (ERC)

The LM48901 features Texas Instruments' advanced edge rate control (ERC) that reduces EMI, while maintaining high quality audio reproduction and efficiency. The LM48901 ERC greatly reduces the high frequency components of the output square waves by controlling the output rise and fall times, slowing the transitions to reduce RF emissions, while maximizing THD+N and efficiency performance. The overall result of the E<sup>2</sup>S system is a filterless Class D amplifier that passes FCC Class B radiated emissions standards with 24in of twisted pair cable, with excellent 0.06% THD+N and high 89% efficiency.

## POWER DISSIPATION AND EFFICIENCY

The major benefit of a Class D amplifier is increased efficiency versus a Class AB. The efficiency of the LM48901 is attributed to the region of operation of the transistors in the output stage. The Class D output stage acts as current steering switches, consuming negligible amounts of power compared to their Class AB counterparts. Most of the power loss associated with the output stage is due to the IR loss of the MOSFET on-resistance, along with switching losses due to gate charge.

## ANALOG INPUT

The LM48901 features a differential input, stereo ADC for analog systems. A differential amplifier amplifies the difference between the two input signals. Traditional audio power amplifiers have typically offered only single-ended inputs resulting in a 6dB reduction of SNR relative to differential inputs. The LM48901 also offers the possibility of DC input coupling which eliminates the input coupling capacitors. A major benefit of the fully differential amplifier is the improved common mode rejection ratio (CMRR) over single ended input amplifiers. The increased CMRR of the differential amplifier reduces sensitivity to ground offset related noise injection, especially important in noisy systems.

## PARALLEL MODE

In Parallel mode, channels OUT2 and OUT3 are driven from the same audio source, allowing the two channels to be connected in parallel, increasing output power to 3.2W into 4 $\Omega$  at 10% THD+N. Set bit 2 (PARALLEL) of the Analog Configuration Register (0x532h) = 1 to configured the device in Parallel mode. After the device is set to Parallel mode, make an external connection between OUT2+ and OUT3+, and a connection between OUT2- and OUT3- (Figure 2). In Parallel mode, the combined channels are driven from the OUT2 source. OUT1 and OUT4 are unaffected. Signal routing, mixing, filtering, and equalization are done through the Spatial Engine.

Make sure the device is configured in Parallel mode, before connecting OUT2 and OUT3 and enabling the outputs. Do not make a connection between OUT2 and OUT3 together while the outputs are enabled. Disable the outputs first, then make the connections between OUT2 and OUT3.

## GAIN SETTING

The LM48901 has three gain stages, the ADC preamplifier, and two independent volume controls in the Digital Mixer, one for the ADC path and one for the I<sup>2</sup>S path. The ADC preamplifier has four gain settings (0dB, 2.4dB, 3.5dB, and 6dB). The preamplifier gain is set by bits 0 and 1 (ANA\_LVL) of the Analog Configuration Register (0x523h). The Digital Mixer has two 64 step volume controls. The ADC path volume control is set by bits 5:0 (ADC\_LVL) in the Digital Mixer Control Register (0x522h). The I<sup>2</sup>S path volume control is set by bits 13:8 (I<sup>2</sup>S\_LVL) in the Digital Mixer Control Register (0x522h). Both volume controls have a range of -76.5dB to 18dB in 1.5dB increments.

## MODULATOR POWER SUPPLY ( $AV_{DD1}$ )

The  $AV_{DD1}$  ( $R_L$  package: bump C2, SQ package: pin 12) powers the class D modulators. For maximum output swing, set  $AV_{DD1}$  and  $PV_{DD}$  to the same voltage. Table 22 shows the output voltage for different  $AV_{DD1}$  levels.

**TABLE 22. Amplifier Output Voltage with Variable  $AV_{DD1}$  Voltage**

$AV_{DD1}$ (V)	$V_{OUT}$ ( $V_{RMS}$ ) @ $PV_{DD} = 5V$ , THD+N = 1%	$V_{OUT}$ ( $V_{RMS}$ ) @ $PV_{DD} = 3.6V$ , THD+N = 1%
5	3.3	-
4.5	3.1	-
4.2	2.9	-
4	2.7	-
3.6	2.5	2.4
3.3	2.3	2.2
3	2.1	2.1
2.8	2	1.9

## CLOCK REQUIREMENTS

The LM48901 requires an external clock source for proper operation, regardless of input source or device configuration. The device derives the ADC, digital mixer, DSP, I<sup>2</sup>S port, and PWM clocks from the external clock. The clock can be derived from either MCLK or SCLK inputs. Set bit 11 (I<sup>2</sup>S\_CLK) of the Enable and Clock configuration register (0x521h) to 0 to select MCLK, set I<sup>2</sup>S\_CLK to 1 to select SCLK. The LM48901 accepts five different clock frequencies, 1.536, 3.072, 6.114, 12.288, and 24.576MHz. Set bits 10:8 (MCLK\_RATE) of the Enable and Clock Configuration Register to the appropriate clock frequency. In systems where both MCLK and SCLK are available, choose the lower frequency clock for improved power consumption.

## SHUTDOWN FUNCTION

There are two ways to shutdown the LM48901, hardware mode, and software mode. The default is hardware mode.

Set bit 1 (FORCE) of the Enable and Clock Configuration Register (0x521h) to 0 to enable hardware shutdown mode. In hardware mode, the device is enabled and disabled through  $\overline{SHDN}$ . Connect  $\overline{SHDN}$  to  $V_{DD}$  for normal operation. Connect  $\overline{SHDN}$  to GND to disable the device. Hardware shutdown mode supports a one shot, or momentary switch  $\overline{SHDN}$  input. When bit 2 (PULSE) of the Enable and Clock Configuration Register (0x521h) is set to 1, the LM48901 responds to a rising edge on  $\overline{SHDN}$  to change the device state. When PULSE = 0, the device requires a stable logic level on  $\overline{SHDN}$ .

Set FORCE = 1 to enable software shutdown mode. In software shutdown mode, the device is enabled and disabled through bit 0 (ENABLE) of the Enable and Clock Configuration Register (0x512h). Set ENABLE = 0 to disable the LM48901. Set ENABLE = 1 to enable the LM48901.

In either hardware or software mode, the content of the LM48901 memory registers is retained after the device is disabled, as long as power is still applied to the device. Minimize power consumption by disabling the PMC clock oscillator when the LM48901 is shutdown. Set bit 12 (PMC\_CLK\_SEL) and bit 14 (QSA\_CLK\_STOP) of the Enable and Clock configuration Register (0x521h) = 1 to disable the PMC clock oscillator.

## EXTERNAL CAPACITOR SELECTION

### Power Supply Bypassing and Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Typical applications employ a voltage regulator with 10 $\mu$ F and 0.1 $\mu$ F bypass capacitors that increase supply stability. These capacitors do not eliminate the need for bypassing of the LM48901 supply pins. A 1 $\mu$ F capacitor is recommended for IOV<sub>DD</sub>, PLLV<sub>DD</sub>, DV<sub>DD</sub>, and AV<sub>DD</sub>. A 2.2 $\mu$ F capacitor is recommended for PV<sub>DD</sub>.

### REF and BYPASS Capacitor Selection

For best performance, bypass REF with a 4.7 $\mu$ F ceramic capacitor.

## INPUT CAPACITOR SELECTION

The LM48901 analog inputs require input coupling capacitors. Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48901. The input capacitors create a high-pass filter with the input resistors  $R_{IN}$ . The -3dB point of the high pass filter is found using Equation (1) below.

$$f = 1 / 2\pi R_{IN} C_{IN}$$

Where the value of  $R_{IN}$  is 20k $\Omega$ .

The input capacitors can also be used to remove low frequency content from the audio signal. Small speakers cannot reproduce, and may even be damaged by low frequencies. High pass filtering the audio signal helps protect the speakers. When the LM48901 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

## PCB LAYOUT GUIDELINES

As output power increases, interconnect resistance (PCB traces and wires) between the amplifier, load, and power supply create a voltage drop. The voltage loss due to the traces between the LM48901 and the load results in lower output power and decreased efficiency. Higher trace resistance between the supply and the LM48901 has the same effect as a poorly regulated supply, increasing ripple on the supply line, and reducing peak output power. The effects of residual trace resistance increases as output current increases due to higher output power, decreased load impedance or both. To maintain the highest output voltage swing and corresponding peak output power, the PCB traces that connect the output pins to the load and the supply pins to the power supply should be as wide as possible to minimize trace resistance.

The use of power and ground planes will give the best THD+N performance. In addition to reducing trace resistance, the use of power planes creates parasitic capacitors that help to filter the power supply line.

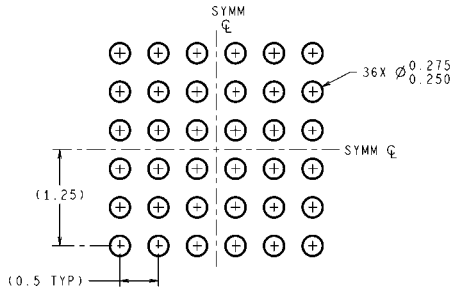
The inductive nature of the transducer load can also result in overshoot on one of both edges, clamped by the parasitic diodes to GND and  $V_{DD}$  in each case. From an EMI standpoint, this is an aggressive waveform that can radiate or conduct to other components in the system and cause interference. It is essential to keep the power and output traces short and well shielded if possible. Use of ground planes beads and micro-strip layout techniques are all useful in preventing unwanted interference.

As the distance from the LM48901 and the speaker increases, the amount of EMI radiation increases due to the output wires or traces acting as antennas become more efficient with length. Ferrite chip inductors placed close to the LM48901 outputs may be needed to reduce EMI radiation.

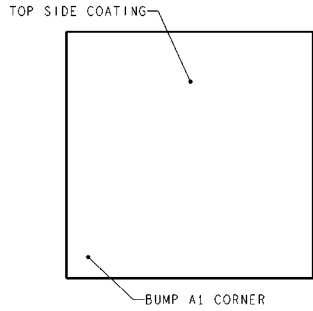
## Revision History

Rev	Date	Description
1.0	10/31/11	Initial Web released.
1.01	12/02/11	Fixed a typo (LM488901 to LM48901) on page 45.
1.02	12/12/11	Added two sections "Modulator Power Supply" and Clock Requirements.
1.03	12/16/11	Changed National to Texas Instruments.

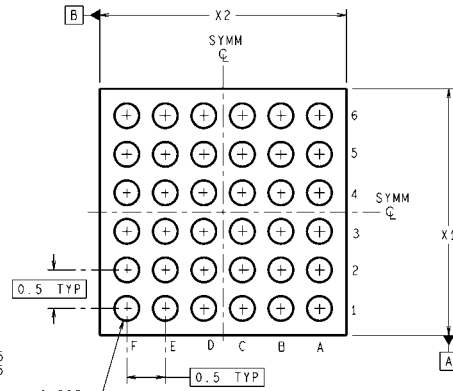
# Physical Dimensions inches (millimeters) unless otherwise noted



LAND PATTERN RECOMMENDATION



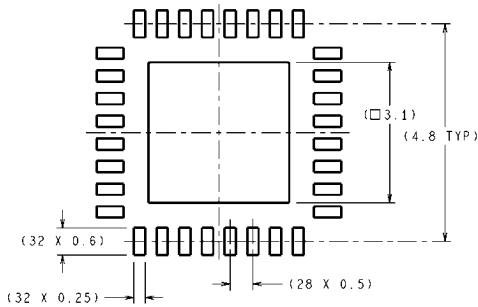
DIMENSIONS ARE IN MILLIMETERS  
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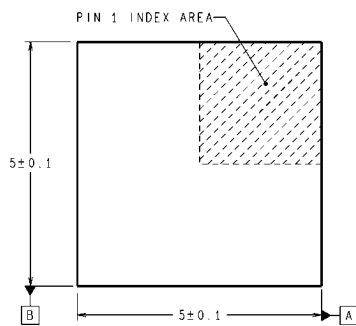
TLA36XXX (Rev D)

**36-pin micro SMD**  
**Order Number LM48901RL**  
**NS Package Number TLA36JSA**

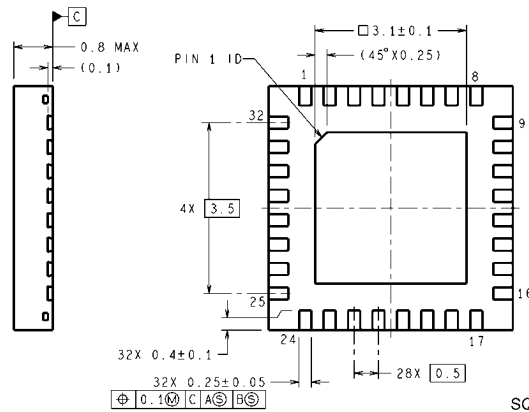
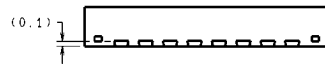
**X1 = 3.204±0.03mm X2 = 3.434±0.03mm X3 = 0.65±0.075mm**



RECOMMENDED LAND PATTERN



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SQA32A (Rev B)

**LLP Package**  
**Order Number LM48901SQ**  
**NS Package Number SQA32A**

**X1 = 5mm X2 = 5mm X3 = 0.8mm**



# Notes

LM48901

**Notes**

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