TPS709xxEVM-110 Evaluation Module

This User's Guide describes the operational use of the TPS709xxEVM-110 Evaluation Module (EVM) as a reference design for engineering demonstration and evaluation of the TPS709xx, low dropout linear regulator (LDO). Included in this user's guide are setup instructions, a schematic diagram, board layout, thermal guidelines, a bill of materials, and test results.

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1 Introduction

The TI TPS709xxEVM-110 Evaluation Module (EVM) helps design engineers evaluate the operation and performance of the TPS709xx family of linear regulators for possible use in their own circuit application. This EVM configuration contains a single linear regulator with internal thermal protection, reverse current protection, and overcurrent protection in a SOT23-5 package. The regulator is capable of delivering up to 150 mA to the load, depending on the input-output power dissipation across the part which can be minimized because of the low dropout voltage. The input and output capacitors for the TPS709xx must be 2.2 µF (effective minimum) for stability. An additional input capacitor connection is added to the EVM if smaller, lower voltage capacitors are desired.

2 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, setup, and use the TPS709xxEVM-110.

2.1 *Input/Output Connectors and Jumper Descriptions*

2.1.1 J1 – V_{IN}

J1 is the input power supply voltage connector. The positive input lead and ground return lead from the input power supply should be twisted and kept as short as possible to minimize EMI transmission. Additional bulk capacitance should be added between J1 and J2 if the supply leads are greater than six inches. For example, an additional 47-µF electrolytic capacitor connected from J1 to ground eliminates unwanted ringing on the input due to long wires.

2.1.2 J2 – GND

J2 is the return connector for the input power supply.

2.1.3 J3 – EN

This jumper enables or disables the output of the TPS709xx. Placing a shorting jumper between pins 1 and 2 (OFF position) disables the TPS709xx. There is a pull-up resistor connected internally in the device; therefore, removing the jumper enables the TPS709xx. The maximum rating of EN is 7 V. If EN is connected to V_{IN} or an external voltage source, be sure EN does not exceed 7 V.

2.1.4 J4 – VOUT

J4 is the regulated output voltage connector.

2.1.5 J5 – GND

J5, the return connector for VOUT, is connected to J2 on the PCB.

2.2 *Equipment Setup*

- Set the power supply voltage to the desired operating input voltage. Turn the power supply off. Connect the positive voltage lead from the power supply to J1 (V_{IN}). Connect the ground lead from the power supply to J2 (GND).
- Connect a 0- to 150-mA load between J4 (VOUT) and J5 (GND).

3 Operation

- Turn on the power supply.
- Vary the respective load and input voltage as necessary, for test purposes.

4 Test Results

This section provides typical performance waveforms for the EVM. Actual performance data is affected by measurement techniques and environmental variables; therefore, these curves are presented for reference and may differ from actual results obtained.

4.1 Turn-on Waveform

Figure 1 shows the turn-on characteristic, where 5 V is applied to V_{IN}. The output drives a 22-Ω load (full load).

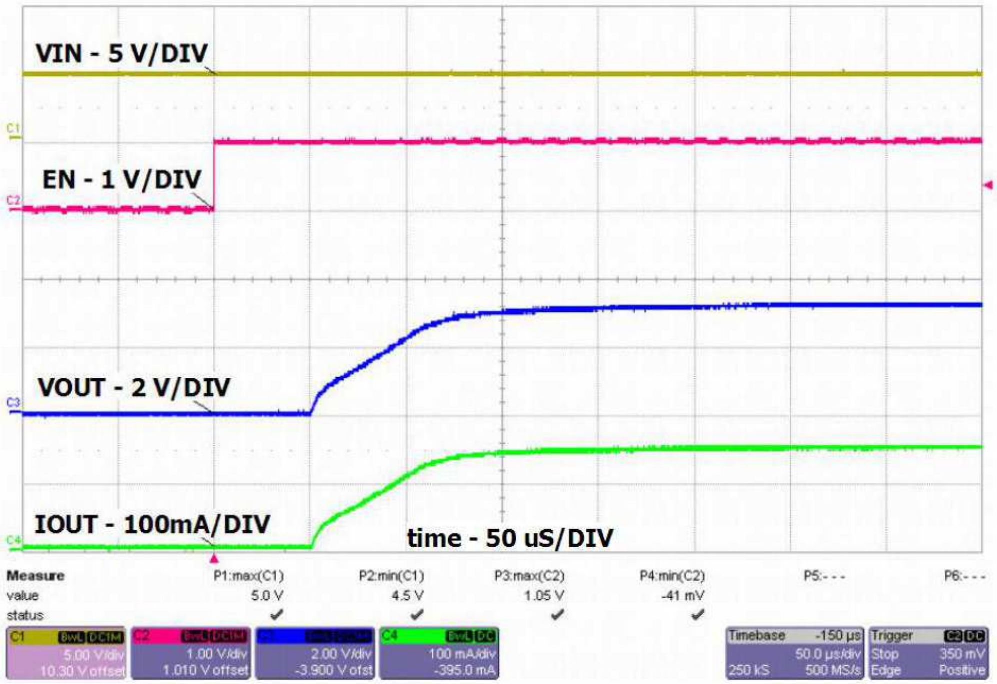

Figure 1. Turn-on Waveforms Into Full Load (22 Ω) of the TPS70933EVM-110

4.2 Turn-off Waveform

Figure 2 shows the turn-off characteristic, where 5 V is applied to V_{IN}. The output drives a 22-Ω load.

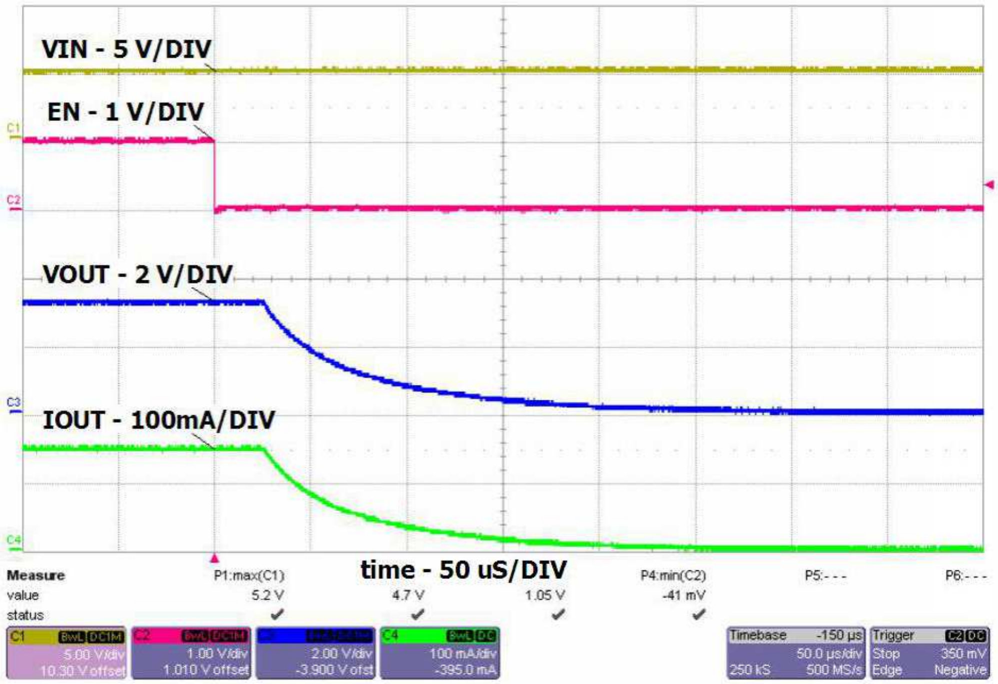

Figure 2. Turn-off Waveforms of the TPS70933EVM-110

4.3 Load Transient Waveform

Figure 3 shows the load transient response for a load-step transient from 15 mA to 135 mA, where 5 V is applied to V_{IN}.

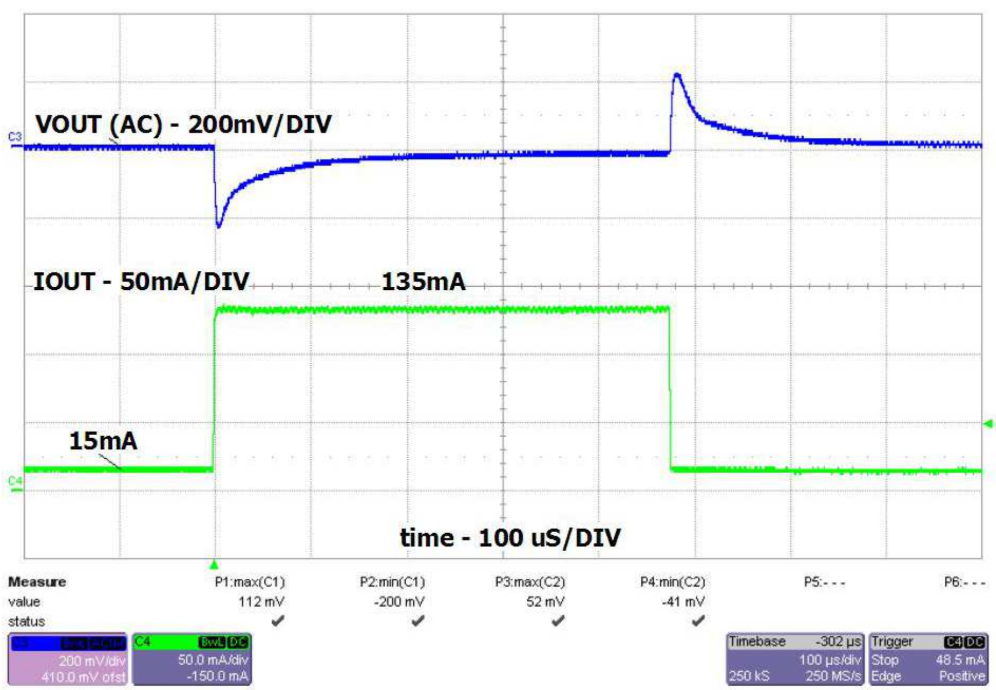

Figure 3. Load Step and Transient Response of the TPS70933EVM-110

4.4 PSRR

Figure 4 shows the PSRR of the TPS70933EVM-110 at different load currents and Figure 5 shows the PSRR of the TPS70933EVM-110 at different input voltages.

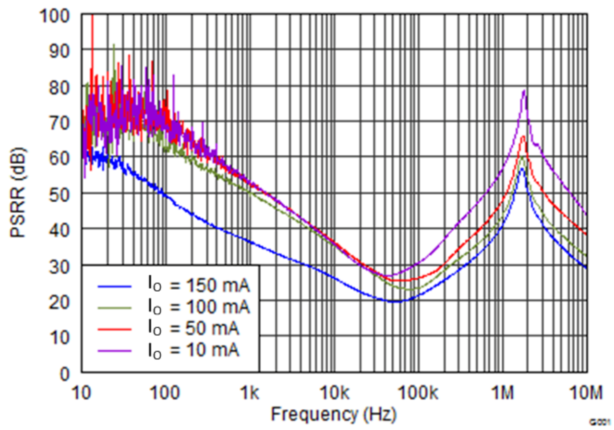

Figure 4. PSRR of the TPS70933EVM for Various Output Currents

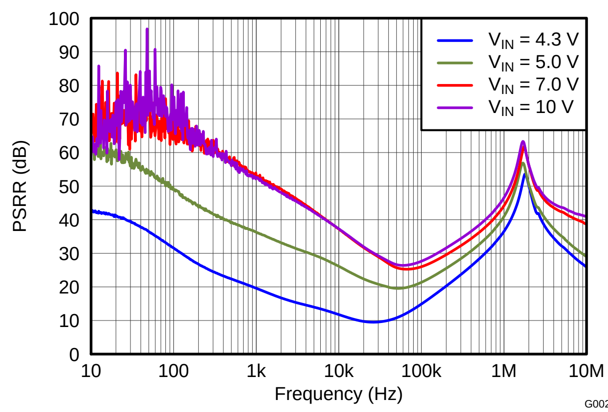

Figure 5. PSRR of the TPS70933EVM for Various Input Voltages

5 Thermal Guidelines and Layout Recommendations

Thermal management is a key component in the design of any power converter and is especially important when the power dissipation in the LDO is high. Use the following formula to approximate the maximum power dissipation for the ambient temperature:

$$T_J = T_A + P_D \times \theta_{JA}$$

Where T_J is the junction temperature, T_A is the ambient temperature, P_D is the power dissipation in the device (Watts), and θ_{JA} is the thermal resistance from junction to ambient. All temperatures are in degrees Celsius. The maximum operating junction temperature, T_J, must not be allowed to exceed 125°C. The layout design must be copper trace and plane areas smartly, as thermal sinks, in order to not allow T_J to exceed the absolute maximum rating under all temperature and voltage conditions across the part.

Table 1 repeats information from the Dissipation Ratings Table of the TPS709xx-series datasheet for comparison with the thermal resistance, θ_{JA}, for High-K JEDEC standard boards. The maximum input voltage can be calculated for full loads at different ambient temperatures. The input voltage must be less than these values in order to maintain a safe junction temperature.

Table 1. Thermal Resistance, θ_{JA}, and Maximum Power Dissipation

Board	Package	θ_{JA}	Max V_{IN} @ 150 mA (TA = 25°C)	Max V_{IN} @ 150 mA (T_A = 70°C)
High-K	DBV	212°C/W	6.4 V	5.0 V

6 Board Layout

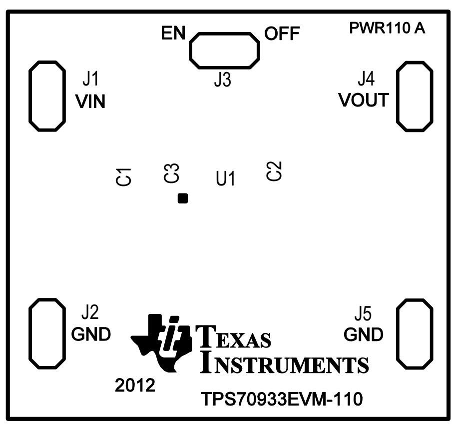

Figure 6. TPS709xxEVM-110 Assembly Layer

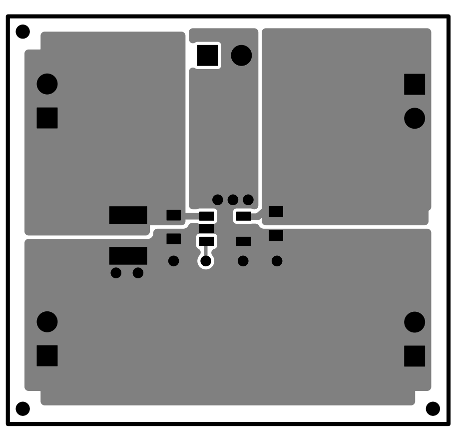

Figure 7. TPS709xxEVM-110 Top Layer Routing

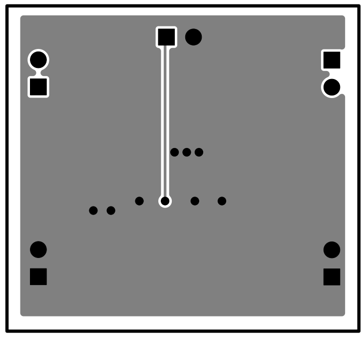

Figure 8. TPS709xxEVM-110 Bottom Layer Routing

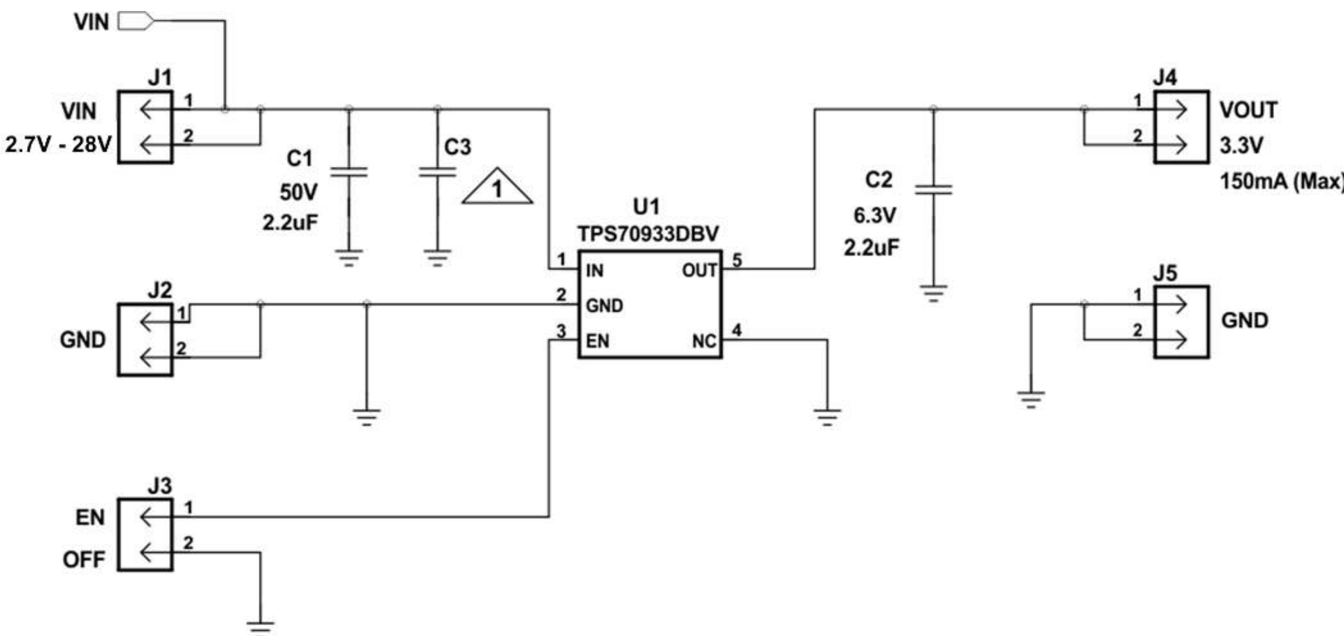

Figure 9. TPS709xxEVM-110 Schematic

Table 2. TPS709xxEVM-110 Bill of Materials

Count	RefDes	Value	Description	Size	Part Number	MFR
1	C1	2.2 µF	Capacitor, ceramic chip, 50 V, X7R, ±10%	1210	STD	STD
1	C2	2.2 µF	Capacitor, ceramic chip, 6.3 V, X7R, ±10%	0603	STD	STD
0	C3	DNP	Capacitor, ceramic chip	0603	STD	STD
5	J1-5	PEC02SAAN	Header, Male 2-pin, 100mil spacing	0.100 in × 2	PEC02SAAN	Sullins
1	U1	TPS70933DBV	IC, 150 mA, ultra-low IQ, 1-µA LDO regulator with enable	SOT-23	TPS709xxDBV	TI
1	J3		Shunt, black	100 mil	929950-00	3M
1	–	–	PCB, 1.20 in × 1.30 in × 0.062 in		PWR110	Any
Notes:	1. These assemblies are ESD sensitive, observe ESD precautions. 2. These assemblies must be clean and free from flux and all contaminants. Use of no-clean flux is not acceptable. 3. These assemblies must comply with workmanship standards IPC-A-610 Class 2. 4. Ref designators marked with an asterisk ('**') cannot be substituted. All other components can be substituted with equivalent MFG's components.					

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EVM Warnings and Restrictions

It is important to operate this EVM within the input voltage range of -22 V to 0.3 V and the output voltage range of -20 V to -3 V .

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 125° C. The EVM is designed to operate properly with certain components above 125° C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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