BQ25611D I²C Controlled 1-Cell 3.0-A Buck Battery Charger with USB Detection and 1.2-A Boost Operation

1 Features

- High-efficiency, 1.5-MHz, synchronous switch-mode buck charger
  - 92% charge efficiency at 2-A from 5-V input
  - ±0.4% charge voltage regulation with 10-mV step
  - Programmable JEITA thresholds
  - Remote battery sensing to charge faster
- Support USB On-The-Go (OTG) with adjustable output from 4.6 V to 5.15 V
  - Boost converter with up to 1.2-A output
  - 92% boost efficiency at 1-A output
  - Accurate constant current (CC) limit
  - Soft-start up to 500-µF capacitive load
- Single input supporting USB input, high-voltage adapter, or wireless power
  - Support 4-V to 13.5-V input voltage range with 22-V absolute max input rating
  - 130-ns fast turn-off input over voltage protection
  - Programmable input current limit (IINDPM) with I²C (100-mA to 3.2-A, 100-mA/step)
  - VINDPM threshold up to 5.4-V automatically tracks battery voltage for maximum power
  - Auto detect USB SDP, CDP, DCP and non-standard adaptors
- Narrow VDC (NVDC) power path management
  - System instant-on with no battery or deeply discharged battery
- Low R_{DSON} 19.5-mΩ BATFET to minimize charging loss and extend battery run time
  - BATFET control for ship mode, and full system reset with and without adapter
- 7-µA low battery leakage current in ship mode
- 9.5-µA low battery leakage current with system standby
- High accuracy battery charging profile
  - ±6% charge current regulation
  - ±7.5% input current regulation
  - ±3% VINDPM voltage regulation
  - Programmable top-off timer for full battery charging
- High integration includes all MOSFETs, current sensing and loop compensation
- Safety-Related Certifications:
  - IEC 62368-1 CB Certification

2 Applications

- Mobile phone, tablet
- Industrial, medical, portable electronics

3 Description

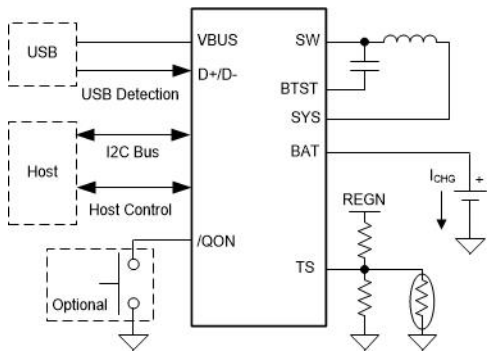
The BQ25611D is a highly integrated 3-A switch-mode battery charge management and system power path management device for single cell Li-Ion and Li-polymer batteries. The solution is highly integrated with input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. The low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time and extends battery run time during discharging phase.

The BQ25611D is a highly integrated 3-A switch-mode battery charge management and system Power Path management device for Li-ion and Li-polymer batteries. It features fast charging with high input voltage support for a wide range of applications including smart phones and tablets . Its low impedance power path optimizes switch-mode operation efficiency, reduces battery charging time, and extends battery run time during discharging phase. Its input voltage and current regulation and battery remote sensing deliver maximum charging power to the battery.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
BQ25611D	WQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Simplified Application

Table of Contents

4 Revision History

Changes from Revision A (June 2020) to Revision B (September 2020)	Page
• Added Safety-Related Certifications bullet to the *Features* list	1
• Updated the numbering format for tables, figures and cross-references throughout the document	1
• Added description about VQON to $\overline{QON}$ pin description	4
• Changed max of BAT, SYS from 17 V to 7 V	6
• Changed max of V_{BAT_DPL} from 2.62 V to 2.55 V	7
• Changed typ of V_{BAT_DPL} to 2.40 V	7
• Added additional 25°C spec for V_{BAT_DPL}	7
• Added I_{HSFET_OCP} row	7
• Updated Table 9-2	17
• Updated *BATFET Full System Reset* section	24
• Changed Bits 3-6 description from "Reserved" to "BQ25611D: 1010" in Table 9-19	31

Changes from Revision * (January 2020) to Revision A (June 2020)	Page
• Changed max of V_{REG_ACC} at 4.19 V from 4.206 V to 4.200 V	7

5 Description (continued)

The solution is highly integrated with input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4) between system and battery. It also integrates the bootstrap diode for the high-side gate drive for simplified system design. The I^2C serial interface with charging and system settings makes the device a truly flexible solution.

The device supports a wide range of input sources, including standard USB host port, USB charging port, USB compliant high voltage adapter and wireless power. It is compliant with USB 2.0 and USB 3.0 power spec with input current and voltage regulation. The device takes the result from the detection circuit in the system, such as USB PHY device.

The device integrates the buck charger and boost regulator into one solution with single inductor. It meets USB On-The-Go (OTG) operation power rating specification by supplying 5 V (adjustable 4.6V / 4.75 V / 5 V / 5.15 V) with constant current limit up to 1.2 A.

The Power Path management regulates the system slightly above battery voltage but does not drop below 3.5-V minimum system voltage (programmable) with adapter applied. With this feature, the system maintains operation even when the battery is completely depleted or removed. When the input current limit or voltage limit is reached, the Power Path management automatically reduces the charge current. As the system load continues to increase, the battery starts to discharge the battery until the system power requirement is met. This supplement mode prevents overloading the input source.

The device initiates and completes a charging cycle without software control. It senses the battery voltage and charges the battery in three phases: pre-conditioning, constant current and constant voltage. At the end of the charging cycle, the charger automatically terminates when the charge current is below a preset limit and the battery voltage is higher than the recharge threshold. If the fully charged battery falls below the recharge threshold, the charger automatically starts another charging cycle.

The charger provides various safety features for battery charging and system operations, including battery negative temperature coefficient thermistor monitoring, charging safety timer and overvoltage and over-current protections. Thermal regulation reduces charge current when the junction temperature exceeds 110°C. The status register reports the charging status and any fault conditions. With I^2C, the VBUS_GD bit indicates if a good power source is present, and the $\overline{INT}$ output immediately notifies host when a fault occurs.

The device also provides the $\overline{QON}$ pin for BATFET enable and reset control to exit low power ship mode or full system reset function.

The BQ25611D device is available in 24-pin, 4 mm × 4 mm x 0.75 mm thin WQFN package.

6 Device Comparison Table

	BQ25601	BQ25601D	BQ25611D
Programmable Charge Voltage	3.856 - 4.624 V, 32 mV per step	3.856 - 4.624 V, 32 mV per step	3.5 - 4.3 V (100 mV per step); 4.3 - 4.52 V (10 mV per step)
D+/D- USB Detection	No	Yes	Yes
Default I_{CHG}	2.04 A	2.04 A	1 A
Default V_{ACOV}	6.4 V	6.4 V	14.2 V
VBUS OVP reaction-time	200 ns	200 ns	130 ns
Battery remote sensing with open/ short detection	No	No	Yes
TS profile	JEITA, with fixed temperature thresholds	JEITA, with fixed temperature thresholds	JEITA, with adjustable temperature thresholds
TS ignore bit	No	No	Yes
Charge safety timer	5hr, 10 hr (default)	5 hr, 10 hr (default)	20 hr, 10 hr (default)
Allow $\overline{QON}$ fire when adapter is present	No	No	Yes
Deglitch time for chagre termination	250 ms	250 ms	50 ms

7 Pin Configuration and Functions

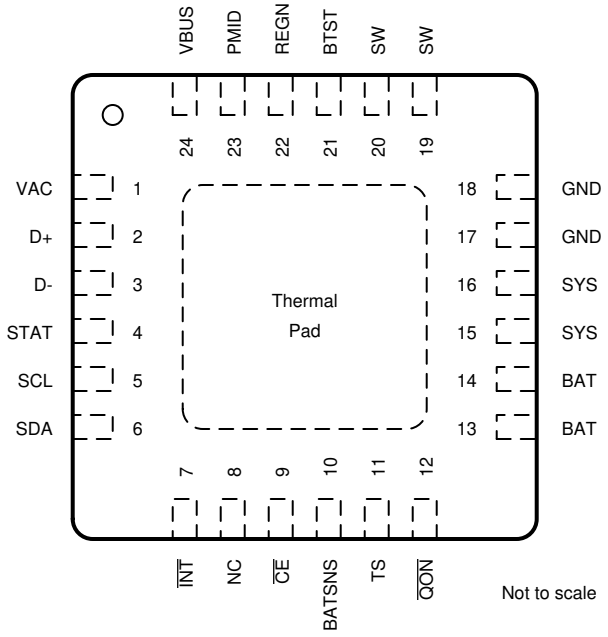


Figure 7-1. RTW Package 24-Pin WQFN Top View

Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
BAT	13	P	Battery connection point to the positive terminal of the battery pack. The internal current sensing resistor is connected between SYS and BAT. Connect a 10 µF[2] closely to the BAT pin.
	14		
BATSNS	10	AI	Battery voltage sensing pin for charge voltage regulation. In order to minimize the parasitic trace resistance during charging, BATSNS pin is connected to the positive terminal of battery pack as close as possible. If BATSNS pin is open or short to ground, BATSNS_STAT bit is set to 1 and charger regulates the battery voltage through BAT pin.
BTST	21	P	PWM high side driver positive supply. Internally, the BTST is connected to the cathode of the boot-strap diode. Connect the 0.047-µF bootstrap capacitor[2] from SW to BTST.

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
$\overline{CE}$	9	DI	Charge enable pin. When this pin is driven LOW, battery charging is enabled.
D+	2	AIO	Positive line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors.
D-	3	AIO	Negative line of the USB data line pair. D+/D– based USB host/charging port detection. The detection includes data contact detection (DCD), primary and secondary detection in BC1.2 and nonstandard adaptors.
GND	17	—	Ground.
	18		
$\overline{INT}$	7	DO	Open-drain interrupt output. Connect the $\overline{INT}$ to a logic rail through a 10-kΩ resistor. The $\overline{INT}$ pin sends an active low, 256-µs pulse to the host to report charger device status and fault.
NC	8	—	Not connected.
PMID	23	P	Connected to the drain of the reverse blocking MOSFET (RBFET) and the drain of HSFET. Place a 10-µF capacitor(2) on PMID to GND.
$\overline{QON}$	12	DI	BATFET enable/reset control input. When the BATFET is in ship mode, a logic LOW of $t_{SHIPMODE}$ duration turns on BATFET to exit ship mode. When the BATFET is not in ship mode, a logic LOW of t_{QON_RST} (minimum 8 s) duration resets SYS (system power) by turning BATFET off for t_{BATFET_RST} (minimum 250 ms) and then re-enables BATFET to provide full system power reset. The host chooses the BATFET reset function with VBUS unplugged or not through I^2C bit BATFET_RST_WVBUS. The pin is pulled up to V_{QON} through 200 kΩ to maintain default HIGH logic during ship mode. It has an internal clamp to 6.5 V. $\overline{QON}$ pin is pulled through 200-kΩ resistor to V_{QON}. V_{QON} is supplied from VBUS minus 2 diode voltage drop or from VBAT minus 1 diode voltage drop. It has an internal voltage clamp to 6.5 V.
REGN	22	P	PWM low side driver positive supply output. Internally, REGN is connected to the anode of the boot-strap diode. Connect a 4.7-µF (10-V rating) ceramic capacitor(2) from REGN to analog GND. The capacitor should be placed close to the IC.
SCL	5	DI	I^2C interface clock. Connect SCL to the logic rail through a 10-kΩ resistor.
SDA	6	DIO	I^2C interface data. Connect SDA to the logic rail through a 10-kΩ resistor.
STAT	4	DO	Open-drain interrupt output. Connect the STAT pin to a logic rail via 10-kΩ resistor. The STAT pin indicates charger status. Charge in progress: LOW. Charge complete or charger in SLEEP mode: HIGH. Charge suspend (fault response): blink at 1 Hz.
SW	19	P	Switching node connecting to output inductor. Internally, SW is connected to the source of the n-channel HSFET and the drain of the n-channel LSFET. Connect the 0.047-µF bootstrap capacitor(2) from SW to BTST.
	20		
SYS	15	P	System output connection point. The internal current sensing resistor is connected between SYS and BAT. Connect a 10 µF (min)(2) closely to the SYS pin.
	16		
TS	11	AI	Battery temperature qualification voltage input. Connect a negative temperature coefficient thermistor (NTC). Program temperature window with a resistor divider from REGN to TS to GND. Charge and boost mode suspended when TS pin voltage is out of range. When TS pin is not used, connect a 10-kΩ resistor from REGN to TS and a 10-kΩ resistor from TS to GND or set TS_IGNORE to HIGH to ignore TS pin. It is recommended to use a 103AT-2 thermistor.
VAC	1	P	Input voltage sensing. This pin must be tied to VBUS.
VBUS	24	P	Charger input voltage. The internal n-channel reverse block MOSFET (RBFET) is connected between VBUS and PMID with VBUS on source. Place a 1-uF ceramic capacitor(2) from VBUS to GND and place it as close as possible to the device.
Thermal Pad	—	P	Ground reference for the device that is also the thermal pad used to conduct heat from the device. This connection serves two purposes. The first purpose is to provide an electrical ground connection for the device. The second purpose is to provide a low thermal-impedance path from the device die to the PCB. This pad should be tied externally to a ground plane.

(1) AI = Analog Input, AO = Analog Output, AIO = Analog Input Output, DI = Digital input, DO = Digital Output, DIO = Digital Input Output, P = Power

(2) All capacitors are ceramic unless otherwise specified

8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VAC (converter not switching)	–2	22	V
Voltage	VBUS (converter not switching)	-2	22	V
Voltage	PMID (converter not switching)	–0.3	22	V
Voltage	SW	–0.3	16	V
Voltage	BAT, SYS (converter not switching)	–0.3	7	V
Voltage	BTST	–0.3	22	V
Voltage	BATSNS (converter not switching)	–0.3	7	V
Voltage	D+. D-, STAT, SCL, SDA, $\overline{INT}$, $\overline{CE}$, TS, $\overline{QON}$, REGN	–0.3	7	V
Output Sink Current	STAT, INT		6	mA
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/ JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VBUS}	Input voltage	4		13.5	V
V_{BAT}	Battery voltage			4.52	V
I_{VBUS}	Input current			3.2	A
I_{SW}	Output current (SW)			3.2	A
I_{BAT}	Fast charging current			3	A
	RMS discharge current			6	A
T_A	Ambient temperature	–40		85	°C

8.4 Thermal Information

THERMAL METRIC(1)		BQ25611D RTW (WQFN) 24 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance (JEDEC(1))	35.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	22.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	11.9	°C/W

8.4 Thermal Information (continued)

THERMAL METRIC[1]		BQ25611D RTW (WQFN) 24 Pins	UNIT
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	1.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

8.5 Electrical Characteristics

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
QUIESCENT CURRENTS						
I_{Q_BAT}	Quiescent battery current (BATSNS, BAT, SYS, SW)	VBAT = 4.5 V, VBUS floating or VBUS = 0V - 5 V, SCL, SDA = 0 V or 1.8 V, T_J < 85 °C, BATFET enabled		9.5	15	µA
I_{SHIP_BAT}	Shipmode battery current (BATSNS, BAT, SYS, SW)	VBAT = 4.5 V, VBUS floating or VBUS = 0V - 5 V, SCL, SDA = 0 V or 1.8 V, T_J < 85 °C, BATFET disabled		7	9.5	µA
I_{VBUS}	Input current (VBUS) in buck mode when converter is switching	VBUS=5 V, charge disabled, converter switching, ISYS = 0 A		2.3		mA
I_{HIZ_VBUS}	Quiescent input current in HIZ	VAC/VBUS = 5 V, HIZ mode, no battery		37	50	µA
		VAC/VBUS = 12 V, HIZ mode, no battery		68	90	µA
I_{BST}	Quiescent battery current (BATSNS, BAT, SYS, SW) in boost mode when converter is switching	VBAT = 4.5 V, VBUS = 5 V, boost mode enabled, converter switching, I_{PMID} = 0A		2.4		mA
VBUS / VBAT SUPPLY						
V_{VBUS_OP}	VBUS operating range		4		13.5	V
V_{VBUS_UVLOZ}	VBUS rising for active I2C, no battery	VBUS rising		3.3	3.7	V
V_{VBUS_UVLO}	VBUS falling to turnoff I2C, no battery	VBUS falling		3	3.3	V
$V_{VBUS\_PRESENT}$	VBUS to enable REGN	VBUS rising		3.65	3.9	V
$V_{VBUS\_PRESENTZ}$	VBUS to disable REGN	VBUS falling		3.15	3.4	V
V_{SLEEP}	Enter Sleep mode threshold	VBUS falling, VBUS - VBAT, VBAT = 4V	15	60	110	mV
V_{SLEEPZ}	Exit Sleep mode threshold	VBUS rising, VBUS - VBAT, VBAT = 4V	115	220	340	mV
V_{ACOV}	VAC overvoltage rising threshold to turn of switching	VAC rising, OVP[1:0]=00	5.45	5.85	6.07	V
		VAC rising, OVP[1:0]=01	6.1	6.4	6.75	V
		VAC rising, OVP[1:0]=10	10.45	11	11.55	V
		VAC rising, OVP[1:0]=11 (default)	13.5	14.2	14.85	V
	VAC overvoltage falling threshold to resume switching	VAC falling, OVP[1:0]=00	5.2	5.6	5.8	V
		VAC falling, OVP[1:0]=01	5.8	6.2	6.45	V
		VAC falling, OVP[1:0]=10	10	10.7	11.1	V
		VAC falling, OVP[1:0]=11 (default)	13	13.9	14.5	V
V_{BAT_UVLOZ}	BAT voltage for active I2C, no VBUS	VBAT rising	2.5			V
V_{BAT_DPLZ}	BAT depletion rising threshold to turn on BATFET	VBAT rising	2.35		2.8	V

8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{BAT_DPL}	BAT depletion falling threshold to turn off BATFET	VBAT falling	2.18	2.40	2.55	V
V_{BAT_DPL}	BAT depletion falling threshold to turn off BATFET	VBAT falling T_J = 25°C		2.40	2.50	V
$V_{POORSRC}$	Bad adapter detection threshold	VBUS falling	3.75	3.9	4.0	V
POWER-PATH MANAGEMENT						
V_{SYS_MIN}	Typical minimum system regulation voltage	VBAT=3.2 V < SYS_MIN = 3.5 V, ISYS = 0 A	3.5	3.65		V
V_{SYS_OVP}	System overvoltage threshold	VREG = 4.35 V, Charge disabled, ISYS = 0 A		4.7		V
R_{ON_RBFET}	Blocking FET on-resistance			45		mΩ
R_{ON_HSFET}	High-side switching FET on-resistance			62		mΩ
R_{ON_LSFET}	Low-side switching FET on-resistance			71		mΩ
V_{BATFET_FWD}	BATFET forward voltage in supplement mode	BAT discharge current 10 mA, converter running		30		mV
BATTERY CHARGER						
V_{REG_RANGE}	Typical charge voltage regulation range		3.49		4.51	V
V_{REG_STEP}	Typical charge voltage step	4.29 V < VREG < 4.51 V		10		mV
V_{REG_ACC}	Charge voltage accuracy	VREG = 4.09 V, T_J = –40°C - 85°C	4.073	4.09	4.106	V
V_{REG_ACC}	Charge voltage accuracy	VREG = 4.19 V, T_J = –40°C - 85°C	4.173	4.19	4.200	V
V_{REG_ACC}	Charge voltage accuracy	VREG = 4.35 V, T_J = –40°C - 85°C	4.332	4.35	4.367	V
V_{REG_ACC}	Charge voltage accuracy	VREG = 4.45 V, T_J = –40°C - 85°C	4.432	4.45	4.468	V
I_{CHG_RANGE}	Typical charge current regulation range		0		3	A
I_{CHG_STEP}	Typical charge current regulation step			60		mA
I_{CHG_ACC}	Fast charge current regulation accuracy	ICHG = 0.24 A, VBAT = 3.1 V or 3.8 V, T_J = –40°C - 85°C	0.2112	0.24	0.2688	A
		ICHG = 0.72 A, VBAT = 3.1 V or 3.8 V, T_J = –40°C - 85°C	0.6768	0.72	0.7632	A
		ICHG = 1.38 A, VBAT = 3.1 V or 3.8 V, T_J = –40°C - 85°C	1.2972	1.38	1.4628	A
I_{PRECHG_RANGE}	Typical pre-charge current range		60		780	mA
I_{PRECHG_STEP}	Typical pre-charge current step			60		mA
I_{PRECHG_ACC}	Precharge current accuracy	VBAT = 2.6 V, IPRECHG = 120 mA	102	120	138	mA
		VBAT = 2.6 V, IPRECHG = 240 mA	204	240	276	mA
I_{TERM_RANGE}	Typical termination current range		60		780	mA
I_{TERM_STEP}	Typical termination current step			60		mA
I_{TERM_ACC}	Termination current accuracy	ITERM = 180 mA, ICHG > 780 mA, VREG = 4.35 V, T_J = –40°C - 85°C	162	180	192	mA
		ITERM = 60mA, ICHG = < 780 mA, VREG = 4.35 V, T_J = –40°C - 85°C	42	60	78	mA
V_{BAT_SHORTZ}	Battery short voltage rising threshold to start pre-charge	VBAT rising	2.13	2.25	2.35	V
V_{BAT_SHORT}	Battery short voltage falling threshold to stop pre-charge	VBAT falling	1.85	2	2.15	V

8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{BAT_SHORT}	Battery short trickle charging current	VBAT < V_{BAT_SHORTZ}	70	90	110	mA
$V_{BATLOWV}$	Battery LOWV rising threshold to start fast-charge	VBAT rising	3	3.12	3.24	V
	Battery LOWV falling threshold to stop fast-charge	VBAT falling	2.7	2.8	2.9	V
V_{RECHG}	Battery recharge threshold	VRECHG=0, VBAT falling (default)	90	120	150	mV
		VRECHG=1, VBAT falling	185	210	245	mV
I_{SYS_LOAD}	System discharge load current during SYSOVP			30		mA
R_{ON_BATFET}	Battery FET on-resistance	T_J = –40°C - 85°C		19.5	26	mΩ
		T_J = –40°C - 125°C		19.5	30	mΩ
BATTERY OVER-VOLTAGE PROTECTION						
V_{BAT_OVP}	Battery overvoltage rising threshold	VBAT rising, as percentage of VREG	103	104	105	%
	Battery overvoltage falling threshold	VBAT falling, as percentage of VREG	101	102	103	%
INPUT VOLTAGE / CURRENT REGULATION						
V_{INDPM_RANGE}	Typical input voltage regulation range		3.9		5.4	V
V_{INDPM_STEP}	Typical input voltage regulation step			100		mV
V_{INDPM_ACC}	Typical input voltage regulation accuracy		4.365	4.5	4.635	V
V_{INDPM_TRACK}	VINDPM threshold to track battery voltage	VBAT = 4.35 V, VINDPM_BAT_TRACK = VBAT + 200 mV	4.45	4.55	4.74	V
I_{INDPM_RANGE}	Typical input current regulation range		0.1		3.2	A
I_{INDPM_STEP}	Typical input current regulation step			100		mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 500 mA (T_J=-40°C - 85°C)	450	465	500	mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 900 mA (T_J=-40°C-85°C)	750	835	900	mA
I_{INDPM_ACC}	Input current regulation accuracy	IINDPM = 1500 mA (T_J=-40°C-85°C)	1300	1390	1500	mA
D+ / D- Detection						
V_{DP_SRC}	D+ line source voltage		500	600	700	mV
I_{DP_SRC}	D+ line data contact detect current source	VD + = 200 mV,	7	10	14	µA
I_{DP_SINK}	D+ line sink current	VD + = 500 mV,	50	100	150	µA
$V_{DP\_DAT\_REF}$	D+ line data detect voltage	D+ pin Rising,	250		400	mV
$V_{DP\_LGC\_LOW}$	D+ line logic low.	D+ pin Rising,			800	mV
R_{DP_DWN}	D+ line pull-down resistance	VD+ = 500 mV	14.25		24.8	kΩ
I_{D+_LKG}	Leakage current into D+ line	Pull up to 1.8 V	–1		1	µA
V_{DM_SRC}	D- line source voltage		500	600	700	mV
I_{DM_SINK}	D- line sink current	VD- = 500 mV,	50	100	150	µA
$V_{DM\_DAT\_REF}$	D- line data detect voltage	D- pin Rising,	250		400	mV
R_{DM_DWN}	D- line pull-down resistance	VD- = 500 mV	14.25		24.8	kΩ
I_{D-_LKG}	Leakage current into D- line	Pull up to 1.8 V	–1		1	µA

8.5 Electrical Characteristics (continued)

V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{D+/D-\_2p8}$	D+/D- comparator threshold for non-standard adapter		2.55		2.85	V
$V_{D+/D-\_2p0}$	D+/D- comparator threshold for non-standard adapter		1.85		2.15	V
$V_{D+/D-\_1p2}$	D+/D- comparator threshold for non-standard adapter		1.05		1.35	V
THERMAL REGULATION AND THERMAL SHUTDOWN						
T_{REG}	Junction temperature regulation accuracy	TREG = 90°C		90		°C
		TREG = 110°C		110		°C
T_{SHUT}	Thermal Shutdown Rising threshold	Temperature Increasing		150		°C
	Thermal Shutdown Falling threshold	Temperature Decreasing		130		°C
CHARGE MODE THERMISTOR COMPARATOR (JEITA 616J or HOT/COLD 616)						
$V_{T1\_RISE\%}$	TS pin voltage rising threshold, Charge suspended above this voltage.	As Percentage to REGN (0°C w/ 103AT)	72.4	73.3	74.2	%
$V_{T1\_FALL\%}$	TS pin voltage falling threshold. Charge re-enabled to 20% of ICHG and VREG below this voltage.	As Percentage to REGN	71.5	72	72.5	%
$V_{T2\_RISE\%}$	TS pin voltage rising threshold, Charge back to 20% of ICHG and VREG above this voltage.	As Percentage to REGN, JEITA_T2 = 5°C w/ 103AT	70.25	70.75	71.25	%
		As Percentage to REGN, JEITA_T2 = 10°C w/ 103AT	67.75	68.25	68.75	%
		As Percentage to REGN, JEITA_T2 = 15°C w/ 103AT	64.75	65.25	65.75	%
		As Percentage to REGN, JEITA_T2 = 20°C w/ 103AT	61.75	62.25	62.75	%
$V_{T2\_FALL\%}$	TS pin voltage falling threshold. Charge back to ICHG and VREG below this voltage.	As Percentage to REGN, JEITA_T2=5°C w/ 103AT	68.7	69.2	69.7	%
		As Percentage to REGN, JEITA_T2=10°C w/ 103AT	66.45	66.95	67.45	%
		As Percentage to REGN, JEITA_T2=15°C w/ 103AT	63.7	64.2	64.7	%
		As Percentage to REGN, JEITA_T2=20°C w/ 103AT	60.7	61.2	61.7	%
$V_{T3\_FALL\%}$	TS pin voltage falling threshold. Charge to ICHG and 4.1V below this voltage.	As Percentage to REGN, JEITA_T3=40°C w/ 103AT	47.75	48.25	48.75	%
		As Percentage to REGN, JEITA_T3=45°C w/ 103AT	44.25	44.75	45.25	%
		As Percentage to REGN, JEITA_T3=50°C w/ 103AT	40.2	40.7	41.2	%
		As Percentage to REGN, JEITA_T3=55°C w/ 103AT	37.2	37.7	38.2	%
$V_{T3\_RISE\%}$	TS pin voltage rising threshold. Charge back to ICHG and VREG above this voltage.	As Percentage to REGN, JEITA_T3 = 40°C w/ 103AT	48.8	49.3	49.8	%
		As Percentage to REGN, JEITA_T3 = 45°C w/ 103AT	45.3	45.8	46.3	%
		As Percentage to REGN, JEITA_T3 = 50°C w/ 103AT	41.3	41.8	42.3	%

8.5 Electrical Characteristics (continued)

$V_{VBUS\_UVLOZ} < V_{VBUS} < V_{VBUS\_OV}$ and $V_{VBUS} > V_{BAT} + V_{SLEEP}$, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
		As Percentage to REGN, JEITA_T3 = 55°C w/ 103AT	38.5	39	39.5	%
$V_{T5\_FALL\%}$	TS pin voltage falling threshold, charge suspended below this voltage.	As Percentage to REGN (60°C w/ 103AT)	33.7	34.2	35.1	%
$V_{T5\_RISE\%}$	TS pin voltage rising threshold. Charge back to ICHG and 4.1V above this voltage.	As Percentage to REGN	35	35.5	36	%
BOOST MODE THERMISTOR COMPARATOR (HOT/COLD)						
$V_{BCOLD\_RISE\%}$	TS pin voltage rising threshold, boost mode is suspended above this voltage.	As Percentage to REGN (–19.5°C w/ 103AT)	79.5	80	80.5	%
$V_{BCOLD\_FALL\%}$	TS pin voltage falling threshold	As Percentage to REGN (0°C w/ 103AT)		72		%
$V_{BHOT\_FALL\%}$	TS pin voltage threshold. boost mode is suspended below this voltage.	As Percentage to REGN, (64°C w/ 103AT)	30.2	31.2	32.2	%
$V_{BHOT\_RISE\%}$	TS pin voltage rising threshold	As Percentage to REGN, (55°C w/ 103AT), REG0C[1:0] = 11		39		%
SWITCHING CONVERTER						
F_{SW}	PWM switching frequency	Oscillator frequency	1.32	1.5	1.68	MHz
D_{MAX}	Maximum PWM Duty Cycle			97		%
BOOST MODE CONVERTER						
V_{BST_BAT}	Battery voltage exiting boost mode	BAT falling	2.4	2.5	2.6	V
V_{BST_RANGE}	Typical boost mode voltage regulation range		4.6		5.15	V
V_{BST_ACC}	Boost mode voltage regulation accuracy	IVBUS = 0 A, BOOST_V = 5 V	4.85	5	5.15	V
I_{BST_RANGE}	Typical boost mode current regulation		0.5		1.2	A
I_{BST_ACC}	Boost mode maximum output current limit		1.2	1.4	1.6	A
$I_{BST\_OCP\_Q1}$	Boost mode battery discharge current clamp on RBFET Q1	BOOST_LIM = 0.5 A	0.5		0.72	A
$I_{SYS\_OCP\_Q4}$	Boost mode battery discharge current clamp on BATFET Q4		9	10		A
REGN LDO						
V_{REGN}	REGN LDO output voltage	V_{VBUS} = 5 V, I_{REGN} = 20 mA	4.58	4.7	4.8	V
		V_{VBUS} = 9 V, I_{REGN} = 20 mA	5.6	6	6.5	V
I_{REGN}	REGN LDO current limit	V_{VBUS} = 5 V, V_{REGN} = 3.8 V	50			mA
I2C INTERFACE (SCL, SDA)						
V_{IH}	Input high threshold level, SDA and SCL	Pull up rail 1.8 V	1.3			V
V_{IL}	Input low threshold level	Pull up rail 1.8 V			0.4	V
V_{OL}	Output low threshold level	Sink current = 5 mA			0.4	V
I_{BIAS}	High-level leakage current	Pull up rail 1.8 V			1	µA
V_{IH_SDA}	Input high threshold level, SDA	Pull up rail 1.8 V	1.3			V
V_{IL_SDA}	Input low threshold level	Pull up rail 1.8 V			0.4	V

8.5 Electrical Characteristics (continued)

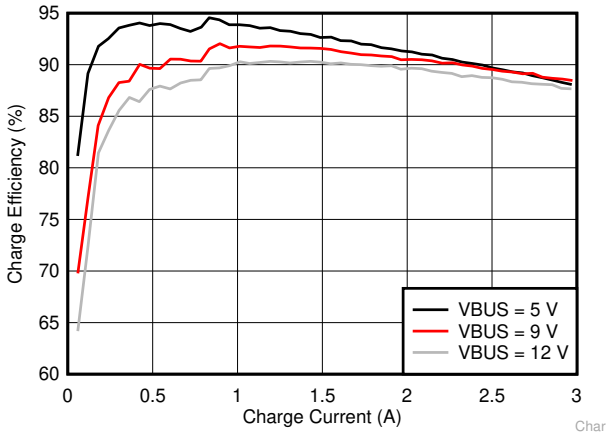
V_{VBUS_UVLOZ} < V_{VBUS} < V_{VBUS_OV} and V_{VBUS} > V_{BAT} + V_{SLEEP}, T_J = -40°C to +125°C, and T_J = 25°C for typical values (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OL_SDA}	Output low threshold level	Sink current = 5 mA			0.4	V
I_{BIAS_SDA}	High-level leakage current	Pull up rail 1.8 V			1	µA
V_{IH_SCL}	Input high threshold level, SDA	Pull up rail 1.8 V	1.3			V
V_{IL_SCL}	Input low threshold level	Pull up rail 1.8 V			0.4	V
V_{OL_SCL}	Output low threshold level	Sink current = 5 mA			0.4	V
I_{BIAS_SCL}	High-level leakage current	Pull up rail 1.8 V			1	µA
LOGIC INPUT PIN						
V_{IH}	Input high threshold level (/CE)		1.3			V
V_{IL}	Input low threshold level (/CE)				0.4	V
I_{IN_BIAS}	High-level leakage current (/CE)	Pull up rail 1.8 V			1	µA
LOGIC OUTPUT PIN						
V_{OL}	Output low threshold level (/INT, STAT, /PG)	Sink current = 5 mA			0.4	V
I_{OUT_BIAS}	High-level leakage current (/INT, STAT, /PG)	Pull up rail 1.8 V			1	µA
CHARGE OVERCURRENT COMPARATOR (CYCLE-BY-CYCLE)						
I_{HSFET_OCP}	HSFET cycle-by-cycle over-current threshold		5.2		8.0	A

8.6 Timing Requirements

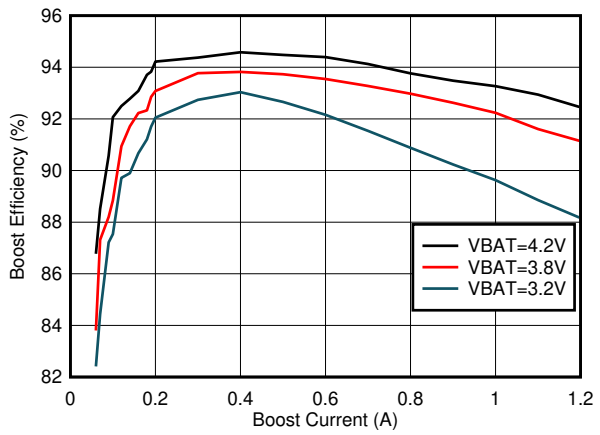
		MIN	NOM	MAX	UNIT
VBUS / VBAT POWER UP					
t_{VBUS_OV}	VBUS OVP Reaction-time		130		ns
$t_{POORSRC}$	Bad adapter detection duration		30		ms
$t_{POORSRC\_RETRY}$	Bad adapter detection retry wait time		2		s
BATTERY CHARGER					
t_{TERM_DGL}	Deglitch time for charge termination		30		ms
t_{RECHG_DGL}	Deglitch time for recharge threshold		30		ms
t_{TOP_OFF}	Typical top-off timer accuracy TOP_OFF_TIMER[1:0]=10	24	30	36	min
t_{SAFETY}	Charge safety timer accuracy, CHG_TIMER = 20hr	17	20	24	hr
t_{SAFETY}	Charge safety timer accuracy, CHG_TIMER = 10hr	8	10	12	hr
$\overline{QON}$ Timing					
$t_{SHIPMODE}$	$\overline{QON}$ low time to turn on BATFET and exit shipmode (–10℃ ≤ TJ ≤ 60℃)	0.9		1.3	s
t_{QON_RST}	$\overline{QON}$ low time before BATFET full system reset (–10℃ ≤ TJ ≤ 60℃)	8		12	s
t_{BATFET_RST}	BATFET off time during full system reset (–10℃ ≤ TJ ≤ 60℃)	250		400	ms
t_{BATFET_DLY}	Delay time before BATFET turn off in ship mode (–10℃ ≤ TJ ≤ 60℃)	10		15	s
DIGITAL CLOCK AND WATCHDOG					
f_{LPDIG}	Digital low-power clock (REGN LDO is disabled)		30		kHz
f_{DIG}	Digital power clock		500		kHz
t_{LP_WDT}	Watchdog Reset time		160		s
t_{WDT}	Watchdog Reset time (WATCHDOG REG05[5:4] = 160s)		160		s

8.7 Typical Characteristics



V_{BUS} = 5 V, 9 V, 12 V V_{BAT} = 3.8 V Inductor 1µH, DCR = 14.6 mΩ

Figure 8-1. Charge Efficiency



V_{BAT} = 3.2 V, 3.8 V, 4.2 V V_{BUS} = 5 V Inductor 1µH, DCR = 14.6 mΩ

Figure 8-2. Boost Efficiency

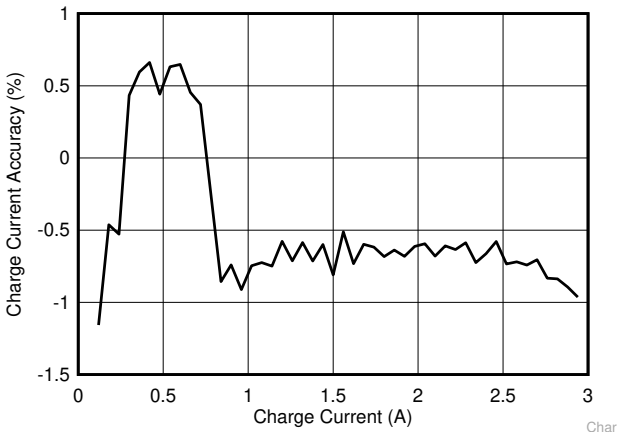


Figure 8-3. Charge Current Accuracy

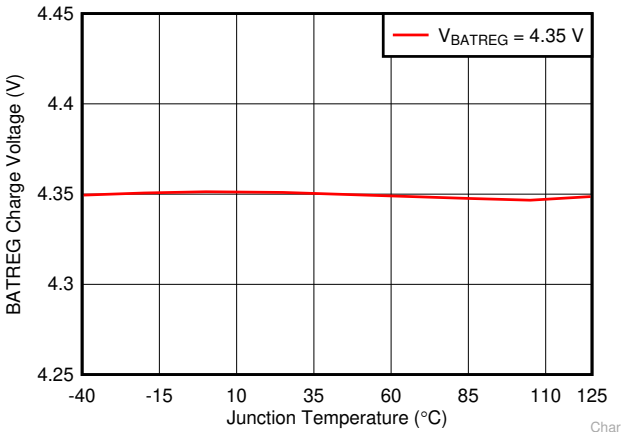


Figure 8-4. Battery Charge Voltage vs Junction Temperature

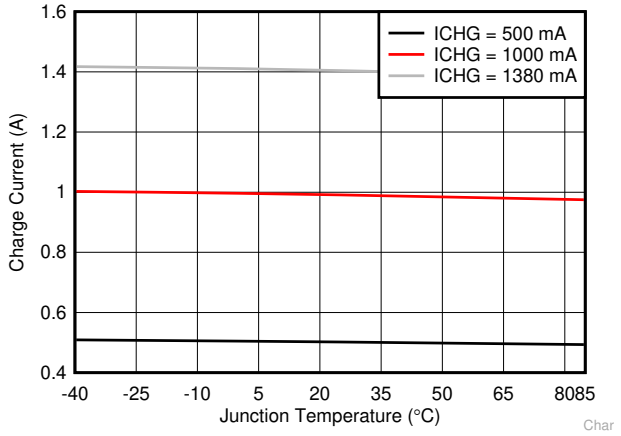


Figure 8-5. Charge Current vs Junction Temperature

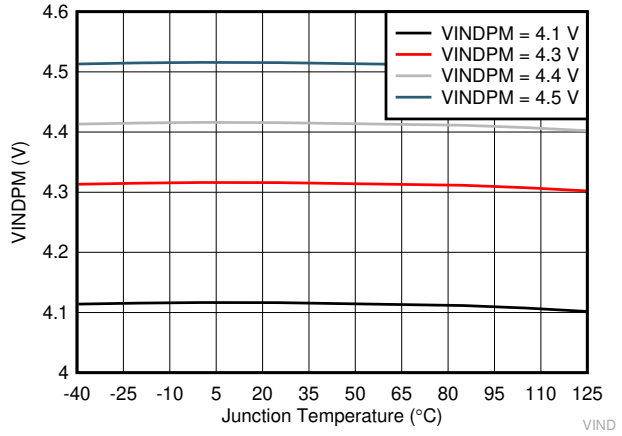


Figure 8-6. VINDPM vs Junction Temperature

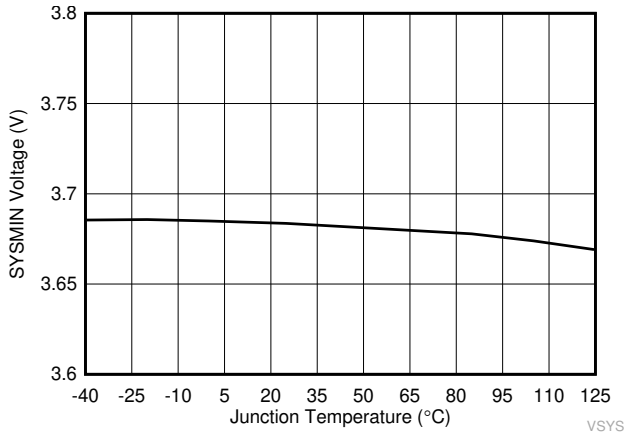


Figure 8-7. SYSMIN Voltage vs Junction Temperature (VSYS set at 3.5V)

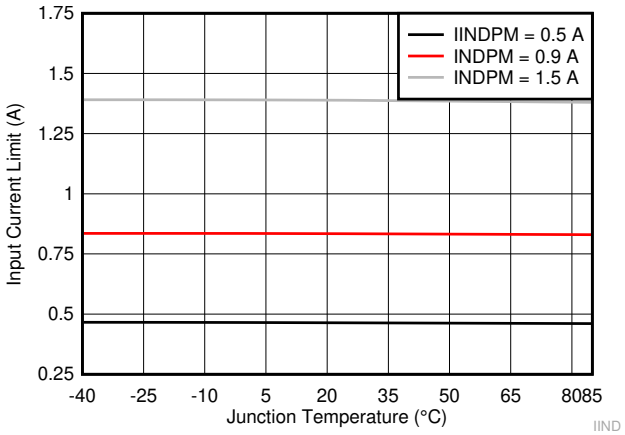


Figure 8-8. Input Current Limit vs Junction Temperature

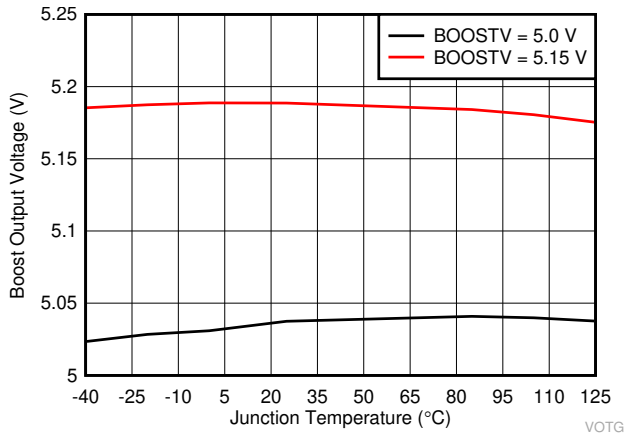


Figure 8-9. Boost Output Voltage vs Junction Temperature

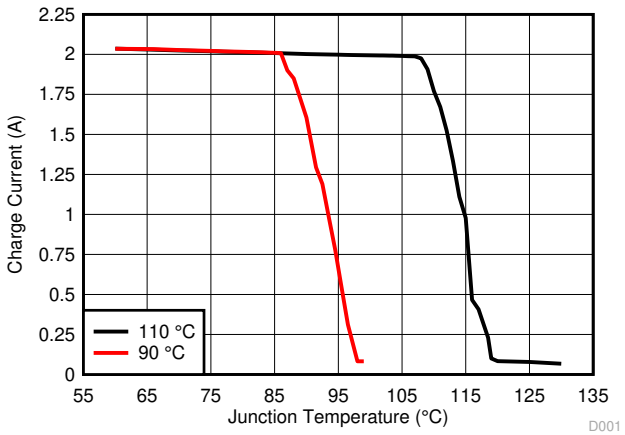


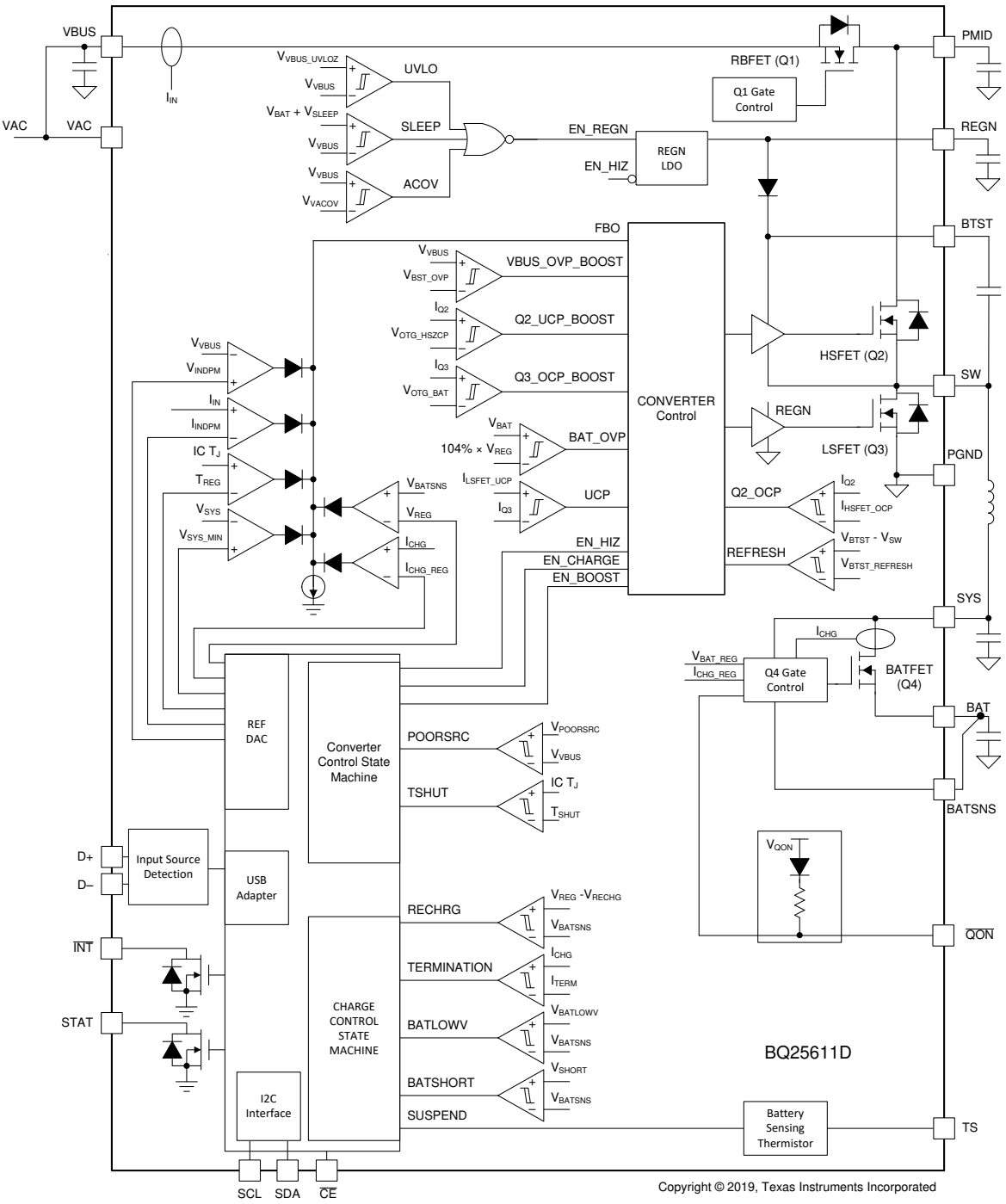
Figure 8-10. Charge Current vs Junction Temperature

9 Detailed Description

9.1 Overview

The BQ25611D device is a highly integrated 3.0-A switch-mode battery charger for single cell Li-Ion and Li-polymer battery. It includes the input reverse-blocking FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET, Q4), and bootstrap diode for the high-side gate drive.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Power-On-Reset (POR)

The device powers internal bias circuits from the higher voltage of VBUS and BAT. When V_{VBUS} rises above V_{VBUS_UVLOZ} or V_{BAT} rises above V_{BAT_UVLOZ} , the sleep comparator, battery depletion comparator and BATFET driver are active. I^2C interface is ready for communication and all the registers are reset to default value. The host can access all the registers after POR.

9.3.2 Device Power Up from Battery without Input Source

If only the battery is present and the voltage is above depletion threshold (V_{BAT_DPLZ}), the BATFET turns on and connects the battery to the system. The REGN stays off to minimize the quiescent current. The low R_{DSON} of BATFET and the low quiescent current on BAT minimize the conduction loss and maximize the battery run time.

The device always monitors the discharge current through BATFET. When the system is overloaded or shorted ($I_{BAT} > I_{SYS\_OCP\_Q4}$), the device turns off BATFET immediately until the input source plugs in again.

With I^2C, when the BATFET turns off due to over-current, the device sets the BATFET_DIS bit to indicate the BATFET is disabled until the input source plugs in again or one of the methods described in the Section 9.3.7.2 section is applied to re-enable BATFET.

9.3.3 Power Up from Input Source

When an input source is plugged in, the device checks the input source voltage to turn on the REGN LDO and all the bias circuits. It detects and sets the input current limit before the buck converter is started. The power up sequence from input source is as listed:

1. Power Up REGN LDO, see Power Up REGN LDOsection
2. Poor Source Qualification, see Poor Source Qualification section
3. Input Source Type Detection is based on D+/D– to set default input current limit (IINDPM threshold), see Input Source Type Detection (IINDPPM Threshold) section
4. Input Voltage Limit Threshold Setting (VINDPM threshold), see Input Voltage Limit Thresholding Setting (VINDPM Threshold) section
5. Power Up Converter, see Power Up Converter in Buck Mode section

9.3.3.1 Power Up REGN LDO

The REGN LDO supplies internal bias circuits as well as the HSFET and LSFET gate drive. It also provides the bias rail to TS external resistors. The pull-up rail of STAT can be connected to REGN as well. The REGN LDO is enabled when all the below conditions are valid:

- $V_{VBUS} > V_{VBUS\_UVLOZ}$
- In buck mode, $V_{VBUS} > V_{BAT} + V_{SLEEPZ}$
- In boost mode, $V_{VBUS} < V_{BAT} + V_{SLEEPZ}$
- After 220-ms delay is completed

During high impedance mode when EN_HIZ bit is 1, REGN LDO turns off. The battery powers up the system.

9.3.3.2 Poor Source Qualification

After the REGN LDO powers up, the device starts to check current capability of the input source. The first step is poor source detection.

- VBUS voltage above $V_{POORSRC}$ when pulling I_{BADSRC} (typical 30 mA)

With I^2C, once the input source passes poor source detection, the status register bit VBUS_GD is set to 1 and the $\overline{INT}$ pin is pulsed to signal to the host.

If the device fails the poor source detection, it repeats poor source qualification every 2 seconds.

9.3.3.3 Input Source Type Detection (IINDPM Threshold)

After poor source detection, the device runs input source detection through D+/D– lines . The D+/D– detection follows the USB Battery Charging Specification 1.2 (BC1.2) to detect standard (SDP/CDP/DCP) and non-standard adapters through USB D+/D– lines.

With I^2C, after input source type detection is completed, an $\overline{INT}$ pulse is asserted to the host. in addition, the following register bits are updated:

The host can over-write the IINDPM register to change the input current limit if needed.

9.3.3.3.1 D+/D– Detection Sets Input Current Limit

The device contains a D+/D– based input source detection to set the input current limit when a 5-V adapter is plugged-in. The D+/D– detection includes standard USB BC1.2 and non-standard adapters. When an input source is plugged in, the device starts standard USB BC1.2 detection. The USB BC1.2 is capable of identifying Standard Downstream Port (SDP), Charging Downstream Port (CDP) and Dedicated Charging Port (DCP). The non-standard detection is used to distinguish vendor specific adapters (Apple and Samsung) based on their unique dividers on the D+/D– pins. If an adapter is detected as DCP, the input current limit is set at 2.4-A. If an adapter is detected as unknown, the input current limit is set at 0.5 A by ILIM pin.

The secondary detection is used to distinguish two types of charging ports (CDP and DCP). The protocol for secondary detection is as follows:

Most of the time, a CDP requires the portable device (such as smart phone, tablet) to send back an enumeration within 2.5 seconds of CDP plug-in. Otherwise, the port will power cycle back to SDP even the D+/D– detection indicates CDP.

Table 9-1. Non-Standard Adapter Detection

NON-STANDARD ADAPTER	D+ THRESHOLD	D– THRESHOLD	INPUT CURRENT LIMIT (A)
Divider 1	V_{D+} within $V_{D+/D-\_2p8}$	$V_{D–}$ within $V_{D+/D-\_2p0}$	2.1
Divider 2	V_{D+} within $V_{D+/D-\_1p2}$	$V_{D–}$ within $V_{D+/D-\_1p2}$	2
Divider 3	V_{D+} within $V_{D+/D-\_2p0}$	$V_{D–}$ within $V_{D+/D-\_2p8}$	1
Divider 4	V_{D+} within $V_{D+/D-\_2p8}$	$V_{D–}$ within $V_{D+/D-\_2p8}$	2.4

Table 9-2. Input Current Limit Setting from D+/D– Detection

D+/D– DETECTION	INPUT CURRENT LIMIT (IINLIM)
USB SDP (USB500)	500 mA
USB DCP	2.4 A
Divider 3	1 A
Divider 1	2.1 A
Divider 4	2.4 A
Divider 2	2 A
Unknown 5-V Adapter	500 mA

9.3.3.4 Input Voltage Limit Threshold Setting (VINDPM Threshold)

The device has two modes to set the VINDPM threshold.

- Fixed VINDPM threshold. The VINDPM is in default set at 4.5 V (programmable from 3.9 V to 5.4 V) .
- VINDPM threshold tracks the battery voltage to optimize the converter headroom between input and output. When it is enabled in REG07[1:0], the actual input voltage limit is the higher of the VINDPM setting in register and V_{BAT} + offset voltage in VINDPM_BAT_TRACK[1:0] .

9.3.3.5 Power Up Converter in Buck Mode

After the input current limit is set, the converter is enabled and the HSFET and LSFET start switching. The system voltage is powered from the converter instead of the battery. If battery charging is disabled, the BATFET turns off. Otherwise, the BATFET stays on to charge the battery.

The device provides soft-start when system rail is ramping up. When the system rail is below V_{BAT_SHORT}, the input current is limited to the lower of 200-mA or IINDPM register setting. The system load shall be appropriately planned not to exceed the 200-mA IINDPM limit. After the system rises above V_{BAT_SHORTZ}, the device input current limit is the value set by the IINDPM register .

As a battery charger, the device deploys a highly efficient 1.5-MHz step-down switching regulator. The fixed frequency oscillator keeps tight control of the switching frequency under all conditions of input voltage, battery voltage, charge current and temperature simplifying output filter design.

The converter supports PFM operation by default for fast transient response during system voltage regulation and better light load efficiency. The PFM_DIS bit disables PFM operation if system voltage is not in regulation.

9.3.3.6 HIZ Mode with Adapter Present

By setting EN_HIZ bit to 1 with adapter, the device enters high impedance state (HIZ). In HIZ mode, the system is powered from battery even with good adapter present. The device is in the low input quiescent current state with Q1 RBFET, REGN LDO and the bias circuits off.

9.3.4 Boost Mode Operation From Battery

The device supports boost converter operation to deliver power from the battery to other portable devices through a USB port. The output voltage is regulated at 5-V (programmable 4.6/4.75/5.0/5.15 V) and output current is up to 1.2 A (programmable 0.5 A/1.2 A) with constant current regulation. The user needs to have at least 350 mV between V_{BAT} and boost mode regulation voltage (V_{BST}) to power up boost mode reliably. For example, BOOSTV[1:0] setting is recommended to be 4.75 V or higher if the battery voltage is 4.4 V.

The boost operation is enabled if the conditions below are valid:

1. Register setting: BATFET_DIS = 0, CHG_COFNIG = 0 and BST_CONFIG = 1
2. BAT above V_{BST_BAT} set by MIN_VBAT_SEL bit,
3. VBUS less than V_{BAT} + V_{SLEEP} (in sleep mode) before converter starts.
4. Voltage at TS (thermistor) pin, as a percentage of V_{REGN}, is within acceptable range ($V_{BHOT\_RISE\%}$ < $V_{TS\%}$ < $V_{BCOLD\_FALL\%}$)
5. After 30-ms delay from boost mode enable .

During boost mode, the status register VBUS_STAT bits is set to 111 .

The converter supports PFM operation at light load in boost mode. The PFM_DIS bit can be used to disable PFM operation in boost configuration.

9.3.5 Power Path Management

The device accommodates a wide range of input sources such as USB, wall adapter, or car charger. The device provides automatic power path selection to supply the system (SYS) from the input source (VBUS), battery (BAT), or both.

9.3.5.1 Narrow VDC Architecture

The device deploys Narrow VDC architecture (NVDC) with BATFET separating system from battery. The minimum system voltage is set by SYS_Min bits. Even with a fully depleted battery, the system is regulated above the minimum system voltage.

When the battery is below the minimum system voltage setting, the BATFET operates in linear mode (LDO mode), and the system is typically 180 mV above the minimum system voltage setting. As the battery voltage rises above the minimum system voltage, the BATFET is fully on and the voltage difference between the system and battery is the V_{DS} of the BATFET.

When battery charging is disabled and above the minimum system voltage setting or charging is terminated, the system is always regulated at typically 50 mV above the battery voltage. The status register VSYS_STAT bit goes to 1 when the system is in minimum system voltage regulation.

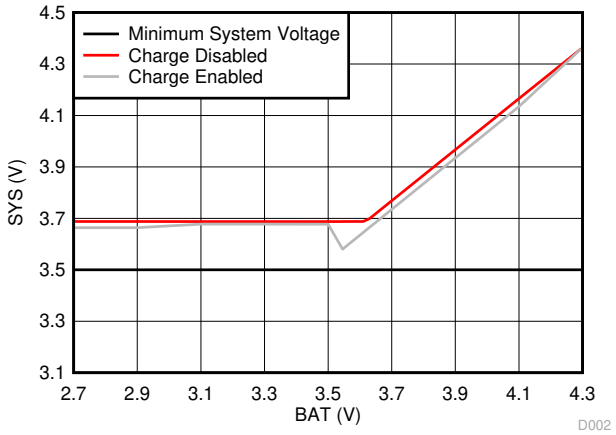


Figure 9-1. System Voltage vs Battery Voltage

9.3.5.2 Dynamic Power Management

To meet the maximum current limit in the USB specification and avoid overloading the adapter, the device features Dynamic Power Management (DPM), which continuously monitors the input current and input voltage. When input source is overloaded, either the current exceeds the input current limit (IINDPM) or the voltage falls below the input voltage limit (VINDPM). The device then reduces the charge current until the input current falls below the input current limit or the input voltage rises above the input voltage limit.

When the charge current is reduced to zero, but the input source is still overloaded, the system voltage starts to drop. Once the system voltage falls below the battery voltage, the device automatically enters the supplement mode where the BATFET turns on and the battery starts discharging so that the system is supported from both the input source and battery.

During DPM mode, the status register bits VINDPM_STAT or IINDPM_STAT go to 1.

Figure 9-2 shows the DPM response with 9-V/1.2-A adapter, 3.2-V battery, 2.8-A charge current and 3.5-V minimum system voltage setting.

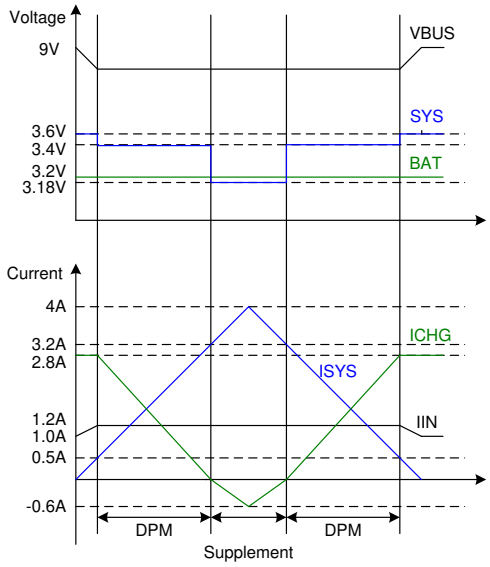


Figure 9-2. DPM Response

9.3.5.3 Supplement Mode

When the system voltage falls below the battery voltage, the BATFET turns on and the BATFET gate is regulated so that the minimum BATFET V_{DS} stays at 30 mV when the current is low. This prevents oscillation from entering and exiting the supplement mode.

As the discharge current increases, the BATFET gate is regulated with a higher voltage to reduce R_{DSON} until the BATFET is in full conduction. At this point onwards, the BATFET V_{DS} linearly increases with discharge current. Figure 9-3 shows the V-I curve of the BATFET gate regulation operation. The BATFET turns off to exit supplement mode when the battery is below battery depletion threshold.

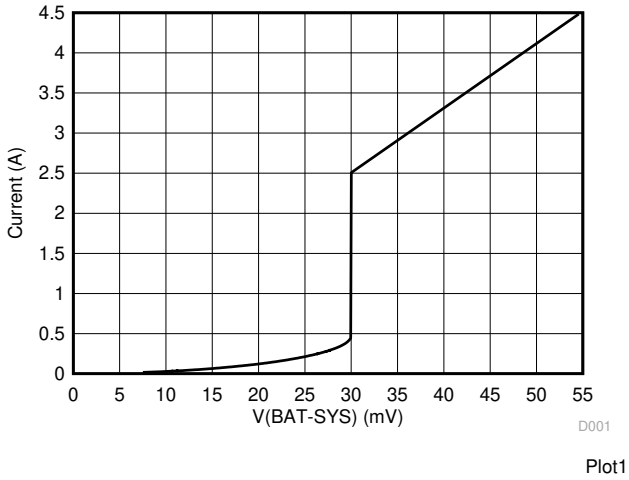


Figure 9-3. BAFET V-I Curve

9.3.6 Battery Charging Management

The device charges 1-cell Li-Ion battery with up to 3.0-A charge current for high capacity tablet battery. The 19.5-mΩ BATFET improves charging efficiency and minimizes the voltage drop during discharging.

9.3.6.1 Autonomous Charging Cycle

When battery charging is enabled (CHG_CONFIG bit = 1 and $\overline{CE}$ pin is LOW), the device autonomously completes a charging cycle without host involvement. The device default charging parameters are listed in Table 9-3. The host configures the power path and charging parameters by writing to the corresponding registers through I^2C.

Table 9-3. Charging Parameter Default Setting

DEFAULT MODE	BQ25611D
Charging voltage	4.20 V
Charging current	1.02 A
Pre-charge current	180 mA
Termination current	180 mA
Temperature profile	JEITA
Safety timer	10 hours

A new charge cycle starts when the following conditions are valid:

- Converter starts
- Battery charging is enabled (CHG_CONFIG bit = 1 and I_{CHG} register is not 0 mA and $\overline{CE}$ is low)
- No thermistor fault on TS. (TS pin can be ignored by setting TS_IGNORE bit to 1)
- No safety timer fault
- BATFET is not forced to turn off (BATFET_DIS bit = 0)

The device automatically terminates the charging cycle when the charging current is below the termination threshold, the battery voltage is above the recharge threshold, and the device is not in DPM mode or thermal regulation. When a fully charged battery is discharged below recharge threshold (selectable through VRECHG bit), the device automatically starts a new charging cycle. After the charge is done, toggle $\overline{CE}$ pin or CHG_CONFIG bit will initiate a new charging cycle. Adapter removal and replug will also restart a charging cycle.

The STAT output indicates the charging status: charging (LOW), charging complete or charge disable (HIGH) or charging fault (blinking). The status register (CHRG_STAT) indicates the different charging phases: 00-charging disable, 01-pre-charge, 10-fast charge (CC) and constant voltage (CV), 11-charging done. Once a charging cycle is completed, an $\overline{INT}$ pulse is asserted to notify the host.

9.3.6.2 Battery Charging Profile

The device charges the battery in five phases: battery short, preconditioning, constant current, constant voltage and top-off trickle charging (optional). At the beginning of a charging cycle, the device checks the battery voltage and regulates current and voltage accordingly.

Resistance between charger output and battery cell terminal such as board routing, connector, MOSFETs and sense resistor can force the charging process to move from constant current to constant voltage too early and increase charge time. To speed up the charging cycle, the device provides BATSNS pin to extend the constant current charge time to delivery maximum power to battery. BATSNS pin is connected directly to battery cell terminal to remotely sense battery cell voltage. BATSNS is by default enabled, and can be disabled through BATSNS_DIS bit. If BATSNS is connected to GND or left floating, the charger regulates BAT pin instead.

Table 9-4. Charging Current Setting

V_{BAT}	CHARGING CURRENT	DEFAULT SETTING	CHRG_STAT
< 2.2 V	I_{BAT_SHORT}	100 mA	01
2.2 V to 3 V	I_{PRECHG}	180 mA	01
> 3 V	I_{CHG}	1020 mA	10

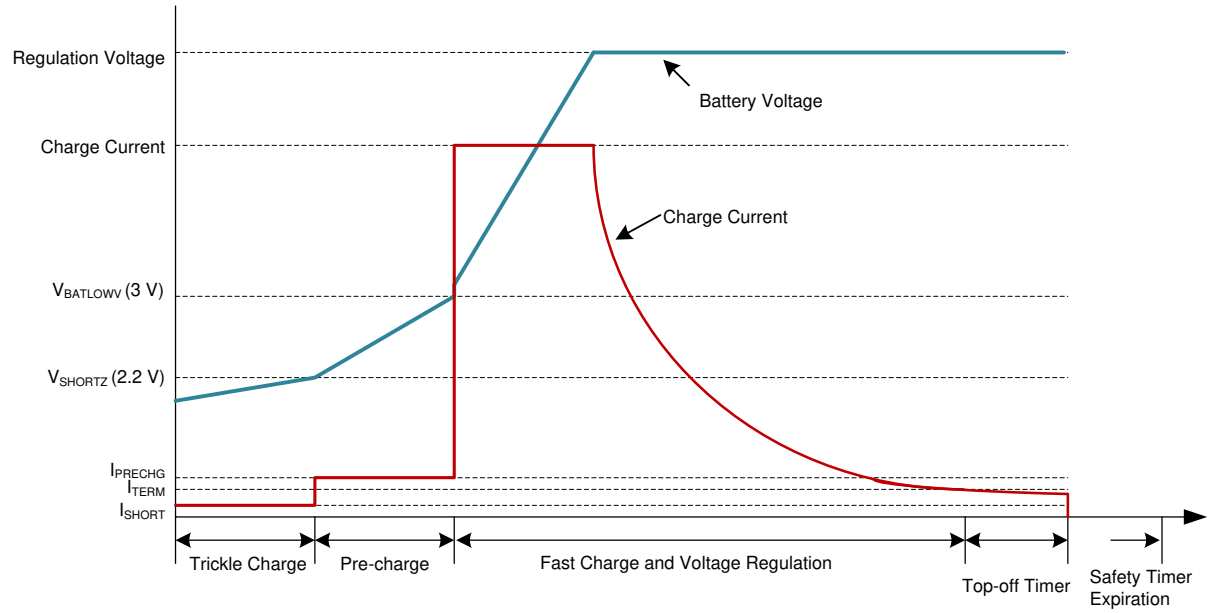


Figure 9-4. Battery Charging Profile

9.3.6.3 Charging Termination

The device terminates a charge cycle when the battery voltage is above the recharge threshold, and the current is below termination current. After the charging cycle is completed, the BATFET turns off. The STAT is asserted HIGH to indicate charging done. The converter keeps running to power the system, and BATFET can turn on again to engage Supplement Mode.

If the device is in IINDPM/VINDPM regulation, or thermal regulation, the actual charging current will be less than the termination value. In this case, termination is temporarily disabled.

When termination occurs, STAT pin goes HIGH. The status register CHRG_STAT is set to 11, and an $\overline{INT}$ pulse is asserted to the host. Termination can be disabled by writing 0 to EN_TERM bit prior to charge termination.

The termination current is set in REG03[3:0]. Due to the termination current accuracy, the actual termination current may be higher than the termination target. In order to compensate for termination accuracy, a programmable top-off timer can be applied after termination is detected . The top-off timer will follow safety timer constraints, such that if safety timer is suspended, so will the top-off timer. Similarly, if safety timer is doubled, so will the termination top-off timer. TOPOFF_ACTIVE bit reports whether the top off timer is active or not. The host can read CHRG_STAT and TOPOFF_ACTIVE to find out the termination status. STAT pin stays HIGH during top-off timer counting cycle.

Top-off timer gets reset at one of the following conditions:

1. Charge disable to enable
2. Charger enters termination
3. REG_RST register bit is set

The top-off timer settings are read in once termination is detected by the charger. Programming a top-off timer value (01, 10, 11) after termination will have no effect unless a recharge cycle is initiated. The top-off timer will immediately stop if it is disabled (00). An $\overline{INT}$ is asserted to the host when entering top-off timer segment as well as when top-off timer expires.

9.3.6.4 Thermistor Qualification

The device provides a single thermistor input for battery temperature monitoring.

9.3.6.4.1 JEITA Guideline Compliance During Charging Mode

To improve the safety of charging Li-ion batteries, the JEITA guideline was released on April 20, 2007. The guideline emphasized the importance of avoiding a high charge current and high charge voltage at certain low and high temperature ranges.

To initiate a charge cycle, the voltage on TS pin, as a percentage of V_{REGN}, must be within the $V_{T1\_FALL\%}$ to $V_{T5\_RISE\%}$ thresholds. If the TS voltage percentage exceeds the T1-T5 range, the controller suspends charging, a TS fault is reported and waits until the battery temperature is within the T1 to T5 range.

At cool temperature (T1-T2), the charge current is reduced to a programmable fast charge current (0%, 20% default, 50%, 100% of I_{CHG}, by JEITA_ISET). At warm temperature (T3-T5), the charge voltage is reduced to 4.1 V or kept at V_{REG} (JEITA_VSET). and the charge current can be reduced to a programmable level (0%, 20%, 50%, 100% default). Battery termination is disabled in T3-T5. The charger provides more flexible settings on T2 and T3 threshold as well to program the temperature profile beyond JEITA. When the T1 is set to 0°C and T5 is set to 60°C, T2 can be programmed to 5.5°C/10°C(default)/15°C/20°C, and T3 can be programmed to 40°C/ 45.5°C(default)/50.5°C/54.5°C.

When charger does not need to monitor the NTC, host sets TS_IGNORE bit to 1 to ignore the TS pin condition during charging and boost mode. If TS_IGNORE bit is set to 1, TS pin is ignored and the charger ignore TS pin input. In this case, NTC_FAULT bits are 000 to report normal TS status.

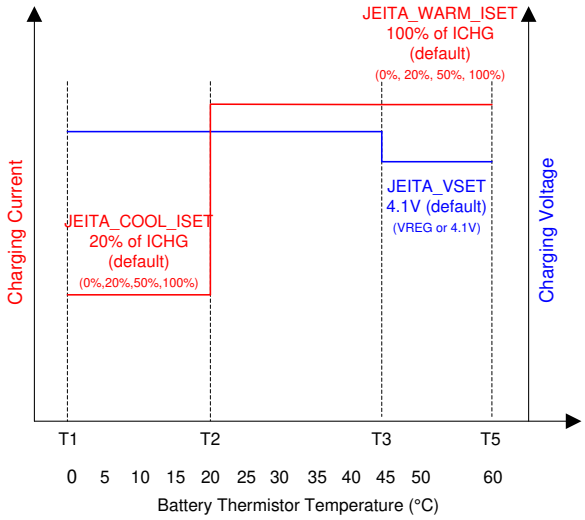


Figure 9-5. JEITA Profile

Equation 1 through Equation 2 describe how to calculate resistor divider values on Ts pin.

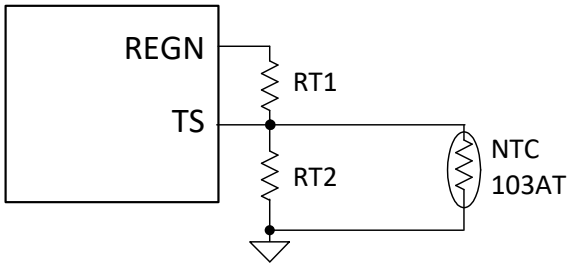


Figure 9-6. TS Pin Resistor Network

$$RT1 = \frac{\frac{1}{V_{T1}\%} - 1}{\frac{1}{R_{T2}} + \frac{1}{R_{NTC,T1}}} \quad (1)$$

$$RT2 = \frac{R_{NTC,T1} \times R_{NTC,T5} \times \left(\frac{1}{V_{T5}\%} - \frac{1}{V_{T1}\%}\right)}{R_{NTC,T1} \times \left(\frac{1}{V_{T1}\%} - 1\right) - R_{NTC,T5} \times \left(\frac{1}{V_{T5}\%} - 1\right)} \quad (2)$$

In the equations above, $R_{NTC,\ T1}$ is NTC thermistor resistance value at temperature T1 and $R_{NTC,\ T5}$ is NTC thermistor resistance values at temperature T5. Select 0°C to 60°C range for Li-ion or Li-polymer battery then

- $R_{NTC,T1}$ = 27.28 KΩ (0°C)
- $R_{NTC,T5}$ = 3.02 KΩ (60°C)
- RT1 = 5.3 KΩ
- RT2 = 31.14 KΩ

9.3.6.4.2 Boost Mode Thermistor Monitor During Battery Discharge Mode

For battery protection during boost mode, the device monitors the battery temperature to be within the V_{BCOLD} and V_{BHOT} thresholds. When RT1 is 5.3 KΩ and RT2 is 31.14 KΩ, T_{BCOLD} default is -19.5°C and T_{BHOT} default is 64°C. When temperature is outside of the temperature thresholds, the boost mode is suspended. In addition, VBUS_STAT bits are set to 000 and NTC_FAULT is reported. Once temperature returns within thresholds, boost mode is recovered and NTC_FAULT is cleared.

9.3.6.5 Charging Safety Timer

The device has a built-in safety timer to prevent extended charging cycle due to abnormal battery conditions. The safety timer is 2 hours when the battery is below $V_{BATLOWV}$ threshold and 10 hours (10/20 hours in REG05[2]) when the battery is higher than $V_{BATLOWV}$ threshold. When the safety timer expires, STAT pin is blinking at 1 Hz to report a safety timer expiration fault.

The user can program the fast charge safety timer through I^2C (CHG_TIMER bit REG05[2]). When safety timer expires, the fault register CHRG_FAULT bits (REG09[5:4]) are set to 11 and an $\overline{INT}$ is asserted to the host. The safety timer (both fast charge and pre-charge) can be disabled through I^2C by setting EN_TIMER bit.

During IINDPM/VINDPM regulation, thermal regulation, or JEITA cool/warm when fast charge current is reduced,the safety timer counts at a half clock rate, because the actual charge current is likely below the setting. For example, if the charger is in input current regulation (IINDPM_STAT = 1) throughout the whole charging cycle, and the safety time is set to 10 hours, the safety timer will expire in 20 hours. This half clock rate feature can be disabled by writing 0 to the TMR2X_EN bit.

During faults of BAT_FAULT, NTC_FAULT that lead to charging suspend, safety timer is suspended as well. Once the fault goes away, timer resumes. If user stops the current charging cycle, and start again, timer gets reset (toggle $\overline{CE}$ pin or CHG_CONFIG bit).

9.3.7 Ship Mode and $\overline{QON}$ Pin

9.3.7.1 BATFET Disable (Enter Ship Mode)

To extend battery life and minimize power when the system is powered off during system idle, shipping, or storage, the device turns off BATFET so that the system voltage is floating to minimize the battery leakage current. When the host sets the BATFET_DIS bit, the charger can turn off the BATFET immediately or delay by t_{BATFET_DLY} as configured by the BATFET_DLY bit. To set the device into ship mode with the adapter present, the host has to first set BATFET_RST_VBUS to 1 and then BATFET_DIS to 1. The charger will turn off the BATFET (no charging, no supplement) while the adapter is still attached. When the adapter is removed, the charger will enter ship mode.

9.3.7.2 BATFET Enable (Exit Ship Mode)

When the BATFET is disabled (in ship mode) as indicated by setting BATFET_DIS, one of the following events can enable the BATFET to restore system power:

1. Plug in adapter
2. Clear BATFET_DIS bit
3. Set REG_RST bit to reset all registers including BATFET_DIS bit to default (0)
4. A logic high to low transition on $\overline{QON}$ pin with $t_{SHIPMODE}$ deglitch time to enable BATFET to exit ship mode. EN_HIZ bit is set to 1 (regardless of adapter present or not). Host has to set EN_HIZ bit to 0 before boost mode enable. Once adapter plugs in, EN_HIZ will be cleared.

9.3.7.3 BATFET Full System Reset

The BATFET functions as a load switch between battery and system when input source is not plugged–in. When BATFET_RST_EN=1 and BATFET_DIS=0, BATFET full system reset function is enabled. By changing the state of BATFET from on to off, systems connected to SYS can be effectively forced to have a power-on-reset. The $\overline{QON}$ pin supports push-button interface to reset system power without host by changing the state of BATFET. Internally, it is pulled up to the V_{QON} voltage through a 200-kΩ resistor.

When the $\overline{QON}$ pin is driven to logic low for t_{QON_RST}, BATFET reset process starts. The BATFET is turned off for t_{BATFET_RST} and then it is re-enabled to reset system power. This function can be disabled by setting BATFET_RST_EN bit to 0.

BATFET full system reset functions either with or without adapter present. If BATFET_RST_WVBUS=1, the system reset function starts after t_{QON_RST} when $\overline{QON}$ pin is pushed to LOW. Once the reset process starts, the device first goes into HIZ mode to turn off the converter, and then power cycles BATFET. If BATFET_RST_WVBUS=0, the system reset function doesn't start till t_{QON_RST} after $\overline{QON}$ pin is pushed to LOW and adapter is removed.

After BATFET full system reset is complete, the device will power up again if EN_HIZ is not set to 1 before the system reset.

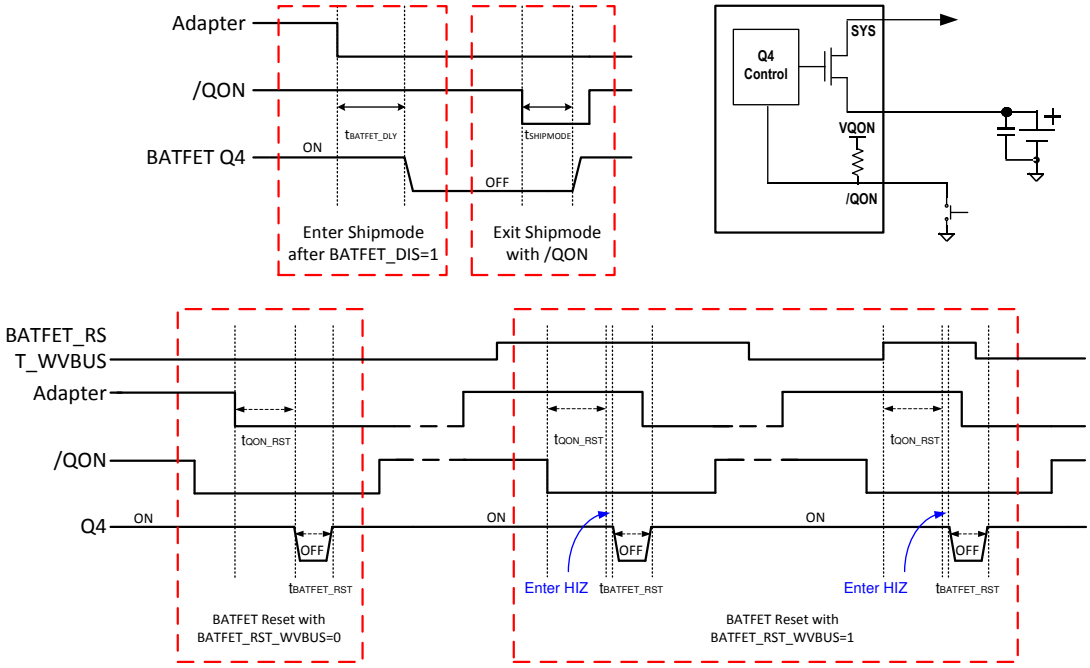


Figure 9-7. $\overline{QON}$ Timing

9.3.8 Status Outputs (STAT, $\overline{INT}$)

9.3.8.1 Charging Status Indicator (STAT)

The device indicates charging state on the open drain STAT pin. The STAT pin can drive LED.

Table 9-5. STAT Pin State

CHARGING STATE	STAT INDICATOR
Charging in progress (including recharge)	LOW
Charging termination (top off timer may be running)	HIGH
Sleep mode, charge disable, boost mode	HIGH
Charge suspend (input over-voltage, TS fault, safety timer fault or system over-voltage)	Blinking at 1 Hz

9.3.8.2 Interrupt to Host ($\overline{INT}$)

In some applications, the host does not always monitor the charger operation. The $\overline{INT}$ pulse notifies the host on the device operation. The following events will generate a 256-μs $\overline{INT}$ pulse.

- Good input source detected
  - V_{VBUS} above battery (not in sleep)
  - V_{VBUS} below V_{ACOV} threshold

  - V_{VBUS} above $V_{POORSRC}$ (typical 3.8 V) when I_{BADSRC} (typical 30 mA) current is applied (not a poor source)
- Input adapter removed
- USB/adapter source identified during Input Source Type Detection (IINDPM Threshold).
- Charge complete
- Any FAULT event in REG09
- VINDPM / IINDPM event detected (REG0A[1:0], maskable)
- Top off timer starts and expires

REG09[7:0] and REG0A[6:4] report charger operation faults and status change to the host. When a fault/status change occurs, the charger sends out an $\overline{INT}$ pulse and keeps the state in REG09[7:0]/REG0A[6:4] until the host reads the registers. Before the host reads REG09[7:0]/REG0A[6:4] and all the ones are cleared, the charger would not send any $\overline{INT}$ upon new fault/status change. To read the current status, the host has to read REG09/REG0A two times consecutively. The first read reports the pre-existing register status and the second read reports the current register status.

9.3.9 Protections

9.3.9.1 Voltage and Current Monitoring in Buck Mode

9.3.9.1.1 Input Over-Voltage Protection (ACOV)

The input voltage is sensed via the VAC pin. The default OVP threshold is 14.2-V, and can be programmed at 5.7 V/6.4 V/11 V/14.2 V via OVP[1:0] register bits . ACOV event will immediately stop converter switching whether in buck or boost mode. The device will automatically resume normal operation once the input voltage drops back below the OVP threshold. During ACOV, REGN LDO is on, and the device doesn't enter HIZ mode.

During ACOV, the fault register CHRG_FAULT bits are set to 01. An $\overline{INT}$ pulse is asserted to the host.

9.3.9.1.2 System Over-Voltage Protection (SYSOVP)

The charger device clamps the system voltage during a load transient so that the components connected to the system are not damaged due to high voltage. V_{SYS_OVP} threshold is about 300-mV above battery regulation voltage when battery charging is terminated. Upon SYSOVP, converter stops switching immediately to clamp the overshoot. The charger pulls 30-mA I_{SYS_LOAD} discharge current to bring down the system voltage.

9.3.9.2 Voltage and Current Monitoring in Boost Mode

9.3.9.2.1 Boost Mode Over-Voltage Protection

When the PMID voltage rises above regulation the target and exceeds V_{BST_OVP}, the device stops switching immediately and the device exits boost mode and PMID_GOOD is pulled low as well after the boost mode OVP lasts for 12 ms. Meanwhile, if VAC (and VBUS when shorted to VAC) voltage exceed V_{ACOV}, the device will exit boost mode as well. BST_CONFIG bit is set to 0. During boost mode over-voltage, the fault register bit BOOST_FAULT is set tot 1 to indicate fault in boost operation. An $\overline{INT}$ is asserted to the host.

9.3.9.3 Thermal Regulation and Thermal Shutdown

9.3.9.3.1 Thermal Protection in Buck Mode

Besides the battery temperature monitor on TS pin, the device monitors the internal junction temperature T_J to avoid overheating the chip and limits the IC junction temperature in buck mode. When the internal junction temperature exceeds thermal regulation limit (110°C), the device lowers down the charge current. During thermal regulation, the actual charging current is usually below the programmed battery charging current. Therefore, termination is disabled, the safety timer runs at half the clock rate, and the status register THERM_STAT bit goes high.

Additionally, the device has thermal shutdown to turn off the converter and BATFET when IC surface temperature exceeds T_{SHUT} 150°C. The BATFET and converter is enabled to recover when IC temperature is 130°C. The fault register CHRG_FAULT is set to 10 during thermal shutdown and an $\overline{INT}$ is asserted to the host.

9.3.9.3.2 Thermal Protection in Boost Mode

Besides the battery temperature monitor on TS pin, The device monitors the internal junction temperature to provide thermal shutdown during boost mode. When IC junction temperature exceeds T_{SHUT} 150°C, the boost

mode is disabled by setting BST_CONFIG bit low . When IC junction temperature is below 145°C, the host can re-enable boost mode.

9.3.9.4 Battery Protection

9.3.9.4.1 Battery Over-Voltage Protection (BATOVP)

The battery over-voltage limit is clamped at 4% above the battery regulation voltage. When battery over-voltage occurs, the charger device immediately stops switching. The fault register BAT_FAULT bit goes high and an $\overline{INT}$ is asserted to the host.

9.3.9.4.2 Battery Over-Discharge Protection

When battery is discharged below $V_{BAT\_DPL\_FALL}$, the BATFET will latch off to protect battery from over discharge. To recover from over-discharge latch-off, an input source plug-in is required at VAC/VBUS.

9.3.9.4.3 System Over-Current Protection

$I_{SYS\_OCP\_Q4}$ sets battery discharge current limit. Once $I_{BAT} > I_{SYS\_OCP\_Q4}$, charger will latch off Q4 and put the device into ship mode. All methods to exit ship mode are valid to bring the part out of Q4 latch off.

9.3.10 Serial Interface

The device uses I^2C compatible interface for flexible charging parameter programming and instantaneous device status reporting. I^2C^{TM} is a bi-directional 2-wire serial interface developed by Philips Semiconductor (now NXP Semiconductors). Only two bus lines are required: a serial data line (SDA) and a serial clock line (SCL). Devices can be considered as masters or slaves when performing data transfers. A master is the device which initiates a data transfer on the bus and generates the clock signals to permit that transfer. At that time, any device addressed is considered a slave.

The device operates as a slave device with address 6BH , receiving control inputs from the master device like micro controller or a digital signal processor through REG00-REG0C. Register read beyond REG0C returns 0xFF. The I^2C interface supports both standard mode (up to 100 kbits), and fast mode (up to 400 kbits). connecting to the positive supply voltage via a current source or pull-up resistor. When the bus is free, both lines are HIGH. The SDA and SCL pins are open drain.

9.3.10.1 Data Validity

The data on the SDA line must be stable during the HIGH period of the clock. The HIGH or LOW state of the data line can only change when the clock signal on the SCL line is LOW. One clock pulse is generated for each data bit transferred.

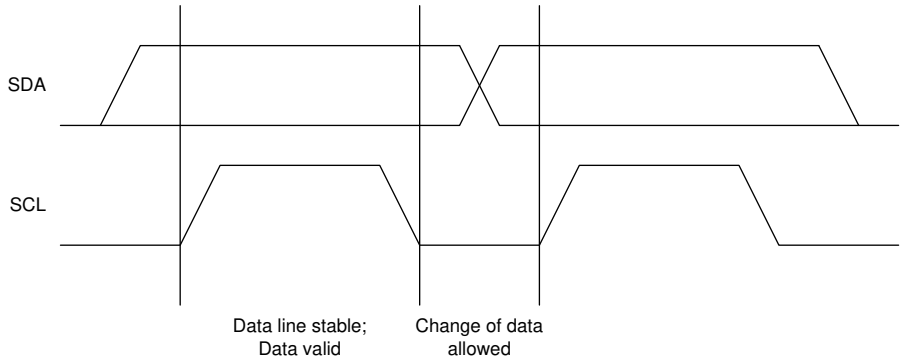


Figure 9-8. Bit Transfer on the I^2C Bus

9.3.10.2 START and STOP Conditions

All transactions begin with a START (S) and can be terminated by a STOP (P). A HIGH to LOW transition on the SDA line while SCL is HIGH defines a START condition. A LOW to HIGH transition on the SDA line when the SCL is HIGH defines a STOP condition. START and STOP conditions are always generated by the master. The bus is considered busy after the START condition, and free after the STOP condition.

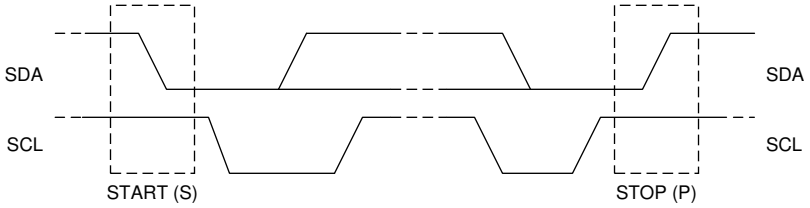


Figure 9-9. TS START and STOP conditions

9.3.10.3 Byte Format

Every byte on the SDA line must be 8 bits long. The number of bytes to be transmitted per transfer is unrestricted. Each byte has to be followed by an Acknowledge bit. Data is transferred with the Most Significant Bit (MSB) first. If a slave cannot receive or transmit another complete byte of data until it has performed some other function, it can hold the clock line SCL low to force the master into a wait state (clock stretching). Data transfer then continues when the slave is ready for another byte of data and release the clock line SCL.

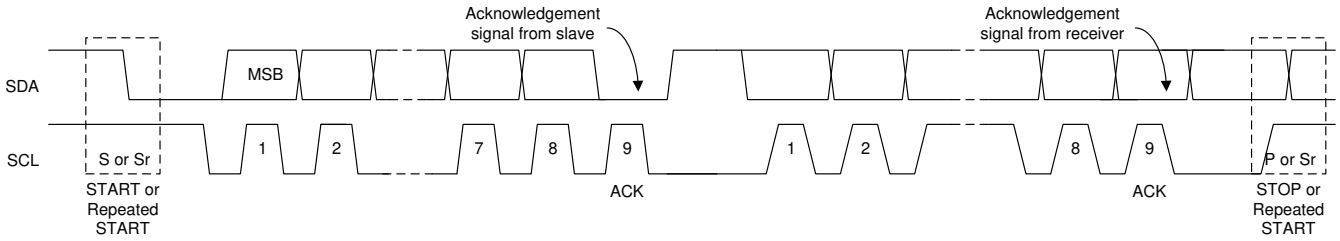


Figure 9-10. Data Transfer on the I²C Bus

9.3.10.4 Acknowledge (ACK) and Not Acknowledge (NACK)

The acknowledge takes place after every byte. The acknowledge bit allows the receiver to signal the transmitter that the byte was successfully received and another byte may be sent. All clock pulses, including the acknowledge ninth clock pulse, are generated by the master. The transmitter releases the SDA line during the acknowledge clock pulse so the receiver can pull the SDA line LOW and it remains stable LOW during the HIGH period of this clock pulse.

When SDA remains HIGH during the ninth clock pulse, this is the Not Acknowledge signal. The master can then generate either a STOP to abort the transfer or a repeated START to start a new transfer.

9.3.10.5 Slave Address and Data Direction Bit

After the START, a slave address is sent. This address is 7 bits long followed by the eighth bit as a data direction bit (bit R/W). A zero indicates a transmission (WRITE) and a one indicates a request for data (READ).

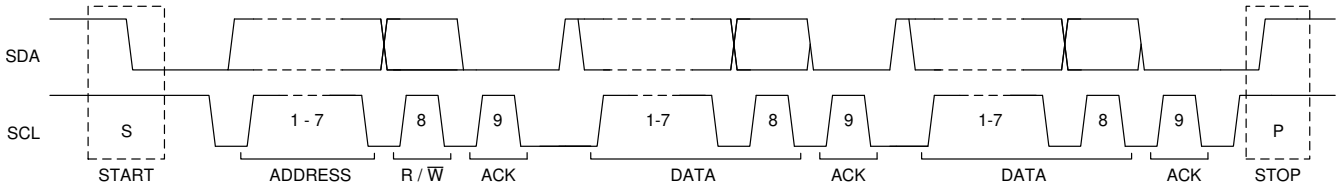


Figure 9-11. Complete Data Transfer

9.3.10.6 Single Read and Write

If the register address is not defined, the charger IC send back NACK and go back to the idle state.

1	7	1	1	8	1	8	1	1
S	Slave Address	0	ACK	Reg Addr	ACK	Data to Addr	ACK	P

Figure 9-12. Single Write

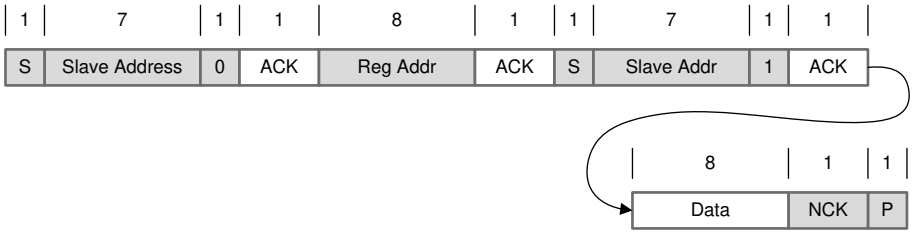


Figure 9-13. Single Read

9.3.10.7 Multi-Read and Multi-Write

The charger device supports multi-read and multi-write on REG00 through REG0C.

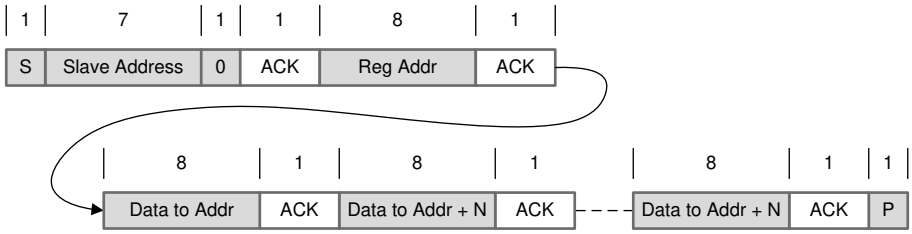


Figure 9-14. Multi-Write

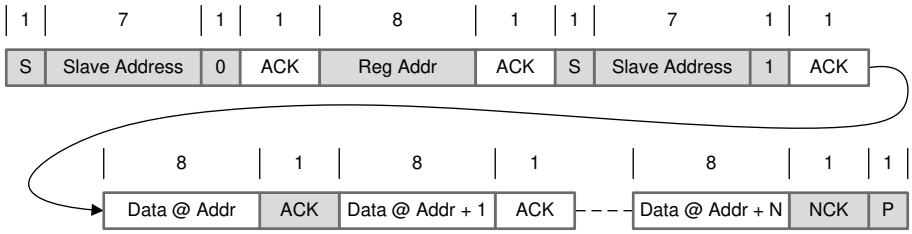


Figure 9-15. Multi-Read

REG09[7:0]/REG0A[6:4] are fault/status change register. They keep all the fault/status information from last read until the host issues a new read. For example, if Charge Safety Timer Expiration fault occurs but recovers later, the fault register REG09 reports the fault when it is read the first time, but returns to normal when it is read the second time. In order to get the fault information at present, the host has to read REG09/REG0A for the second time.

9.4 Device Functional Modes

9.4.1 Host Mode and Default Mode

The device is a host controlled charger, but it can operate in default mode without host management. In default mode, the device can be used an autonomous charger with no host or while host is in sleep mode. When the charger is in default mode, WATCHDOG_FAULT bit is HIGH. When the charger is in host mode, WATCHDOG_FAULT bit is LOW.

After power-on-reset, the device starts in default mode with watchdog timer expired, or default mode. All the registers are in the default settings.

All the device parameters can be programmed by the host. To keep the device in host mode, the host has to reset the watchdog timer by writing 1 to WD_RST bit before the watchdog timer expires (WATCHDOG_FAULT bit is set), or disable watchdog timer by setting WATCHDOG bits = 00.

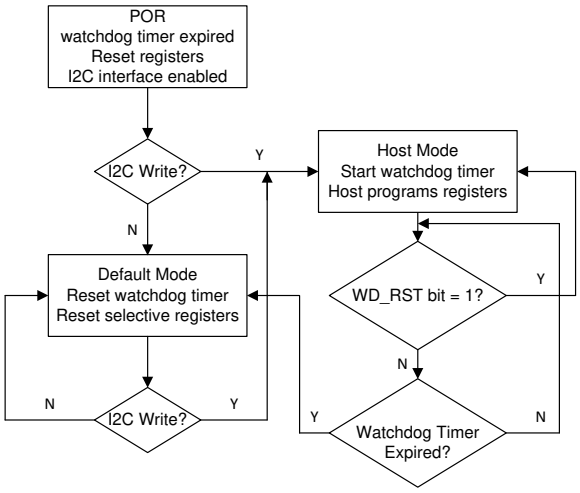


Figure 9-16. Watchdog Timer Flow Chart

9.5 Register Maps

I²C Slave Address: 6BH

Default I²C Slave Address: 0x6B (1101 011B + R/ $\overline{W}$)

Table 9-6. I²C Registers

Address	Access Type	Acronym	Register Name	Section
00h	R/W	REG00	Input Current Limit	Go
01h	R/W	REG01	Charger Control 0	Go
02h	R/W	REG02	Charge Current Limit	Go
03h	R/W	REG03	pre-charge and Termination Current Limit	Go
04h	R/W	REG04	Battery Voltage Limit	Go
05h	R/W	REG05	Charger Control 1	Go
06h	R/W	REG06	Charger Control 2	Go
07h	R/W	REG07	Charger Control 3	Go
08h	R	REG08	Charger Status 0	Go
09h	R	REG09	Charger Status 1	Go
0Ah	R	REG0A	Charger Status 2	Go
0Bh	R	REG0B	Part Information	Go
0Ch	R/W	REG0C	Charger Control 4	Go

Complex bit access types are encoded to fit into small table cells. Table 9-7 shows the codes that are used for access types in this section.

Table 9-7. I²C Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset Value		
-n		Value after reset
-X		Undefined value

9.5.1 Input Current Limit Register (Address = 00h) [reset = 17h]

Figure 9-17. REG00 Register

7	6	5	4	3	2	1	0
0	0	0	1	0	1	1	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-8. REG00 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	EN_HIZ	0	R/W	by REG_RST by Watchdog	HIZ mode enable in buck mode. 0 – Disable (default) 1 – Enable	
6	TS_IGNORE	0	R/W	by REG_RST	When charger does not monitor the NTC, host sets this bit to 1 to ignore the TS pin condition during charging and boost mode. 0 – Include TS pin into charge and boost mode enable conditions. (default) 1 – Ignore TS pin. Always consider TS is good to allow charging and boost mode. NTC_FAULT bits are 000 to report normal status.	
5	BATSNS_DIS	0	R/W	by REG_RST	Select either BATSNS pin or BAT pin to regulate battery voltage. 0 – Enable BATSNS in battery CV regulation. If the device fails BATSNS open/short detection (BATSNS_STAT = 1). Battery voltage is regulated through BAT pin. (default) 1 – Disable BATSNS. Use BAT pin in battery CV regulation.	
4	IINDPM[4]	1	R/W	by REG_RST	1600 mA	Input current limit setting (maximum limit, not typical) Offset: 100 mA Range: 100 mA (000000) – 3.2 A (11111) Default: 2400 mA (10111) IINDPM bits are changed automatically after Onput Source Type Detection (IINDPM Threshold) is completed USB SDP = 500 mA USB CDP = 1.5 A USB DCP = 2.4 A Unknown Adapter = 500 mA Non-Standard Adapter = 1 A, 2 A, 2.1 A, or 2.4 Host can reprogram IINDPM register bits after input source detection is completed.
3	IINDPM[3]	0	R/W	by REG_RST	800 mA	
2	IINDPM[2]	1	R/W	by REG_RST	400 mA	
1	IINDPM[1]	1	R/W	by REG_RST	200 mA	
0	IINDPM[0]	1	R/W	by REG_RST	100 mA	

LEGEND: R/W = Read/Write; R = Read only

9.5.2 Charger Control 0 Register (Address = 01h) [reset = 1Ah]

Figure 9-18. REG01 Register

7	6	5	4	3	2	1	0
0	0	0	1	1	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-9. REG01 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	PFM_DIS	0	R/W	by REG_RST	PFM disable in both buck and boost mode. 0 – PFM enable (default) 1 – PFM disable
6	WD_RST	0	R/W	by REG_RST by Watchdog	I^2C Watchdog timer reset. Back to 0 after watchdog timer reset 0 – Normal (default) 1 – Reset
5	BST_CONFIG	0	R/W	by REG_RST by Watchdog	Boost mode enable. In charging case application, based on adapter plug-in or removal, the charger will automatically transit between charging mode and boost mode by setting BST_CONFIG bit and CHG_CONFIG bit both to 1. 0 – Boost mode disable (default) 1 – Boost mode enable
4	CHG_CONFIG	1	R/W	by REG_RST by Watchdog	Battery charging buck mode enable. Charging is enabled when $\overline{CE}$ pin is pulled low, CHG_CONFIG bit is 1 and charge current is not zero. 0 – Charge Disable 1 – Charge Enable (default)
3	SYS_MIN[2]	1	R/W	by REG_RST	System minimum voltage setting. 000 – 2.6 V 001 – 2.8 V 010 – 3 V 011 – 3.2 V 100 – 3.4 V 101 – 3.5 V (default) 110 – 3.6 V 111 – 3.7 V
2	SYS_MIN[1]	0	R/W	by REG_RST	
1	SYS_MIN[0]	1	R/W	by REG_RST	
0	MIN_VBAT_SEL	0	R/W	by REG_RST	Minimum battery voltage when exiting boost mode. The rising threshold allows the device to start boost mode if other conditions are valid. 0 – 2.8V V_{BAT} falling, 3 V rising (default) 1 – 2.5V V_{BAT} falling, 2.8V rising

LEGEND: R/W = Read/Write; R = Read only

9.5.3 Charge Current Limit Register (Address = 02h) [reset = 91h]

Figure 9-19. REG02 Register

7	6	5	4	3	2	1	0
1	0	0	1	0	0	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-10. REG02 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	BOOST_LIM	1	R/W	by REG_RST by Watchdog	Boost mode current regulation limit (minimum current limit, not typical). 0 – 0.5 A 1 – 1.2 A (default)
6	Q1_FULLON	0	R/W	by REG_RST	In buck mode, charger will fully turn on Q1 RBFET according to this bit setting when IINDPM is below 700 mA. When IINDPM is over 700 mA, Q1 is always fully on. In boost mode , Q1 is always fully on too, regardless of this bit setting. 0 – Partially turn on Q1 for better regulation accuracy when IINDPM is below 700 mA. (default) 1 – Fully turn on Q1 for better efficiency when IINDPM is below 700 mA.
5	ICHG[5]	0	R/W	by REG_RST by Watchdog	1920 mA
4	ICHG[4]	1	R/W	by REG_RST by Watchdog	960 mA
3	ICHG[3]	0	R/W	by REG_RST by Watchdog	480 mA
2	ICHG[2]	0	R/W	by REG_RST by Watchdog	240 mA
1	ICHG[1]	0	R/W	by REG_RST by Watchdog	120 mA
0	ICHG[0]	1	R/W	by REG_RST by Watchdog	60 mA

Fast charge current setting
Default: 1020 mA (010001)
Range: 0 mA (0000000) – 3000 mA (110010)
I_{CHG} 0 mA disables charge.
I_{CHG} > 3000 mA is clamped to 3000 mA (110010)

LEGEND: R/W = Read/Write; R = Read only

9.5.4 Pre-charge and Termination Current Limit Register (Address = 03h) [reset = 12h]

Figure 9-20. REG03 Register

7	6	5	4	3	2	1	0
0	0	0	1	0	0	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-11. REG03 Field Descriptions

Bit	Field	POR	Type	Reset	Description	
7	IPRECHG[3]	0	R/W	by REG_RST by Watchdog	480 mA	Pre-charge current setting Default: 180 mA (0010) Range: 60 mA (0000) – 780 mA (1100) Offset: 60 mA Note: I_{PRECHG} > 780 mA is clamped to 780 mA (1100)
6	IPRECHG[2]	0	R/W	by REG_RST by Watchdog	240 mA	
5	IPRECHG[1]	1	R/W	by REG_RST by Watchdog	120 mA	
4	IPRECHG[0]	0	R/W	by REG_RST by Watchdog	60 mA	
3	ITERM[3]	0	R/W	by REG_RST by Watchdog	480 mA	Termination current setting Default: 180 mA (0010) Range: 60 mA – 780 mA (1100) Offset: 60 mA
2	ITERM[2]	0	R/W	by REG_RST by Watchdog	240 mA	
1	ITERM[1]	1	R/W	by REG_RST by Watchdog	120 mA	
0	ITERM[0]	0	R/W	by REG_RST by Watchdog	60 mA	

LEGEND: R/W = Read/Write; R = Read only

9.5.5 Battery Voltage Limit Register (Address = 04h) [reset = 40h]

Figure 9-21. REG04 Register

7	6	5	4	3	2	1	0
0	1	0	0	0	0	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-12. REG04 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	VBATREG[4]	0	R/W	by REG_RST by Watchdog	Battery voltage setting, also called V_{REG}. Default: 4.190 V (01000) 00000 – 3.494 V 00001 – 3.590 V 00010 – 3.686 V 00011 – 3.790 V 00100 – 3.894 V 00101 – 3.990 V 00110 – 4.090 V 00111 – 4.140 V 01000 – 4.190 V 01001 - 11111 – 4.290 V - 4.510 V, 10 mV/step 01110 4.340 V, 10011 4.390V, 11000 4.440 V, 11101 4.490 V
6	VBATREG[3]	1	R/W	by REG_RST by Watchdog	
5	VBATREG[2]	0	R/W	by REG_RST by Watchdog	
4	VBATREG[1]	0	R/W	by REG_RST by Watchdog	
3	VBATREG[0]	0	R/W	by REG_RST by Watchdog	
2	TOPOFF_TIMER[1]	0	R/W	by REG_RST by Watchdog	Top-off timer setting. 00 – Disabled (Default) 01 – 15 minutes 10 – 30 minutes 11 – 45 minutes
1	TOPOFF_TIMER[0]	0	R/W	by REG_RST by Watchdog	
0	VRECHG	0	R/W	by REG_RST by Watchdog	Battery recharge threshold setting. 0 – 120 mV (default) 1 – 210 mV

LEGEND: R/W = Read/Write; R = Read only

9.5.6 Charger Control 1 Register (Address = 05h) [reset = 9Eh]

Figure 9-22. REG05 Register

7	6	5	4	3	2	1	0
1	0	0	1	1	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-13. REG05 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	EN_TERM	1	R/W	by REG_RST by Watchdog	Battery charging termination enable. 0 – Disable 1 – Enable (default)
6	Reserved	0	R/W	by REG_RST by Watchdog	Reserved
5	WATCHDOG[1]	0	R/W	by REG_RST by Watchdog	Watchdog timer setting. 00 – Disable timer 01 – 40 s (default) 10 – 80 s 11 – 160 s
4	WATCHDOG[0]	1	R/W	by REG_RST by Watchdog	
3	EN_TIMER	1	R/W	by REG_RST by Watchdog	Battery charging safety timer enable, including both fast charge and pre-charge timers. Pre-charge timer is 2 hours. Fast charge timer is set by REG05[2] 0 – Disable 1 – Enable timer (default)
2	CHG_TIMER	1	R/W	by REG_RST by Watchdog	Battery fast charging safety timer setting. 0 – 20 hrs 1 – 10 hrs (default)
1	TREG	1	R/W	by REG_RST by Watchdog	Thermal Regulation Threshold: 0 – 90°C 1 – 110°C (default)
0	JEITA_VSET (45C-60C)	0	R/W	by REG_RST by Watchdog	Battery voltage setting during JEITA warm (T3 - T5, typically 45C - 60C) 0 – Set Charge Voltage to 4.1 V (max) (default) 1 – Set Charge Voltage to V_{REG}

LEGEND: R/W = Read/Write; R = Read only

9.5.7 Charger Control 2 Register (Address = 06h) [reset = E6h]

Figure 9-23. REG06 Register

7	6	5	4	3	2	1	0
1	1	1	0	0	1	1	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-14. REG06 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	OVP[1]	1	R/W	by REG_RST	V_{ACOV} threshold during buck mode and boost mode. 00 – 5.85 V 01 – 6.4 V (5-V input) 10 – 11 V (9-V input) 11 – 14.2 V (12-V input) (default)
6	OVP[0]	1	R/W	by REG_RST	
5	BOOSTV[1]	1	R/W	by REG_RST	Boost regulation voltage setting 00 – 4.6 V 01 – 4.75 V 10 – 5.0 V (default) 11 – 5.15 V
4	BOOSTV[0]	0	R/W	by REG_RST	
3	VINDPM[3]	0	R/W	by REG_RST	800 mV VINDPM threshold setting Default: 4.5 V (0110) Range: 3.9 V (0000) – 5.4 V (1111) Offset: 3.9 V
2	VINDPM[2]	1	R/W	by REG_RST	400 mV
1	VINDPM[1]	1	R/W	by REG_RST	200 mV
0	VINDPM[0]	0	R/W	by REG_RST	100 mV

LEGEND: R/W = Read/Write; R = Read only

9.5.8 Charger Control 3 Register (Address = 07h) [reset = 4Ch]

Figure 9-24. REG07 Register

7	6	5	4	3	2	1	0
0	1	0	0	1	1	0	0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-15. REG07 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	IINDET_EN	0	R/W	by REG_RST by Watchdog	Force input source type detection. After the detection is complete, this bit returns to 0. 0 – Not in input current limit detection. (default) 1 – Force input current limit detection when adapter is present.
6	TMR2X_EN	1	R/W	by REG_RST by Watchdog	Safety timer is slowed by 2X during input DPM, JEITA cool/warm or thermal regulation. 0 – Disable. Safety timer duration is set by REG05[2]. 1 – Safety timer slowed by 2X during input DPM (both V and I) or JEITA cool/warm (except I_{CHG}=100%), or thermal regulation. (default)
5	BATFET_DIS	0	R/W	by REG_RST	BATFET Q4 ON/OFF control. Set this bit to 1 to enter ship mode. To reset the device with adapter present, the host shall set BATFET_RST_WVBUS to 1 and then BATFET_DIS to 1. 0 – Turn on Q4. (default) 1 – Turn off Q4 after t_{BATFET_DLY} delay time (REG07[3])
4	BATFET_RST_WVBUS	0	R/W	by REG_RST	Start BATFET full system reset with or without adapter present. 0 – Start BATFET full system reset after adapter is removed from VBUS. (default) 1 – Start BATFET full system reset when adapter is present on VBUS.
3	BATFET_DLY	1	R/W	by REG_RST	Delay from BATFET_DIS (REG07[5]) set to 1 to BATFET turn off during ship mode. 0 – Turn off BATFET immediately when BATFET_DIS bit is set. 1 – Turn off BATFET after t_{BATFET_DLY} (typ 10 s) when BATFET_DIS bit is set. (default)
2	BATFET_RST_EN	1	R/W	by REG_RST by Watchdog	Enable BATFET full system reset. The time to start of BATFET full system reset is based on the setting of BATFET_RST_WVBUS bit. 0 – Disable BATFET reset function 1 – Enable BATFET reset function when REG07[5] is also 1. (default)
1	VINDPM_BAT_TRACK[1]	0	R/W	by REG_RST	Sets VINDPM to track BAT voltage. Actual VINDPM is higher of register value and V_{BAT} + VINDPM_BAT_TRACK. 00 – Disable function (VINDPM set by register) (default) 01 – V_{BAT} + 200 mV 10 – V_{BAT} + 250 mV 11 – V_{BAT} + 300 mV
0	VINDPM_BAT_TRACK[0]	0	R/W	by REG_RST	

LEGEND: R/W = Read/Write; R = Read only

9.5.9 Charger Status 0 Register (Address = 08h)

Figure 9-25. REG08

7	6	5	4	3	2	1	0
x	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-16. REG08 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	VBUS_STAT[2]	x	R	NA	VBUS Status register Software current limit is reported in IINDPM register
6	VBUS_STAT[1]	x	R	NA	
5	VBUS_STAT[0]	x	R	NA	
4	CHRG_STAT[1]	x	R	NA	Charging status: 00 – Not Charging 01 – Pre-charge or trickle charge (< $V_{BATLOWV}$) 10 – Fast Charging 11 – Charge Termination
3	CHRG_STAT[0]	x	R	NA	
2	Reserved	x	R	NA	Reserved
1	THERM_STAT	x	R	NA	0 – Not in thermal regulation 1 – In thermal regulation
0	VSYS_STAT	x	R	NA	0 – Not in SYS_MIN regulation (V_{BAT} > V_{SYS_MIN}) 1 – In SYS_MIN regulation (V_{BAT} < V_{SYS_MIN})

LEGEND: R/W = Read/Write; R = Read only

9.5.10 Charger Status 1 Register (Address = 09h)

Figure 9-26. REG09 Register

7	6	5	4	3	2	1	0
1	x	x	x	x	x	x	x
R	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-17. REG09 Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	WATCHDOG_FAULT	1	R	NA	0 – Normal, device is in host mode, 1 – Watchdog timer expiration, device is in default mode.
6	BOOST_FAULT	x	R	NA	0 – Normal 1 – Fault detected in boost mode (any conditions that are not valid for boost operation), including VBUS overloaded (BST_OVP) or battery is too low (BST_BAT)
5	CHRG_FAULT[1]	x	R	NA	00 – Normal 01 – Input fault 10 – Thermal shutdown 11 – Charge safety timer expiration
4	CHRG_FAULT[0]	x	R	NA	
3	BAT_FAULT	x	R	NA	0 – Normal, 1 – Battery over voltage.
2	NTC_FAULT[2]	x	R	NA	TS fault in buck mode 000 – Normal 010 – Warm 011 – Cool 101 – Cold 110 – Hot TS fault in boost mode 000 – Normal 101 – Cold 110 – Hot
1	NTC_FAULT[1]	x	R	NA	
0	NTC_FAULT[0]	x	R	NA	

LEGEND: R/W = Read/Write; R = Read only

9.5.11 Charger Status 2 Register (Address = 0Ah)

Figure 9-27. REG0A Register

7	6	5	4	3	2	1	0
x	x	x	x	x	x	0	0
R	R	R	R	R	R	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-18. REG0A Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	VBUS_GD	x	R	NA	0 – VBUS does not pass poor source detection 1 – VBUS passes poor source detection
6	VINDPM_STAT	x	R	NA	0 – Not in VINDPM 1 – In VINDPM
5	IINDPM_STAT	x	R	NA	0 – Not in IINDPM 1 – In IINDPM
4	BATSNS_STAT	x	R	NA	0 – BATSNS pin is in good connection. Regulation battery voltage through BATSNS pin. 1 – BATSNS pin is open/short. Regulate battery voltage through BAT pin.
3	TOPOFF_ACTIVE	x	R	NA	0 – Top off timer not counting. 1 – Top off timer counting
2	ACOV_STAT	x	R	NA	0 – Not in ACOV 1 – In ACOV
1	VINDPM_INT_ MASK	0	R/W	by REG_RST	Allow or block $\overline{\text{INT}}$ pulse assertion to host during VINDPM. 0 – $\overline{\text{INT}}$ is asserted to host during VINDPM (default) 1 – No $\overline{\text{INT}}$ pulse asserted to host during VINDPM
0	IINDPM_INT_ MASK	0	R/W	by REG_RST	Allow or block $\overline{\text{INT}}$ pulse assertion to host during IINDPM 0 – $\overline{\text{INT}}$ is asserted to host during IINDPM (default) 1 – No $\overline{\text{INT}}$ pulse asserted to host during IINDPM

LEGEND: R/W = Read/Write; R = Read only

9.5.12 Part Information Register (Address = 0Bh)

Figure 9-28. REG0B Register

7	6	5	4	3	2	1	0
0	1	0	1	0	1	0	0
R/W	R	R	R	R	R	R	R

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-19. REG0B Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	REG_RST	0	R/W	NA	Register reset 0 – Keep current register setting (default) 1 – Reset to default register value and reset safety timer. This bit returns to 0 after register reset is completed.
6	PN[3]	1	R	NA	BQ25611D: 1010
5	PN[2]	0	R	NA	
4	PN[1]	1	R	NA	
3	PN[0]	0	R	NA	
2	Reserved	1	R	NA	Reserved
1	Reserved	0	R	NA	Reserved
0	Reserved	0	R	NA	

LEGEND: R/W = Read/Write; R = Read only

9.5.13 Charger Control 4 Register (Address = 0Ch) [reset = 75h]

Figure 9-29. REG0C

7	6	5	4	3	2	1	0
0	1	1	1	0	1	0	1
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

LEGEND: R/W = Read/Write; R = Read only; -n = value after reset

Table 9-20. REG0C Field Descriptions

Bit	Field	POR	Type	Reset	Description
7	JEITA_COOL_ISET [1]	0	R/W	by REG_RST by Watchdog	Fast charge current setting during cool temperature range (T1 - T2), as percentage of I_{CHG} in REG02[5:0]. 00 – No Charge 01 – 20% of I_{CHG} (default) 10 – 50% of I_{CHG} 11 – 100% of I_{CHG} (safety timer does not become 2X)
6	JEITA_COOL_ISET [0]	1	R/W	by REG_RST by Watchdog	
5	JEITA_WARM_ISET [1]	1	R/W	by REG_RST by Watchdog	Fast charge current setting during warm temperature range (T3 - T5), as percentage of I_{CHG} in REG02[5:0]. 00 – No Charge 01 – 20% of I_{CHG} 10 – 50% of I_{CHG} 11 – 100% of I_{CHG} (safety timer does not become 2X) (default)
4	JEITA_WARM_ISET [0]	1	R/W	by REG_RST by Watchdog	
3	JEITA_VT2 [1]	0	R/W	by REG_RST by Watchdog	00 – VT2% = 70.75% (5.5°C) 01 – VT2% = 68.25% (10°C) (default) 10 – VT2% = 65.25% (15°C) 11 – VT2% = 62.25% (20°C)
2	JEITA_VT2 [0]	1	R/W	by REG_RST by Watchdog	
1	JEITA_VT3 [1]	0	R/W	by REG_RST by Watchdog	00 – VT3% = 48.25% (40°C) 01 – VT3% = 44.75% (44.5°C) (default) 10 – VT3% = 40.75% (50.5°C) 11 – VT3% = 37.75% (54.5°C)
0	JEITA_VT3 [0]	1	R/W	by REG_RST by Watchdog	

LEGEND: R/W = Read/Write; R = Read only

10 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

A typical application consists of the device configured as an I^2C controlled Power Path management device and a single cell battery charger for Li-Ion and Li-polymer batteries used in a wide range of smart phones and other portable devices. It integrates an input reverse-block FET (RBFET, Q1), high-side switching FET (HSFET, Q2), low-side switching FET (LSFET, Q3), and battery FET (BATFET Q4) between the system and battery. The device also integrates a bootstrap diode for the high-side gate drive.

10.2 Typical Application

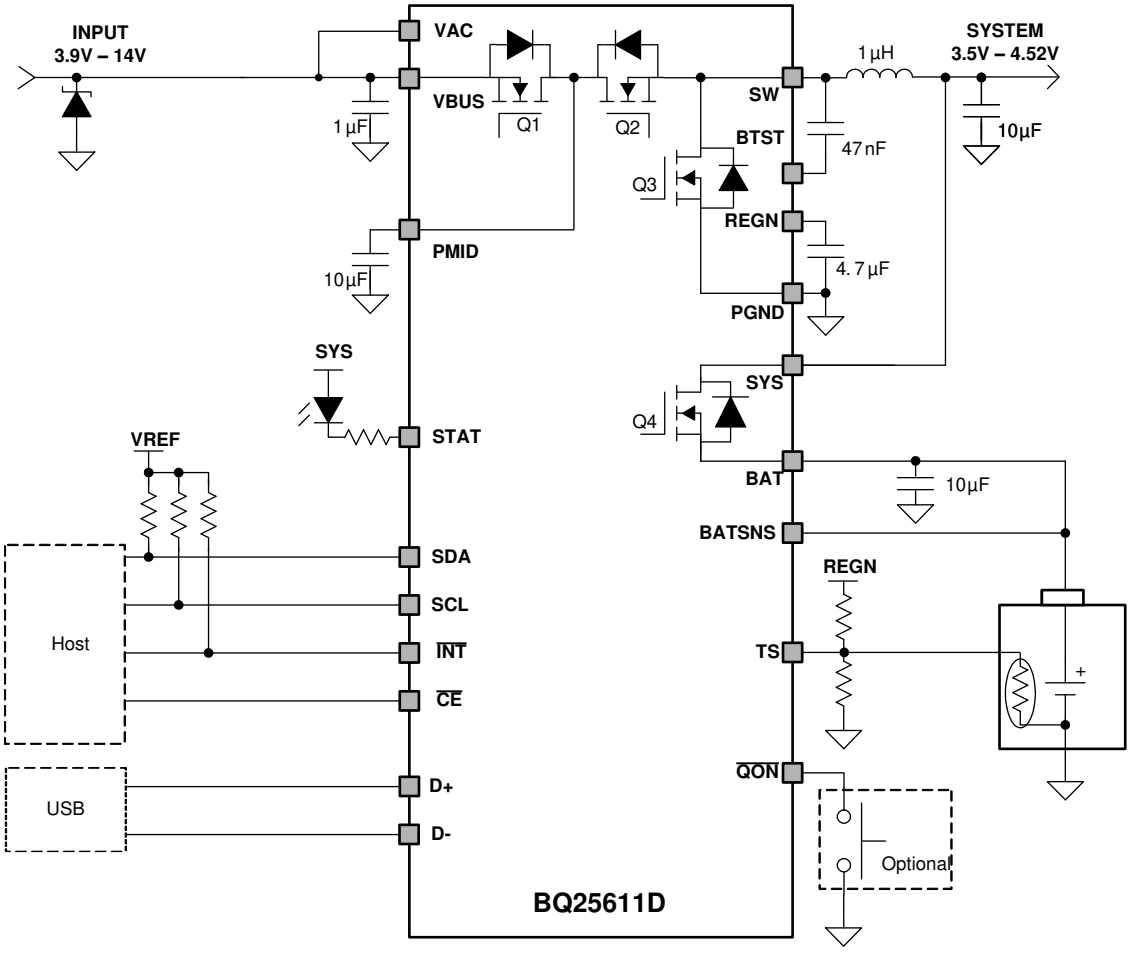


Figure 10-1. BQ25611D Application Diagram

10.2.1 Design Requirements

For this design example, use the parameters shown in the table below.

Table 10-1. Design Parameters

PARAMETER	VALUE
V_{VBUS} voltage range	4 V to 13.5 V
Input current limit (REG00[4:0])	2.4 A
Fast charge current limit (REG02[5:0])	1.024 A
Minimum system voltage (REG01[3:1])	3.5 V
Battery regulation voltage (REG04[7:3])	4.2 V

10.2.2 Detailed Design Procedure

10.2.2.1 Inductor Selection

The 1.5-MHz switching frequency allows the use of small inductor and capacitor values to maintain an inductor saturation current higher than the charging current (I_{CHG}) plus half the ripple current (I_{RIPPLE}):

$$I_{SAT} \geq I_{CHG} + (1/2)\, I_{RIPPLE} \tag{3}$$

The inductor ripple current depends on the input voltage (V_{VBUS}), the duty cycle ($D = V_{BAT}/V_{VBUS}$), the switching frequency (f_S) and the inductance (L).

$$I_{RIPPLE} = \frac{V_{IN} \times D \times (1 - D)}{fs \times L} \tag{4}$$

The maximum inductor ripple current occurs when the duty cycle (D) is 0.5 or approximately 0.5. Usually inductor ripple is designed in the range between 20% and 40% maximum charging current as a trade-off between inductor size and efficiency for a practical design.

10.2.2.2 Input Capacitor and Resistor

Design input capacitance to provide enough ripple current rating to absorb input switching ripple current. The worst case RMS ripple current is half of the charging current when duty cycle is 0.5. If the converter does not operate at 50% duty cycle, then the worst case capacitor RMS current I_{CIN} occurs where the duty cycle is closest to 50% and can be estimated using Equation 5.

$$I_{CIN} = I_{CHG} \times \sqrt{D \times (1 - D)} \tag{5}$$

Low ESR ceramic capacitor such as X7R or X5R is preferred for input decoupling capacitor and should be placed to the drain of the high-side MOSFET and source of the low-side MOSFET as close as possible. Voltage rating of the capacitor must be higher than normal input voltage level. A rating of 25-V or higher capacitor is preferred for 12-V input voltage. Capacitance of minimum 10 µF is suggested for typical of 3-A charging current.

During high current output over 700 mA in boost mode, a 10-kΩ pull-down resistor on VBUS is recommended to keep VBUS low in case Q1 RBFET leakage gets high.

10.2.2.3 Output Capacitor

Ensure that the output capacitance has enough ripple current rating to absorb the output switching ripple current. Equation 6 shows the output capacitor RMS current I_{COUT} calculation.

$$I_{COUT} = \frac{I_{RIPPLE}}{2 \times \sqrt{3}} \approx 0.29 \times I_{RIPPLE} \tag{6}$$

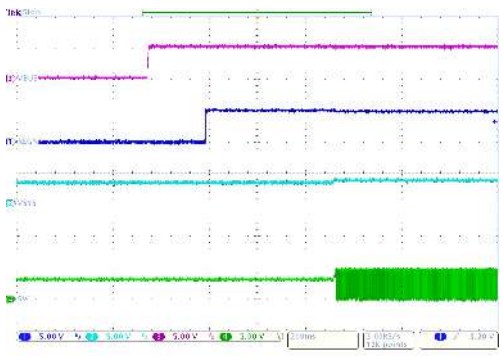
The output capacitor voltage ripple can be calculated as follows:

$$\Delta V_O = \frac{V_{OUT}}{8LCfs^2}\left(1 - \frac{V_{OUT}}{V_{IN}}\right) \quad (7)$$

At certain input and output voltage and switching frequency, the voltage ripple can be reduced by increasing the output filter LC.

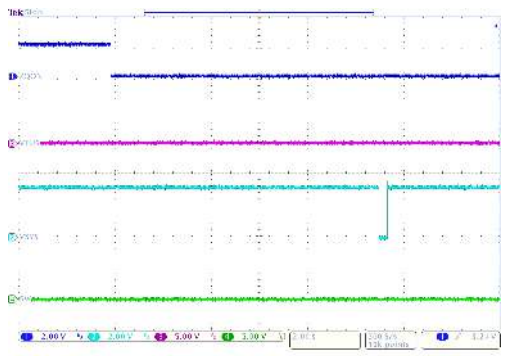
The charger device has internal loop compensation optimized for > 10-µF ceramic output capacitance. The preferred ceramic capacitor is 10-V rating, X7R or X5R.

10.3 Application Curves



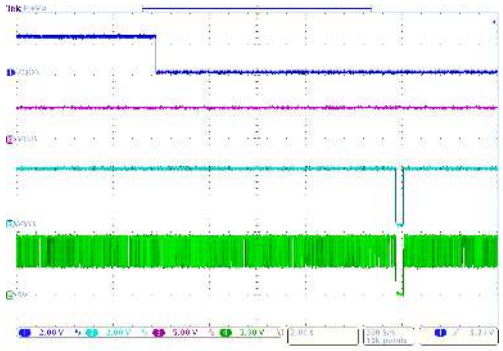
V_{VBUS} = 5 V V_{BAT} = 3.2 V

Figure 10-2. Power Up



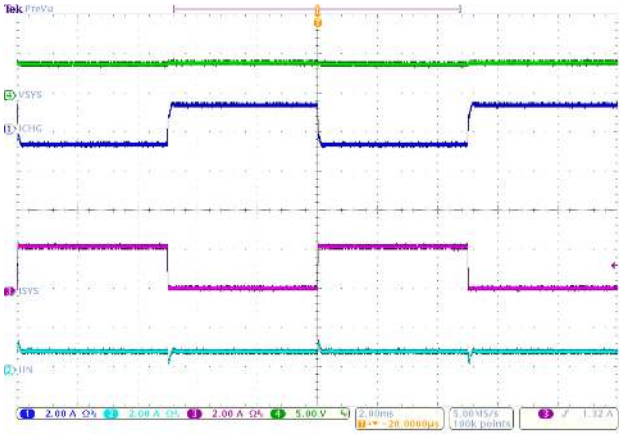
V_{VBAT} = 3.2 V

Figure 10-3. System Reset by $\overline{QON}$ without VBUS Present



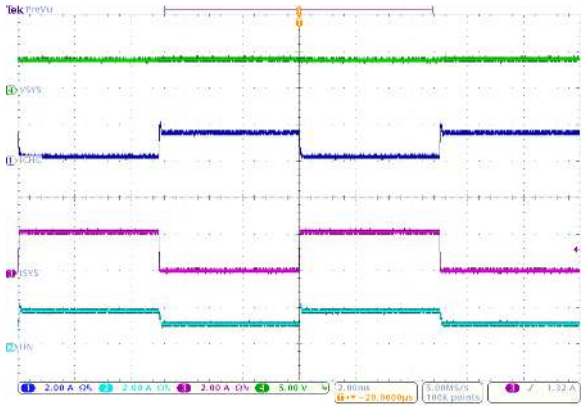
I_{CHG} = 0.5 A V_{VBUS} = 5 V V_{BAT} = 3.2 V

Figure 10-4. System Reset by $\overline{QON}$ with VBUS Present



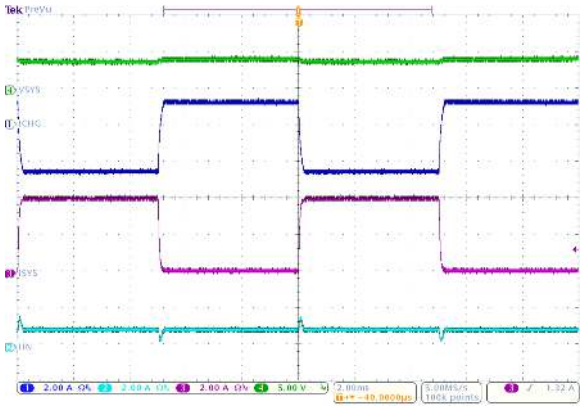
I_{SYS} = 0 - 2 A V_{VBUS} = 5 V IINDPM = 1 A
I_{CHG} = 1.5 A V_{BAT} = 3.7 V

Figure 10-5. System Load Transient Response



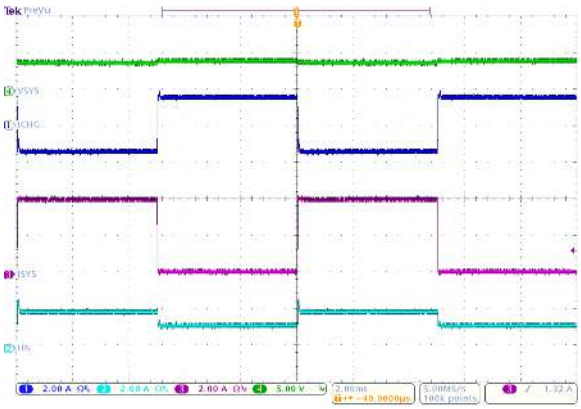
I_{SYS} = 0 – 2 A V_{VBUS} = 5 V IINDPM = 2 A
I_{CHG} = 1 A V_{BAT} = 3.7 V

Figure 10-6. System Load Transient Respose



I_{SYS} = 0 – 4 A V_{VBUS} = 5 V IINDPM = 1 A
I_{CHG} = 1.5 A V_{BAT} = 3.7 V

Figure 10-7. System Load Transient Response



I_{SYS} = 0 – 4 A V_{VBUS} = 5 V IINDPM = 2 A
I_{CHG} = 1.5 A V_{BAT} = 3.7 V

Figure 10-8. System Load Transient Response

11 Power Supply Recommendations

In order to provide an output voltage on SYS, the battery charger requires a power supply between 4-V and 13.5-V input with at least 100-mA current rating connected to VBUS and a single-cell Li-Ion battery with battery voltage greater than V_{BAT_UVLOZ} connected to BAT. The source current rating needs to be at least 3-A in order for the buck converter of the charger to provide maximum output power to SYS.

12 Layout

12.1 Layout Guidelines

The switching node rise and fall times should be minimized for minimum switching loss. Proper layout of the components to minimize high frequency current path loop (see Figure 12-1) is important to prevent electrical and magnetic field radiation and high frequency resonant problems. Follow this specific order carefully to achieve the proper layout.

1. Place input capacitor as close as possible to PMID pin and GND pin connections and use shortest copper trace connection or GND plane. Add 1 nF small size (such as 0402 or 0201) decoupling cap for high frequency noise filter and EMI improvement.
2. Place inductor input pin to SW pin as close as possible. Minimize the copper area of this trace to lower electrical and magnetic field radiation but make the trace wide enough to carry the charging current. Do not use multiple layers in parallel for this connection. Minimize parasitic capacitance from this area to any other trace or plane.
3. Put output capacitor near to the inductor and the device. Ground connections need to be tied to the IC ground with a short copper trace connection or GND plane.
4. Route analog ground separately from power ground. Connect analog ground and connect power ground separately. Connect analog ground and power ground together using thermal pad as the single ground connection point. Or using a 0-Ω resistor to tie analog ground to power ground.
5. Use single ground connection to tie charger power ground to charger analog ground. Just beneath the device. Use ground copper pour but avoid power pins to reduce inductive and capacitive noise coupling.
6. Place decoupling capacitors next to the IC pins and make trace connection as short as possible.
7. It is critical that the exposed thermal pad on the backside of the device package be soldered to the PCB ground. Ensure that there are sufficient thermal vias directly under the IC, connecting to the ground plane on the other layers.
8. Ensure that the number and sizes of vias allow enough copper for a given current path.

See the *BQ25619 BMS025 Evaluation Module EVM User's Guide* for the recommended component placement with trace and via locations. For the VQFN information, refer to *Quad Flatpack No-Lead Logic Packages Application Report* and *QFN and SON PCB Attachment Application Report*.

12.2 Layout Example

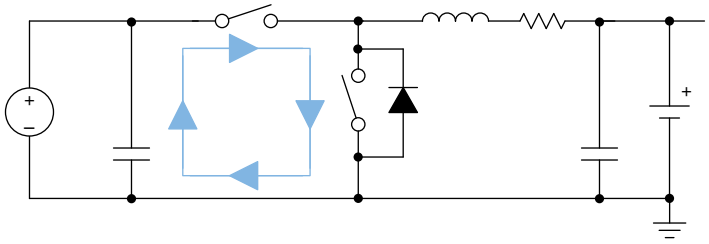


Figure 12-1. High Frequency Current Path

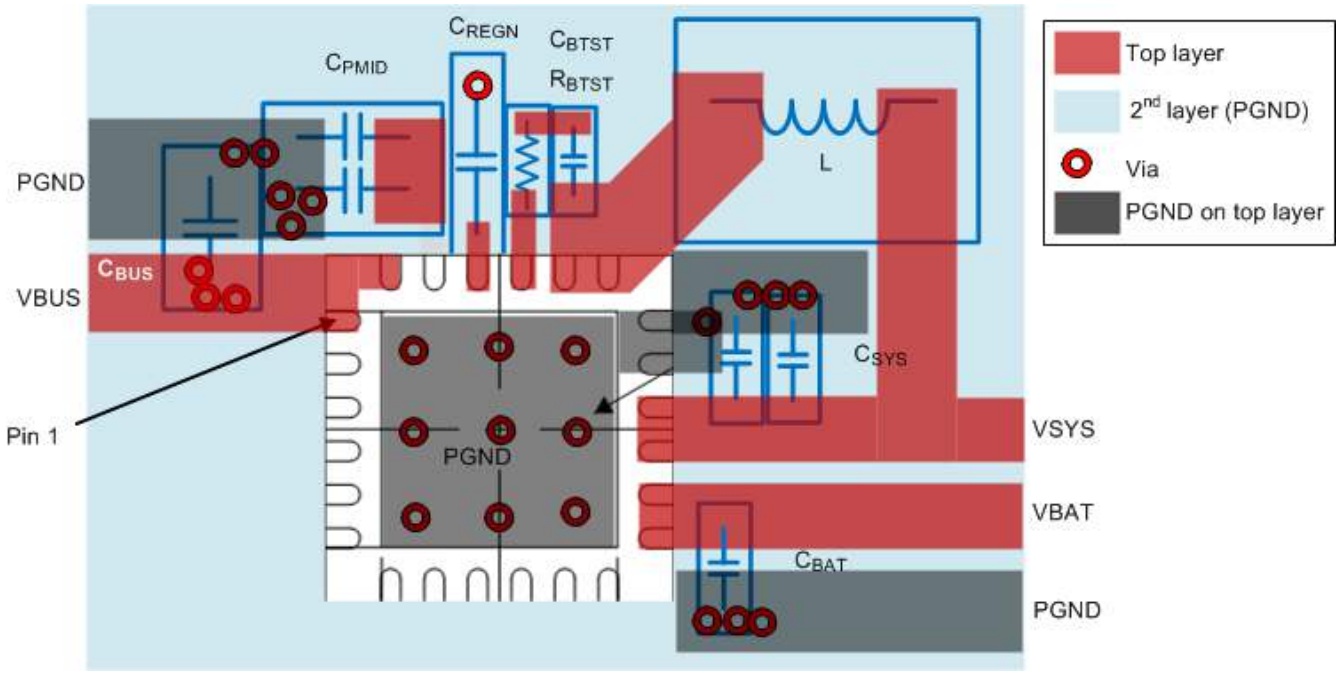


Figure 12-2. Layout Example

13 Device and Documentation Support

13.1 Device Support

13.2 Documentation Support

13.2.1 Related Documentation

For related documentation see the following:

- *BQ25619 BMS025 Evaluation Module User's Guide*

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
BQ25611DRTWR	ACTIVE	WQFN	RTW	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25611D	Samples
BQ25611DRTWT	ACTIVE	WQFN	RTW	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BQ 25611D	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

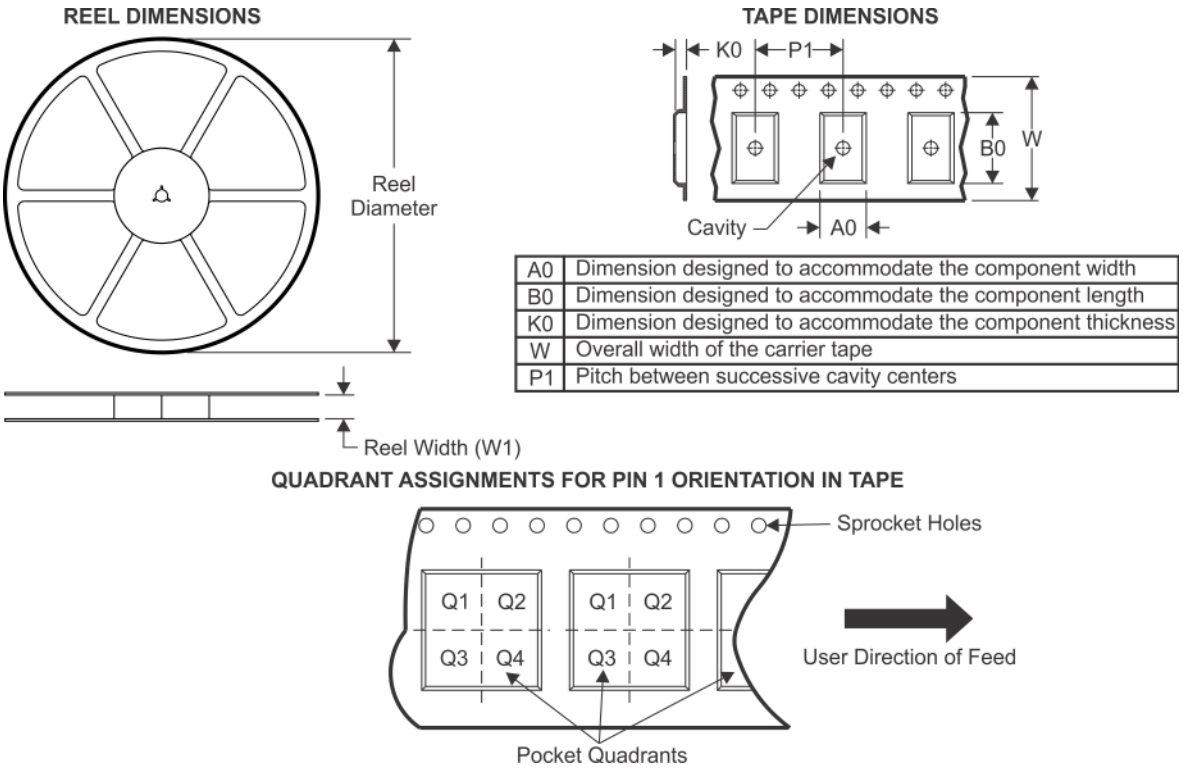
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

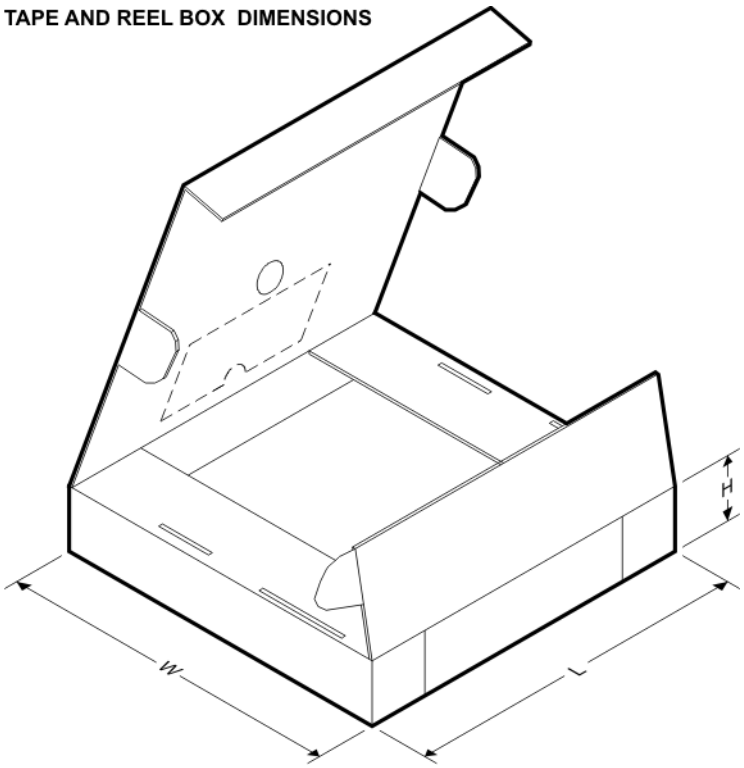


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
BQ25611DRTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2
BQ25611DRTWT	WQFN	RTW	24	250	180.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
BQ25611DRTWR	WQFN	RTW	24	3000	367.0	367.0	35.0
BQ25611DRTWT	WQFN	RTW	24	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

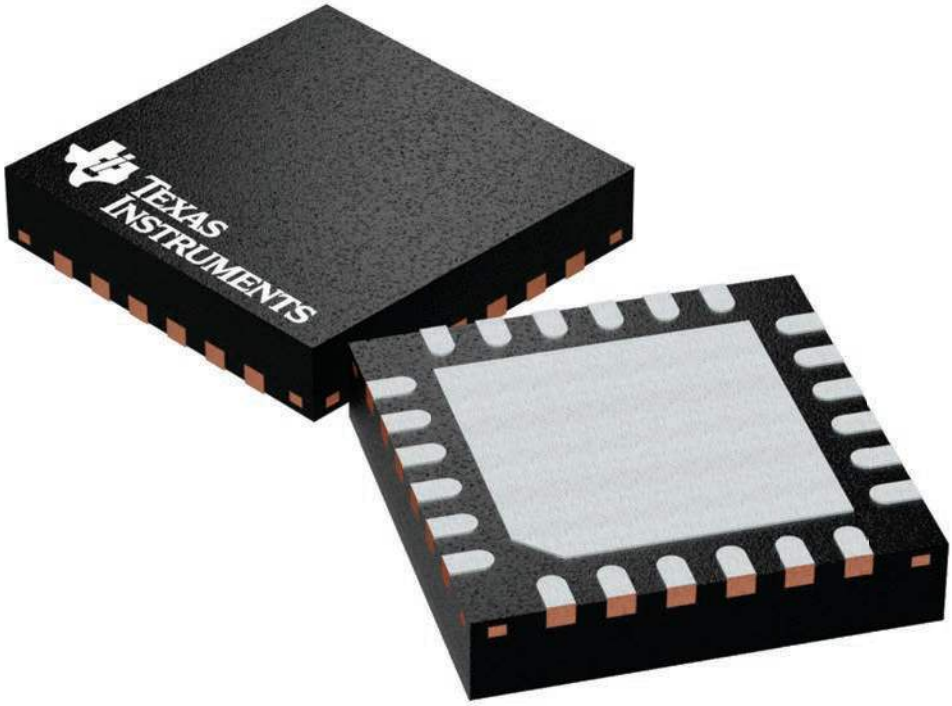
RTW 24

WQFN - 0.8 mm max height

4 x 4, 0.5 mm pitch

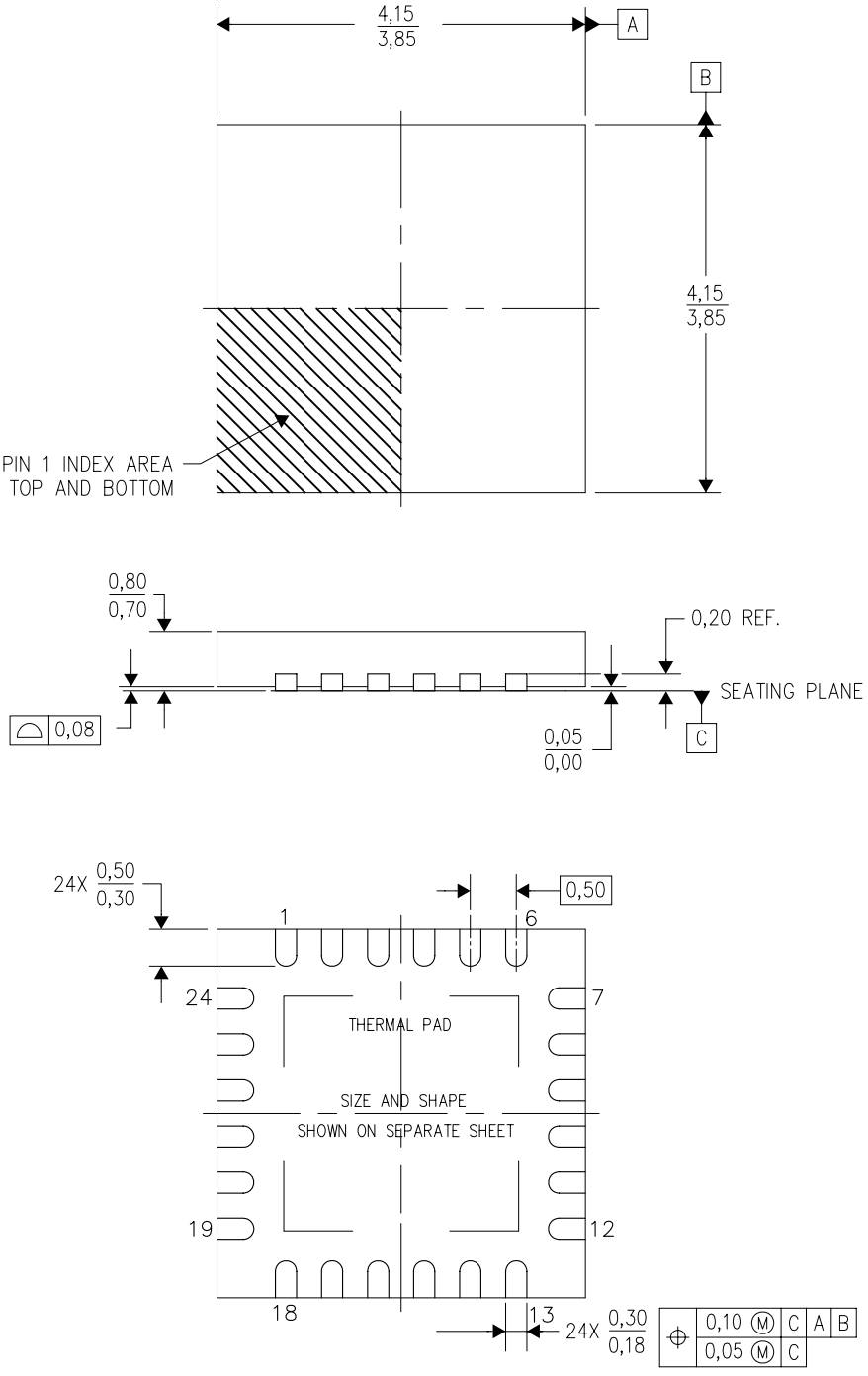
PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224801/A

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

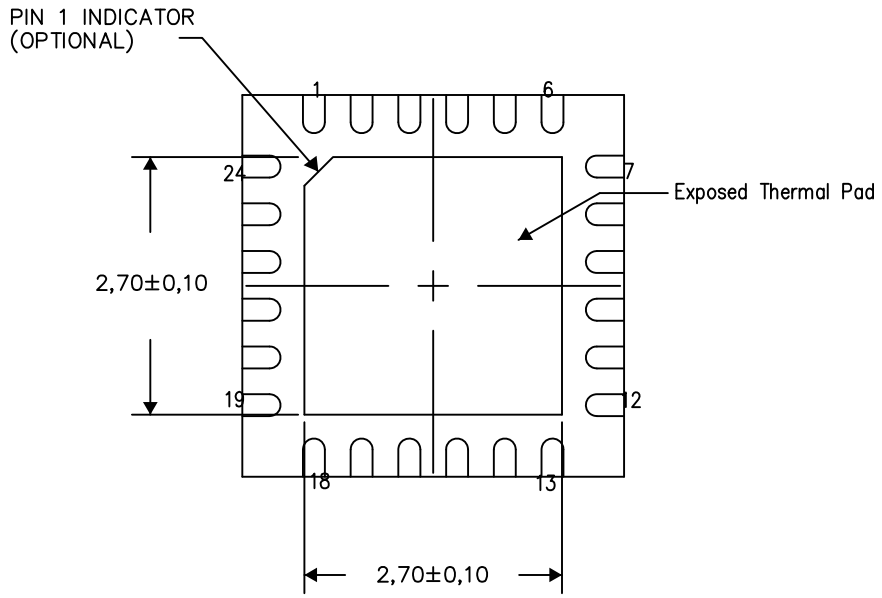
RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



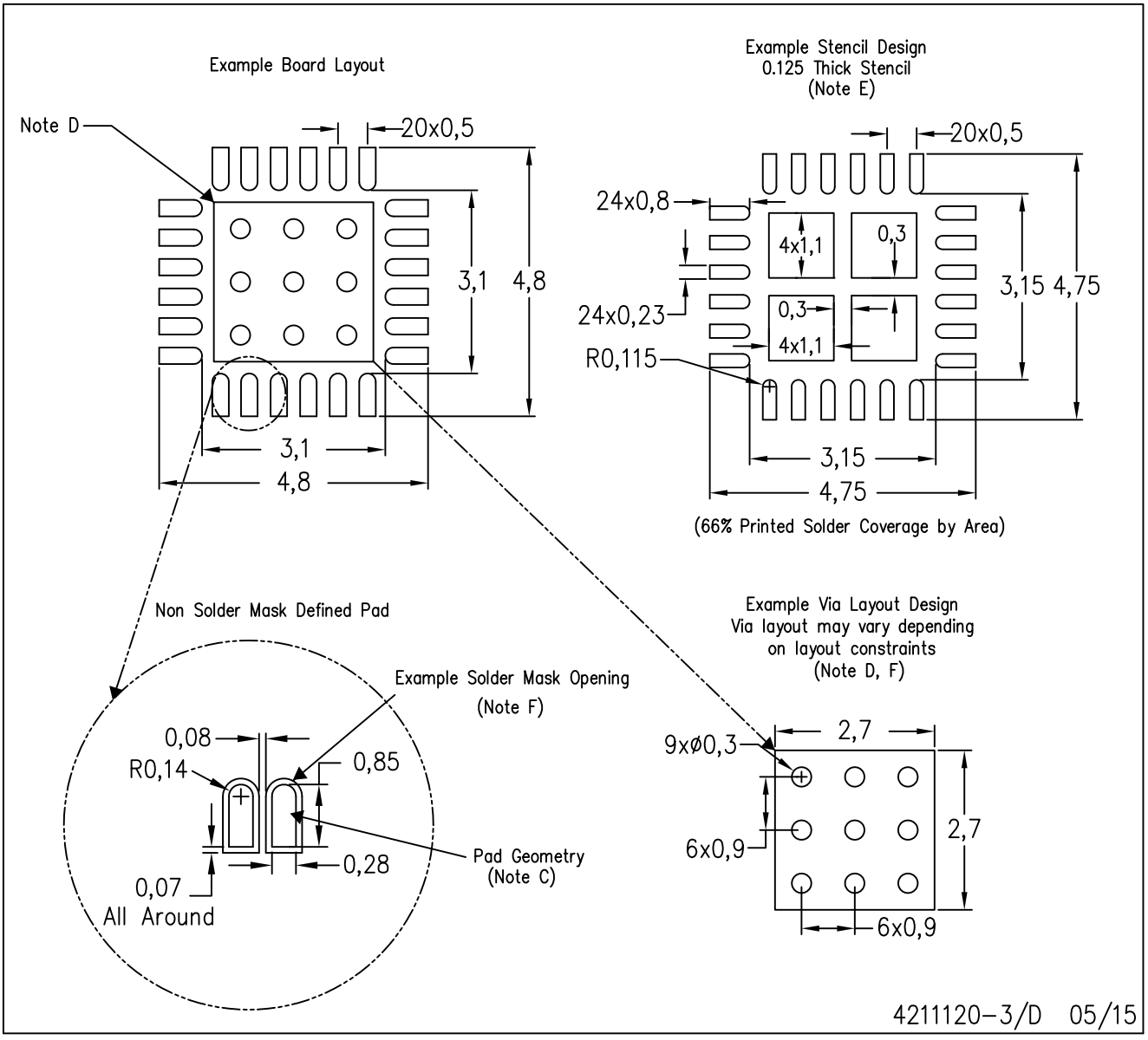
Bottom View

Exposed Thermal Pad Dimensions

4206249–5/P 05/15

NOTES: A. All linear dimensions are in millimeters

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265