

## N-Channel Power MOSFET

900V, 9.0A, 1.4Ω

### FEATURES

- 100% Avalanche Tested
- G-S ESD Protection Diode Embedded
- Pb-free plating
- Compliant to RoHS Directive 2011/65/EU and in accordance to WEE 2002/96/EC
- Halogen-free according to IEC 61249-2-21 definition

### APPLICATION

- Power Supply
- Lighting

KEY PERFORMANCE PARAMETERS		
PARAMETER	VALUE	UNIT
$V_{DS}$	900	V
$R_{DS(on)}$ (max)	1.4	Ω
$Q_g$	72	nC



ABSOLUTE MAXIMUM RATINGS (T <sub>A</sub> = 25°C unless otherwise noted)				
PARAMETER	SYMBOL	TO-220	ITO-220	UNIT
Drain-Source Voltage	$V_{DS}$	900		V
Gate-Source Voltage	$V_{GS}$	±30		V
Continuous Drain Current (Note 1)	$I_D$	T <sub>C</sub> = 25°C		A
		T <sub>C</sub> = 100°C		
Pulsed Drain Current (Note 2)	$I_{DM}$	36		A
Total Power Dissipation @ T <sub>C</sub> = 25°C	$P_{DTOT}$	290	89	W
Single Pulsed Avalanche Energy (Note 3)	$E_{AS}$	454		mJ
Single Pulsed Avalanche Current (Note 3)	$I_{AS}$	9		A
Operating Junction and Storage Temperature Range	T <sub>J</sub> , T <sub>STG</sub>	- 55 to +150		°C

THERMAL PERFORMANCE				
PARAMETER	SYMBOL	TO-220	ITO-220	UNIT
Junction to Case Thermal Resistance	$R_{\theta JC}$	0.43	1.4	°C/W
Junction to Ambient Thermal Resistance	$R_{\theta JA}$	62.5		°C/W

**Notes:**  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistances. The case thermal reference is defined at the solder mounting surface of the drain pins.  $R_{\theta JA}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.  $R_{\theta JA}$  shown below for single device operation on FR-4 PCB with minimum recommended footprint in still air.

**ELECTRICAL SPECIFICATIONS** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

PARAMETER	CONDITIONS	SYMBOL	MIN	TYP	MAX	UNIT
<b>Static</b> (Note 4)						
Drain-Source Breakdown Voltage	$V_{GS} = 0V, I_D = 250\mu A$	$BV_{DSS}$	900	--	--	V
Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	$V_{GS(TH)}$	2.0	--	4.0	V
Gate Body Leakage	$V_{GS} = \pm 30V, V_{DS} = 0V$	$I_{GSS}$	--	--	$\pm 100$	$\mu A$
Zero Gate Voltage Drain Current	$V_{DS} = 900V, V_{GS} = 0V$	$I_{DSS}$	--	--	10	$\mu A$
Drain-Source On-State Resistance	$V_{GS} = 10V, I_D = 4.5A$	$R_{DS(on)}$	--	1.13	1.4	$\Omega$
<b>Dynamic</b> (Note 5)						
Total Gate Charge	$V_{DS} = 720V, I_D = 9.0A,$ $V_{GS} = 10V$	$Q_g$	--	72	--	nC
Gate-Source Charge		$Q_{gs}$	--	11	--	
Gate-Drain Charge		$Q_{gd}$	--	31	--	
Input Capacitance	$V_{DS} = 25V, V_{GS} = 0V,$ $f = 1.0MHz$	$C_{iss}$	--	2470	--	pF
Output Capacitance		$C_{oss}$	--	192	--	
Reverse Transfer Capacitance		$C_{rss}$	--	27	--	
<b>Switching</b> (Note 6)						
Turn-On Delay Time	$V_{DD} = 450V,$ $R_{GEN} = 25\Omega,$ $I_D = 9.0A, V_{GS} = 10V,$	$t_{d(on)}$	--	52	--	ns
Turn-On Rise Time		$t_r$	--	97	--	
Turn-Off Delay Time		$t_{d(off)}$	--	212	--	
Turn-Off Fall Time		$t_f$	--	159	--	
<b>Source-Drain Diode</b> (Note 4)						
Forward On Voltage	$I_S = 9.0A, V_{GS} = 0V$	$V_{SD}$	--	--	1.5	V
Reverse Recovery Time	$V_{GS} = 0V, I_S = 9A,$ $di/dt = 100A/us$	$t_{fr}$	--	570	--	ns
Reverse Recovery Charge		$Q_{fr}$	--	6.6	--	$\mu C$

**Notes:**

1. Current limited by package
2. Pulse width limited by the maximum junction temperature
3.  $L = 10.6mH, I_{AS} = 9A, V_{DD} = 50V, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$   
100% Eas Test Condition:  $L = 10.6mH, I_{AS} = 4.5A, V_{DD} = 50V, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
4. Pulse test:  $PW \leq 300\mu s$ , duty cycle  $\leq 2\%$
5. For DESIGN AID ONLY, not subject to production testing.
6. Switching time is essentially independent of operating temperature.

**ORDERING INFORMATION**

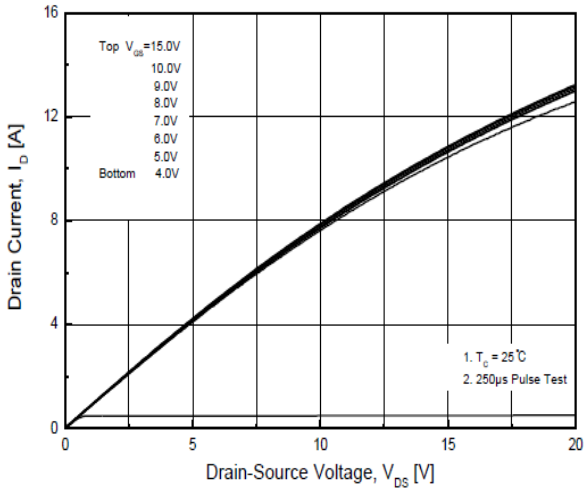
<b>PART NO.</b>	<b>PACKAGE</b>	<b>PACKING</b>
TSM9N90ECZ C0G	TO-220	50pcs / Tube
TSM9N90ECI C0G	ITO-220	50pcs / Tube

**Not Recommended**

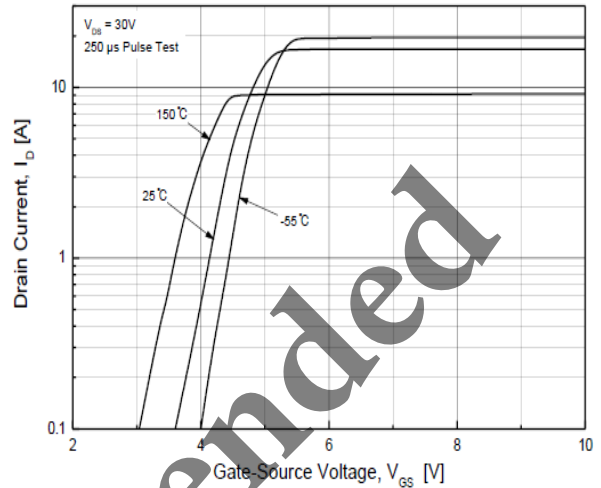
**CHARACTERISTICS CURVES**

( $T_C = 25^\circ\text{C}$  unless otherwise noted)

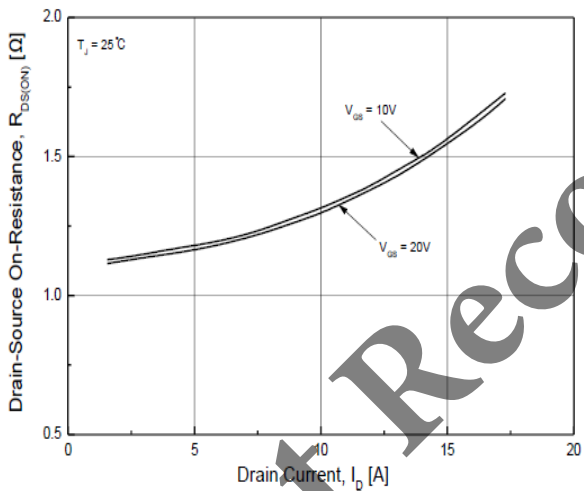
**Output Characteristics**



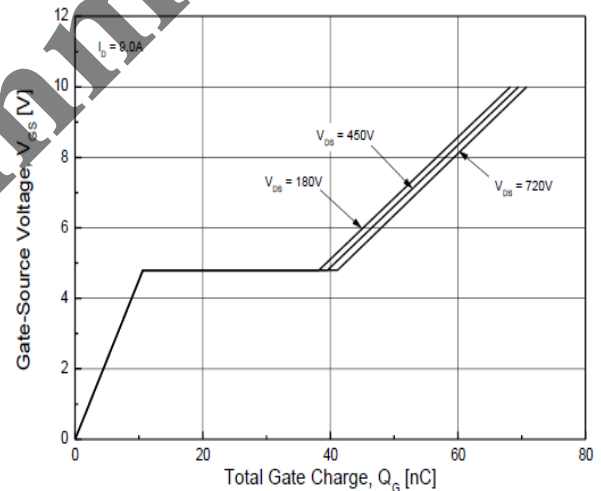
**Transfer Characteristics**



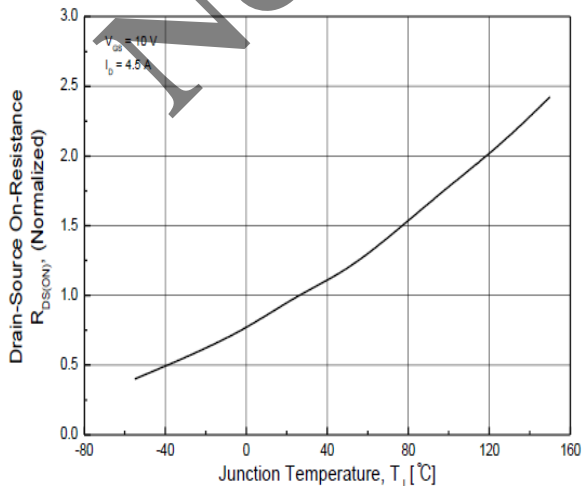
**On-Resistance vs. Drain Current**



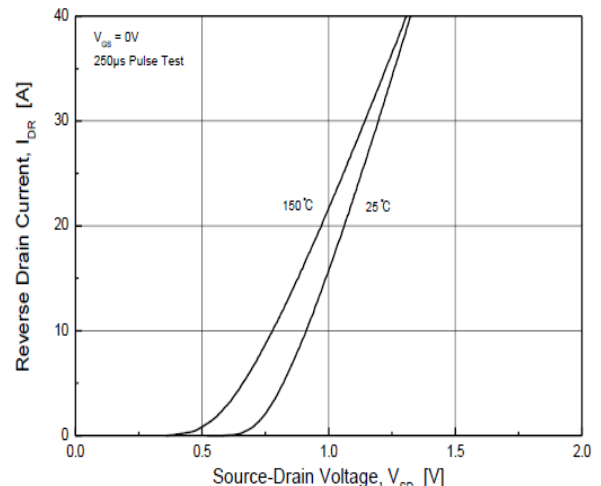
**Gate Charge**



**On-Resistance vs. Junction Temperature**



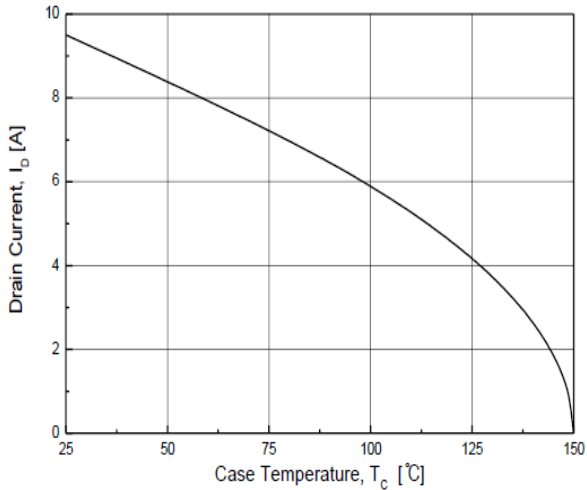
**Source-Drain Diode Forward Voltage**



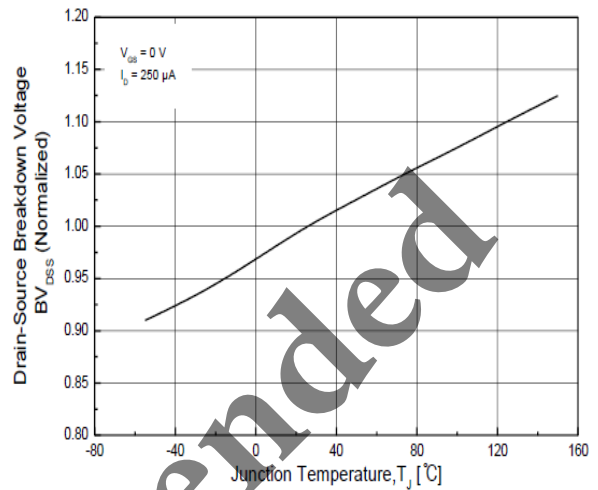
**CHARACTERISTICS CURVES**

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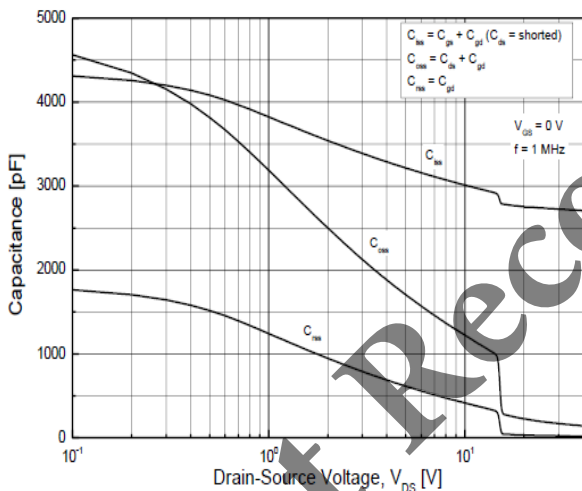
**Drain Current vs. Case Temperature**



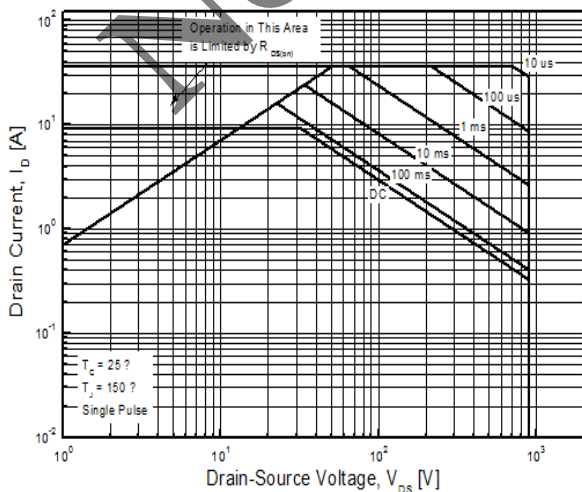
**$BV_{DSS}$  vs. Junction Temperature**



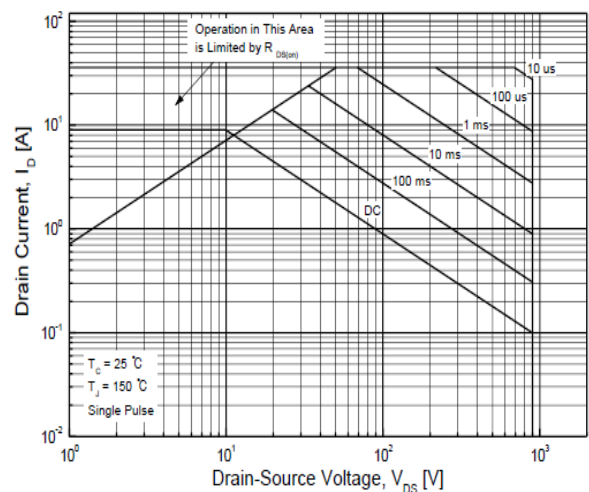
**Capacitance vs. Drain-Source Voltage**



**Maximum Safe Operating Area (TO-220)**



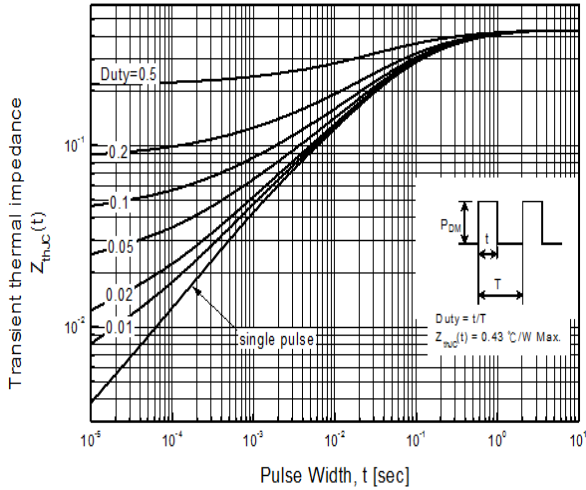
**Maximum Safe Operating Area (ITO-220)**



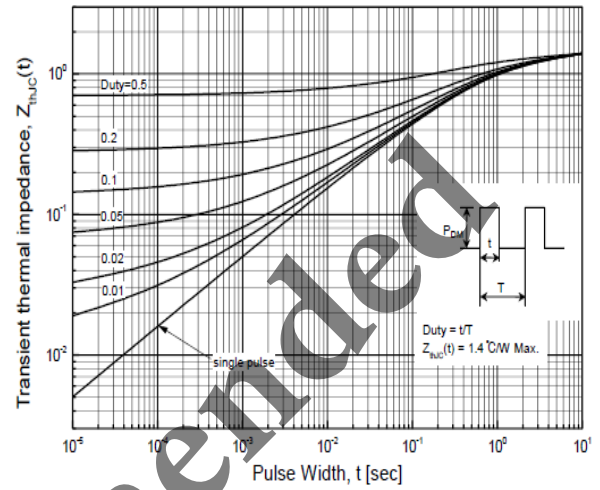
**ELECTRICAL CHARACTERISTICS CURVES**

( $T_C = 25^\circ\text{C}$  unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient (TO-220)**

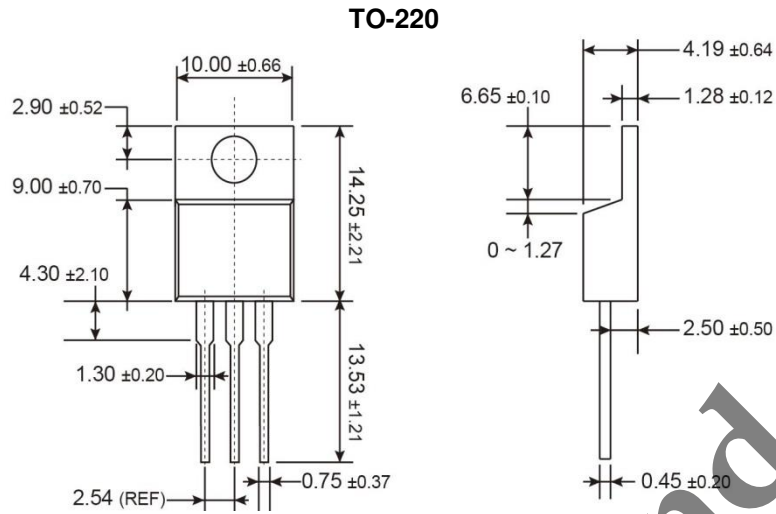


**Normalized Thermal Transient Impedance, Junction-to-Ambient (ITO-220)**



Not Recommended

**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)



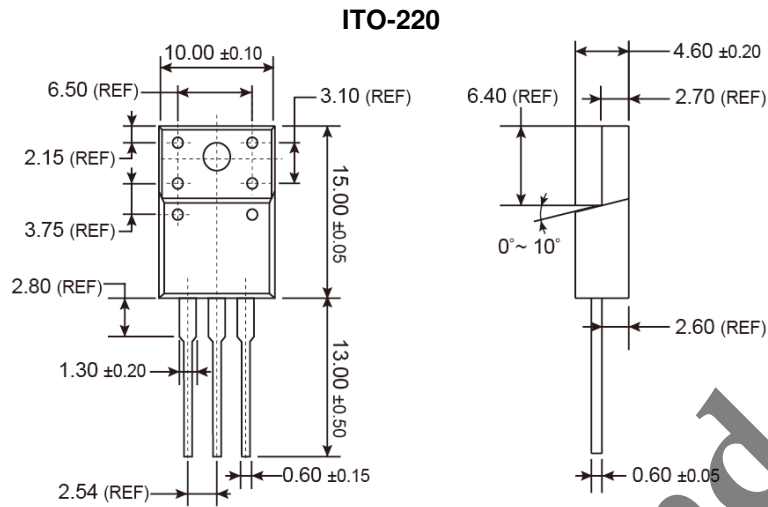
**MARKING DIAGRAM**



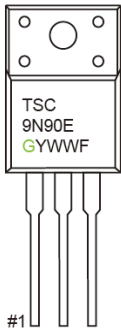
- G** = Halogen Free
- Y** = Year Code
- WW** = Week Code (01~52)
- F** = Factory Code

Not Recommended

**PACKAGE OUTLINE DIMENSIONS** (Unit: Millimeters)



**MARKING DIAGRAM**



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Not Recommended



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