ADSANTEC
Ultra High-Speed Mixed Signal ASICs

Advanced Science And Novel Technology Company, Inc.
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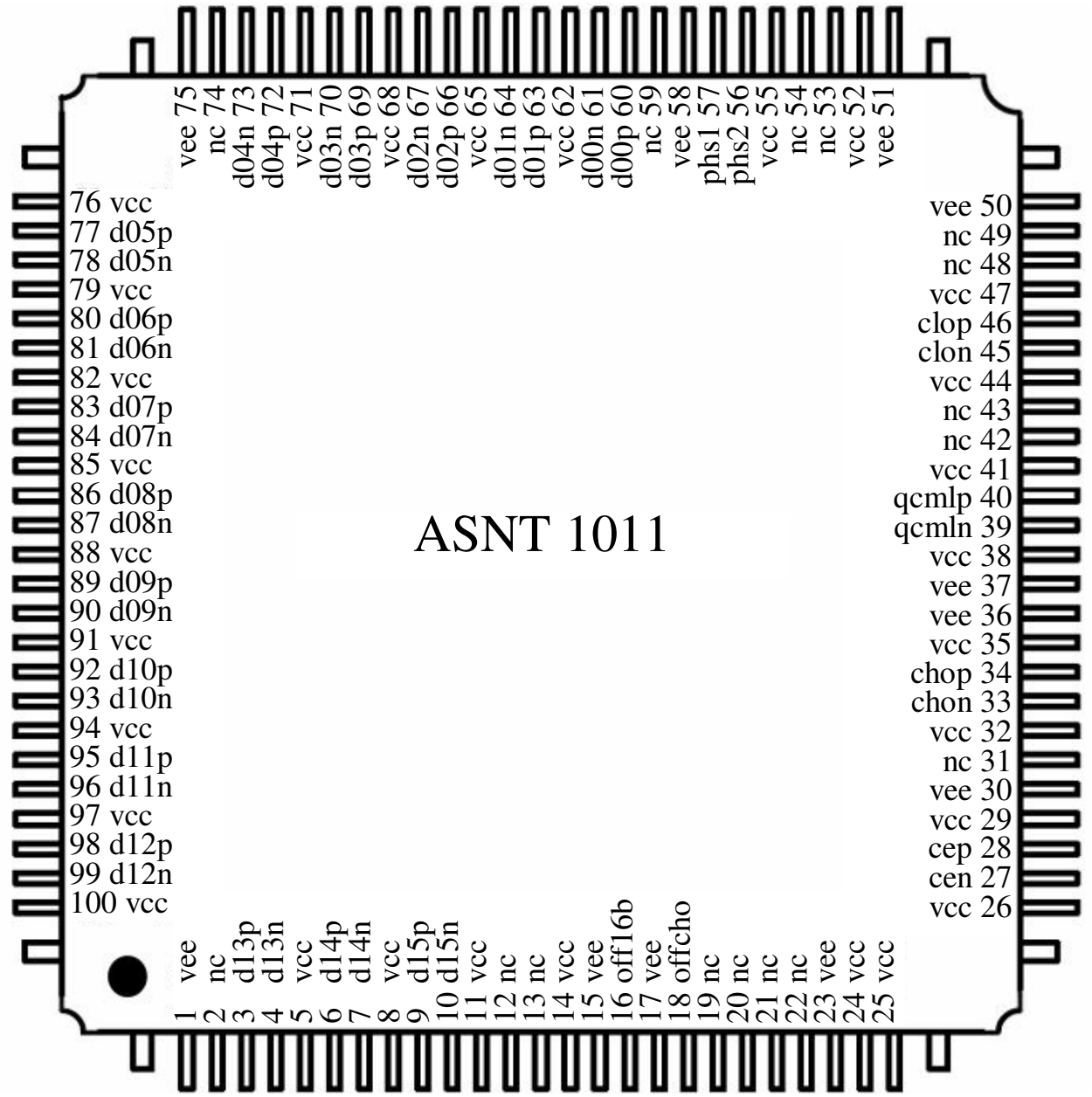
ASNT1011-KMA
DC-to-17*Gbps* Digital Multiplexer / Serializer 16:1or 8:1

- Broadband programmable digital serializer 16-to-1 or 8-to-1
- LVDS compliant input data buffers
- Full-rate clock output
- Selectable LVDS-compliant divided output clock with optional 90°-step phase adjustment
- Single +3.3*V* power supply
- Industrial temperature range
- Low power consumption of 660*mW* at the maximum speed
- Custom 100-pin CQFP package (13*mm* x 13*mm*)



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DESCRIPTION

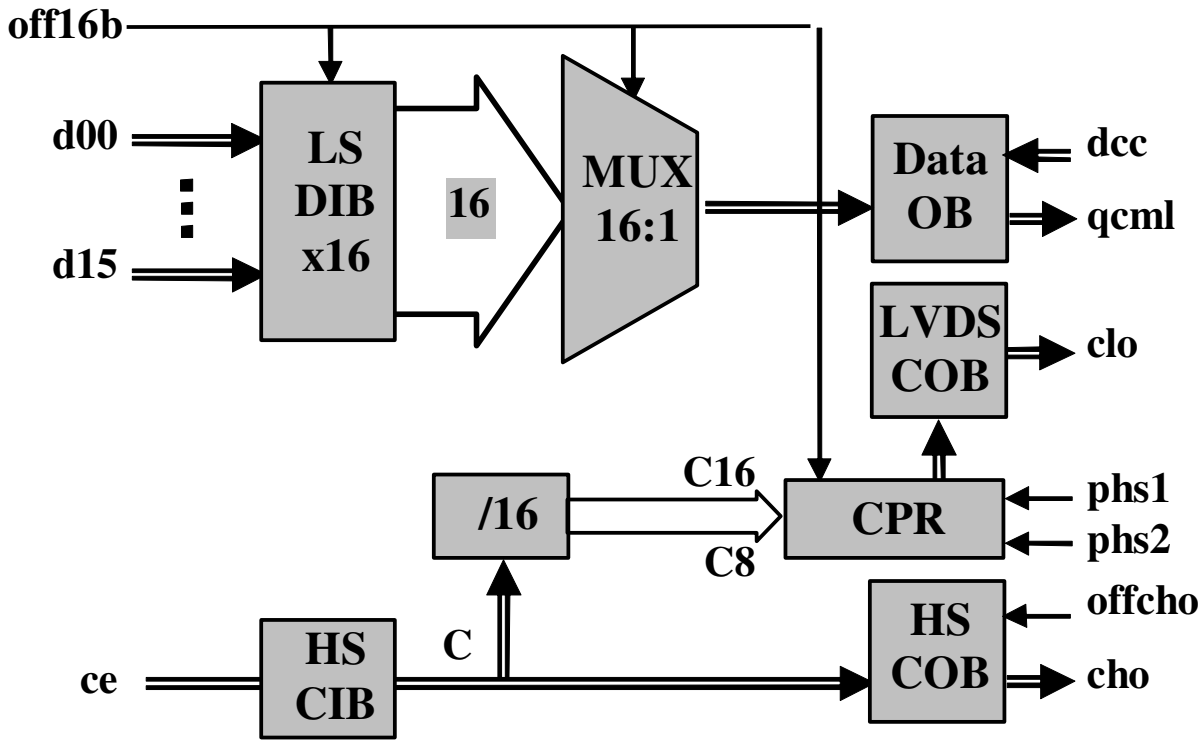

Fig. 1. Functional Block Diagram

ASNT1011-KMA is a low power and high-speed programmable multiplexer (MUX) 16-to-1 (16:1) or 8-to-1 (8:1) IC. The IC shown in Fig. 1 functions seamlessly over data rates (f_{bit}) ranging from DC to maximum.

The main function of the chip shown in Fig. 1 is to multiplex/serialize M input parallel data channels running at a bit rate of f_{bit}/M into a high-speed serial bit stream running at f_{bit}. The value of M is selected by the control signal off16b. It provides a high-speed output data channel for point-to-point data transmission over a controlled impedance media of 50*Ohm*. The transmission media can be a printed circuit board or copper coaxial cables. The functional distance of the data transfer is dependent upon the attenuation characteristics of the transportation media and the degree of noise coupling to the signaling environment.

During normal operation with M=16 (off16b ="0"), the serializer's low-speed input buffer (LS DIBx16) accepts external 16-bit wide parallel data words d00p/d00n-d15p/d15n through 16 differential LVDS inputs and delivers them to the multiplexer's core (MUX16:1) for serialization. A full rate clock must be provided by an external source cep/cen to the high-speed clock input buffer (HS CIB) where it is routed to the high speed clock output buffer (HS COB) and the internal divider-by-16 (/16). The divider provides signaling for MUX16:1 and produces a clock divided-by-16 (C16) for the low speed LVDS compliant clock output buffer (LVDS COB).The phase of clop/clon can be modified by 90° increments by utilizing pins phs1 and phs2 and the clock processing block (CPR).

During normal operation with M=8 (off16b ="1"), the part operates in a similar way but the serializer's low-speed input buffer (LS DIBx16) accepts only l 8-bit wide parallel data words d00p/d00n-d07p/d07n through

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the first eight differential LVDS inputs. In this mode, the divider (/16) also generates a clock divided-by-8 (C8) that is delivered to LVDS COB. The phs1 and phs2 controls are disabled in this operational mode.

The serialized words are transmitted as 2-level signals qcmlp/qcmln by a differential CML output buffer (Data OB). A full-rate clock is transmitted by HS COB in parallel with the high-speed data. The clock and data outputs are well phase matched to each other resulting in very little relative skew over the operating temperature range of the device. Both output stages are back terminated with on-chip 50*Ohm* resistors.

The serializer uses a single +3.3*V* power supply and is characterized for operation from −25°*C* to 125°*C* of junction temperature.

LS DIBx16

The Low-Speed Data Input Buffer (LS DIBx16) consists of 16 proprietary universal input buffers (UIBs) that exceed the LVDS standards IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995. UIB is designed to accept differential signals with amplitudes above 60*mV* peak-to-peak (p-p), DC common mode voltage variation between the negative vee and positive vcc supply rails, and AC common mode noise with a frequency up to 5*MHz* and voltage levels ranging from 0 to 2.4*V*. It can also receive single-ended signals with amplitudes above 60*mV*p-p and threshold voltages between vee and vcc. The input termination impedance is set to 100*Ohm* differential.

HS CIB

The High-Speed Clock Input Buffer (HS CIB) can accept high-speed clock signals at its differential CML input port cep/cen. It can also accept a single-ended signal with a threshold voltage applied to the unused pin. HS CIB can handle a wide range of input signal amplitudes. The buffer utilizes on-chip single-ended termination of 50*Ohm* to vcc for each input line.

/16

The Divider-by-16 (/16) includes 4 divide-by-2 circuits connected in series. The high-speed clock C is fed into the first divide-by-2 circuit that generates half rate clock C2. C2 is routed internally to the next divide-by-two circuit and outside of the block to MUX16:1. Other divided down clock signals are formed and routed to MUX16:1 in similar fashion. C16 and/or C8 are passed on to LVDS COB to become the output low speed clock signal clop/clon.

MUX16:1

The 16-to-1 Multiplexer (MUX16:1) utilizes a tree type architecture that latches the incoming data on the negative edge of the C16 clock signal that is supplied by /16. The 16-bit wide data word is subsequently multiplexed and delivered to Data OB as a single serial data stream running at a data rate up to specified maximum. The latency of this circuit block is equal to roughly one period of C16 or C8 depending on the mode of operation. The input MSB corresponds to d00p/d00n.

Data OB

The Data Output Buffer (Data OB) receives high-speed serial data from MUX16:1 and converts it into differential CML output signal qcmlp/qcmln. The buffer requires 50*Ohm* external termination resistors connected between vcc and each output to match its internal 50*Ohm* resistors.

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HS COB

The High Speed Clock Output Buffer (HS COB) utilizes the same termination scheme as Data OB. The buffer can be enabled or disabled by the external 2-state control signal offcho. The logic "0" state provides a full-rate clock output signal while the logic "1" state disables the buffer completely to save power.

CLK Proc

By utilizing the CMOS control pins phs1 and phs2 in the 16-bit operational mode, the phase of clop/clon can be altered in accordance with Table 1.

Table 1. Output Clock Phase Selection

phs1	phs2	C16 phase
vee (default)	vee (default)	270°
vee	vcc	180°
vcc	vee	90°
vcc	vcc	0°

LVDS COB

The LVDS Clock Output Buffer (LVDS COB) receives C16 or C8 and converts it into an LVDS output signal clop/clon. The proprietary low-power LVDS output buffer utilizes a special architecture that ensures operation at frequencies up to 2.0*GHz* with a nominal output current of 3.5*mA*. The buffer satisfies all the requirements of the IEEE Std. 1596.3-1996 and ANSI/TIA/EIA-644-1995.

Output Timing

The phase relation between the output data qcmlp/qcmln and the full rate output clock chop/chon is specified in Table 2 and illustrated by Fig. 2.

Table 2. Output Data-to-Clock Phase Difference

Junction temperature, *°C*	τ,*ps*	
	Min.	Max.
-25	77	80
50	82	86
125	87	91

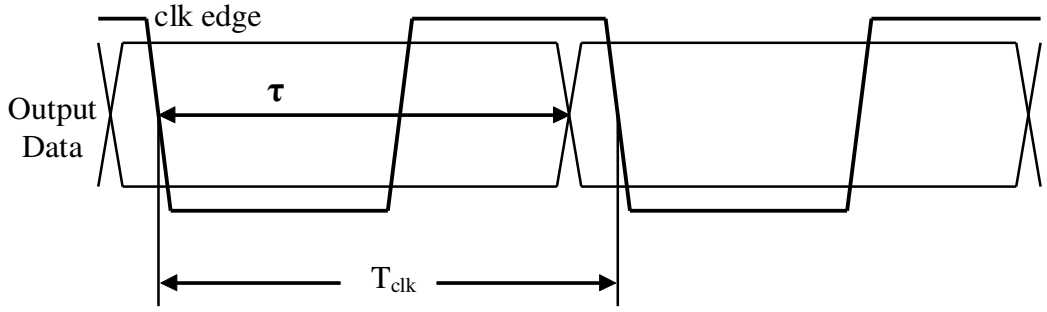

Fig. 2. Output Timing Diagram

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ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 3 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vee).

Table 3. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vcc)		+3.6	*V*
Power Consumption		0.72	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*°C*
Storage Temperature	-40	+100	*°C*
Operational Humidity	10	98	%
Storage Humidity	10	98	%

TERMINAL FUNCTIONS

Supply And Termination Voltages		
Name	**Description**	**Pin Number**
vcc	Positive power supply (+3.3*V*)	5, 8, 11, 14, 24, 25, 26, 29, 32, 35, 38, 41, 44, 47, 52, 55, 62, 65, 68, 71, 76, 79, 82, 85, 88, 91, 94, 97, 100
vee	Negative power supply (GND or 0*V*)	1, 15, 17, 23, 30, 36, 37, 50, 51, 58, 75
nc	Not connected pins	2, 12, 13, 19, 20, 21, 22, 31, 42, 43, 48, 49, 53, 54, 59, 74

TERMINAL			DESCRIPTION
Name	**No.**	**Type**	
High-Speed I/Os			
cep	28	Input	CML differential external clock inputs with internal SE 50*Ohm* termination to vcc
cen	27		
chop	34	Output	CML differential clock outputs. Require external SE 50*Ohm* termination to vcc
chon	33		
qcmlp	40	Output	CML differential data outputs. Require external SE 50*Ohm* termination to vcc
qcmln	39		
Controls			
phs1	57	LS In., CMOS	Low-speed output clock phase selection (default: both low)
phs2	56		
off16b	16		Multiplexation coefficient M control (active: high, M=8; default: low, M=16)
offcho	18		HS COB control (active: high, buffer is disabled; default: low, full-rate output clock)

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TERMINAL			DESCRIPTION
Name	No.	Type	
Low-Speed I/Os			
clop	46	Output	LVDS clock outputs. Can transmit four different clock phases as defined by phs1 and phs2
clon	45		
d00p	60	Input	LVDS data inputs
d00n	61		
d01p	63		
d01n	64		
d02p	66		
d02n	67		
d03p	69		
d03n	70		
d04p	72		
d04n	73		
d05p	77		
d05n	78		
d06p	80		
d06n	81		
d07p	83		
d07n	84		
d08p	86		
d08n	87		
d09p	89		
d09n	90		
d10p	92		
d10n	93		
d11p	95		
d11n	96		
d12p	98		
d12n	99		
d13p	3		
d13n	4		
d14p	6		
d14n	7		
d15p	9		
d15n	10		

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ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vcc	+3.14	+3.3	+3.47	*V*	±5%
vee		0.0		*V*	External ground
Ivcc		200		*mA*	
Power consumption		660		*mW*	
Junction temperature	-25	50	125	*°C*	
LS Input Data (d00p/d00n-d15p/d15n)					
Data Rate	0.0	937.5	1063	*Mbps*	
Differential Swing	0.06		0.8	*V*	Peak-to-peak
CM Voltage Level	vee		vcc	*V*	
HS Input Clock (cep/cen)					
Frequency	0.0	15	17	*GHz*	
Swing (Diff or SE)	0.2		1.2	*V*	Peak-to-peak
CM Voltage Level	vcc -0.8		vcc	*V*	
Duty Cycle	40%	50%	60%		
HS Output Data (qcmlp/qcmln)					
Data Rate	0.0	15	17	*Gbps*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc -0.6		*V*	
Jitter		12		*ps*	Peak-to-peak @12.5*Gb/s*
HS Output Clock (chop/chon)					
Frequency	0.0	15	17	*GHz*	
Logic “1” level		vcc		*V*	
Logic “0” level		vcc -0.6		*V*	
Jitter		6		*ps*	Peak-to-peak @12.5*GHz*
Duty Cycle		50%			
LS Output Clock (clop/clon)					
Frequency	0.0	937.5	1063	*MHz*	
Interface		LVDS			Meets the IEEE Std.
CMOS Control Inputs					
Logic “1” level	vcc -0.4			*V*	
Logic “0” level			vee +0.4	*V*	

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PACKAGE INFORMATION

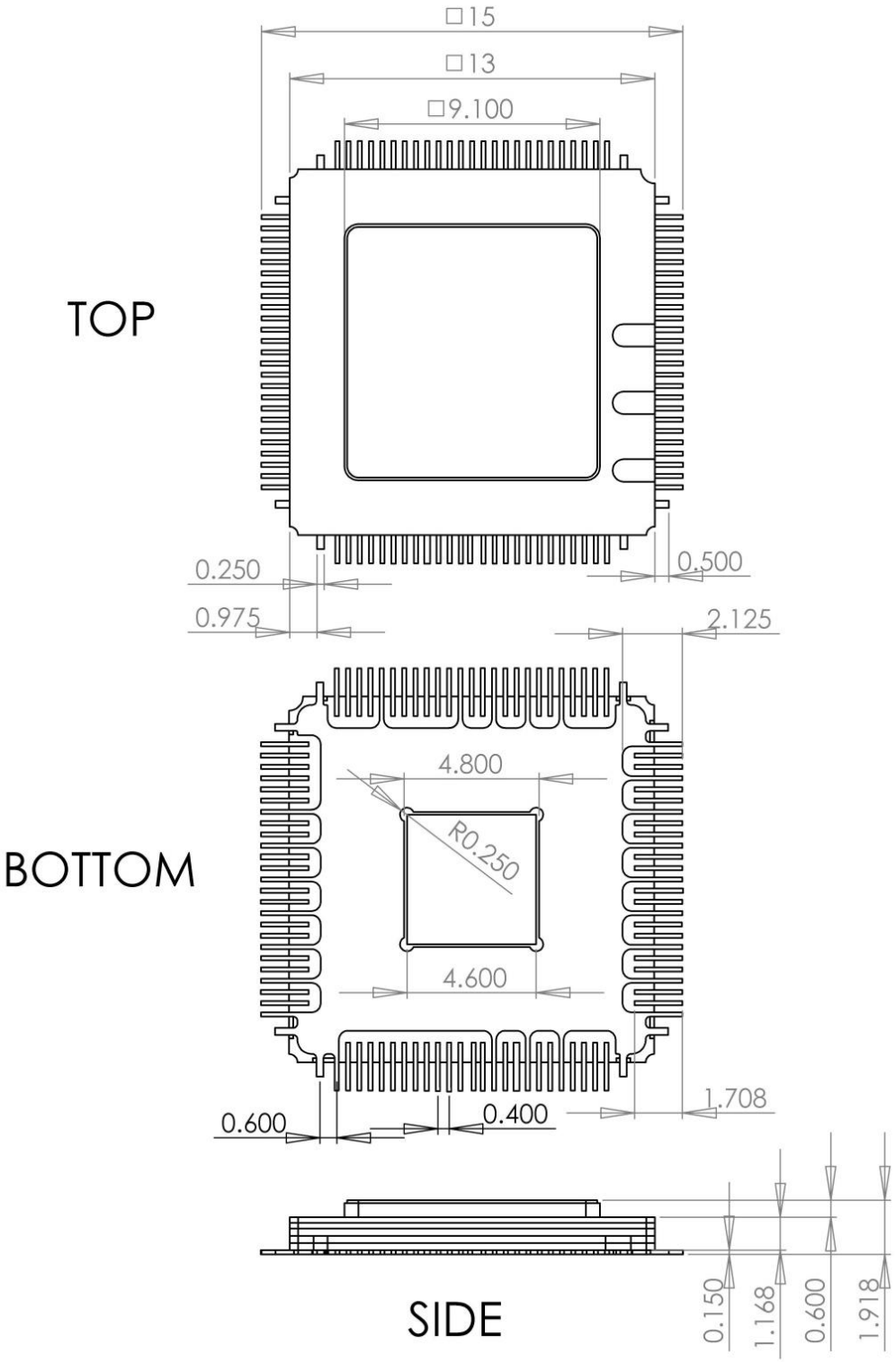

Fig. 3. Package Drawing

The chip die is housed in a custom 100-pin CQFP package shown in Fig. 3. The package's leads will be trimmed to a length of 1.0mm. After trimming, the package's leads will be further processed as follows:

1. The lead's gold plating will be removed per the following sections of J-STD-001D:
   - 3.9.1 Solderability
   - 3.2.2 Solder Purity Maintenance
   - 3.9.2 Solderability Maintenance
   - 3.9.3 Gold Removal
2. The leads will be tinned with Sn63Pb37 solder

Even though the package provides a center heat slug located on the back side of the package to be used for heat dissipation, ADSANTEC does **NOT** recommend for this section to be soldered to the board. If the customer wishes to solder it, it should be connected to the vcc plain that is ground for the negative supply or power for the positive supply.

The part's identification label is ASNT1011-KMA. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

REVISION HISTORY

Revision	Date	Changes
3.3.2	01-2020	Updated Package Information
3.2.2	07-2019	Updated Letterhead
3.2.1	08-2018	Corrected recommendations for heat slug handling
3.1.1	08-2018	Corrected title Corrected Pin Diagram (pin 16 is off16b) Added description of the 8-bit mode Corrected Terminal Functions table Corrected Package Information section
2.3.1	07-2016	Revised Terminal Functions section
2.2.1	05-2015	Corrected Absolute Maximum Ratings section Revised Package Information section Updated format
2.1	06-2012	Corrected package dimensions
2.0	01-2012	Revised Electrical Characteristics section Revised Package Information section Added Absolute Maximums Rating table Added Pin Diagram
1.0	01-2011	First release