10-Bit, 400 MSPS D/A Converters

AD9720/AD9721

FEATURES
400 MSPS (ECL)/100 MSPS (TTL) Update Rate
Low Glitch Impulse: 1.5 pV-s
Fast Settling: 4.5 ns to 1/2 LSB
Low Power: 1.1 W
On-Board Quadrature Logic for DDS Applications
Differential Clock (ECL)

APPLICATIONS
Direct Digital Synthesis
Arbitrary Waveform Synthesis
Waveform Reconstruction
High Speed Imaging

GENERAL DESCRIPTION

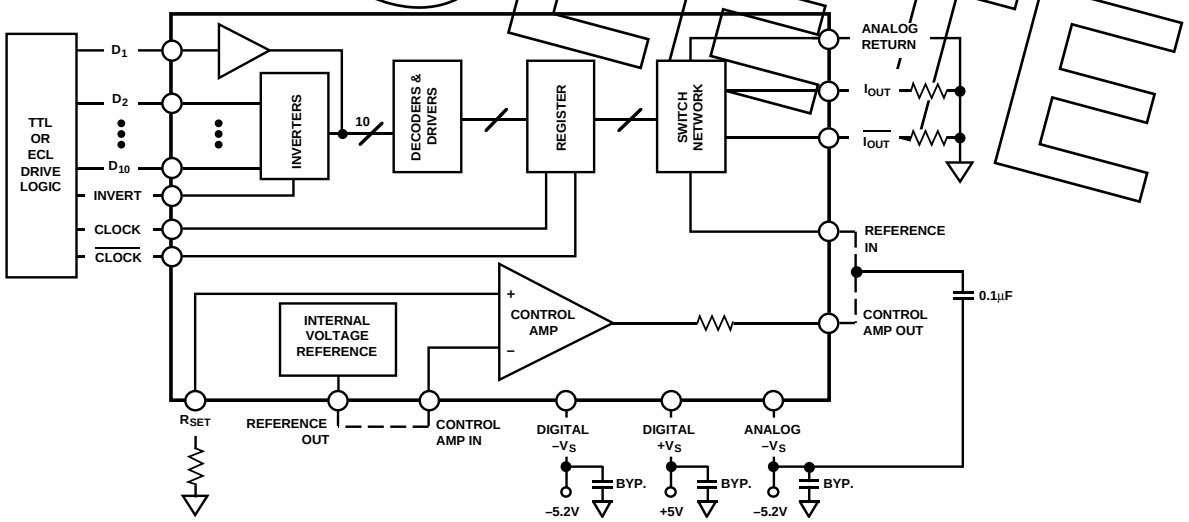
The AD9720 and AD9721 D/A converters are 10-bit, high speed digital-to-analog converters constructed in an oxide isolated bipolar process. The AD9720 is ECL compatible, and will update up to 400 MSPS; the AD9721 is TTL compatible and will update up to 100 MSPS.

Designed for direct digital synthesis (DDS), waveform reconstruction, and high resolution video applications, both devices feature low glitch impulse of 1.5 pV-s and fast settling times of 4.5 ns to 1/2 LSB.

Both converters are characterized for dynamic performance, and have excellent harmonic suppression and spectral purity in waveform generation applications.

The units are available in 28-pin DIPs, LCCs and SOICs. Industrial temperature range devices are packaged in plastic for operation from –25°C to +25°C; extended temperature range devices for operation from –55°C to +125°C are in hermetic ceramic packages. Contact the factory for information about the availability of MIL-STD-883 devices.

FUNCTIONAL BLOCK DIAGRAM



REV. A

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AD9720/AD9721–SPECIFICATIONS

ELECTRICAL CHARACTERISTICS

($-V_S$ = −5.2 V; $+V_S$ = +5 V (AD9721 only); Reference Voltage = −1.25 V; R_{SET} = 1,960 Ω, unless otherwise noted)

Parameter (Conditions)	Temp	Test Level	AD9720BN/BR Min	AD9720BN/BR Typ	AD9720BN/BR Max	AD9720TE/TQ Min	AD9720TE/TQ Typ	AD9720TE/TQ Max	AD9721BN/BR Min	AD9721BN/BR Typ	AD9721BN/BR Max	AD9721TE/TQ Min	AD9721TE/TQ Typ	AD9721TE/TQ Max	Units
RESOLUTION				10			10			10			10		Bits
DC ACCURACY															
Differential Nonlinearity	+25°C	I		0.25	0 75		0.6	1.0		0.25	0.75		0.6	1.0	LSB
	Full	VI			1.0			1.5			1.0			1.5	LSB
Integral Nonlinearity	+25°C	I		0.5	1.0		0.7	1.5		0.5	1.0		0.7	1.5	LSB
("Best Fit" Straight Line)	Full	VI			1.5			2.0			1.5			2.0	LSB
INITIAL OFFSET ERROR															
Zero-Scale Offset Error	+25°C	I		16	60		16	60		16	60		16	60	µA
	Full	VI		20	75		20	75		20	75		20	75	µA
Full-Scale Gain Error[1]	+25°C	I		2	15		2	15		2	15		2	15	%
	Full	VI			15			15			15			15	%
Offset Drift Coefficient	+25°C	V		0.04			0.04			0.04			0.04		µA/°C
REFERENCE/CONTROL AMP															
Internal Reference Voltage	+25°C	I	–1.15	–1.25	–1.35	–1.15	–1.25	–1.35	–1.15	–1.25	–1.35	–1.15	–1.25	–1.35	V
	Full	VI	–1.15		–1.35	–1.15		–1.35	–1.15		–1.35	–1.15		–1.35	V
Internal Reference Voltage Drift	Full	V		100			100			100			100		µV/°C
Internal Reference Output Current	Full	IV	–50		+500	–50		+500	–50		+500	–50		+500	µA
Amplifier Input Impedance	+25°C	V		50			50			50			50		kΩ
Amplifier Bandwidth	+25°C	V		1			1			1			1		MHz
REFERENCE INPUT[2]															
Reference Input Impedance	+25°C	V		4.6			4.6			4.6			4.6		kΩ
Reference Multiplying Bandwidth[3]	+25°C	V		75			75			75			75		MHz
OUTPUT PERFORMANCE															
Full-Scale Output Current[2, 4]	+25°C	V		20.48			20.48			20.48			20.48		mA
Output Compliance Range	+25°C	IV	–1.5		+3	–1.5		+3	–1.5		+3	–1.5		+3	V
Output Resistance	+25°C	V		210			210			210			210		Ω
Output Capacitance	+25°C	V		6			6			6			6		pF
Output Update Rate	+25°C	V		400			400			100			100		MSPS
Voltage Settling Time (1/2 LSB)[5]	+25°C	V		4.5			4.5			4.5			4.5		ns
Propagation Delay (t_{PD})[6]	+25°C	V		4.0			4.0			4.5			4.5		ns
Glitch Impulse[7]	+25°C	V		1.5			1.5			1.5			1.5		pV s
Output Slew Rate[8]	+25°C	V		1,000			1,000			1,000			1,000		V/µs
Output Rise Time[8]	+25°C	V		675			675			675			675		ps
Output Fall Time[8]	+25°C	V		470			470			470			470		ps
DIGITAL INPUTS															
Logic "1" Voltage	Full	VI	–1.0			–0.9			2.0			2.0			V
Logic "0" Voltage	Full	VI			–1.5			–1.6			0.8			0.8	V
Logic "1" Current	Full	VI			50			50			400			400	µA
Logic "0" Current	Full	VI			2			2			700			700	µA
Input Capacitance	+25°C	V		3			3			3			3		pF
Input Setup Time (t_S)[9]	+25°C	IV	1.0	0.4		1.0	0.4		1.0	0.5		1.0	0.5		ns
	Full	IV	1.2			1.2			1.2			1.2			ns
Input Hold Time (t_H)[10]	+25°C	IV	1.6	1.2		1.6	1.2		2.0	1.25		2.0	1.25		ns
	Full	IV	2.8			2.8			2.3			2.3			ns
Clock Pulse Width (Low)	+25°C	IV	1.1	0.85		1.1	0.85		1.0	0.85		1.0	0.85		ns
Clock Pulse Width (High)	+25°C	IV	1.4	0.85		1.4	0.85		1.1	0.85		1.1	0.85		ns
DYNAMIC PERFORMANCE															
Spurious-Free Dynamic Range (SFDR)[11]															
2.02 MHz; 100 MSPS; 2 MHz Span	+25°C	V		75			75			75			75		dBc
25.01 MHz; 100 MSPS; 2 MHz Span	+25°C	V		66			66			66			66		dBc
10.02 MHz; 250 MSPS; 5 MHz Span	+25°C	V		70			70			N/A			N/A		dBc
62.54 MHz; 250 MSPS; 5 MHz Span	+25°C	V		55			55			N/A			N/A		dBc
70 MHz; 220 MSPS; 10 MHz Span	+25°C	V		70			70			N/A			N/A		dBc
POWER SUPPLY[12]															
Negative Supply Current (–5.2 V)[13]	+25°C	I		210	280		210	280		218	290		218	290	mA
	Full	VI			290			290			300			300	mA
Positive Supply Current (+5.0 V)	+25°C	I		N/A			N/A			14	30		14	30	mA
	Full	VI		N/A			N/A				30			30	mA
Nominal Power Dissipation	+25°C	V		1.1			1.1			1.2			1.2		W
Power Supply Rejection Ratio (PSRR)[14]	+25°C	V		50			50			50			50		µA/V

NOTES
[1]Measured as error in ratio of full-scale current to current through R_{SET} (640 µA nominal); ratio is nominally 32. DAC load is virtual ground.
[2]Full-scale current variations among devices are higher when driving REFERENCE IN directly.
[3]Frequency at which a 3 dB change in output of DAC is observed, R_L = 50 Ω; 100 mV modulation at midscale.
[4]Based on I_{FS} = 32 (CONTROL AMP IN/R_{SET}) when using internal control amplifier. DAC load is virtual ground.
[5]Measured as voltage settling at midscale transition to ±0.1%; R_L = 50 Ω.
[6]Measured from 50% point of rising edge of CLOCK signal to 1/2 LSB change in output signal.
[7]Peak glitch impulse is measured as the largest area under a single positive or negative transient.
[8]Measured with R_L = 50 Ω and DAC operating in latched mode.
[9]Data must remain stable for specified time prior to rising edge of CLOCK.
[10]Data must remain stable for specified time after rising edge of CLOCK.
[11]SFDR is defined as the difference in signal energy between the fundamental and worst case spurious frequencies in the output spectrum window, which is centered at the fundamental frequency and covers the indicated span.
[12]Supply voltages should remain stable within ±5% for normal operation.
[13]190 mA typ on Digital $-V_S$, 30 mA typ on Analog $-V_S$.
[14]Measured at ±5% of $+V_S$ (AD9721 only) and $-V_S$ (AD9720 or AD9721) using external reference.

Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS[1]

Positive Supply Voltage ($+V_S$) (AD9721 Only) . . . . . +6 V
Negative Supply Voltage ($-V_S$)
(AD9720 and AD9721) . . . . . –7 V
Digital Input Voltages (D_1–D_{10}, CLOCK, $\overline{CLOCK}$)
AD9720 . . . . . 0 V to $-V_S$
AD9721 . . . . . –0.5 V to $+V_S$
Internal Reference Output Current . . . . . 500 µA
Control Amplifier Input Voltage Range . . . . . 0 V to –4 V
Control Amplifier Output Current . . . . . ±2.5 mA
Reference Input Voltage Range (V_{REF}) . . . . . 0 V to $-V_S$
Analog Output Current . . . . . 30 mA
Operating Temperature Range
AD9720/AD9721BN/BR . . . . . –25°C to +85°C
AD9720/AD9721TE/TQ . . . . . –55°C to +125°C
Maximum Junction Temperature[2]
AD9720/AD9721BN/BR . . . . . +150°C
AD9720/AD9721TE/TQ . . . . . +175°C
Lead Temperature (Soldering, 10 sec) . . . . . +300°C
Storage Temperature Range . . . . . –65°C to +150°C

NOTES
[1]Absolute maximum ratings are limiting values to be applied individually, and beyond which the serviceability of the circuit may be impaired. Functional operability is not necessarily implied. Exposure to absolute maximum rating conditions for an extended period of time may affect device reliability.
[2]Typical thermal impedances:
28-pin plastic DIP: θ_{JA} = 37°C/W, θ_{JC} = 10°C/W;
28-pin LCC: θ_{JA} = 41°C/W, θ_{JC} = 13°C/W;
28-pin SOIC: θ_{JA} = 46°C/W, θ_{JC} = 10°C/W;
Cerdip: θ_{JA} = 35°C/W, θ_{JC} = 10°C/W.
Soldered to board; no air flow.

ORDERING GUIDE

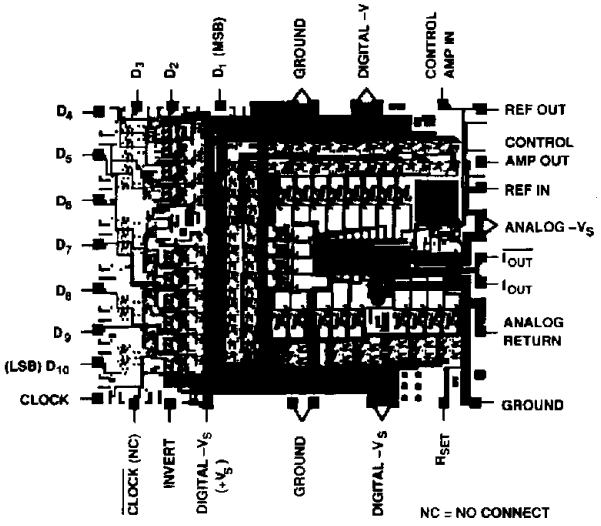
Model	Temperature Range	Package Description	Package Option
AD9720BN	–25°C to +85°C	28-Pin Plastic DIP	N-28
AD9720BR	–25°C to +85°C	28-Pin SOIC	R-28
AD9720TE	–55°C to +125°C	28-Pin LCC	E-28A
AD9720TQ	–55°C to +125°C	28-Pin Cerdip	Q-28
AD9721BN	–25°C to +85°C	28-Pin Plastic DIP	N-28
AD9721BR	–25°C to +85°C	28-Pin SOIC	R-28
AD9721TE	–55°C to +125°C	28-Pin LCC	E-28A
AD9721TQ	–55°C to +125°C	28-Pin Cerdip	Q-28

EXPLANATION OF TEST LEVELS

Test Level
I – 100% production tested.
II – 100% production tested at +25°C, and sample tested at specified temperatures.
III – Sample tested only.
IV – Parameter is guaranteed by design and characterization testing.
V – Parameter is a typical value only.
VI – All devices are 100% tested at +25°C. 100% production tested at temperature extremes for extended temperature devices; sample tested at temperature extremes for commercial/industrial devices.

DIE LAYOUT AND MECHANICAL INFORMATION

Die Dimensions . . . . . 199 × 165 × 15 (±2) mils
Pad Dimensions . . . . . 4 × 4 mils
Metalization . . . . . Aluminum
Backing . . . . . None
Substrate Potential . . . . . $-V_S$
Passivation . . . . . Nitride

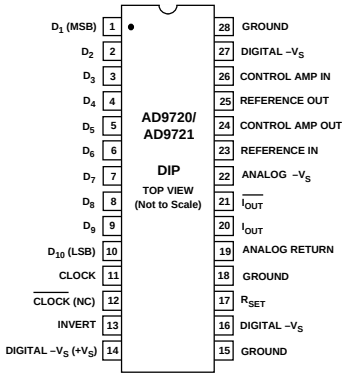


PIN DESCRIPTIONS

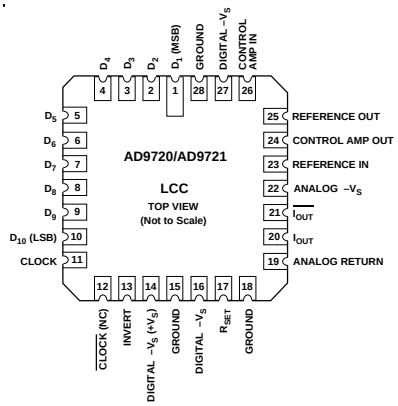
DIP Pin #	Name	Function
1	D_1 (MSB)	Most Significant Bit (MSB) of digital input word.
2-9	D_2–D_9	Eight of 10 digital input bits. Digital inputs are 10K ECL compatible for AD9720; TTL compatible for AD9721. See coding table elsewhere.
10	D_{10} (LSB)	Least Significant Bit (LSB) of digital input word. **Input Coding vs. Current Output** Input Code D_1–D_{10} / I_{OUT} (mA) / $\overline{I_{OUT}}$ (mA) 1111111111 / –20.48 / 0 0000000000 / 0 / –20.48
11	CLOCK	Edge-triggered latch enable signal for on-board registers. 10K ECL compatible for AD9720. TTL compatible for AD9721. Register loads data on rising edge of CLOCK signal; must be driven in conjunction with CLOCK.
12	$\overline{\text{CLOCK}}$/NC	Complementary edge-triggered latch enable signal for on-board registers. 10K ECL compatible for AD9720; not connected (NC) for AD9721.
13	INVERT	Normally connected to logic LOW; inverters are transparent in this mode. Logic High inverts the 9 LSBs (D_2–D_{10}) when the MSB is LOW. No internal pull-down resistor.
14	DIGITAL $-V_S$/$+V_S$	One of three digital supply pins; nominally –5.2 V for AD9720; +5 V for AD9721.
15	GROUND	Converter ground return.
16	DIGITAL $-V_S$	One of three negative digital supply pins; nominally –5.2 V.
17	R_{SET}	Connection for external resistance reference; nominally 1,960 Ω. Full-scale current out = 32 × (CONTROL AMP IN/R_{SET}) when using internal amplifier. DAC load is virtual ground.
18	GROUND	Converter ground return.
19	ANALOG RETURN	Analog current return. This point and the reference side of the DAC load resistors should be connected to the same potential (nominally ground).
20	I_{OUT}	Analog current output; full-scale output occurs with digital inputs at all "1." With external load resistor, output voltage $I_{OUT} \times (R_{LOAD} \parallel R_{INTERNAL})$. $R_{INTERNAL}$ is nominally 210 Ω.
21	$\overline{I_{OUT}}$	Complementary analog current output; zero-scale output occurs with digital inputs at all "1."
22	ANALOG $-V_S$	Negative analog supply; nominally –5.2 V.
23	REFERENCE IN	Normally connected to CONTROL AMP OUT (Pin 24). Direct line to DAC current source network. Voltage changes (noise) at this point have a direct effect on the full-scale output current of DAC. Full-scale current output = 32 × (CONTROL AMP IN/R_{SET}) when using internal amplifier. DAC load is virtual ground.
24	CONTROL AMP OUT	Normally connected to REFERENCE INPUT (Pin 23). Output of internal control amplifier, which provides a reference for the current switch network.
25	REFERENCE OUT	Normally connected to CONTROL AMP IN (Pin 26). Internal voltage reference, nominally –1.25 V.
26	CONTROL AMP IN	Normally connected to REFERENCE OUT (Pin 25) if not connected to external reference.
27	DIGITAL $-V_S$	One of three negative digital supply pins; nominally –5.2 V.
28	GROUND	Converter ground return.

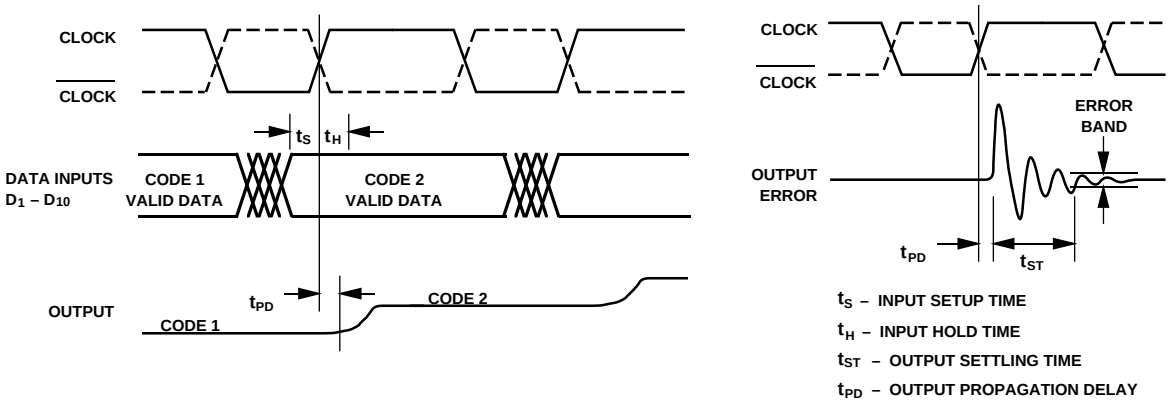
PIN CONFIGURATIONS

DIP & SOIC Packages



LCC Package





AD9720/AD9721 Timing Diagram

THEORY AND APPLICATIONS

The AD9720/AD9721 high speed digital-to-analog converters utilize Most Significant Bit (MSB) decoding and segmentation techniques to reduce glitch impulse and maintain 10-bit linearity without trimming.

As shown in the functional block diagram, the design is based on four main subsections: the Decoder/Driver circuits, the Edge Triggered Data Register, the Switch Network, and the Control Amplifier. An internal bandgap reference is also included to allow operation with a minimum of external components. The block labeled "Inverters" is transparent in normal operation, but can be used to minimize the external components requirements in DDS applications using the AD9950, a 300 MSPS phase accumulator (see AD9950 data sheet).

Digital Inputs/Timing

The AD9720 employs single-ended ECL-compatible inputs for data inputs D_1–D_{10} and the differential clock signals CLOCK and $\overline{\text{CLOCK}}$. The internal ECL midpoint reference is designed to match 10K ECL device thresholds. On the AD9721, a TTL translator is added at each input and the clock becomes single ended; with these exceptions, the AD9720 and AD9721 are identical. (NOTE: Pin 14 is $+V_S$ on AD9721; $-V_S$ on AD9720.)

In the Decoder/Driver section, the four MSBs (D_1–D4) are decoded to 15 "thermometer code" lines. An equalizing delay is included for the six Least Significant Bits (LSBs) and the clock signals. This delay minimizes data skew and data setup and hold times at the register inputs.

The on-board register is rising-edge-triggered and should be used to synchronize data to the current switches by applying a pulse with proper data set-up and hold times as shown in the timing diagram.

Although the AD9720/AD9721 chip is designed to provide isolation from digital inputs to the outputs, some coupling of digital transitions is inevitable, especially with TTL or CMOS inputs applied to the AD9721. Digital feedthrough can be reduced by forming a low-pass filter using a resistor in series with the capacitance of each digital input; this rolls off the slew rate of the digital inputs.

References

As shown in the functional block diagram, the internal band-gap reference, control amplifier, and reference input are pinned out for maximum user flexibility when setting the reference.

When using the internal reference, REFERENCE OUT (Pin 25) should be connected to CONTROL AMP IN (Pin 26). CONTROL AMP OUT (Pin 24) should be connected to REFERENCE IN (Pin 23). A 0.1 µF ceramic capacitor from Pin 23 to ANALOG $-V_S$ (Pin 22) improves settling by decoupling switching noise from the current sink base line. A reference current cell provides feedback to the control amp by sinking current through R_{SET} (Pin 17).

Full-scale output current is determined by CONTROL AMP IN and R_{SET} according to the equation:

$$I_{OUT}(FS) = (CONTROL\ AMP\ IN/R_{SET}) \times 32$$

The internal reference is nominally –1.25 V with a tolerance of ±8% and typical drift over temperature of 100 ppm/°C. If greater accuracy or better temperature stability is required, an external reference can be utilized. The AD589 reference features ±10 ppm/°C drift over temperatures from 0°C to +70°C.

Two modes of multiplying operation are possible with the AD9720/AD9721. Signals with bandwidths up to 1 MHz and input swings from –0.6 V to –1.2 V can be applied to the CONTROL AMP input as shown in Figure 1. Because the control amplifier is internally compensated, the 0.1 µF capacitor discussed above can be reduced to maximize the multiplying bandwidth. However, it should be noted that settling time for changes to the digital inputs will be degraded.

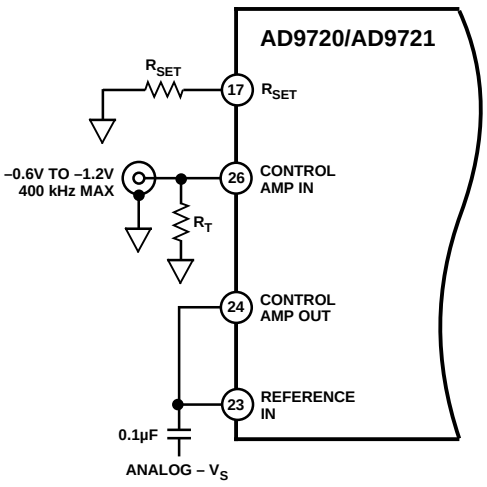


Figure 1. Low Frequency Multiplying Circuit

The REFERENCE IN pin can also be driven directly for wider bandwidth multiplying operation. The analog signal for this mode of operation must have a signal swing in the range of –3.3 V to –4.25 V. This can be implemented by capacitively coupling into REFERENCE IN a signal with a dc bias of –3.3 V (I_{OUT} ~ 22.5 mA) to –4.25 V (I_{OUT} ~ 3 mA), as shown in Figure 2, or by driving REFERENCE IN with a low impedance op amp whose signal swing is limited to the stated range.

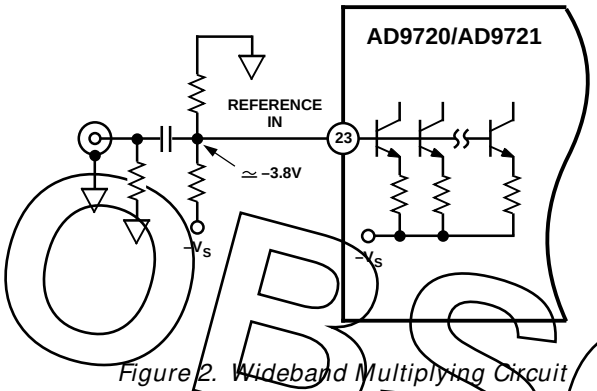


Figure 2. Wideband Multiplying Circuit

Outputs

The Switch Network provides complementary current outputs I_{OUT} and $\overline{I_{OUT}}$. The design of the AD9720/AD9721 is based on statistical current source matching which provides 10-bit linearity without trim. Current is steered to either I_{OUT} or $\overline{I_{OUT}}$ in proportion to the digital input code. The sum of the two currents is always equal to the full-scale output current minus one LSB.

The current output can be converted to a voltage by resistive loading as shown in the block diagram. Both I_{OUT} and $\overline{I_{OUT}}$ should be loaded equally for best overall performance. The voltage which is developed is the product of the output current and the value of the load resistor.

An operational amplifier can also be used to perform the I to V conversion of the DAC output. Figure 3 shows an example of a circuit which uses the AD9617, a high speed, current feedback amplifier. The resistor values in Figure 3 provide a 4.096 V swing, centered at ground, at the output of the AD9617 amplifier.

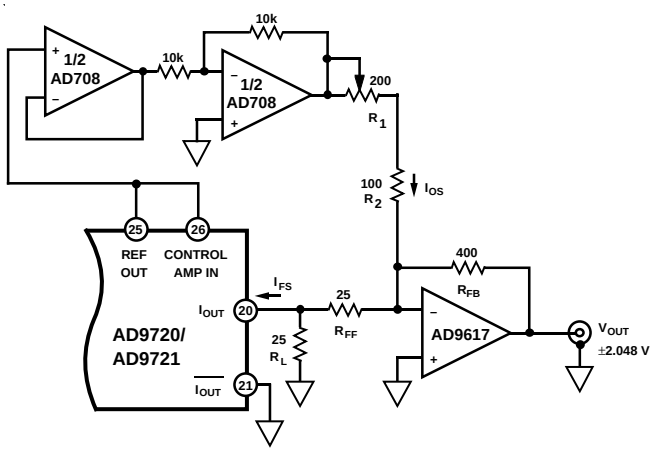


Figure 3. I/V Conversion Using Current Feedback Amp

DDS Applications

The performance characteristics of the AD9720/AD9721 make it ideally suited for direct digital synthesis (DDS) and other waveform generation applications. Since the aliased distortion of the DAC collects around the fundamental when generating frequencies which are nearly integer fractions of the clock rate, these are often considered worst case conditions.

Please contact the factory for information concerning the availability of an evaluation board or for additional characterization data.

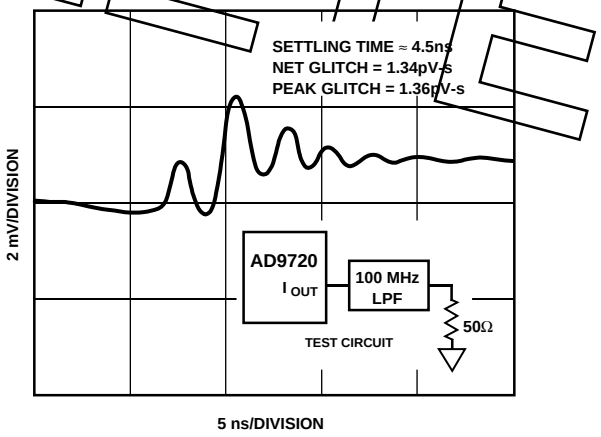


Figure 4. AD9720 Glitch Impulse

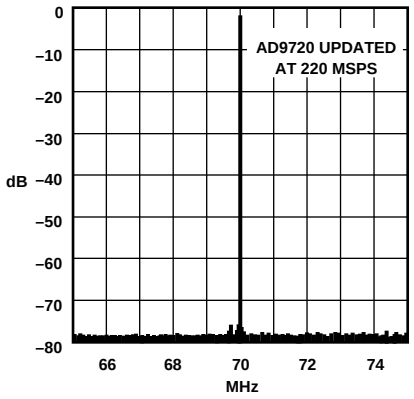


Figure 5. Typical Output Spectrum

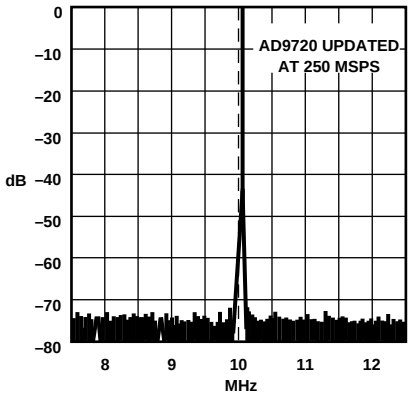


Figure 6. Typical Output Spectrum

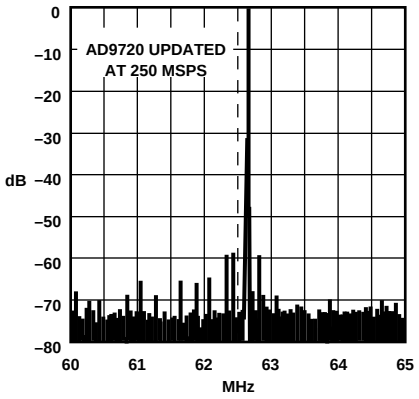


Figure 7. Typical Output Spectrum

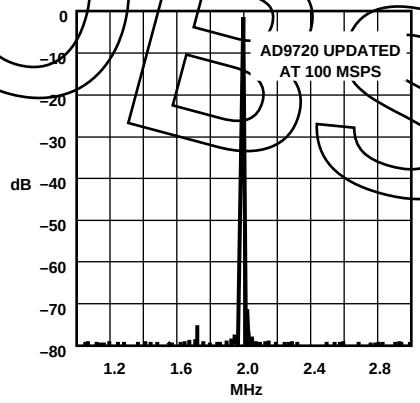


Figure 8. Typical Output Spectrum

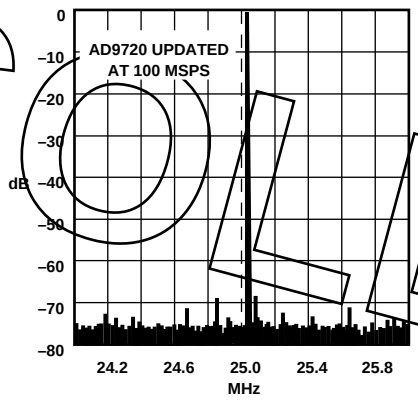


Figure 9. Typical Output Spectrum

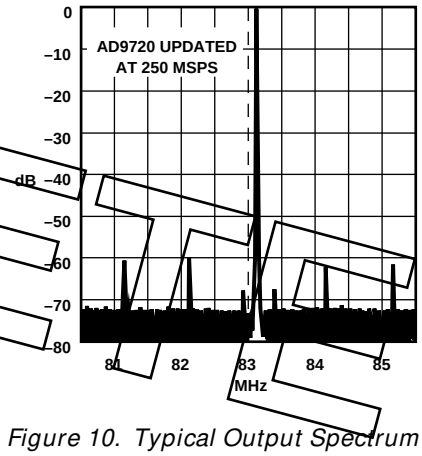


Figure 10. Typical Output Spectrum

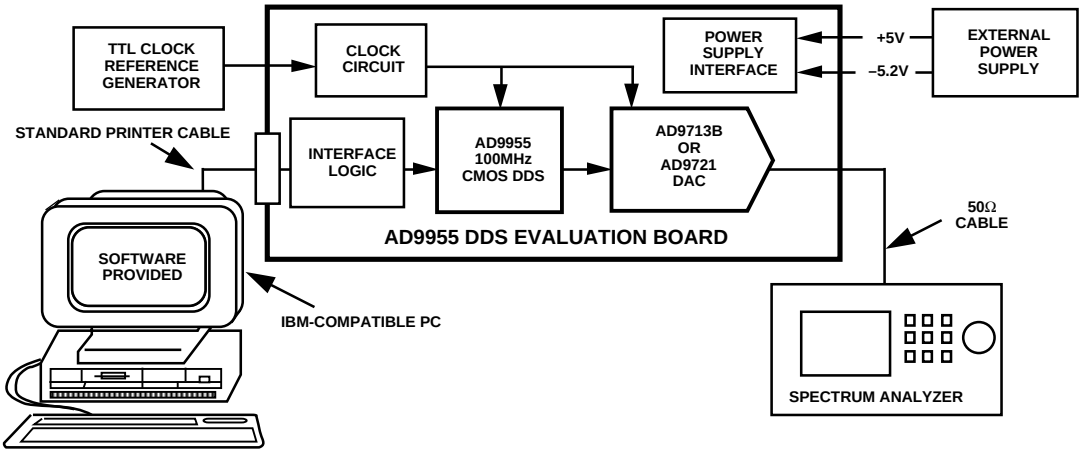
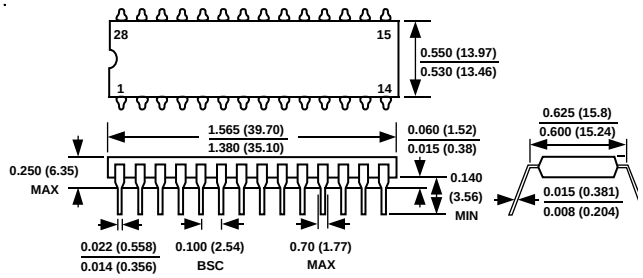


Figure 11. Direct Digital Synthesis System Diagram

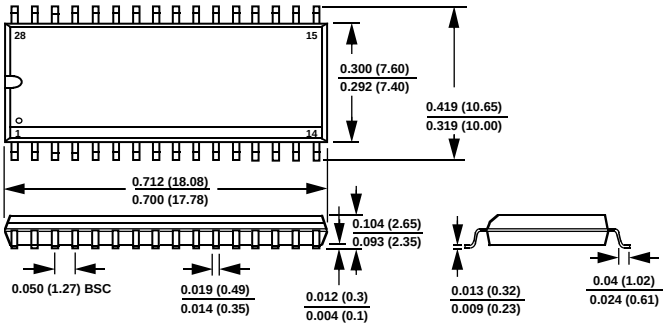
OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

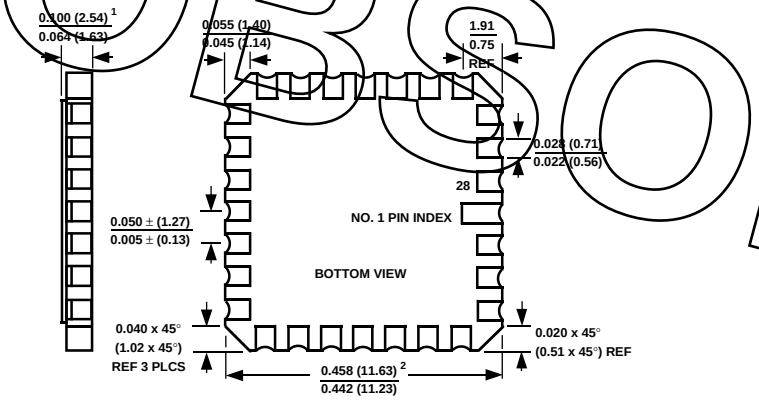
28-Pin Plastic DIP (Suffix N)



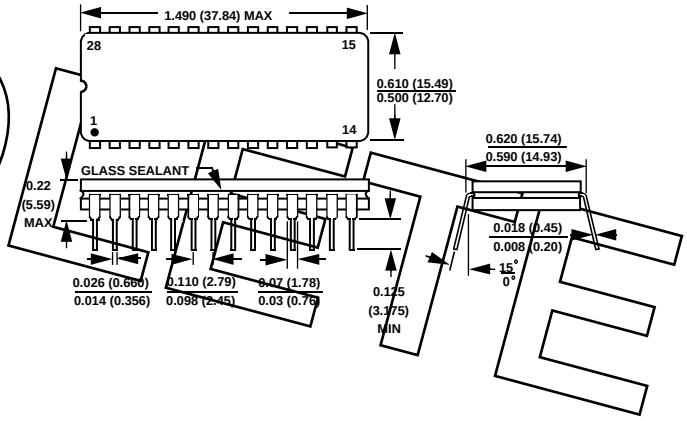
28-Pin SOIC (Suffix R)



28-Pin Leadless Chip Carrier (Suffix E)



28-Pin Cerdip (Suffix Q)



NOTES

1. THIS DIMENSION CONTROLS THE OVERALL PACKAGE THICKNESS.
2. APPLIES TO ALL FOUR SIDES.
3. ALL TERMINALS ARE GOLD PLATED.

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