CML Microcircuits

COMMUNICATION SEMICONDUCTORS

CMX649

ADM Codec

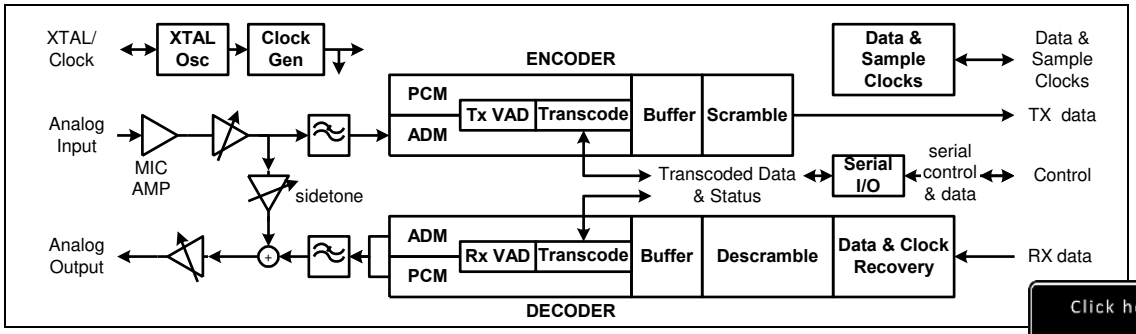
D/649/6 February 2013

Features

- Multiple Codec Modes, 16 to 128 kbps
  - Full duplex ADM and CVSD
  - Full duplex PCM: µ-law, A-law, Linear
  - Configurable ADM time constants
  - Dual channel transcoder/decoder mode
- High Performance Digital Architecture
- Low Power: 2.4mA at 3.0V typ.
- 2.7V - 5.5V Supply
- Data Clock Recovery
- Programmable Voice Activity Detector (VAD)
  - Adjust threshold level and attack/decay time
  - Use to powersave on low signal level
  - Silence/blank low level signals
- Programmable Digital Scrambler
- Flexible Interfaces
  - 8-bit and 16-bit burst data with sync strobe
  - 1 bit serial data with clock
  - Host serial control/data interface
- Internal and External Sample Clocking
- Programmable Filters
  - Encoder mic input ADC anti-alias
  - Decoder audio out DAC anti-imaging
- Low Noise Differential Mic Input Amp
- Programmable Analog Interface Gain
  - Microphone in
  - Decoder audio out
  - Sidetone path

Applications

- Low Cost Digital Cordless Headset
- Personal Area Network (PAN) Voice Link
- Digital Cordless Telephone
- Wireless Digital PBX
- Full Duplex Digital Radio Systems
- Time Division Duplex (TDD) Systems
- Portable Digital Voice Communicator
- Digital Voice Delay



1. Brief Description

The CMX649 Adaptive Delta Modulation (ADM) Voice Codec provides full duplex ADM, companded (µ/A-law) PCM and linear PCM codec and transcoder functions for cost effecive, low power, wireless voice applications. Selectable modes and algorithms support many requirements. Robust ADM coding (e.g. CVSD) reduces host protocol and software burdens, eliminating forward error correction, framing protocols and algorithm processing. Dual transcode/decode mode supports multichannel applications.

Integrated filter responses adjust independently of 16kbps to 128kbps codec data rates. Codec sample clocks are externally applied or internally generated. High performance analog interfaces and sidetone include digital gain controls. Encoder and decoder voice activity detectors support powersaving.

The CMX649 ADM Voice Codec supports 2.7V to 5.5V operation and is available in 20-pin SOIC (D3) and TSSOP packages (E3) packages.

CONTENTS

2. Block Diagram

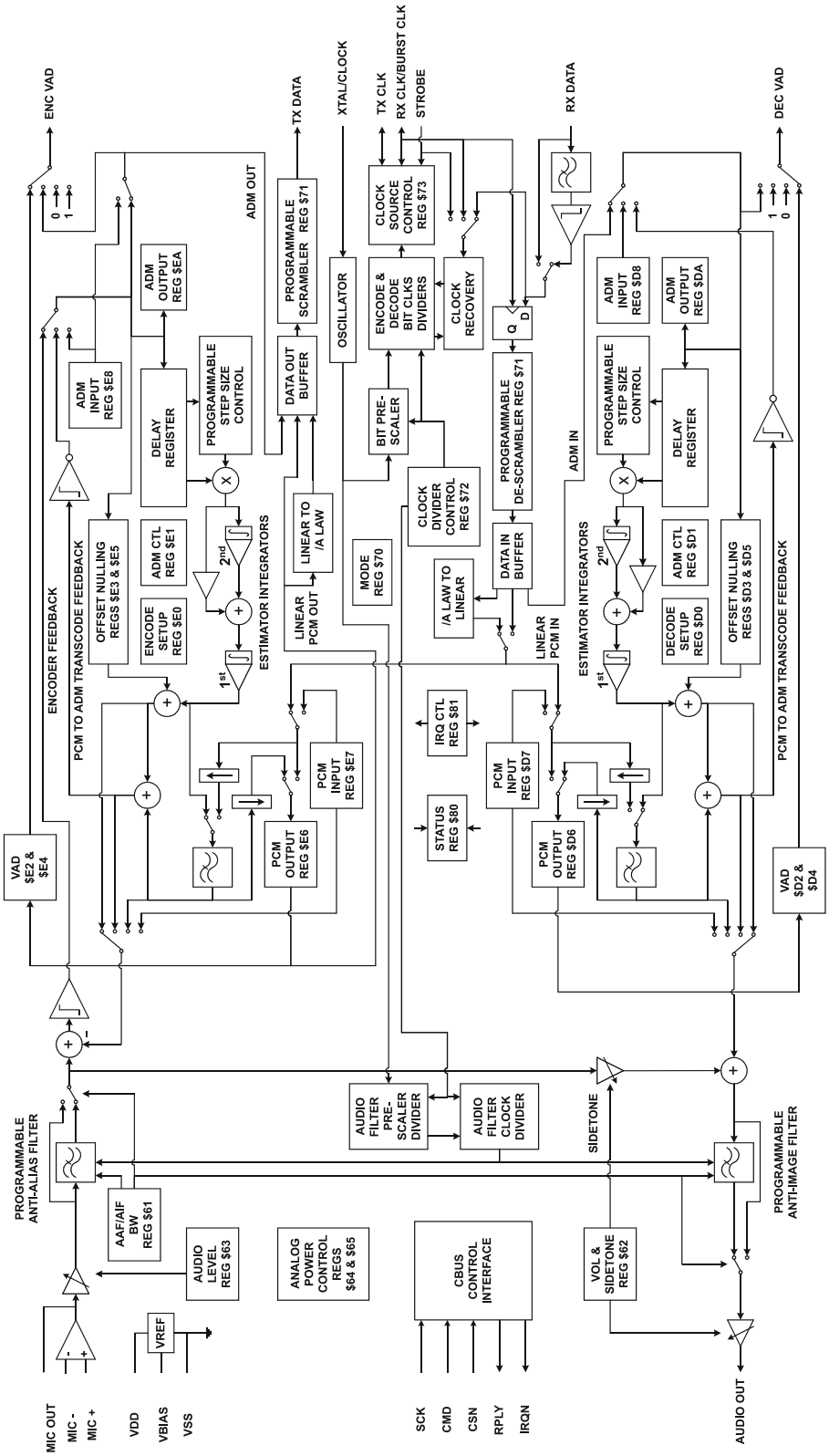


Figure 1 Block Diagram

3. Signal List

SOIC (D3) Package	TSSOP (E3) Package	Signal		Description
Pin No.	**Pin No.**	**Name**	**Type**	
1	1	STRB	Digital Input	Strobe signal for 8/16 buffered serial I/O.
2	2	ENC VAD	Digital Output	Encoder voice activity detector output.
3	3	V_{DD}	Power	Positive supply rail.
4	4	MIC OUT	Analog Output	Analog output signal from microphone amplifier.
5	5	MIC +	Analog Input	Analog non-inverting input to microphone amplifier.
6	6	MIC -	Analog Input	Analog inverting input to microphone amplifier.
7	7	V_{BIAS}	Analog Output	$V_{DD}/2$ – Not suitable for external applications without buffering. Pin should be decoupled to V_{SS} with a capacitor (>1µF).
8	8	AUDIO OUT	Analog Output	Analog Output signal from decoder.
9	9	V_{SS}	Power	Negative supply rail (Ground).
10	10	DEC VAD	Digital Output	Decoder voice activity detector output.
11	11	RX DATA	Digital Input	Received signal serial data input.
12	12	RX CLK	Digital I/O	Decoder data clock.
13	13	XTAL/CLK	Analog Input	Crystal oscillator input.
14	14	IRQN	Digital Output	)
15	15	RPLY	Digital Output	)
16	16	CMD	Digital Input	) C-BUS control signals.
17	17	SCLK	Digital Input	)
18	18	CSN	Digital Input	)
19	19	TX CLK	Digital I/O	Clock signal for encoded data out.
20	20	TX DATA	Digital Output	Encoded data output.

Notes: I/O = Input/Output
NC = No Connection

4. External Components

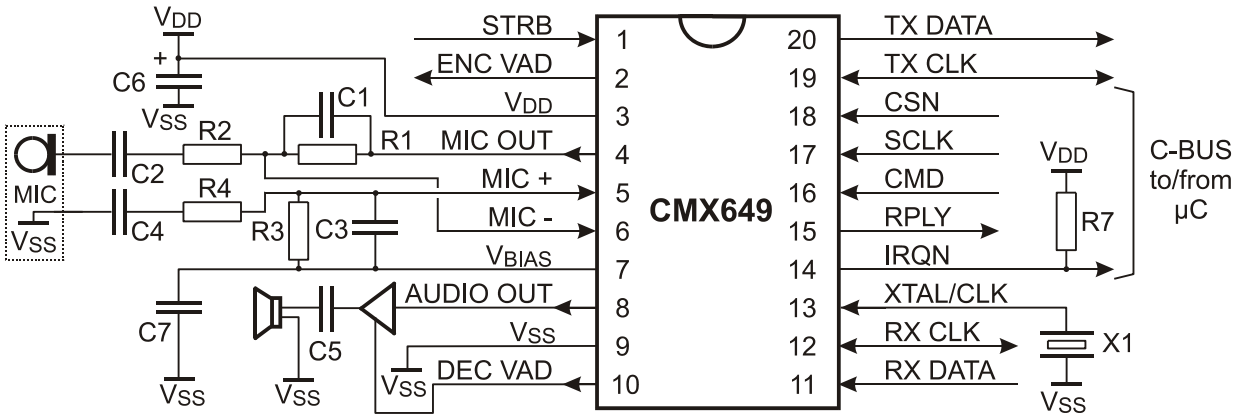


Figure 2 Recommended External Components

R1, R2	Note 1	100kΩ	±10%	C5	Note 2	33.0µF	±20%
R3, R4	Note 1	100kΩ	±10%	C6	Note 3	1.0µF	±20%
R7		100kΩ	±20%	C7	Note 4	1.0µF	±20%
C1, C3	Note 1	100 pF	±20%				
C2, C4	Note 1	0.01µF	±20%	X1	Note 5	8.192MHz	

Notes:

1. C1 - C4 and R1 - R4 set the microphone amplifier gain and frequency response. The values shown set the gain to unity and the low and high –3dB frequency rolloff points to approximately 150Hz and 15kHz respectively.
2. DC blocking capacitor for driving a speaker from an external speaker amplifier. The value shown is based on a 32Ω impedance speaker where the highpass rolloff frequency is set to approximately 150Hz.
3. V_{DD} decoupling capacitor.
4. Bias decoupling capacitor.
5. A 8.192MHz Xtal/Clock input will yield exactly 16kbps/32kbps/64kbps internally generated data clock rates.
6. To achieve good noise performance, V_{DD} and V_{BIAS} decoupling and protection of the signal path from extraneous in-band signals are very important. It is recommended that the printed circuit board is laid out with a ground plane in the CMX649 area to provide a low impedance connection between the V_{SS} pin and the V_{DD} and V_{BIAS} decoupling capacitors.

5. General Description

The CMX649 encodes and decodes analog audio signals to/from ADM, Linear PCM, µ-law PCM or A-law PCM. It has programmable clock dividers that enable it to use an 8.000 MHz to 16.384 MHz crystal (or a 2.048 MHz to 16.384 MHz external clock source) and to sample the data over a large range of data rates. Programmable current sources for on-chip op-amps enable the overall power consumption to be optimised for any given supply voltage and clocking scheme, thus achieving extremely low working power levels.

Anti-Alias Image filters and gain controls are fully programmable. All the time constants and other parameters of the ADM can be programmed for optimum performance.

The CMX649 also includes a Microphone Amplifier, Data Clock Recovery, Data Scrambler/De-Scrambler and Voice Activity Detector (VAD) circuits.

All of these parameters are controlled via C-BUS.

5.1 Block Descriptions

The CMX649 contains a full duplex speech codec supporting common Adaptive Delta Modulation (ADM) and non-linear PCM coding algorithms. In addition, it supports linear PCM coding for DSP interface applications. This codec offers simple interface and application, yet is configurable to support a wide variety of speech quantisation systems.

5.1.1 ADM Coding Engine

ADM is a differential waveform coding technique predominantly applied to speech. Figure 3 illustrates the ADM encoder employed. The device is for speech quantising applications and is based on popular Continuously Variable Slope Delta (CVSD) encoder approaches, with optional modifications and improvements configurable through the ENCODE and DECODE ADM CONTROL Registers ($E1 and $D1). Optional second order integration in the feedback loop provides improved speech quality at a given bit rate or similar quality at a lower bit rate. Toll quality is achieved at bit rates much lower than for PCM. The decoder is embedded in the encoder, as is the case with most differential encoders. Note the symmetry between the encoder and decoder of Figures 3 and 4 respectively. The signal flows for ADM are shown in bold.

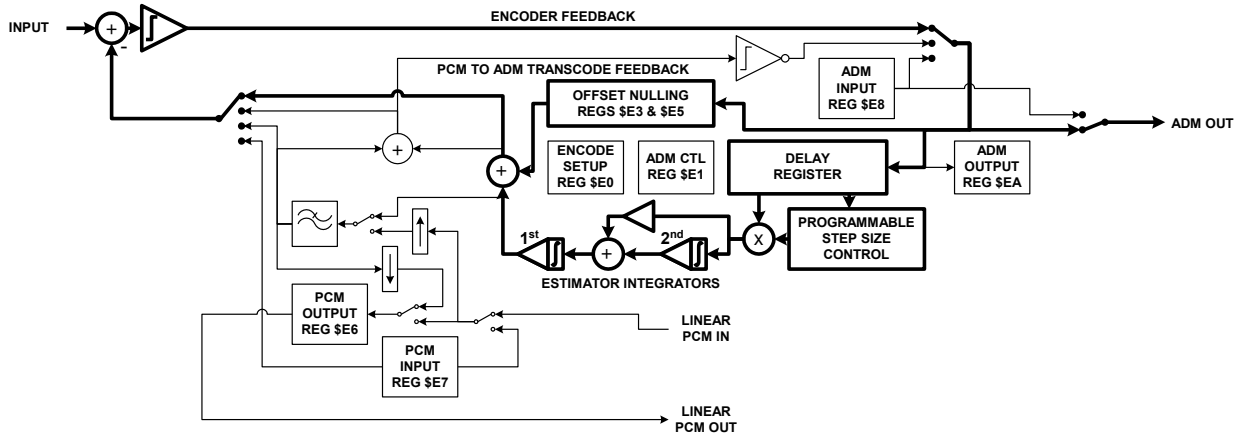


Figure 3 ADM Encoding

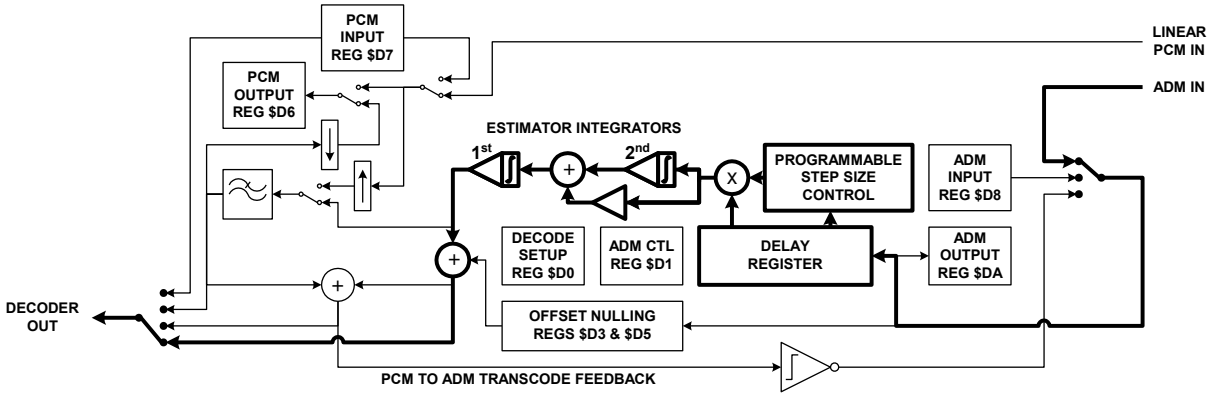


Figure 4 ADM Decoding

The estimator integrators (principal and second) as well as the step size decay (companding integrator) have programmable time constants. Additionally, the minimum and maximum step height and the depth of the delay register are programmable via preset values in the DECODE and ENCODE ADM CONTROL Registers ($D1 and $E1) to support a wide variety of different ADM algorithms including CVSD of Bluetooth™ version 1.1. The switches in Figures 3 and 4 are controlled by the ENCODER and DECODER MODE and SETUP Registers ($E0 and $D0). Various signal flows are possible to allow standard ADM and PCM encoding and decoding as well as transcoding either direction between ADM and PCM (e.g. Figures 7 and 8). Additionally, several summing options are possible. In the decoder a PCM and ADM input stream may be summed – note that this requires at least one of the streams to be input via C-BUS. In the encoder a PCM input stream may be summed with the ADM estimate causing the encoded ADM bit stream to represent the sum of the analog input and linear PCM stream input over C-BUS.

5.1.2 PCM Encoding and Decoding

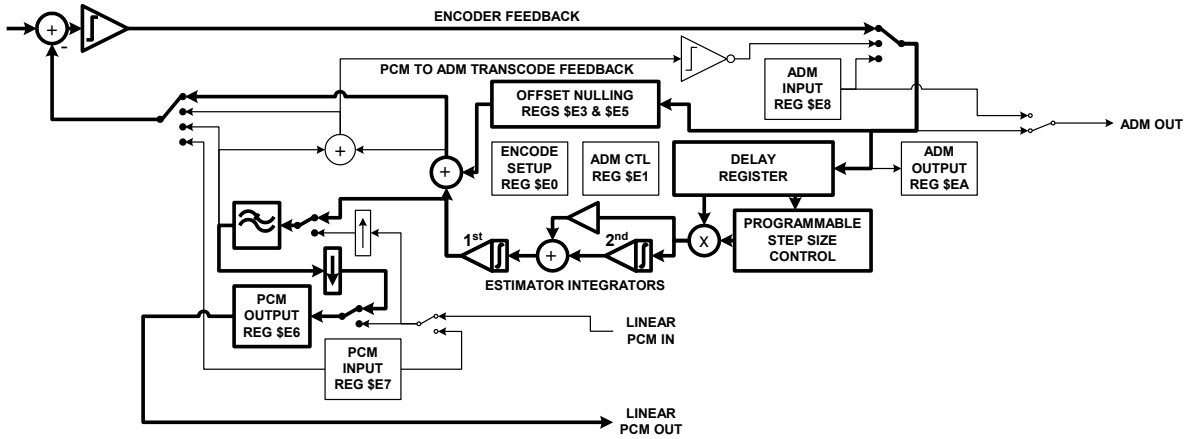


Figure 5 PCM Encoding

The output of the first or principal estimator integrator in Figures 3 and 4 is linear PCM. By decimating and filtering this signal it is possible to obtain a linear PCM representation, as shown in Figures 5 and 6. Employing either 8:1 or 4:1 decimation filters provides about 30dB attenuation of out of band quantisation noise prior to decimation. The ADM coding engine, which suppresses out of band noise by roughly 20dB, provides (in conjunction with the decimating filter) an overall out of band suppression of approximately 50dB. Using second order ADM at 64kbps with the 8:1 decimation filter provides better than toll quality linear speech samples. Accordingly, 8k samples/sec linear PCM encoder performance can be enhanced when the ADM codec second order integrator is enabled and the ADM codec is operated at the maximum rate. Decoding PCM simply requires interpolation and filtering to compensate for sin(x)/x roll-off of zero holding the PCM samples. The interpolation ratio can be programmed to 4 or 8.

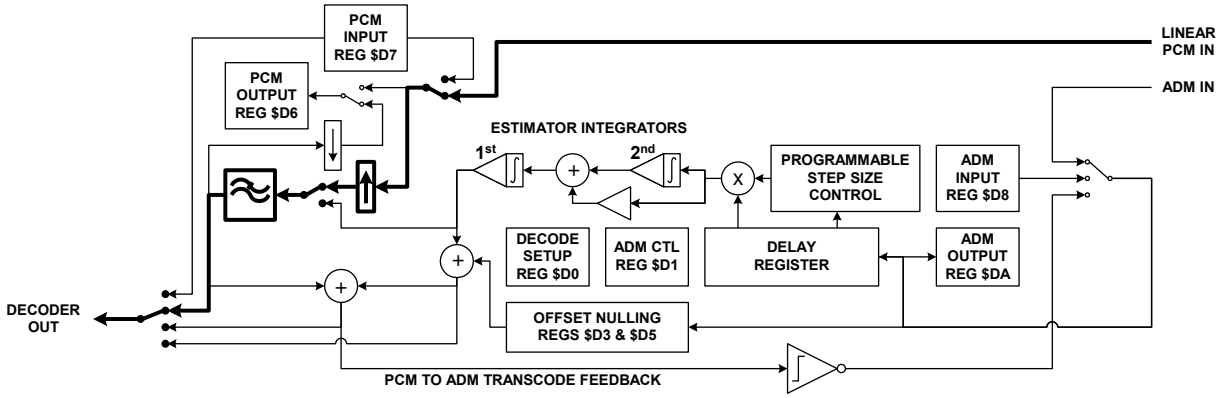


Figure 6 PCM Decoding

5.1.3 Transcoding with the Encoder and Decoder

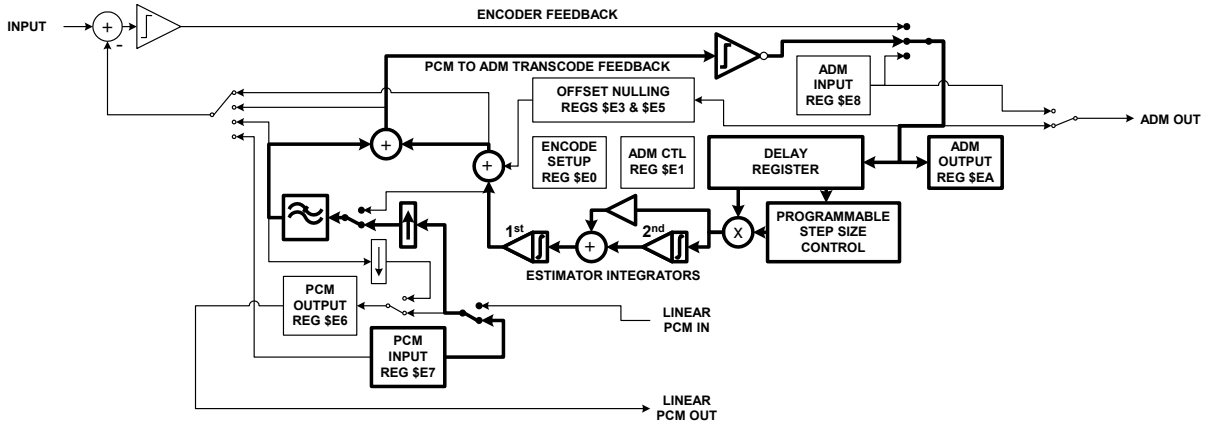


Figure 7 PCM to ADM transcoding with Encoder

(note that the decoder also can be configured to do this function and in this example all data is read and written via C-BUS registers $EA ($DA) and $E7 ($D7) respectively (for decoder)).

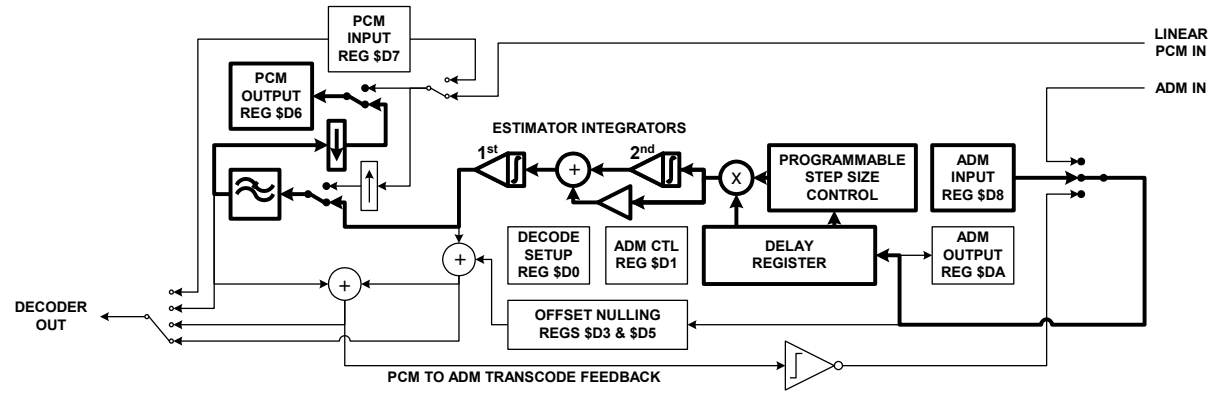


Figure 8 ADM to PCM transcoding with Decoder

(note that the encoder can also be configured to do this function and in this example all data is read and written via C-BUS registers $D6 ($E6) and $D8 ($E8) respectively (for encoder)).

5.1.4 Non-Linear Instantaneous Companding

When using the device over its standard PCM codec style interface, instantaneous companding can be enabled to cut in half the PCM word size. Either μ-law or A-law type companding algorithms are provided and use 16-chord piecewise linear approximations. Essentially the companded 8-bit PCM word is a simple floating-point representation with a sign bit, a 3-bit exponent and a 4-bit mantissa. This approach yields toll quality speech at reduced data rates.

5.1.5 Digitally Controlled Amplifiers

There are three Digitally Controlled Amplifiers (DCA) on-chip, which are used to set the signal levels for transmit-audio-in, side-tone-audio, and receive-audio-out (volume control). The transmit-audio DCA is adjustable in 0.5dB steps over a +7.5dB to –7.5dB range. The side-tone DCA is adjustable in 6.0dB steps over a 0dB to –21.0dB range. Side-tone audio is added to the audio output signal via an operational amplifier configured as a summing amplifier. This feeds the receive-audio DCA, which is adjustable in 1.5dB steps over a +12.0dB to –33.0dB range.

5.1.6 Microphone Amplifier

The input amplifier is a high gain low-noise operational amplifier capable of interfacing with a variety of different microphones. Figure 9 is a simplified schematic showing the external components required for typical application with an electret condenser microphone. Typical values for R1, R3, C1 and C3 should be set according to microphone sensitivity requirements, those shown are for unity gain. Note also that the microphone biasing resistors (R5 and R6) are microphone specification dependent.

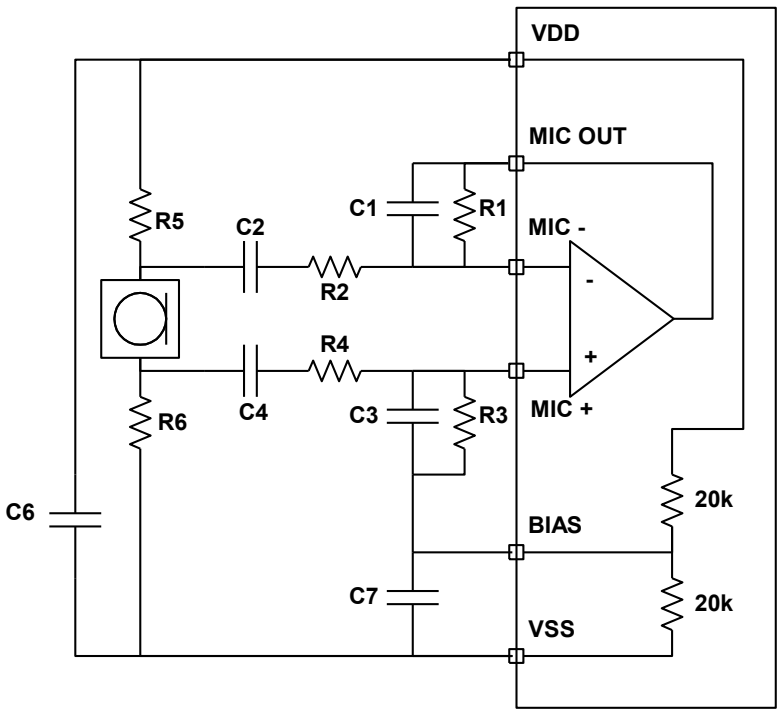


Figure 9 Electret Microphone - Input Amplifier Schematic

R1, R3	100kΩ	±10%	R5	100kΩ	±10%
R2, R4	100kΩ	±10%	R6	100kΩ	±10%
C1, C3	100 pF	±20%	C6	1.0μF	±20%
C2, C4	0.01μF	±20%	C7	1.0μF	±20%

5.1.7 Programmable Anti-alias/image SC Filters

The anti-aliasing (AAF) and anti-imaging (AIF) switched capacitor (SC) filters have a programmable cut-off frequency to accommodate different input signal bandwidths. Typically, the audio filter bandwidth should be programmed to be 1/10th of the ADM bit rate (or lower) for "toll" (or better) quality audio reconstruction. For "communications" quality, the audio bandwidth may approach 1/6th of the ADM bit rate for ADM rates below 20kbps. The anti-alias/image SC filter bandwidth is programmed directly via C-BUS commands to the AAF/AIF BANDWIDTH Register ($61). Additionally, the switched capacitor clock frequency can be altered via C-BUS commands to the CLK DIVIDER CONTROL Register ($72). Typically, the CLK DIVIDER CONTROL Register should be programmed to provide a 256kHz SC filter clock. Altering the SC filter clock from the recommended 256kHz frequency proportionally scales the frequency axis in the plot below:

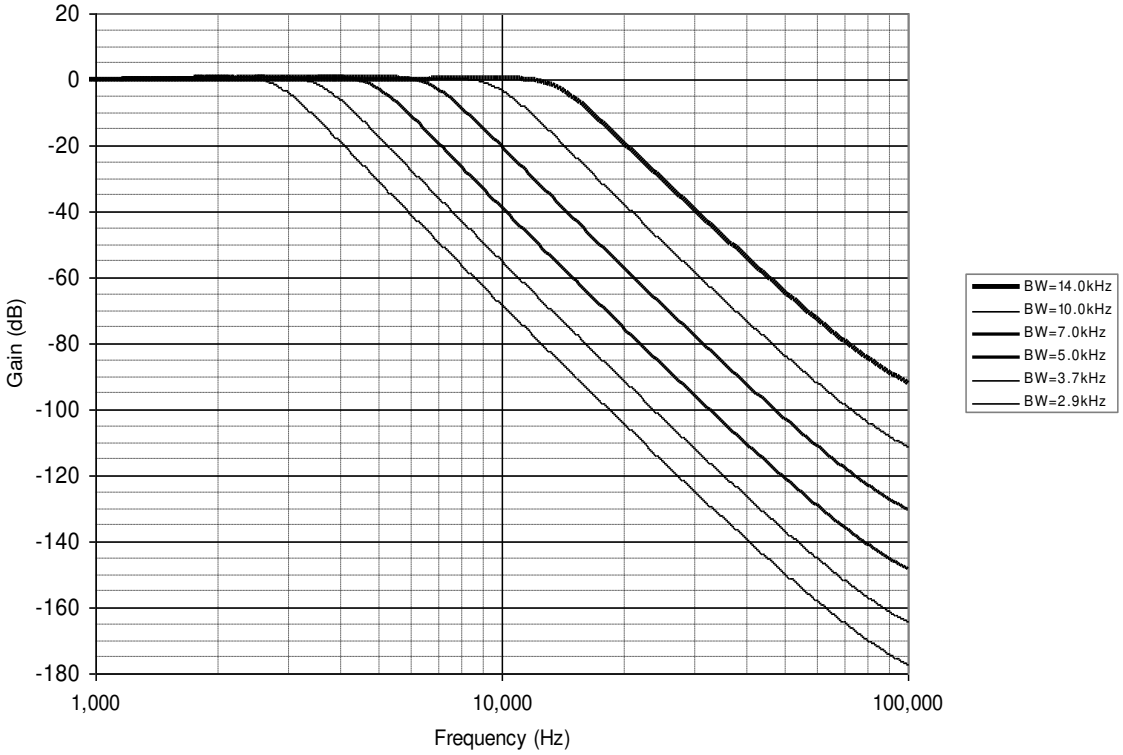


Figure 10a Typical Anti-Alias/Image Filter Frequency Response

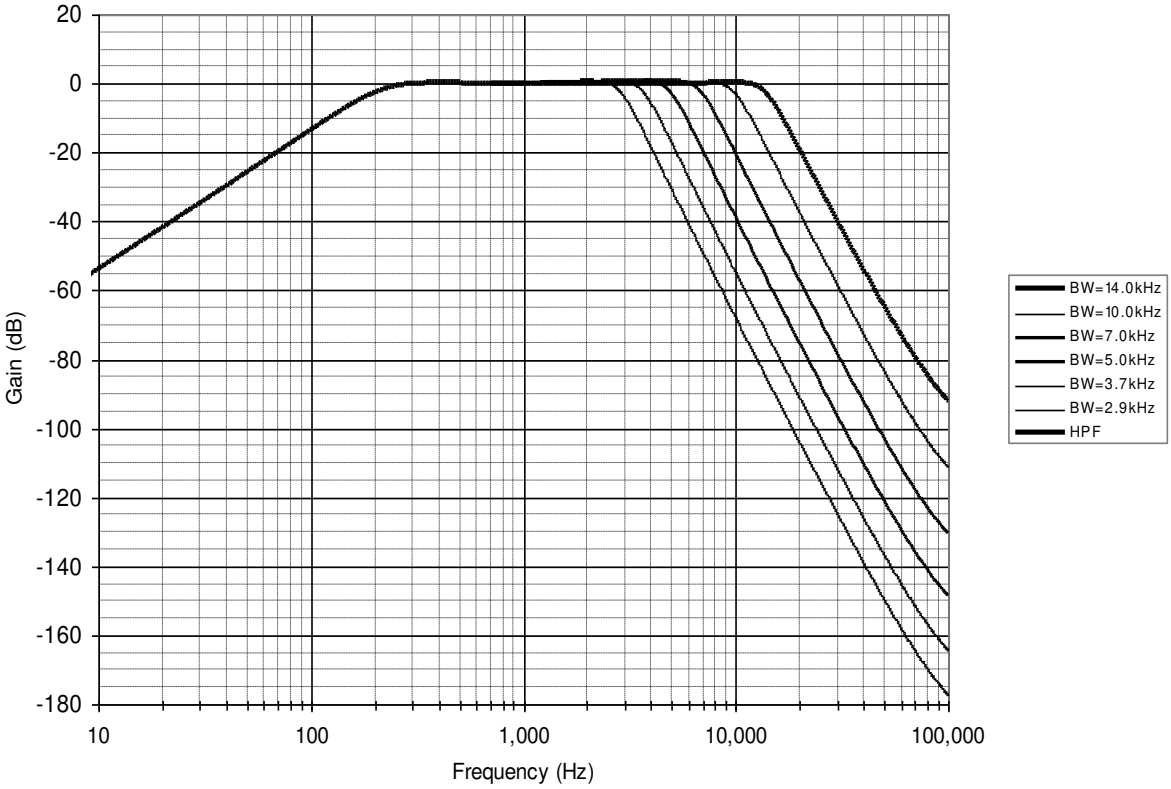


Figure 10b Typical Anti-Image Filter Frequency Response

5.1.8 Data Clock Recovery

Data from the RX DATA pin is driven into a comparator to remove amplitude variations. The output of the comparator is a logic signal that can be inverted by setting the appropriate control bit in the SCRAMBLER CONTROL Register ($71). Using the output of the comparator, the clock recovery block can be enabled to generate a phase-locked clock equal to the CVSD data rate, which is used to clock data from the RX DATA pin into the decoder. The recovered clock frequency is controlled by the CLK DIVIDER CONTROL Register ($72). If the clock recovery block is bypassed, data must then be applied which is synchronised to the clock on the RX CLK pin (either internally generated or externally applied).

External ADM rate bit clocks can be used for both the encoder and decoder paths and do not require use of the clock recovery PLL. Externally applied clocks act directly as the ADM sample clocks and should be generated with little jitter for best performance. Please note that the maximum usable frequency of externally applied bit clocks is 1/60th of the frequency of the output of the internal bit clock prescaler.

The clock recovery circuit is normally applied to the decoder. However, it is possible to use the recovered clock for the encoder section as well. This supports systems where the base unit is using an internal clock or local external clock for transmit and clock recovery for the decoder clock. The remote unit can then be configured to use the recovered clock for both encode and decode. Internal data clocks for the encoder and decoder can also be selected for data input and output control.

5.1.9 Data Scrambler/De-scrambler

The scrambler receives digital data from the encoder. It is implemented with a 10-bit programmable linear feedback shift register (LFSR) allowing a choice of various maximal length scrambling codes. The scrambler, also known as a randomizer, provides not only a level of communication security, but may also help reduce the occurrence of abnormally long strings of 1s or 0s.

The de-scrambler receives the scrambled data from the data slicer and de-scrambles it to the original data as long as the selected LFSR maximal length sequence is the same as that in the transmitting scrambler. The de-scrambler block has the same configuration as the scrambler and is self-synchronizing. Both the scrambler and de-scrambler can be bypassed.

Nine example maximal length codes are represented below through their polynomial coefficients which can be directly programmed in Bits 9-0 of the SCRAMBLER CONTROL Register ($71):

Length	Polynomial coefficients in hex format
2	0x003
3	0x006
4	0x00C
5	0x014
6	0x030
7	0x060
8	0x08E
9	0x110
10	0x240

5.1.10 Voice Activity Detector (VAD)

The VAD function is implemented with an energy detector circuit. This circuit consists of an absolute value function, an integrator and a threshold detector. The threshold detector level and the integrator time constants (i.e. attack and decay time control) are user programmable via the DECODE and ENCODE VAD THRESHOLD Registers ($D2 and $E2) and the DECODER and ENCODER MODE AND SETUP Registers ($D0 and $E0). Referring to Figure 11, the input to the VAD comes from the PCM signal. The signal is rectified and averaged with a lossy integrator. The output of the integrator is compared to the VAD threshold to derive the logic signal VAD_OUT. If VAD_OUT is a logic one, signal energy greater than the threshold is present. If VAD_OUT is a logic zero, signal energy is below the threshold. When the VAD "trip" threshold has been reached, the amplitude required to clear this VAD state is set internally to half of the "trip" threshold. For example, if the VAD "trip" threshold is set to 100mV then the "clear" threshold will be 50mV. This hysteresis is provided to minimise chattering and is not user-adjustable. Attack and decay times for the decoder VAD and encoder VAD can be independently controlled via the DECODER and ENCODER MODE AND SETUP Registers ($D0 and $E0). Typical attack and decay times used for detecting voice activity are 5ms and 150ms, respectively. The energy levels may be read from DECODE and ENCODE VAD LEVEL OUTPUT Registers ($D4 and $E4) for the decoder and encoder and used to adaptively set the detector threshold value by observing the energy level of background noise.

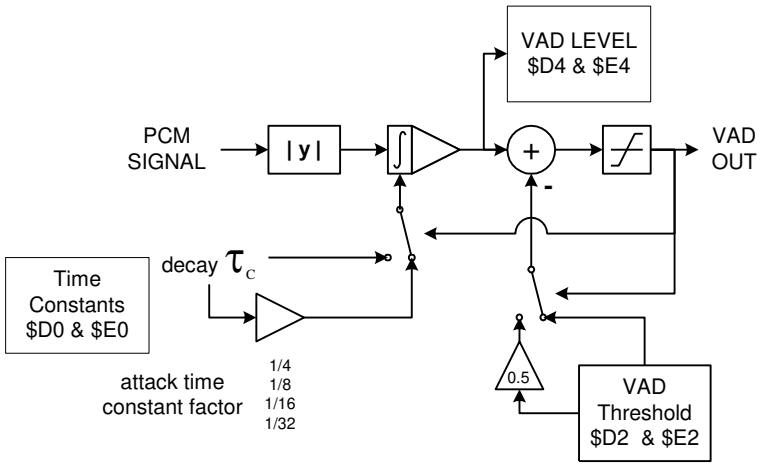


Figure 11 VAD Block Diagram

5.2 C-BUS Description

Address/Commands
Instructions and data are transferred, via C-BUS, in accordance with the timing information given in Figure 12.

Instruction and data transactions to and from the CMX649 consist of an Address/Command (A/C) byte followed by either:

(i) a further instruction or data (1 or 2 bytes) or
(ii) a status or Rx data reply (1 or 2 bytes)

Write Only C-BUS Registers

REGISTER NAME	HEX ADDRESS/ COMMAND	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
GENERAL RESET	**$01**	X	X	X	X	X	X	X	X
AAF/AIF BANDWIDTH	**$61**	Anti-Alias Filter				Anti-Image Filter			
		By-Pass	Band-Width			By-Pass	Band-Width		
VOLUME/SIDE -TONE LEVEL	**$62**	Volume					Side-Tone		ON/OFF
AUDIO INPUT LEVEL CTRL	**$63**	Input Level					0	0	0
POWER CONTROL 1	**$64**	0	Anti-Alias Filter	0	Anti-Image Filter	Enc DAC Current		Dec DAC Current	
POWER CONTROL 2	**$65**	Mic Amp Current		Audio Current		Volume Current		Xtal Current	Analog Enable
CODEC MODE CONTROL	**$70**	0	0	0	0	0	Codec Modes		
SCRAMBLER CONTROL (1)	**$71**	SCRAMBLER			DE-SCRAMBLER			Polynomial	
		EN	0	INVERT	EN	0	INVERT	T9	T8
(2)		Polynomial							
		T7	T6	T5	T4	T3	T2	T1	T0
CLK DIVIDER CONTROL (1)	**$72**	PREN	DCKEN	ECKEN	Filter Pre-Scaler		Filter Divider		
(2)		Bit Clock Pre-Scaler		Decoder Bit Clock Divider			Encoder Bit Clock Divider		
CLK SOURCE CONTROL (1)	**$73**	0	0	Phase Detect Input Select		0	0	0	0
(2)		PLL EN	Rx Bit Clk Select	Tx Bit Clock Select		Data Filter By-Pass	Data Filter and Slicer Power Control		Data Filter BW
CODEC INTERRUPT CONTROL	**$81**	Encode Enable				Decode Enable			

REGISTER NAME	HEX ADDRESS/ COMMAND	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
DECODER MODE AND SETUP (1)	**$D0**	DEC BY 4/8	Select PCM IN		Select ADM IN		Decoder Output Select		0
(2)		VAD Decay Time Constant			VAD Attack Time Constant		Select VAD Output Source		0
DECODE ADM CONTROL (1)	**$D1**	Syllabic Time Constant			Dynamic Range for Step Size Integrator			Companding Rule	
(2)		Estimator Integrator Principal Time Constant			2^{nd} Order Estimator Time Constant		Zero location for 2^{nd} Order Integration		Dec Zero
DECODE VAD THRESHOLD (1)	**$D2**	Voice Activity Detector Threshold Setting Bits 15 - 8							
(2)		Voice Activity Detector Threshold Setting Bits 7 - 0							
DECODE OFF-SET LEVEL (1)	**$D3**	Offset Input Level Bits 15 - 8							
(2)		Offset Input Level Bits 7 – 0							
DECODE LINEAR PCM INPUT (1)	**$D7**	Direct Write to DAC Input Bits 15 - 8							
(2)		Direct Write to DAC Input Bits 7 – 0							
DECODE ADM INPUT	**$D8**	Decode ADM Input							
ENCODER MODE AND SETUP (1)	**$E0**	DEC BY 4/8	Select PCM IN		Select ADM IN		Local Decoder Output Select		Idle Channel Enhance
(2)		VAD Decay Time Constant			VAD Attack Time Constant		Select VAD Output Source		ADM Output Select
ENCODE ADM CONTROL (1)	**$E1**	Syllabic Time Constant			Dynamic Range for Step Size Integrator			Companding Rule	
(2)		Estimator Integrator Principal Time Constant			2^{nd} Order Estimator Time Constant		Zero location for 2^{nd} Order Integration		Dec Zero
ENCODE VAD THRESHOLD (1)	**$E2**	Voice Activity Detector Threshold Setting Bits 15 - 8							
(2)		Voice Activity Detector Threshold Setting Bits 7 - 0							
ENCODE OFF-SET LEVEL (1)	**$E3**	Offset Input Level Bits 15 - 8							
(2)		Offset Input Level Bits 7 – 0							

REGISTER NAME	HEX ADDRESS/ COMMAND	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
ENCODE DAC INPUT (1)	**$E7**	Direct Write to DAC Input Bits 15 - 8							
(2)		Direct Write to DAC Input Bits 7 – 0							
ENCODE ADM INPUT	**$E8**	Encode ADM Input							

Read Only C-BUS Registers

REGISTER NAME	HEX ADDRESS/ COMMAND	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
CODEC STATUS (READ)	**$80**	Encode Process Status				Decode Processor Status			
DECODE VAD LEVEL OUTPUT (1)	**$D4**	Voice Activity Detector Level Output Bits 15 - 8							
(2)		Voice Activity Detector Level Output Bits 7 - 0							
DECODE OFFSET LEVEL OUTPUT (1)	**$D5**	Offset Level Output Bits 15 - 8							
(2)		Offset Level Output Bits 7 - 0							
DECODE LINEAR PCM OUTPUT (1)	**$D6**	Linear PCM Output Signal Bits 15 - 8							
(2)		Linear PCM Output Signal Bits 7 - 0							
DECODE ADM OUTPUT	**$DA**	Decode ADM Output							
ENCODE VAD LEVEL OUTPUT (1)	**$E4**	Voice Activity Detector Level Output Bits 15 - 8							
(2)		Voice Activity Detector Level Output Bits 7 - 0							
ENCODE OFFSET LEVEL OUTPUT (1)	**$E5**	Offset Level Output Bits 15 - 8							
(2)		Offset Level Output Bits 7 - 0							

REGISTER NAME	HEX ADDRESS/ COMMAND	BIT 7 (D7)	BIT 6 (D6)	BIT 5 (D5)	BIT 4 (D4)	BIT3 (D3)	BIT 2 (D2)	BIT 1 (D1)	BIT 0 (D0)
ENCODE LINEAR PCM OUTPUT (1)	**$E6**	Linear PCM Output Signal Bits 15 - 8							
(2)		Linear PCM Output Signal Bits 7 - 0							
ENCODE ADM OUTPUT	**$EA**	Encode ADM Output							

5.2.1 Write Only Register Description

5.2.1.1 GENERAL RESET ($01)

The reset command has no data attached to it. Application of the GENERAL RESET sets all write only register bits to 0.

5.2.1.2 AAF/AIF BANDWIDTH Register ($61)

AAF Bypass (Bit 7) When this bit is set to logic 1 the anti-alias filter is bypassed.

AAF Bandwidth (Bits 6 – 4) The –3dB cutoff frequency of the anti-alias filter is controlled by bits 4 – 6. The filter shape is not altered other than to move the cutoff frequency.

Bit 6	Bit 5	Bit 4	-3dB Frequency
0	0	0	2.9kHz
0	0	1	3.7kHz
0	1	0	5.0kHz
0	1	1	7.0kHz
1	0	0	10.0kHz
1	0	1	14.0kHz

AIF Bypass (Bit 3) When this bit is set to a logic 1 the anti-image filter is bypassed.

AIF Bandwidth (Bits 2 – 0) The –3dB cutoff frequency of the anti-image filter is controlled by bits 0-2. The filter shape is not altered other than to move the cutoff frequency.

Bit 2	Bit 1	Bit 0	-3dB Frequency
0	0	0	2.9kHz
0	0	1	3.7kHz
0	1	0	5.0kHz
0	1	1	7.0kHz
1	0	0	10.0kHz
1	0	1	14.0kHz

5.2.1.3 VOLUME/SIDETONE LEVEL Register ($62)

Volume Level (Bits 7 – 3) The five most significant bits in this register are used to set the gain of the volume control according to the table below:

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Increment Per Step = 1.5dB Steps
0	0	0	0	0	Off
0	0	0	0	1	-33.0dB
0	0	0	1	0	-31.5dB
0	0	0	1	1	-30.0dB
0	0	1	0	0	-28.5dB
0	0	1	0	1	-27.0dB
0	0	1	1	0	-25.5dB
0	0	1	1	1	-24.0dB
0	1	0	0	0	-22.5dB
0	1	0	0	1	-21.0dB
0	1	0	1	0	-19.5dB
0	1	0	1	1	-18.0dB
0	1	1	0	0	-16.5dB
0	1	1	0	1	-15.0dB
0	1	1	1	0	-13.5dB
0	1	1	1	1	-12.0dB
1	0	0	0	0	-10.5dB
1	0	0	0	1	-9.0dB
1	0	0	1	0	-7.5dB
1	0	0	1	1	-6.0dB
1	0	1	0	0	-4.5dB
1	0	1	0	1	-3.0dB
1	0	1	1	0	-1.5dB
1	0	1	1	1	0.0dB
1	1	0	0	0	1.5dB
1	1	0	0	1	3.0dB
1	1	0	1	0	4.5dB
1	1	0	1	1	6.0dB
1	1	1	0	0	7.5dB
1	1	1	0	1	9.0dB
1	1	1	1	0	10.5dB
1	1	1	1	1	12.0dB

Sidetone Level (Bits 2 – 1) These bits control the gain of the sidetone signal coming from the AAF output to be summed in with the decode signal at the input to the AIF.

Bit 2	Bit 1	Gain Setting
0	0	0dB
0	1	-9dB
1	0	-15dB
1	1	-21dB

Sidetone Enable (Bit 0) When this bit is a logic 1 the sidetone path is enabled with the gain setting controlled as shown above. When this bit is logic 0 the sidetone path is disabled.

5.2.1.4 AUDIO INPUT LEVEL CONTROL Register ($63)

Audio Input Level Control (Bits 7 – 3)

These bits are used to set the gain of the Digitally Controlled Amplifier (DCA) at the output of the microphone amplifier.

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Audio Input Gain
0	0	0	0	0	Off
0	0	0	0	1	-7.5dB
0	0	0	1	0	-7.0dB
0	0	0	1	1	-6.5dB
0	0	1	0	0	-6.0dB
0	0	1	0	1	-5.5dB
0	0	1	1	0	-5.0dB
0	0	1	1	1	-4.5dB
0	1	0	0	0	-4.0dB
0	1	0	0	1	-3.5dB
0	1	0	1	0	-3.0dB
0	1	0	1	1	-2.5dB
0	1	1	0	0	-2.0dB
0	1	1	0	1	-1.5dB
0	1	1	1	0	-1.0dB
0	1	1	1	1	-0.5dB
1	0	0	0	0	0.0dB
1	0	0	0	1	0.5dB
1	0	0	1	0	1.0dB
1	0	0	1	1	1.5dB
1	0	1	0	0	2.0dB
1	0	1	0	1	2.5dB
1	0	1	1	0	3.0dB
1	0	1	1	1	3.5dB
1	1	0	0	0	4.0dB
1	1	0	0	1	4.5dB
1	1	0	1	0	5.0dB
1	1	0	1	1	5.5dB
1	1	1	0	0	6.0dB
1	1	1	0	1	6.5dB
1	1	1	1	0	7.0dB
1	1	1	1	1	7.5dB

Reserved (Bits 2– 0)

These bits are reserved and should be set to a logic 0.

5.2.1.5 POWER CONTROL 1 Register ($64)

AAF Power Control (Bit 7)

This bit is reserved and should be set to a logic 0

AAF Power Control (Bit 6)

This bit is dedicated to power/current control for the AAF. Note: It is necessary to keep the power level set to one of the “ON” settings when the AAF is bypassed.

Bit 7	Bit 6	Power Level Setting
0	0	Power down (Off).
0	1	Normal operation.

AIF Power Control (Bit 5) This bit is reserved and should be set to a logic 0.

AIF Power Control (Bit 4) This bit is dedicated to power/current control for the AIF and the Sidetone DCA. Note: It is necessary to keep the power level set to one of the "ON" settings when the AIF is bypassed.

Bit 5	Bit 4	Power Level Setting
0	0	Power down (Off).
0	1	Normal operation.

Encode DAC Power Control (Bits 3 – 2) These bits are dedicated to power/current control for the Encode DAC.

Bit 3	Bit 2	Power Level Setting
0	0	Power down (Off).
0	1	Lowest power (for bit rates less than 32kbps).
1	0	Low power (for bit rates between 32kbps and 64kbps).
1	1	Normal operation (for bit rates greater than 64kbps).

Decode DAC Power Control (Bits 1 – 0) These bits are dedicated to power/current control for the Decode DAC.

Bit 1	Bit 0	Power Level Setting
0	0	Power down (Off).
0	1	Lowest power (for bit rates less than 32kbps).
1	0	Low power (for bit rates between 32kbps and 64kbps).
1	1	Normal operation (for bit rates greater than 64kbps).

5.2.1.6 POWER CONTROL 2 Register ($65)

MIC AMP Power Control (Bits 7 – 6) These bits are dedicated to power/current control for the Microphone Amplifier.

Bit 7	Bit 6	Power Level Setting
0	0	Power down (Off).
0	1	Lowest power (for audio bandwidths less than 3.3kHz).
1	0	Low power (for bit rates between 3.3kHz and 10kHz).
1	1	Normal operation (for audio bandwidths greater than 10kHz).

AUDIO DCA Power Control (Bits 5 – 4) These bits are dedicated to power/current control for the Audio Input Digitally Controlled Amplfier.

Bit 5	Bit 4	Power Level Setting
0	0	Power down (Off).
0	1	Lowest power (for audio bandwidths less than 3.3kHz).
1	0	Low power (for audio bandwidths between 3.3kHz and 10kHz).
1	1	Normal operation (for audio bandwidths greater than 10kHz).

VOLUME DCA Power Control (Bits 3 – 2)

These bits are dedicated to power/current control for the Volume Digitally Controlled Amplifier.

Bit 3	Bit 2	Power Level Setting
0	0	Power down (Off).
0	1	Lowest power (for bit rates less than 32kbps).
1	0	Low power (for bit rates between 32kbps and 64kbps).
1	1	Normal operation (for bit rates greater than 64kbps).

XTAL Power Save (Bit 1)

When this bit is a logic 1 the one-pin crystal oscillator circuit is powered down.

ANALOG Enable (Bit 0)

When this bit is set to a logic 1 all of the analog circuitry (register $64 and bits 7-2 of register $65) is enabled. When this bit is set to a logic 0 all of the analog circuitry is powered down (on-chip bandgap reference is powered down). This is equivalent to setting all of the bits of register $64 and bits 7-2 of register $65 to a logic 0. So to enable the AAF pabk, register $64 bit 6 and register $65 bit 0 must both be set to logic 1. Note that these bits control power to their respective blocks and that a signal path may still exist even if the block is powersaved.

5.2.1.7 CODEC MODE CONTROL Register ($70)

Reserved (Bits 7 – 3)

These bits are reserved and should be set to a logic 0.

CODEC MODE (Bits 2 – 0)

Bit 2	Bit 1	Bit 0	CODEC Mode
0	0	0	ADM mode without buffered I/O
0	0	1	ADM mode with buffered I/O
0	1	0	Linear PCM with buffered I/O
0	1	1	µ-law PCM with buffered I/O
1	0	0	A-law PCM with buffered I/O

5.2.1.8 SCRAMBLER CONTROL Register ($71)

Scrambler Enable (Bit 15)

Setting this bit to a logic 1 enables the scrambler.

Reserved (Bit 14)

Reserved for future use. Set to '0'.

Scrambler Output Invert (Bit 13)

Setting this bit to a logic 1 inverts the scrambler output polarity.

De-Scrambler Enable (Bit 12)

Setting this bit to a logic 1 enables the de-scrambler.

Reserved (Bit 11) Reserved for future use. Set to '0'.

De-Scrambler Input Invert. (Bit 10) Setting this bit to a logic 1 inverts the de-scrambler input polarity.

LFSR Tap Select (Bits 9 – 0) These bits directly program the polynomial for the scrambler and de-scrambler:
$PR = B9X^9 + B8X^8 + B7X^7 + B6X^6 + B5X^5 + B4X^4 + B3X^3 + B2X^2 + B1X^1 + B0X^0$

5.2.1.9 CLK DIVIDER CONTROL Register ($72)

Pre-Scaler Enable (Bit 15) Setting this bit to a logic 1 enables the pre-scaler divider.

Decode Bit Clock Enable (Bit 14) Setting this bit to a logic 1 enables the decode bit clock.

Encode Bit Clock Enable (Bit 13) Setting this bit to a logic 1 enables the encode bit clock.

5.2.1.8 SCRAMBLER CONTROL Register ($71)

Filter Clock Pre-Scaler (Bits 12 – 11) These bits control the internal switched capacitor (SC) filter clock pre-scaler.

Bit 12	Bit 11	Divider Ratio
0	0	1
0	1	2
1	0	3
1	1	4

Filter Clock Divider (Bits 10 – 8) These bits control the internal switched capacitor filter clock divider.

Bit 10	Bit 9	Bit 8	Divider Ratio
0	0	0	2.000
0	0	1	8.000
0	1	0	15.500
0	1	1	15.750
1	0	0	16.000
1	0	1	22.000
1	1	0	31.250
1	1	1	46.750

Bit Clock Pre-Scaler (Bits 7 – 6)

These bits control the bit clock pre-scaler.

Bit 7	Bit 6	Divider Ratio
0	0	1
0	1	2
1	0	3
1	1	4

Decode Bit Clock Divider (Bits 5 – 3)

These bits control the decode bit clock divider.

Bit 5	Bit 4	Bit 3	Divider Ratio
0	0	0	1.000
0	0	1	2.000
0	1	0	2.250
0	1	1	2.625
1	0	0	3.000
1	0	1	3.125
1	1	0	3.375
1	1	1	3.500

Encode Bit Clock Divider (Bits 2 – 0)

These bits control the encode bit clock divider.

Bit 2	Bit 1	Bit 0	Divider Ratio
0	0	0	1.000
0	0	1	2.000
0	1	0	2.250
0	1	1	2.625
1	0	0	3.000
1	0	1	3.125
1	1	0	3.375
1	1	1	3.500

The CLK DIVIDER CONTROL Register should be programmed to provide a 256kHz nominal SC filter clock. Programming the SC filter clock to different frequencies will introduce a proportionate frequency shift in the configured anti-alias/image SC filter frequency responses. See also section 6.3.

The audio filter clock divider should be programmed to set the audio filter clock as near as possible to 256kHz, via selection of the XTAL frequency and the Filter Prescaler and Filter Divider settings.

The encoder and decoder ADM bit rate clocks should be programmed to the desired ADM bit rate or PCM sample rate, multiplied by the interpolation/decimation setting of the PCM filter. The PCM filter can be programmed to run at either 4x or 8x the PCM sample rate depending on the corresponding setting in the encode/decode processors.

The encoder and decoder ADM bit rate clocks are further divided by a constant factor of 64 (unless the PLL is enabled in which case the average is near 64 but can pull off slightly depending on the reference source).

5.2.1.10 CLK SOURCE CONTROL Register ($73)

Reserved (Bits 15-14) These bits are reserved and should be set to a logic 0.

Phase Detect Input Select (Bit 13)
0 = PLL locks to external input clock
1 = PLL locks to external input strobe.

(Bit 12)
0 = PLL locks to data edges.
1 = PLL locks to external clock or strobe edges according to Bit 13 value.

Reserved (Bits 11-10) These bits are reserved and should be set to a logic 0.

TX Data Pad Tri-State control (Bit 9)
0=TX DATA pin always driven by device.
1=in buffered I/O mode the TX DATA pin is driven only when valid data is present after the strobe pulse.

Reserved (Bit 8) This bit is reserved and should be set to a logic 0.

PLL Enable (Bit 7) Setting this bit to a logic 1 enables the phase locked loop in the clock recover circuit. When the PLL is enabled the decoder ADM bit clock adjusts its phase in increments of 1/32 of the programmed period to minimise noise due to timing jitter. Setting this bit to a logic 0 free-wheels the post divide by 64 decode clock divider and thus produces a bit clock which is synchronised to the XTAL/CLK input.

Decode Bit Clock Select (Bit 6) Setting this bit to a logic 1 selects the bit clock generated by the clock recovery circuit. Setting this bit to a logic 0 selects a bit clock externally applied to the RX CLK pin.

Encode Bit Clock Select (Bits 5 – 4) These bits allow for the selection of three different sources for the encode bit clock.

Bit 5	Bit 4	Encode Bit Clock
X	0	External Tx Clock Pin.
0	1	Internally Generated encode clock.
1	1	Internally Generated from decode clock.

Note that a system clock or crystal is always required on the XTAL/CLK pin, in order to generate the various internal timing signals, even when Rx and Tx Clocks are recovered from the RX DATA pin.

Data Filter Bypass (Bit 3) Setting this bit to a logic 1 bypasses the data filter and inputs the RX DATA signal directly into the data slicer.

Data Filter and Slicer Power Control (Bits 2 – 1)

These bits are dedicated to power/current control for the data filter and slicer.

Bit 2	Bit 1	Power Level Setting
0	0	Power down (Off).
0	1	Lowest power (for bit rates less than 32kbps).
1	0	Low power (for bit rates between 32kbps and 64kbps).
1	1	Normal operation (for bit rates greater than 64kbps).

When the Data Filter and Slicer are powered off, the RX DATA input pin signal must conform to logic level amplitudes. When operating the device in buffered I/O modes, the Data Filter and Slicer should be powered off.

Data Filter Bandwidth (Bit 0)

Setting this bit to a logic 1 forces the data filter to narrow bandwidth mode.

5.2.1.11 CODEC INTERRUPT CONTROL Register ($81)

Encoder Control (Bits 7 – 4)

Bit 7	Bit 6	Bit 5	Bit 4	Encoder Setting
0	X	X	X	Encoder is disabled and reset.
1	0	0	0	Encoder is enabled to run without generating IRQs.
1	1	X	X	Encoder is enabled and will generate IRQs to indicate VAD status changes.
1	X	1	X	Encoder is enabled and will generate periodic IRQs to indicate whether PCM data is available or needed when transcoding.
1	X	X	1	Encoder is enabled and will generate periodic IRQs to indicate whether ADM data is available or needed when transcoding.

Decoder Control (Bits 3 – 0)

Bit 3	Bit 2	Bit 1	Bit 0	Decoder Setting
0	X	X	X	Decoder is disabled and reset.
1	0	0	0	Decoder is enabled to run without generating IRQs.
1	1	X	X	Decoder is enabled and will generate IRQs to indicate VAD status changes.
1	X	1	X	Decoder is enabled and will generate periodic IRQs to indicate whether the PCM data is needed or available when transcoding.
1	X	X	1	Decoder is enabled and will generate periodic IRQs to indicate whether the ADM data is needed or available when transcoding.

5.2.1.12 DECODER MODE AND SETUP Register ($D0)

Decimation Rate (by 4/8) (Bit 15)

The decoder PCM filter functions as an interpolator for the DAC when PCM words are being received by the decoder and as a decimator when the decoder is receiving delta modulation. In the case where delta modulation is received, transcoded PCM values are available in the DECODE LINEAR PCM OUTPUT Register ($D6) at the decimation rate. When PCM is received the device can be set to transcode to an ADM stream available in the DECODE ADM OUTPUT Register ($DA) at the interpolated rate. A logic 1 sets the interpolation (decimation) rate to 4 ($1/4^{th}$ the bit rate). A logic 0 sets the interpolation (decimation) rate to 8 ($1/8^{th}$ the bit rate).

PCM Input Select (Bits 14 – 13)

Allows selection of the input to the PCM rate converting filter.

Bit 14	Bit 13	Selected PCM Input
0	X	PCM filter decimates ADM estimator output. PCM words available in register $D6.
1	0	PCM filter interpolates linear PCM input from burst mode interface (RX DATA pin). This selection must be made in conjunction with the CODEC MODE CONTROL Register ($70). Note that the burst interface expands μLaw or Alaw signals to linear PCM prior to the PCM filter.
1	1	PCM filter interpolates linear PCM input from C-BUS interface via the DECODE LINEAR PCM INPUT Register ($D7).

If PCM filter interpolates, the decoder can digitally transcode a PCM signal to ADM.
If PCM filter decimates, the decoder can digitally transcode an ADM signal to PCM.

ADM Input Select (Bits 12 – 11)

Bit 12	Bit 11	Selected ADM Input
0	0	ADM decoder input from the RX DATA pin. (Normal mode operation).
0	1	ADM decoder gets input from C-BUS via the DECODE ADM INPUT Register ($D8). This could be used to force in an idle pattern or to play out an arbitrary stored signal. (Alternate ADM input operation).
1	X	ADM input from digital feedback. When ADM input comes from digital feedback it will transcode from PCM to ADM. PCM filter must be set to interpolate. In this mode the analog interface can be powered down since all signal processing is done digitally. (PCM to ADM transcoding input operation).

Decoder Output Select (Bits 10 – 9)

Bit 10	Bit 9	Selected Decoder Output
0	0	ADM estimator output drives decoder output.
0	1	ADM estimator output summed with PCM interpolation filter output drives decoder output. The ADM and PCM signals can be input from any combination of RX DATA pin and C-BUS input registers.
1	0	Direct PCM test mode.
1	1	Interpolated PCM output.

Reserved (Bit 8) This bit is reserved and should be set to a logic 0.

Decoder VAD Decay Time Constant (Bits 7 – 5) Allows selection of the Voice Activity Detector decay time constant.

Bit 7	Bit 6	Bit 5	Decay Time Constant (ms), Bit Rate in kbps
0	0	0	128/(Bit Rate)
0	0	1	256/(Bit Rate)
0	1	0	512/(Bit Rate)
0	1	1	1024/(Bit Rate)
1	0	0	2048/(Bit Rate)
1	0	1	4096/(Bit Rate)
1	1	0	8192/(Bit Rate)
1	1	1	16384/(Bit Rate)

Decoder VAD Attack Time Constant (Bits 4 – 3) Allows selection of the Voice Activity Detector attack time constant.

Bit 4	Bit 3	Attack Time Constant (ms)
0	0	(VAD Decay Time Constant)/4
0	1	(VAD Decay Time Constant)/8
1	0	(VAD Decay Time Constant)/16
1	1	(VAD Decay Time Constant)/32

Decoder VAD Output Source (Bits 2 – 1) Allows selection of the Voice Activity Detector output source.

Bit 2	Bit 1	VAD Output
0	0	Normal VAD operation.
0	1	ADM bits are driven over VAD pin at the ADM bit rate (may be useful when transcoding or verifying proper application of the burst interface).
1	0	VAD output driven to 0.
1	1	VAD output driven to 1.

Reserved (Bit 0) This bit is reserved and should be set to a logic 0.

5.2.1.13 DECODE ADM CONTROL Register ($D1)

Syllabic Time Constant (Bits 15 – 13) Step size integrator Loss Coefficient: allows selection of syllabic time constant.

Bit 15	Bit 14	Bit 13	Syllabic Filter Time Constant (ms)
0	0	0	512/(3*Bit Rate)
0	0	1	768/(3*Bit Rate)
0	1	0	1024/(3*Bit Rate)
0	1	1	1536/(3*Bit Rate)
1	0	0	2048/(3*Bit Rate)
1	0	1	3072/(3*Bit Rate) Bluetooth compatible when running at 64kbps.
1	1	0	4096/(3*Bit Rate)
1	1	1	6144/(3*Bit Rate)

Dynamic Range for Step Size Integrator (Bits 12 – 10)

Maximum and minimum step size are based on 16-bit word length (-32768 to 32767).

Bit 12	Bit 11	Bit 10	Maximum Step	Minimum Step
0	0	0	10240	20
0	0	1	10240	10
0	1	0	5120	20
0	1	1	5120	10
1	0	0	2560	20
1	0	1	2560	10
1	1	0	1280	20
1	1	1	1280	10 Bluetooth compatible when running at 64kbps.

Companding Rule (Bits 9 – 8)

This is the number of consecutive ones or zeros that must occur for the step size to be adjusted.

Bit 9	Bit 8	Companding Rule
0	0	3 of 3
0	1	4 of 4 Bluetooth compatible when running at 64kbps.
1	0	5 of 5
1	1	6 of 6

Estimator Integrator Time Constant (Bits 7 – 5)

Allows selection of the estimator integrator time constant.

Bit 7	Bit 6	Bit 5	Decay Time Constant (ms)
0	0	0	16/(3*Bit Rate)
0	0	1	24/(3*Bit Rate)
0	1	0	32/(3*Bit Rate)
0	1	1	48/(3*Bit Rate)
1	0	0	64/(3*Bit Rate)
1	0	1	96/(3*Bit Rate) Bluetooth compatible when running at 64kbps.
1	1	0	128/(3*Bit Rate
1	1	1	192/(3*Bit Rate)

Second Order Estimator Time Constant (Bits 4 – 3)

Allows selection of the second order estimator time constant.

Bit 4	Bit 3	Time Constant (ms), Bit Rate in kbps
0	0	N/A (selects first order estimator).
0	1	(Estimator Time Constant)/2
1	0	(Estimator Time Constant)/4
1	1	(Estimator Time Constant)/8

Zero Selection (Bits 2 – 1)

When second order integration is used, a zero can be inserted to help encoder stability. Not generally used in the decoder unless set to digitally transcode from PCM to ADM.

Bit 2	Bit 1	Time Constant (ms), Bit Rate in kbps
0	0	N/A (select for first order estimator).
0	1	1.5/Bit Rate
1	0	2.5/Bit Rate
1	1	4.5/Bit Rate

Zero at ½ Bit Rate (Bit 0)

When decoding ADM, a zero at (bit rate)/2 can be enabled by setting this bit to logic 1. When transcoding from PCM to ADM this bit should always be set to logic 0 to avoid instability in the transcoding loop.

5.2.1.14 DECODE VAD THRESHOLD Register ($D2)

Decode VAD Threshold (Bits 15 – 0)

These bits directly program the threshold of detection for the Voice Activity Detector. The number programmed into this register can range from $0 to $7FFF (0 to 32767). The equation for the VAD threshold is:

$$\text{Register Value} = \frac{(\text{Signal Detection Threshold}) \cdot 2^{15}}{(\text{DAC Full Scale Reference Voltage})}$$

5.2.1.15 DECODE OFFSET LEVEL Register ($D3)

Decode Offset Input (Bits 15 – 0)

For normal Decoder operation this register should be set to logic 0.

These bits allow for an offset amount to be directly programmed. This offset amount is useful in trimming out offsets that may occur in the on-chip analog circuitry. The number format is 2's complement and ranges from $8000 through $0000 to $7FFF (-32768 to 32767).

The equation for the Offset value is:

$$\text{Register Value} = \frac{(\text{Offset Voltage}) \cdot 2^{18}}{(\text{DAC Full Scale Reference Voltage})}$$

The programmed offset will be summed with the decoder output signal.

5.2.1.16 DECODE LINEAR PCM INPUT Register ($D7)

Decode Linear PCM Input (Bits 15 – 0)

This register allows input of linear PCM via C-BUS for transcoding. The number format is 2's complement and ranges from $8000 through $0000 to $7FFF (-32768 to 32767). Bit 1 of the CODEC INTERRUPT CONTROL Register ($81) can be set to a logic 1 to enable interrupts informing a micro-controller when the register should be updated.

5.2.1.17 DECODE ADM INPUT Register ($D8)

Decoder ADM Input (Bits 7 – 0)

This register allows ADM bits to be written into the decoder via C-BUS and is intended for transcoding. Bit 0 of the CODEC INTERRUPT CONTROL Register ($81) can be set to a logic 1 to enable interrupts informing a micro-controller when the register should be updated. Additionally this register can be loaded with an idle data pattern ($55 or $AA) and then selected as the input to the decoder via the DECODER MODE AND SETUP Register ($D0).

5.2.1.18 ENCODER MODE AND SETUP Register ($E0)

Decimation Rate (by 4/8) (Bit 15)

The encoder PCM filter functions as a decimating lowpass when the encoder is running. PCM values are available in the ENCODE LINEAR PCM OUTPUT Register ($E6) at the decimation rate. A logic 1 sets the decimation rate to 4 (1/4th the bit rate). A logic 0 sets the decimation rate to 8 (1/8th the bit rate).

PCM Input Select (Bits 14 – 13)

Allows selection of the input to the PCM rate converting filter.

Bit 14	Bit 13	Selected PCM Input
0	X	PCM filter decimates ADM estimator output PCM words available in register $E6.
1	0	PCM filter interpolates PCM input from burst mode interface (RX DATA pin). This selection must be made in conjunction with the CODEC MODE CONTROL Register ($70).
1	1	PCM filter interpolates PCM input from C-BUS interface via the ENCODE DAC TEST CONTROL Register ($E7).

If PCM filter is interpolating, the encoder can transcode a PCM signal to ADM.
If PCM filter is decimating, the encoder will transcode an ADM signal to PCM.

ADM Input Select (Bits 12 – 11)

Bit 12	Bit 11	Selected ADM Input
0	0	ADM encoder input from Comparator. (Normal mode operation).
0	1	ADM encoder gets input from C-BUS breaking the feedback loop and allowing the local decoder to digitally transcode an ADM signal input via C-BUS to a PCM signal output via C-BUS or the burst interface. (Alternate ADM input operation).
1	X	ADM input from transcode feedback. When ADM input comes from transcode feedback it will transcode from PCM to ADM. The PCM filter must be set to interpolate. In this mode the encode analog interface can be powered down since it is not used. (PCM to ADM transcoding input operation).

Local Decoder Output Select (Bits 10 – 9)

Bit 10	Bit 9	Selected Local Decoder Output
0	0	ADM estimator output drives local decoder output.
0	1	ADM estimator output summed with PCM interpolation filter output drives local decoder output. For encoder, ADM output tracks sum of MIC input analog signal plus a PCM signal input over the C-BUS interface.
1	0	Direct PCM test mode.
1	1	Interpolated PCM output.

Idle Channel Enhance (Bit 8)

This bit improves the perceived low-level sound quality by enabling the automatic tracking of offsets, which reduces internal offset levels. Some increase in harmonic distortion may result from the use of this bit. If automatic compensation is not required, this bit should be set to logic 0 and the ENCODE OFFSET LEVEL Register ($E3) should also be set to logic 0. This bit should normally be set to a logic 1 to allow analog offsets to be automatically compensated.

When running the encoder as a digital ADM to PCM transcoder this bit should be set to 0 since the local ADM decoder runs outside a feedback loop.
When enabling offset compensation, ensure the encoder ADM input selection is set either for feedback from the comparator or for PCM to ADM transcoding. Also load the ENCODE OFFSET LEVEL Register ($E3) with a small positive constant. If transcode feedback is selected then the PCM filter must also be set to interpolate.

Encoder VAD Decay Time Constant (Bits 7 – 5)

These bits allow selection of the Voice Activity Detector decay time constant.

Bit 7	Bit 6	Bit 5	Decay Time Constant (ms), Bit Rate in kbps
0	0	0	128/(Bit Rate)
0	0	1	256/(Bit Rate)
0	1	0	512/(Bit Rate)
0	1	1	1024/(Bit Rate)
1	0	0	2048/(Bit Rate)
1	0	1	4096/(Bit Rate)
1	1	0	8192/(Bit Rate)
1	1	1	16384/(Bit Rate)

Encoder VAD Attack Time Constant (Bits 4 – 3)

Allows selection of the Voice Activity Detector attack time constant.

Bit 4	Bit 3	Attack Time Constant (ms)
0	0	(VAD Decay Time Constant)/4
0	1	(VAD Decay Time Constant)/8
1	0	(VAD Decay Time Constant)/16
1	1	(VAD Decay Time Constant)/32

Encoder VAD Output Source (Bits 2 – 1)

Allows selection of the Voice Activity Detector output source.

Bit 2	Bit 1	VAD Output
0	0	Nominal VAD operation.
0	1	ADM bits are driven over VAD pin at the ADM bit rate (may be useful when transcoding or verifying proper application of the burst interface).
1	0	VAD output driven to 0.
1	1	VAD output driven to 1.

ADM Output Select (Bit 0)

For normal operation this bit should be set to a logic 0. Setting this bit to a logic 1 allows arbitrary ADM streams, written in via the ENCODE ADM INPUT Register ($E8), to be output. For example to force the encoder to output an idle pattern 010101… while running, regardless of the input analog waveform, write $55 into register $E8 and set this bit to a logic 1.

5.2.1.19 ENCODE ADM CONTROL Register ($E1)

Syllabic Time Constant (Bits 15 – 13)

Step size integrator Loss Coefficient: allows selection of syllabic time constant.

Bit 15	Bit 14	Bit 13	Syllabic Filter Time Constant (ms), Bit Rate in kbps
0	0	0	512/(3*Bit Rate)
0	0	1	768/(3*Bit Rate)
0	1	0	1024/(3*Bit Rate)
0	1	1	1536/(3*Bit Rate)
1	0	0	2048/(3*Bit Rate)
1	0	1	3072/(3*Bit Rate) Bluetooth compatible when running at 64kbps.
1	1	0	4096/(3*Bit Rate)
1	1	1	6144/(3*Bit Rate)

Dynamic Range for Step Size Integrator

Numbers given for maximum and minimum step size are based on 16-bit word length (-32768 to 32767).

Step Size Integrator (Bits 12 – 10)

Bit 12	Bit 11	Bit 10	Maximum Step	Minimum Step
0	0	0	10240	20
0	0	1	10240	10
0	1	0	5120	20
0	1	1	5120	10
1	0	0	2560	20
1	0	1	2560	10
1	1	0	1280	20
1	1	1	1280	10 Bluetooth compatible when running at 64kbps.

Companding Rule (Bits 9 – 8)

This is the number of consecutive ones or zeros that must occur for the step size to be adjusted.

Bit 9	Bit 8	Companding Rule
0	0	3 of 3
0	1	4 of 4 Bluetooth compatible when running at 64kbps.
1	0	5 of 5
1	1	6 of 6

Estimator Integrator Time Constant (Bits 7 – 5)

Allows selection of the estimator integrator time constant.

Bit 7	Bit 6	Bit 5	Decay Time Constant (ms), Bit Rate in kbps
0	0	0	16/(3*Bit Rate)
0	0	1	24/(3*Bit Rate)
0	1	0	32/(3*Bit Rate)
0	1	1	48/(3*Bit Rate)
1	0	0	64/(3*Bit Rate)
1	0	1	96/(3*Bit Rate) Bluetooth compatible when running at 64kbps.
1	1	0	128/(3*Bit Rate
1	1	1	192/(3*Bit Rate)

Second Order Estimator Time Constant (Bits 4 – 3)

Allows selection of the second order estimator time constant.

Bit 4	Bit 3	Loss Factor
0	0	N/A (selects first order estimator).
0	1	(Estimator Time Constant)/2
1	0	(Estimator Time Constant)/4
1	1	(Estimator Time Constant)/8

Zero Selection (Bits 2 – 1)

When second order integration is used, a zero can be inserted to help stability.

Bit 2	Bit 1	Time Constant (ms), Bit Rate in kbps
0	0	N/A (select for first order estimator)
0	1	1.5/Bit Rate
1	0	2.5/Bit Rate
1	1	4.5/Bit Rate

Zero at ½ Bit Rate (Bit 0)

When decoding ADM, a zero at (bit rate)/2 can be enabled by setting this bit to logic 1. When encoding or transcoding from PCM to ADM this bit should always be set to a logic 0 to avoid instability of the ADM feedback loop.

5.2.1.20 ENCODE VAD THRESHOLD Register ($E2)

Encode VAD Threshold (Bits 15 – 0)

These bits directly program the threshold of detection for the Voice Activity Detector. The number programmed into this register can range from $0 to $7FFF (0 to 32767). The equation for the VAD threshold is:

$$\text{Register Value} = \frac{(\text{Signal Detection Threshold}) \cdot 2^{15}}{(\text{DAC Full Scale Reference Voltage})}$$

5.2.1.21 ENCODE OFFSET LEVEL Register ($E3)

Encode Offset Input (Bits 15 - 0)

These bits allow for an offset amount to be directly programmed. This offset amount is useful in trimming out offsets that may occur in the on-chip analog circuitry. The number format is 2's complement and ranges from $8000 through $0000 to $7FFF (-32768 to 32767).

The equation for the direct offset value is:

$$\text{Register Value} = \frac{(\text{Offset Voltage}) \cdot 2^{18}}{(\text{DAC Full Scale Reference Voltage})}$$

For normal Encoder operation this register should be loaded with a small positive constant (eg in the range [2-16]) and bit 8 of the ENCODER MODE AND SETUP Register ($E0) should be set to logic 1. The programmed offset will be summed with the encoder input signal. If offset compensation is not required, bit 8 of the register $E0 should be set to logic 0 and the ENCODE OFFSET LEVEL Register should also be set to logic 0.

Offset compensation can be suspended by loading this register with 0 while leaving Bit 8 of register $E0 true. This holds the current offset estimate constant. The offset estimate can be read out via the ENCODE OFFSET LEVEL OUTPUT Register ($E5).

5.2.1.22 ENCODE DAC INPUT Register ($E7)

Encode DAC Input (Bits 15 – 0)	This register allows direct access to the encoder DAC input. The number format is 2's complement and ranges from $8000 through $0000 to $7FFF (-32768 to 32767).

5.2.1.23 ENCODE ADM INPUT TEST Register ($E8)

Encoder ADM Input Test (Bits 7 – 0)	This register allows ADM bits to be written via C-BUS for transcoding from ADM to PCM. An interrupt can be enabled to inform a micro-controller when the register needs reloading.

5.2.2 Read Only Register Description

5.2.2.1 PROCESSOR STATUS READ Register ($80)

Reading this STATUS register clears any pending IRQ. The PCM and ADM data available and data needed flags (bits 5, 4, 1 and 0 respectively) are cleared when the appropriate CBUS register is read (or written), in order to service the IRQ. The VAD detection flags (bits 6 and 2) are constantly updated to indicate the status of voice activity. Any change in state of either flag will cause an IRQ to be generated.

Encoder Status (Bits 7 – 4)
Bit 7 is permanently set to logic 0.
A logic 1 in Bit 6 indicates Voice Activity is detected.
A logic 1 in Bit 5 indicates PCM data is available (or needed when transcoding)
A logic 1 in Bit 4 indicates ADM samples are available (or needed when transcoding).

Decoder Status (Bits 3 – 0)
Bit 3 is permanently set to logic 0.
A logic 1 in Bit 2 indicates Voice Activity is detected.
A logic 1 in Bit 1 indicates PCM data is needed (or available when transcoding).
A logic 1 in Bit 0 indicates ADM samples are needed (or available when transcoding).

5.2.2.2 DECODE VAD LEVEL OUTPUT READ Register ($D4)

Decode VAD Level Output (Bits 15 – 0)
These bits indicate the average amplitude of the envelope of the audio signal. This negative 2's complement number can range from $0 to $8000 (0 to -32768 and can be used to assist in calculating an appropriate value to be programmed into the DECODE VAD THRESHOLD Register ($D2). The equation for the VAD level register value is:

$$\text{Register Value} = \frac{-1 \cdot (\text{Envelope voltage level}) \cdot 2^{15}}{(\text{DAC Full Scale Reference Voltage})}$$

5.2.2.3 DECODE OFFSET LEVEL OUTPUT READ Register ($D5)

Decode Offset Level Output (Bits 15 – 0)
These bits indicate offset level as input by the user in register $D3. The number format is 2's complement and ranges from $8000 through $0000 to $7FFF (-32768 to 32767).

The equation for the offset value is:

$$\text{Register Value} = \frac{(\text{Offset Voltage}) \cdot 2^{18}}{(\text{DAC Full Scale Reference Voltage})}$$

5.2.2.4 DECODE LINEAR PCM OUTPUT READ Register ($D6)

Decode Linear PCM Output (Bits 15 – 0)
This register contains the linear PCM equivalent of the ADM or non-linear PCM input signal. The number format is 2's complement and ranges from $8000 through $0000 to $7FFF (-32768 to 32767). Bit 1 of the CODEC INTERRUPT CONTROL Register ($81) can be set to a logic 1 to enable interrupts, informing a micro-controller when the register has been updated.

The equation for the PCM register value is:

$$\text{Register Value} = \frac{(\text{PCM voltage}) \cdot 2^{15}}{(\text{DAC Full Scale Reference Voltage})}$$

5.2.2.5 DECODE ADM OUTPUT READ Register ($DA)

Decode ADM Output (Bits 7 – 0)

This register allows ADM bits to be read via C-BUS and is updated every eighth bit. Bit 0 of the CODEC INTERRUPT CONTROL Register ($81) can be set to a logic 1 to enable interrupts, informing a micro-controller when the register has been updated. When the decoder is set to transcode from PCM to ADM the ADM bits are available via this register.

5.2.2.6 ENCODE VAD LEVEL OUTPUT READ Register ($E4)

Encode VAD Level Output (Bits 15 – 0)

These bits indicate the average amplitude of the envelope of the audio signal. This negative 2's complement number can range from $0 to $8000 (0 to -32768) and can be used to assist in calculating an appropriate value to be programmed into the ENCODE VAD THRESHOLD Register ($E2).

The equation for the VAD level register value is:

$$\text{Register Value} = \frac{-1 \cdot (\text{Envelope voltage level}) \cdot 2^{15}}{(\text{DAC Full Scale Reference Voltage})}$$

5.2.2.7 ENCODE OFFSET LEVEL OUTPUT READ Register ($E5)

Encode Offset Level Output (Bits 15 – 0)

These bits indicate the offset level as input by the user in register $E3, which is dynamically updated if Idle Channel Enhance is enabled. The number format is 2's complement and ranges from $8000 through $0000 to $7FFF (-32768 to 32767). It can be used as an appropriate value to be programmed into the ENCODE OFFSET LEVEL Register ($E3) if offset compensation will be disabled.

The equation for the offset value is:

$$\text{Register Value} = \frac{(\text{Offset Voltage}) \cdot 2^{18}}{(\text{DAC Full Scale Reference Voltage})}$$

5.2.2.8 ENCODE LINEAR PCM OUTPUT READ Register ($E6)

Encode Linear PCM Output (Bits 15 – 0)

This register containes the linear PCM equivalent of the encoded ADM signal. The number format is 2's complement and ranges from $8000 through $0000 to $7FFF (-32768 to 32767). Bit 5 of the CODEC INTERRUPT CONTROL Register ($81) can be set to a logic 1 to enable interrupts, informing a micro-controller when the register has been updated.

The equation for the PCM register value is:

$$\text{Register Value} = \frac{(\text{PCM voltage}) \cdot 2^{15}}{(\text{DAC Full Scale Reference Voltage})}$$

5.2.2.9 ENCODE ADM OUTPUT READ Register ($EA)

Encode ADM Output Test (Bits 7 – 0)

This register allows Encoder ADM bits to be read via C-BUS and is updated every eighth bit. Bit 4 of the CODEC INTERRUPT CONTROL Register ($81) can be set to a logic 1 to enable interrupts, informing a micro-controller when the register has been updated.

6. Application Notes

6.1 C-BUS Operation

Instructions, status and data are transferred between the CMX649 and the host µC over the C-BUS. Instruction and data transfers to and from the CMX649 consist of an Address/Command (A/C) byte followed by either:

1. a further instruction or
2. 1 or 2 bytes of data (write) or
3. 1 or 2 bytes of status or received data reply (read).

The number of data bytes following an A/C byte is dependent on the value of the A/C byte. The most significant bit of the address or data is sent first. The C-BUS SERIAL_CLOCK input to the CMX649 originates from the host µC.

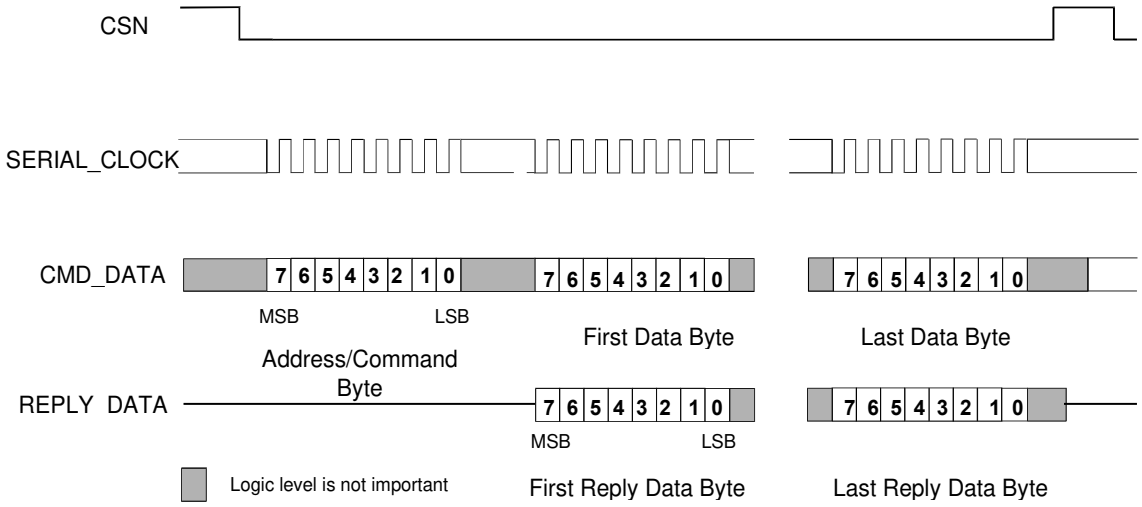


Figure 12 C-BUS Timing Diagram

6.2 CODEC Data Interface

The CMX649 encodes analog audio signals into digital samples, which can be decoded back to analog audio signals. The number of bits per sample is determined by the coding algorithm, which is selected using register $70, CODEC MODE CONTROL. For the ADM coding algorithm, one bit represents one sample and the linear PCM coding algorithm uses 16 bits to represent one sample. The A-law and µ-law PCM algorithms use 8 bits to represent one sample.

The CMX649 CODEC Data Interface is a digital interface responsible for transferring Rx samples into, and Tx samples out of, the device. The interface can be operated in one of two modes: buffered or un-buffered. This selection is made when using the CODEC MODE CONTROL register to choose the coding algorithm.

In burst mode, also called buffered mode, the device will buffer (hold) a data word (either 8 or 16 bits depending on the operating mode) until it is transferred in for processing or out to the listening device. Burst mode requires two timing signals to be furnished by a controlling device: Sync (STRB Pin 1) and Clock (Rx Clk Pin 12). Tx and Rx clocks are tied together internally for burst mode and are driven by the Rx Clk pin. There is only one sync input.

In non-burst mode the device transfers data one bit at a time and only one timing signal is required, Clock. The clock signal can be produced by the CMX649 or supplied by the controlling device. The Tx and Rx clocks can be separate or the same.

The clocking choices of the CMX649 are very flexible. Please refer to the application note: *CMX649 Operation and Application,* for related detail.

Burst Mode

Function	Characteristic	Description
Burst_CLK frequency	5MHz	Maximum Rate Rx Clk, Pin 12
Data word length	8 or 16 bits	
Linear PCM	16 bits	16 bit 2's complement word
A-Law or u-Law	8 bits	One sign bit, a 3-bit exponent and a 4-bit mantissa.
ADM	8 bits	One sample per bit, 8 samples per data word
SYNC Delay	0 Burst CLKs	Continuous Clocking allowed
SYNC Length	1 to (data word length – 1)	Burst Clock Periods
Words (slots) per frame	1	Single sample per slot
Slot start references	from SYNC	STRB, Pin 1

Line	Direction	Start at Clk	Data Transition Edge	Transmission Order	Data Word Length and Byte Order
TX_DATA	Output	1	rise	msb first	8 or 16 bits (m.s. byte first)
RX_DATA	Input	1	rise	msb first	8 or 16 bits (m.s. byte first)

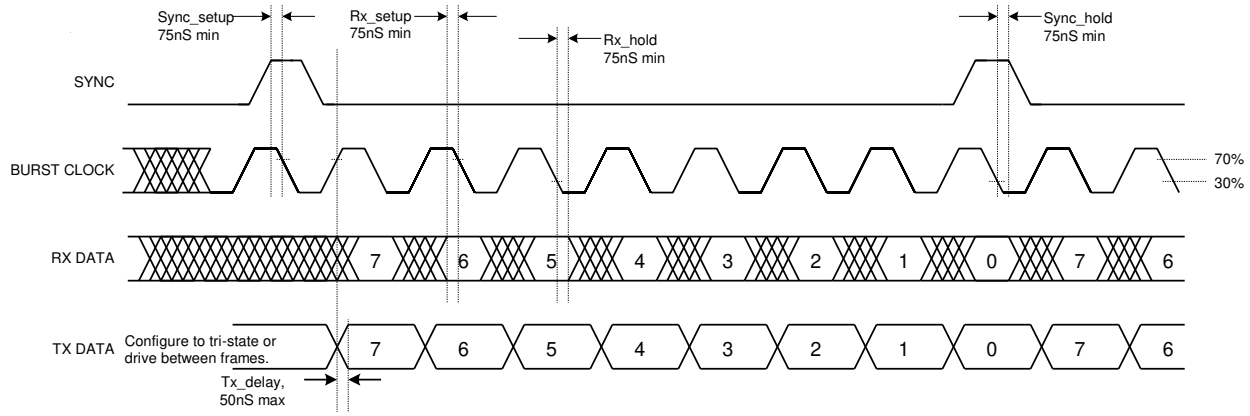


Figure 13 Burst Interface Timing Diagram for Concatenated Byte Transfers

Notes for Figure 13:

- In this example Bit 7 is the most significant bit.
- Once started Rx and Tx data bits are continuously streaming so long as the SYNC pulse continues at the PCM sample rate (for PCM modes) or at 1/8th the data rate for ADM modes.
- Configuration options support some variations of this timing diagram, e.g. data word length, without affecting the timing shown.
- The TX_DATA output may be high impedance between burst frames depending on bit 9 of CLK SOURCE CONTROL Register ($73).
- In ADM mode Data length is 1 bit. Frames are 8 bits in length.

Non-Burst Mode

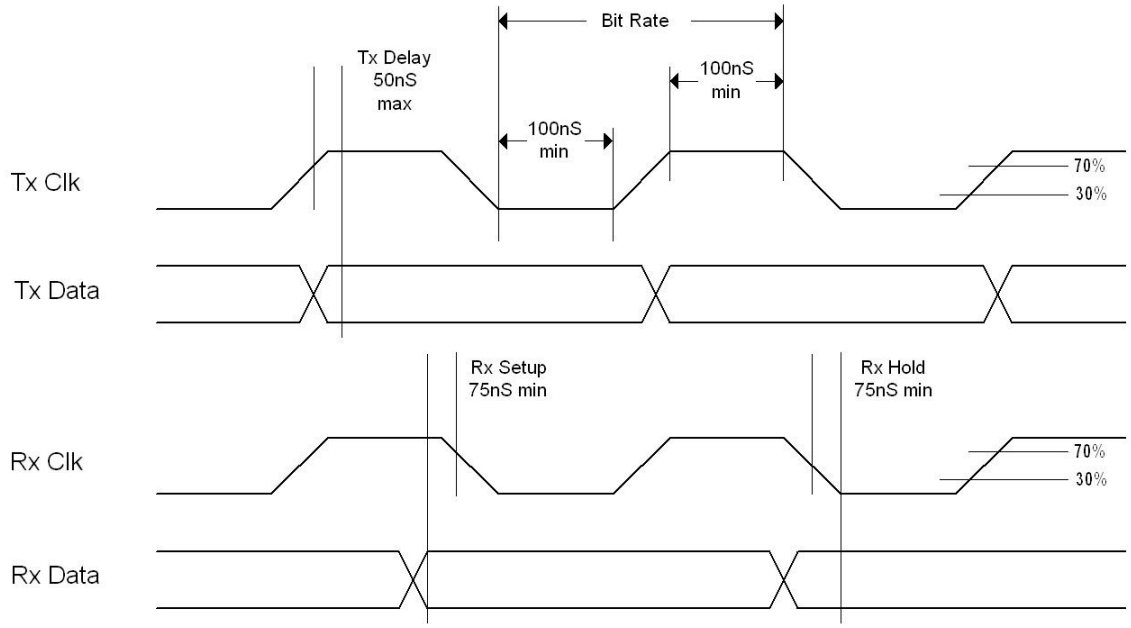


Figure 14 Burst Interface Timing Diagram for Concatenated Byte Transfers

Notes for Figure 14:

- Tx and Rx clocks don't need to be the same rate or phase but the Rx data rate must be at the same rate with which the data was encoded.
- Tx and Rx bit clocks can be internally generated by the CMX649 clock generator section, or they can be supplied from external sources.
- ADM is the only un-buffered mode possible.
- Duty cycle constraints shown for Tx Clk also apply to Rx Clk.

6.3 Example CODEC Setups and Application Help

Below are tabulated some applicable settings for the CLK DIVIDER CONTROL Register ($72). Note that the minimum crystal frequency that can be used is 8.000 MHz, frequencies below this require the use of an external clock source.

Audio Switched Capacitor Filter Clock Settings (clock frequency in kHz) Crystal vs Audio Filter Divider Chart for CMX649 Yielding the Recommended ~256kHz SCF Clock									
		Divider values	8	15.5	15.75	16	22	31.25	47.75
Crystal or external clock Freq MHz	Prescaler Value	Register bits clk ctrl[10:8] \ clk ctrl[12:11]	001	010	011	100	101	110	111
2.048	1	00	256.000						
4	1	00		258.065	253.968				
4.032	1	00			256.000				
4.096	1	00				256.000			
8	1	00						256.000	
8.064	2	01			256.000				
8.192	2	01				256.000			
11.2896	2	01					256.582		
12	1	00							256.684
12.096	3	10			256.000				
12.288	3	10				256.000			
16	2	01						256.000	
16.128	4	11			256.000				
16.384	4	11				256.000			

When selecting divider settings to arrive at a desired bit rate from a given crystal frequency, note that some power savings are realized by selecting a lower divider value in conjunction with a higher prescaler value, thus minimizing the frequency of the prescaler output.

Bit Rate (kbps) Settings with Bit Rate Prescaler = 1 Crystal vs Divider chart for CMX649									
	Divider values	1	2	2.25	2.625	3	3.125	3.375	3.5
Crystal or external clock Freq MHz	Register bits clk ctrl[5:3] [2:0] / clk ctrl[7:6]	000	001	010	011	100	101	110	111
4	00	62.500	31.250	27.778	23.810	20.833	20.000	18.519	17.857
4.032	00	63.000	31.500	28.000	24.000	21.000	20.160	18.667	18.000
4.096	00	64.000	32.000	28.444	24.381	21.333	20.480	18.963	18.286
8	00	125.000	62.500	55.556	47.619	41.667	40.000	37.037	35.714
8.064	00	126.000	63.000	56.000	48.000	42.000	40.320	37.333	36.000
8.192	00	128.000	64.000	56.889	48.762	42.667	40.960	37.926	36.571

Applicable Bit Rate (kbps) Settings with Bit Rate Prescaler = 2 Crystal vs Divider chart for CMX649									
	Divider values	1	2	2.25	2.625	3	3.125	3.375	3.5
Crystal or external clock Freq MHz	Register bits clk ctrl[5:3] [2:0] / clk ctrl[7:6]	000	001	010	011	100	101	110	111
4	01	31.250	15.625						
4.032	01	31.500	15.750						
4.096	01	32.000	16.000						
8	01	62.500	31.250	27.778	23.810	20.833	20.000	18.519	17.857
8.064	01	63.000	31.500	28.000	24.000	21.000	20.160	18.667	18.000
8.192	01	64.000	32.000	28.444	24.381	21.333	20.480	18.963	18.286
11.2896	01	88.200	44.100	39.200	33.600	29.400	28.224	26.133	25.200
12	01	93.750	46.875	41.667	35.714	31.250	30.000	27.778	26.786
12.096	01	94.500	47.250	42.000	36.000	31.500	30.240	28.000	27.000
12.288	01	96.000	48.000	42.667	36.571	32.000	30.720	28.444	27.429
16	01	125.000	62.500	55.556	47.619	41.667	40.000	37.037	35.714
16.128	01	126.000	63.000	56.000	48.000	42.000	40.320	37.333	36.000
16.384	01	128.000	64.000	56.889	48.762	42.667	40.960	37.926	36.571

Applicable Bit Rate (kbps) Settings with Bit Rate Prescaler = 3 Crystal vs Divider chart for CMX649									
Crystal or external clock Freq MHz	Divider values	1	2	2.25	2.625	3	3.125	3.375	3.5
	Register bits clk ctrl[5:3] [2:0] / clk ctrl[7:6]	000	001	010	011	100	101	110	111
4	10	20.833							
4.032	10	21.000							
4.096	10	21.333							
8	10	41.667	20.833	18.519	15.873				
8.064	10	42.000	21.000	18.667	16.000				
8.192	10	42.667	21.333	18.963	16.254				
11.2896	10	58.800	29.400	26.133	22.400	19.600	18.816	17.422	16.800
12	10	62.500	31.250	27.778	23.810	20.833	20.000	18.519	17.857
12.096	10	63.000	31.500	28.000	24.000	21.000	20.160	18.667	18.000
12.288	10	64.000	32.000	28.444	24.381	21.333	20.480	18.963	18.286
16	10	83.333	41.667	37.037	31.746	27.778	26.667	24.691	23.810
16.128	10	84.000	42.000	37.333	32.000	28.000	26.880	24.889	24.000
16.384	10	85.333	42.667	37.926	32.508	28.444	27.307	25.284	24.381

Applicable Bit Rate (kbps) Settings with Bit Rate Prescaler = 4 Crystal vs Divider chart for CMX649									
Crystal or external clock Freq MHz	Divider values	1	2	2.25	2.625	3	3.125	3.375	3.5
	Register bits clk ctrl[5:3] [2:0] / clk ctrl[7:6]	000	001	010	011	100	101	110	111
4	11	15.625							
4.032	11	15.750							
4.096	11	16.000							
8	11	31.250	15.625						
8.064	11	31.500	15.750						
8.192	11	32.000	16.000						
11.2896	11	44.100	22.050	19.600	16.800				
12	11	46.875	23.438	20.833	17.857	15.625	15.000		
12.096	11	47.250	23.625	21.000	18.000	15.750	15.120		
12.288	11	48.000	24.000	21.333	18.286	16.000	15.360		
16	11	62.500	31.250	27.778	23.810	20.833	20.000	18.519	17.857
16.128	11	63.000	31.500	28.000	24.000	21.000	20.160	18.667	18.000
16.384	11	64.000	32.000	28.444	24.381	21.333	20.480	18.963	18.286

6.3.1 32kbps ADM with clock and data recovery

```
//Initialize device with general reset
// This powers down everything excluding the xtal oscillator circuit
$01
//Setup analog section
// $61 00 filters set for 2.9kHz BW (default after reset)
// volume=0dB side_tone=-21dB and off
$62 $BE
// audio_level=0dB
$63 $80
// power_control everything on (lowest current setting)
$64 $55
$65 $55
// codec mode
// default $70 $00 ADM unbuffered (continuous bit serial mode)
// Clock Divider Control
// using 8.192MHz master clock
// filter clock prescale/=4 main divider/=8 => 256kHz SCF clock
// bit clock prescale/=4 encode and decode bit dividers/=1 since constant divider/=64 => 32kbps
$72 $F9 $C0
// PLL is off, Bypass PLL Data Filter and Power it Down
// Internal Decode and Encode clocks from
// Decode internal clock
$73 $00 $78
// setup decoder
// decimate by 8
// decode adm input from RX Data
// adm estimator drives output
// vad attack tc=4ms and decay tc=128ms
// normal vad outputs
$D0 $00 $B8
// adm encode feedback from comparator, nulling for improved idle - otherwise as decoder
$E0 $01 $B8
// to enable offset nulling load small positive constant into encoder offset input reg
$E3 $00 $04
// adm mode syllabic tc=16ms
// step size dynamic range 5120/10
// companding rule = 4 of 4
// principal tc=0.33ms
// second order tc=0.083ms
// encoder zero tc=0.047ms decoder zero tc=N/A
// decoder zero at 16kHz i.e. bit_rate/2 enabled
$D1 $6D $51
$E1 $6D $52
// vad thresholds ~20mv
$D2 $02 $00
$E2 $02 $00
// prime idle pattern into CBUS ADM source byte regs
$D8 $AA
$E8 $AA
//Scrambler and Descrambler both on, using polynomial $14 (5 bit LFSR)
$71 $90 $14
// enable encoder and decoder with no IRQs
$81 $88
// note some useful register changes from the above settings
// force encoder to output an idle pattern ($E0 $81 $B9) (requires $E8 $AA above)
// force decoder to idle via idling its input ($D0 $88 $B8) (requires $D8 $AA above)
// force decoder to mute output via direct PCM out ($D0 $86 $B8) (reset default has $D7 $00 $00)
// turn Scrambler and Descrambler off ($71 $00 $00)
// To Make PLL run with input from data pad
// internal RX and TX clocks
// RX data input acting as analog input i.e. data filter and data slicer running
// ($73 $00 $D2)
```

6.3.2 64kbps burst mode Bluetooth Compatible CVSD

```
//Initialize device with general reset
// This powers down everything excluding the xtal oscillator circuit
$01
//Setup analog section
// $61 00 filters set for 2.9kHz BW (default after reset)
// volume=0dB side_tone=-21dB and on
$62 $BF
// audio_level=0dB
$63 $80
// power_control everything on (lowest current setting)
$64 $55
$65 $55
// codec mode ADM buffered (burst bytes at 1/8 bit rate mode)
$70 $01
// Clock Divider Control
// with 8.192MHz master clock
// filter clock prescale/=4 main divider/=8 => 256kHz SCF clock
// bit clock prescale/=2 main divider/=1 since constant divider/=64 always => 64kHz bit clocks
$72 $F9 $40
// PLL is not running
// internal RX and TX bit clocks both from RX bit clock
// RX data input acting as digital input for burst mode
$73 $00 $70
// setup decoder
// decimate by 8
// decode adm input from RX Data
// adm estimator drives output
// decode vad driven by adm bits at bit rate
$D0 $00 $02
// adm encode feedback from comparator, nulling for improved idle - otherwise as decoder
$E0 $01 $02
// to enable offset nulling load small positive constant into encoder offset input reg
$E3 $00 $04
// adm mode BT CVSD algorithm
// syllabic tc=16ms
// step size dynamic range 1280/10
// companding rule = 4 of 4
// principal tc=0.5ms
// second order tc=N/A
// zero tc=N/A
// zero at bit_rate/2 disabled
$D1 $BD $A0
$E1 $BD $A0
// prime idle pattern into CBUS ADM source byte regs
$D8 $AA
$E8 $AA
// enable encoder and decoder with no IRQs
$81 $88
// Alternative settings for PCM format using second order ADM algorithm
// syllabic tc=16ms
// step size dynamic range 5120/10
// companding rule = 5 of 5
// principal tc=0.5ms
// second order tc=0.0625ms
// predictor zero tc=0.0234ms for encoder
// zero at bit_rate/2 enabled for decoder
//$D1 $AE $A1
//$E1 $AE $BA
// codec mode 2=linear PCM buffered (3=uLaw 4=Alaw)
//$70 $02
// decoder flow for input PCM plus transcode to ADM with offset null and output via VAD output.
//$D0 $57 $02
//$D3 $00 $04
```

7. Performance Specification

7.1 Electrical Performance

7.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (V_{DD} - V_{SS})	-0.3	7.0	V
Voltage on any pin to V_{SS}	-0.3	V_{DD} + 0.3	V
Current into or out of V_{DD} and V_{SS} pins	-30	+30	mA
Current into or out of any other pin	-20	+20	mA

E3 and D3 Package	**Min.**	**Max.**	**Units**
E3 Total Allowable Power Dissipation at Tamb = 25°C	–	300	mW
Derating above 25°C	–	5.0	mW/°C
D3 Total Allowable Power Dissipation at Tamb = 25°C	–	800	mW
Derating above 25°C	–	13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

7.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	Min.	Max.	Units
Supply (V_{DD} - V_{SS})		2.7	5.5	V
Operating Temperature		-40	+85	°C
External Clock Frequency		2.048	16.384	MHz
Xtal Frequency		8.000	16.384	MHz

7.1.3 Operating Characteristics

The following conditions are assumed unless otherwise specified:
V_{DD} = 2.7V to 5.5V at T_{AMB} = -40 to +85°C, Audio Test Frequency = 820Hz, Xtal/Clock f_0 = 8.192MHz, Data Rate = 32kbps, Audio reference level (0 dBm0) = 489mV_{RMS}.

	Notes	Min.	Typ.	Max.	Units
DC Parameters					
I_{DD} (powersaved) at V_{DD} = 3.0V	1	–	2.5	20	µA
I_{DD} (powersaved) at V_{DD} = 5.0V	1	–	4.0	20	µA
I_{DD} (XTAL only) at V_{DD} = 3.0V	1	–	0.70	1.3	mA
I_{DD} (XTAL only) at V_{DD} = 5.0V	1	–	1.23	1.6	mA
I_{DD} (low powermode) at V_{DD} = 3.0V	1	–	2.4	2.9	mA
I_{DD} (low powermode) at V_{DD} = 5.0V	1	–	3.5	4.1	mA
Input logic 1		70%V_{DD}	–	–	V
Input logic 0		–	–	30% V_{DD}	V
Output logic 1		80% V_{DD}	–	–	V
Output logic 0		–	–	20%V_{DD}	V
Logic I/O Pin Input Impedance		1.0	–	–	MΩ
Logic Input Pins, Pull-up Resistor		300	–	–	kΩ
Digital Output Impedance		–	–	4.0	kΩ
Analog Input Impedance		–	200	–	kΩ
AUDIO OUT Driver					
Small Signal Output Impedance at V_{DD} = 2.7V	7	–	70	–	Ω
Small Signal Output Impedance at V_{DD} = 5.5V	7	–	50	–	Ω
Output Current Limit at V_{DD} = 2.7V	7	–	1.1	–	mA
Output Current Limit at V_{DD} = 5.5V	7	–	4.5	–	mA
Three State Output Leakage		–	±4	–	µA
DAC Full Scale Reference Voltage		–	1.235	–	V
Dynamic Values					
Encoder Analog Signal Input Sensitivity					
V_{DD} = 3.0V	2	-37	–	4.0	dB
V_{DD} = 5.0V	2	-37	–	4.0	dB
Encoder Input to Decoder Output Insertion Loss					
V_{DD} = 3.0V	2	–	0	–	dB
V_{DD} = 5.0V	2	–	0	–	dB
Encoder/Decoder (Full Codec)					
Passband Lowest Corner Frequency	3	–	2900	–	Hz
Passband Highest Corner Frequency	3	–	1400	–	Hz
Stopband Lowest Corner Frequency	3	–	6.0	–	kHz
Stopband Highest Corner Frequency	3	–	24	–	kHz
Stopband Attenuation		–	40	–	dB
Passband Gain		–	0	–	dB
Passband Ripple	5	-1.5	–	3.0	dB
Output Noise (Input Short Circuit)	4,6	–	-61	–	dBmOp
Perfect Idle Channel Noise (Encode Forced)	4,6	–	-62	–	dBmOp
MIC Amplifier					
Open Loop Gain		–	6.0	–	dB
Unity Gain Bandwidth		–	1.0	–	MHz
Input Impedance		10	–	–	MΩ
Output Impedance (open loop)		–	10	–	KΩ

Distortion	–	1	2	%

Notes:
1. Not including any current drawn from the device by external circuits.
2. Input and output signal levels are independent of supply voltage.
3. Passband and stopband corner frequencies are programmable. Specified values are at nominal external clock or crystal frequencies of 4.096, 8.192, 12.288, or 16.384MHz with the master clock divider configured for a divide by 1, 2, 3, or 4 respectively. For other clock or crystal frequencies, passband and stopband corner frequencies must be scaled accordingly.
4. dBmOp units imply the use of a psophometrically weighted filter that is commonly used in voice communication applications per ITU Recommendation G.223.
5. From 400Hz to 3000Hz with a 3.7kHz bandwidth.
6. At V_{DD} =2.7V, data rate = 64kbps, 2.9kHz bandwidth, offsets compensated and 1st order integration only.
7. AUDIO OUT driving a resistive load connected to a voltage source of $V_{DD}/2$.

7.1.3 (continued) C-BUS Timing Diagram

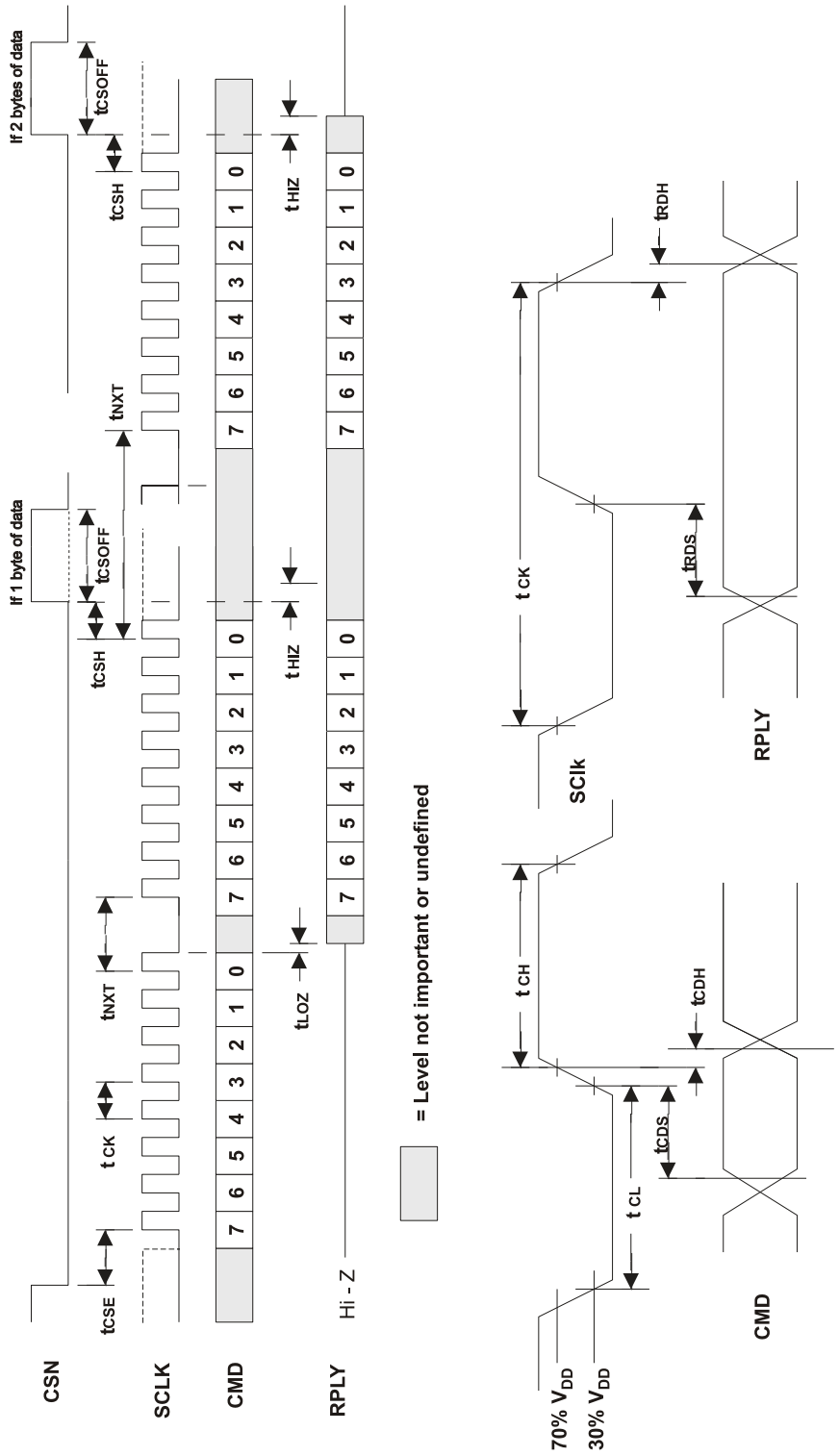


Figure 15 C-BUS Timing Diagram

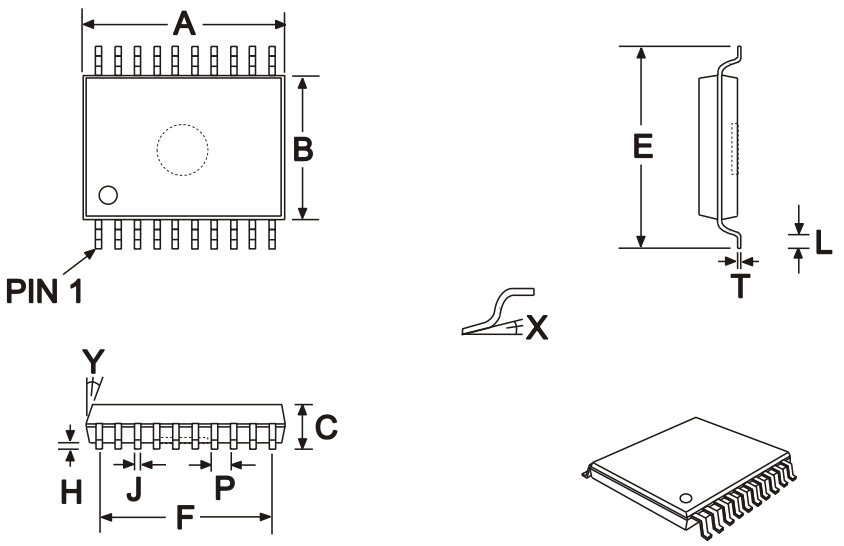
C-BUS Timing (see Figure 15)		Notes	Min.	Typ.	Max.	Unit
t_{CSE}	CSN Enable to SClk high time		100			ns
t_{CSH}	Last SClk high to CSN high time		100			ns
t_{LOZ}	SClk low to ReplyData Output Enable Time		0.0			ns
t_{HIZ}	CSN high to ReplyData high impedance				1.0	µs
t_{CSOFF}	CSN high time between transactions		1.0			µs
t_{NXT}	Inter-byte time		200			ns
t_{CK}	SClk cycle time		200			ns
t_{CH}	SClk high time		100			ns
t_{CL}	SClk low time		100			ns
t_{CDS}	Command Data setup time		75			ns
t_{CDH}	Command Data hold time		25			ns
t_{RDS}	Reply Data setup time		50			ns
t_{RDH}	Reply Data hold time		0			ns

Notes:
1. Depending on the command, 1 or 2 bytes of COMMAND DATA are transmitted to the peripheral MSB (Bit 7) first, LSB (Bit 0) last. REPLY DATA is read from the peripheral MSB (Bit 7) first, LSB (Bit 0) last.
2. Data is clocked into the peripheral on the rising SERIAL_CLOCK edge.
3. Commands are acted upon at the end of each command (rising edge of CSN).
4. To allow for differing µC serial interface formats C-BUS compatible ICs are able to work with SERIAL_CLOCK pulses starting and ending at either polarity.
5. Maximum 30pF load on IRQN pin and each C-BUS interface line.

These timings are for the CMX649 and allow faster transfers than the original C-BUS specification.

For codec data interface timing specifications and diagrams please refer to section 6.2.

7.2 Packaging



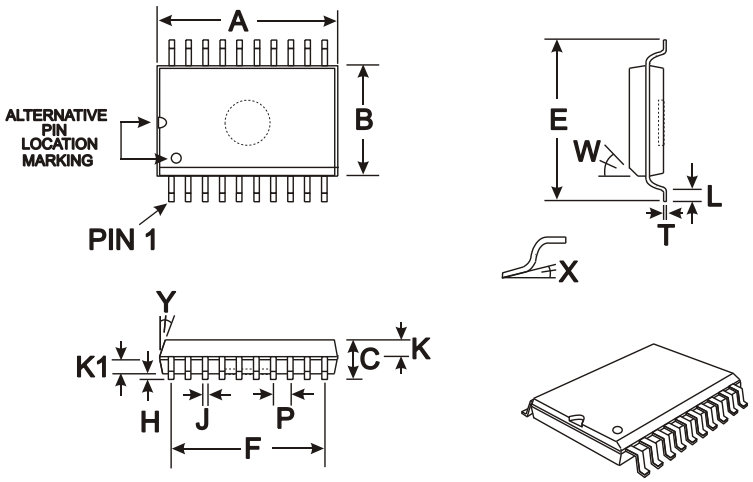
	DIM.	MIN.	TYP.	MAX.
*	A	6.40		6.60
*	B	4.30		4.50
	C	--------		1.20
	E	6.20		6.60
	F		5.85	
	H	0.05		0.15
	J	0.17		0.30
	L	0.45		0.75
	P		0.65	
	T	0.08		0.20
	X	0°		8°
	Y		12°	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Figure 16 20-Lead TSSOP Mechanical Outline: *Order as part no. CMX649E3*



	DIM.	MIN.	TYP.	MAX.
*	A	0.495 (12.57)		0.510 (12.95)
*	B	0.286 (7.26)		0.299 (7.59)
	C	0.088 (2.24)		0.105 (2.67)
	E	0.390 (9.90)		0.419 (10.64)
	F		0.450 (11.43)	
	H	0.003 (0.08)		0.020 (0.51)
	J	0.013 (0.33)		0.020 (0.51)
	K		0.041 (1.04)	
	K1		0.041 (1.04)	
	L	0.016 (0.41)		0.050 (1.27)
	P		0.050 (1.27)	
	T	0.009 (0.23)		0.0125 (0.32)
	W		45°	
	X	0°		10°
	Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees
Co-Planarity of leads within 0.004" (0.1mm)

Figure 17 20-Lead SOIC Mechanical Outline: *Order as part no. CMX649D3*

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