



Integrated Device Technology, Inc.

**512K x 8  
CMOS STATIC RAM MODULE**

**IDT7M4048  
IDT7MB4048**

INTEGRATED DEVICE

**FEATURES:**

- High-density 4-megabit (512K x 8) Static RAM module
- Equivalent to the JEDEC standard for future monolithic 512K x 8 Static RAMs
- Fast access time: 20ns (max.)
- Low power consumption (L version)
  - Active: 110mA (max.)
  - CMOS Standby: 400µA (max.)
  - Data Retention: 250µA (max.) Vcc = 2V
- Surface mounted plastic packages on a 32-pin, 600 mil ceramic or FR-4 DIP substrate
- Single 5V (±10%) power supply
- Inputs/outputs directly TTL-compatible

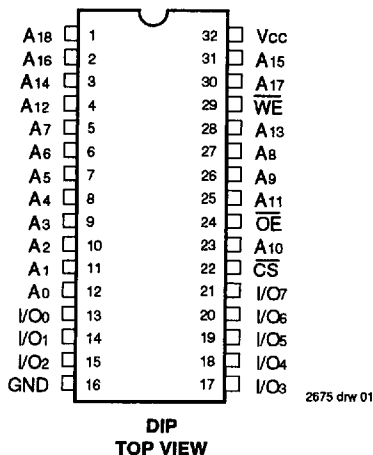
**DESCRIPTION:**

The IDT7M4048/7MB4048 is a 4-megabit (512K x 8) Static RAM module constructed on a co-fired ceramic or multilayer epoxy laminate (FR-4) substrate using four 1 megabit Static RAMs and a decoder. The IDT7MB4048 is available with access times as fast as 20ns. For low-power applications, the IDT7M4048 version offers a data retention current of 200µA and a standby current of 400µA.

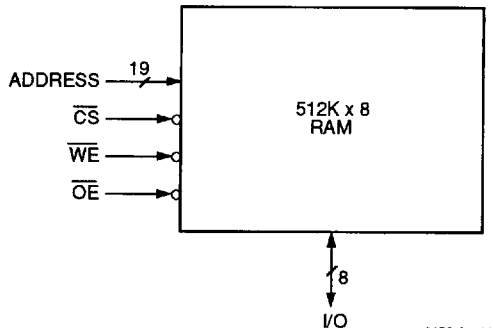
The IDT7M4048 is packaged in a 32-pin ceramic DIP. This results in a package 1.7 inches long and 0.6 inches wide, packing 4 megabits into the JEDEC DIP footprint. The IDT7MB4048 likewise is packaged in a 32-pin FR-4 DIP resulting in the same JEDEC footprint in a package 1.6 inches long and 0.6 inches wide.

All inputs and outputs of the IDT7M4048 and 7MB4048 are TTL-compatible and operate from a single 5V supply. Fully asynchronous circuitry requires no clocks or refresh for operation and provides equal access and cycle times for ease of use.

**PIN CONFIGURATION**



**FUNCTIONAL BLOCK DIAGRAM**



**PIN NAMES**

|                 |                     |
|-----------------|---------------------|
| I/O0-7          | Data Inputs/Outputs |
| A0-18           | Addresses           |
| $\overline{CS}$ | Chip Select         |
| $\overline{WE}$ | Write Enable        |
| $\overline{OE}$ | Output Enable       |
| Vcc             | Power               |
| GND             | Ground              |

The IDT logo is a registered trademark of Integrated Device Technology Inc.

**COMMERCIAL TEMPERATURE RANGE**

**AUGUST 1993**

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DSC-70474

**TRUTH TABLE**

| Mode    | $\overline{CS}$ | $\overline{OE}$ | $\overline{WE}$ | Output | Power   |
|---------|-----------------|-----------------|-----------------|--------|---------|
| Standby | H               | X               | X               | High-Z | Standby |
| Read    | L               | L               | H               | DOUT   | Active  |
| Read    | L               | H               | H               | High-Z | Active  |
| Write   | L               | X               | L               | DIN    | Active  |

2675 tbl 02

**CAPACITANCE<sup>(1)</sup>** ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{MHz}$ )

| Symbol      | Parameter                             | Conditions     | Typ. | Unit |
|-------------|---------------------------------------|----------------|------|------|
| $C_{IN}$    | Input Capacitance                     | $V_{IN} = 0V$  | 35   | pF   |
| $C_{IN(C)}$ | Input Capacitance ( $\overline{CS}$ ) | $V_{IN} = 0V$  | 8    | pF   |
| $C_{OUT}$   | Output Capacitance                    | $V_{OUT} = 0V$ | 35   | pF   |

**NOTE:**

1. This parameter is guaranteed by design, but not tested

2675 tbl 03

**RECOMMENDED DC OPERATING CONDITIONS**

| Symbol   | Parameter          | Min.         | Typ. | Max. | Unit |
|----------|--------------------|--------------|------|------|------|
| $V_{CC}$ | Supply Voltage     | 4.5          | 5    | 5.5  | V    |
| GND      | Supply Voltage     | 0            | 0    | 0    | V    |
| $V_{IH}$ | Input High Voltage | 2.2          | —    | 6    | V    |
| $V_{IL}$ | Input Low Voltage  | $-0.5^{(1)}$ | —    | 0.8  | V    |

**NOTE:**

1.  $V_{IL} = -2.0V$  for pulse width less than 10ns.

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**DC ELECTRICAL CHARACTERISTICS**

( $V_{CC} = 5V \pm 10\%$ ,  $T_A = 0^\circ\text{C}$  to  $+70^\circ\text{C}$ )

| Symbol     | Parameter                                 | Test Conditions   | 7M4048LxxN |      | 7M4048SxxN |      | 7MB4048SxxP |      | Unit          |
|------------|---|---|------------|------|------------|------|-------------|------|---------------|
|            |   |   | Min.       | Max. | Min.       | Max. | Min.        | Max. |               |
| $ I_{LI} $ | Input Leakage                             | $V_{CC} = \text{Max}$ , $V_{IN} = \text{GND to } V_{CC}$                                | —          | 4    | —          | 4    | —           | 8    | $\mu\text{A}$ |
| $ I_{LO} $ | Output Leakage                            | $V_{CC} = \text{Max}$ , $\overline{CS} = V_{IH}$ ,<br>$V_{OUT} = \text{GND to } V_{CC}$ | —          | 4    | —          | 4    | —           | 8    | $\mu\text{A}$ |
| $V_{OL}$   | Output Low Voltage                        | $V_{CC} = \text{Min}$ , $I_{OL} = 2\text{mA}^{(1)}$ ,<br>$I_{OL} = 8\text{mA}^{(2)}$    | —          | 0.4  | —          | 0.4  | —           | 0.4  | V             |
| $V_{OH}$   | Output High Voltage                       | $V_{CC} = \text{Min}$ , $I_{OH} = -1\text{mA}^{(1)}$ ,<br>$I_{OH} = -4\text{mA}^{(2)}$  | 2.4        | —    | 2.4        | —    | 2.4         | —    | V             |
| $I_{CC}$   | Dynamic Operating Current                 | $V_{CC} = \text{Max}$ , $\overline{CS} \leq V_{IL}$ ; $f = f_{MAX}$ ,<br>Outputs Open   | —          | 110  | —          | 150  | —           | 480  | mA            |
| $I_{SB}$   | Standby Supply Current (TTL Levels)       | $\overline{CS} \geq V_{IH}$ , $V_{CC} = \text{Max}$ , $f = f_{MAX}$ ,<br>Outputs Open   | —          | 12   | —          | 12   | —           | 250  | mA            |
| $I_{SB1}$  | Full Standby Supply Current (CMOS Levels) | $\overline{CS} \geq V_{CC} - 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$<br>or $\leq 0.2$       | —          | 0.4  | —          | 12   | —           | 170  | mA            |

**NOTES:**

- For 7M4048LxxN version only
- For 7MB4048SxxP version only

2675 tbl 07

**ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>**

| Symbol     | Rating                               | Commercial   | Unit             |
|------------|--------------------------------------|--------------|------------------|
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5 to +7.0 | V                |
| $T_A$      | Operating Temperature                | 0 to +70     | $^\circ\text{C}$ |
| $T_{BIAS}$ | Temperature Under Bias               | -10 to +85   | $^\circ\text{C}$ |
| $T_{STG}$  | Storage Temperature                  | -55 to +125  | $^\circ\text{C}$ |
| $I_{OUT}$  | DC Output Current                    | 50           | mA               |

**NOTE:**

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability

2675 tbl 05

**RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE**

| Grade      | Ambient Temperature                      | GND | $V_{CC}$      |
|------------|--|-----|---------------|
| Commercial | $0^\circ\text{C}$ to $+70^\circ\text{C}$ | 0V  | $5V \pm 10\%$ |

2675 tbl 06

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**DATA RETENTION CHARACTERISTICS<sup>(3)</sup>**

**INTEGRATED DEVICE**

(TA = 0°C to +70°C)

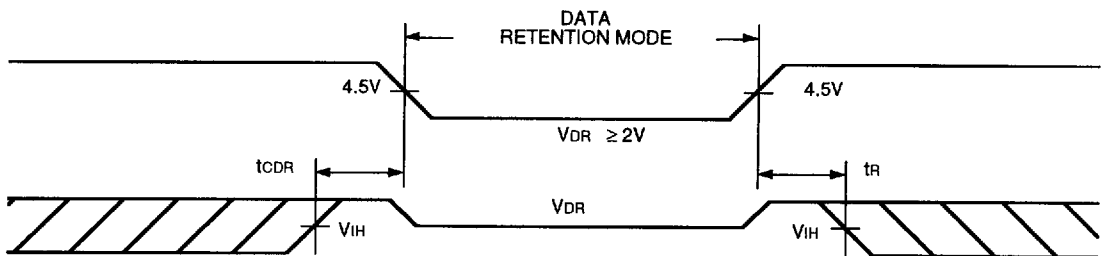
| Symbol              | Parameter                            | Test Condition                     | Min.               | Max.<br>Vcc @ 2.0V | Unit    |
|---------------------|--------------------------------------|------------------------------------|--------------------|--------------------|---------|
| VDR                 | Vcc for Data Retention               | —                                  | 2.0                | —                  | V       |
| IccDR               | Data Retention Current               | $\overline{CS} \geq V_{CC} - 0.2V$ | —                  | 250                | $\mu A$ |
| tCDR <sup>(2)</sup> | Chip Deselect to Data Retention Time | $V_{IN} \leq V_{CC} - 0.2V$ or     | 0                  | —                  | ns      |
| tR <sup>(2)</sup>   | Operation Recovery Time              | $V_{IN} \geq 0.2V$                 | tRC <sup>(1)</sup> | —                  | ns      |

2675 tbl 08

**NOTES:**

1. trc = Read Cycle Time
2. This parameter is guaranteed by design, but not tested.
3. For 7M4048LxxN version only

**DATA RETENTION WAVEFORM**

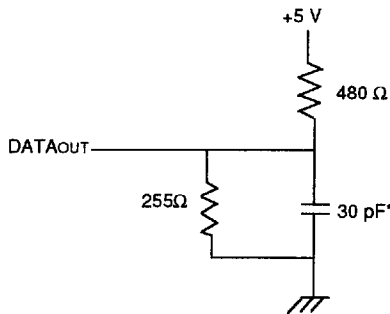


2675 drw 03

**AC TEST CONDITIONS**

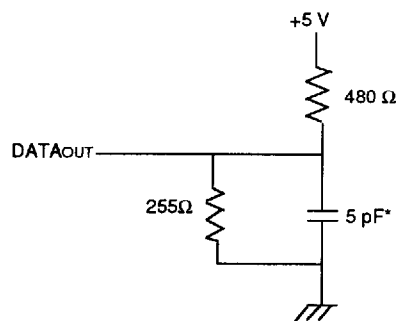
|                               |                   |
|-------------------------------|-------------------|
| Input Pulse Levels            | GND to 3.0V       |
| Input Rise/Fall Times         | 5ns               |
| Input Timing Reference Levels | 1.5V              |
| Output Reference Levels       | 1.5V              |
| Output Load                   | See Figures 1 - 4 |

2675 tbl 09



2675 drw 04

Figure 1. Output Load



2675 drw 05

Figure 2. Output Load  
(for tOLZ, tCHZ, tOHZ, tWHZ, tOW and tCLZ)

**AC ELECTRICAL CHARACTERISTICS**

**INTEGRATED DEVICE**

(VCC = 5V ± 10%, TA = 0°C to +70°C)

| Symbol              | Parameter                          | 7MB4048SxxP        |      |      |      |      |      |      |      | Unit |
|---------------------|------------------------------------|--------------------|------|------|------|------|------|------|------|------|
|                     |                                    | -20 <sup>(3)</sup> |      | -25  |      | -30  |      | -35  |      |      |
|                     |                                    | Min.               | Max. | Min. | Max. | Min. | Max. | Min. | Max. |      |
| <b>Read Cycle</b>   |                                    |                    |      |      |      |      |      |      |      |      |
| tRC                 | Read Cycle Time                    | 20                 | —    | 25   | —    | 30   | —    | 35   | —    | ns   |
| tAA                 | Address Access Time                | —                  | 20   | —    | 25   | —    | 30   | —    | 35   | ns   |
| tACS                | Chip Select Access Time            | —                  | 20   | —    | 25   | —    | 30   | —    | 35   | ns   |
| tOE                 | Output Enable to Output Valid      | —                  | 10   | —    | 12   | —    | 15   | —    | 15   | ns   |
| tOHZ <sup>(1)</sup> | Output Disable to Output in High-Z | —                  | 8    | —    | 12   | —    | 12   | —    | 15   | ns   |
| tOLZ <sup>(1)</sup> | Output Enable to Output in Low-Z   | 0                  | —    | 0    | —    | 0    | —    | 0    | —    | ns   |
| tCLZ <sup>(1)</sup> | Chip Select to Output in Low-Z     | 5                  | —    | 5    | —    | 5    | —    | 5    | —    | ns   |
| tCHZ <sup>(1)</sup> | Chip Deselect to Output in High-Z  | —                  | 13   | —    | 14   | —    | 16   | —    | 20   | ns   |
| tOH                 | Output Hold from Address Change    | 3                  | —    | 3    | —    | 3    | —    | 3    | —    | ns   |
| tPU <sup>(1)</sup>  | Chip Select to Power-Up Time       | 0                  | —    | 0    | —    | 0    | —    | 0    | —    | ns   |
| tPD <sup>(1)</sup>  | Chip Deselect to Power-Down Time   | —                  | 20   | —    | 25   | —    | 30   | —    | 35   | ns   |
| <b>Write Cycle</b>  |                                    |                    |      |      |      |      |      |      |      |      |
| tWC                 | Write Cycle Time                   | 20                 | —    | 25   | —    | 30   | —    | 35   | —    | ns   |
| tWP                 | Write Pulse Width                  | 15                 | —    | 17   | —    | 20   | —    | 25   | —    | ns   |
| tAS <sup>(2)</sup>  | Address Set-up Time                | 3                  | —    | 3    | —    | 0    | —    | 0    | —    | ns   |
| tAW                 | Address Valid to End-of-Write      | 18                 | —    | 20   | —    | 25   | —    | 30   | —    | ns   |
| tCW                 | Chip Select to End-of-Write        | 18                 | —    | 20   | —    | 25   | —    | 30   | —    | ns   |
| tDW                 | Data to Write Time Overlap         | 12                 | —    | 15   | —    | 17   | —    | 20   | —    | ns   |
| tDH <sup>(2)</sup>  | Data Hold Time                     | 0                  | —    | 0    | —    | 0    | —    | 0    | —    | ns   |
| tWR <sup>(2)</sup>  | Write Recovery Time                | 0                  | —    | 0    | —    | 0    | —    | 0    | —    | ns   |
| tWHZ <sup>(1)</sup> | Write Enable to Output in High-Z   | —                  | 13   | —    | 15   | —    | 15   | —    | 15   | ns   |
| tOW <sup>(1)</sup>  | Output Active from End-of-Write    | 2                  | —    | 2    | —    | 5    | —    | 5    | —    | ns   |

**NOTES**

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1. This parameter is guaranteed by design, but not tested.
2. tAS=0ns for  $\overline{CS}$  controlled write cycles. tDH, tWR= 3ns for  $\overline{CS}$  controlled write cycles.
3. Preliminary specifications only

AC ELECTRICAL CHARACTERISTICS

INTEGRATED DEVICE

(VCC = 5V ± 10%, TA = 0°C to +70°C)

| Symbol              | Parameter                          | 7MB4048SxxP      |      |                  |      | 7M4048SxxN         |      |                    |      | 7M4048LxxN |      | Unit |
|---------------------|------------------------------------|------------------|------|------------------|------|--------------------|------|--------------------|------|------------|------|------|
|                     |                                    | 45               |      | -55              |      | -55 <sup>(3)</sup> |      | -70 <sup>(3)</sup> |      | -70        |      |      |
|                     |                                    | Min.             | Max. | Min.             | Max. | Min.               | Max. | Min.               | Max. | Min.       | Max. |      |
| <b>Read Cycle</b>   |                                    |                  |      |                  |      |                    |      |                    |      |            |      |      |
| tRC                 | Read Cycle Time                    | 45               | —    | 55               | —    | 55                 | —    | 70                 | —    | 70         | —    | ns   |
| tAA                 | Address Access Time                | —                | 45   | —                | 55   | —                  | 55   | —                  | 70   | —          | 70   | ns   |
| tACS                | Chip Select Access Time            | —                | 45   | —                | 55   | —                  | 55   | —                  | 70   | —          | 70   | ns   |
| tOE                 | Output Enable to Output Valid      | —                | 25   | —                | 30   | —                  | 35   | —                  | 45   | —          | 45   | ns   |
| tOHZ <sup>(1)</sup> | Output Disable to Output in High-Z | —                | 20   | —                | 20   | —                  | 25   | —                  | 30   | —          | 30   | ns   |
| tOLZ <sup>(1)</sup> | Output Enable to Output in Low-Z   | 5                | —    | 5                | —    | 0                  | —    | 0                  | —    | 0          | —    | ns   |
| tCLZ <sup>(1)</sup> | Chip Select to Output in Low-Z     | 5                | —    | 5                | —    | 5                  | —    | 5                  | —    | 5          | —    | ns   |
| tCHZ <sup>(1)</sup> | Chip Deselect to Output in High-Z  | —                | 20   | —                | 20   | —                  | 25   | —                  | 40   | —          | 40   | ns   |
| tOH                 | Output Hold from Address Change    | 5                | —    | 5                | —    | 5                  | —    | 5                  | —    | —          | 10   | ns   |
| tPU <sup>(1)</sup>  | Chip Select to Power-Up Time       | 0                | —    | 0                | —    | 0                  | —    | 0                  | —    | 0          | —    | ns   |
| tPD <sup>(1)</sup>  | Chip Deselect to Power-Down Time   | —                | 45   | —                | 55   | —                  | 55   | —                  | 70   | —          | 70   | ns   |
| <b>Write Cycle</b>  |                                    |                  |      |                  |      |                    |      |                    |      |            |      |      |
| tWC                 | Write Cycle Time                   | 45               | —    | 55               | —    | 55                 | —    | 70                 | —    | 70         | —    | ns   |
| tWP                 | Write Pulse Width                  | 35               | —    | 45               | —    | 50                 | —    | 55                 | —    | 55         | —    | ns   |
| tAS                 | Address Set-up Time                | 5                | —    | 5                | —    | 5                  | —    | 0                  | —    | 0          | —    | ns   |
| tAW                 | Address Valid to End-of-Write      | 40               | —    | 50               | —    | 55                 | —    | 65                 | —    | 65         | —    | ns   |
| tCW                 | Chip Select to End-of-Write        | 40               | —    | 50               | —    | 50                 | —    | 65                 | —    | 65         | —    | ns   |
| tDW                 | Data to Write Time Overlap         | 20               | —    | 20               | —    | 30                 | —    | 35                 | —    | 35         | —    | ns   |
| tDH                 | Data Hold Time                     | 0 <sup>(2)</sup> | —    | 0 <sup>(2)</sup> | —    | 0 <sup>(2)</sup>   | —    | 0 <sup>(2)</sup>   | —    | 0          | —    | ns   |
| tWR                 | Write Recovery Time                | 0 <sup>(2)</sup> | —    | 0 <sup>(2)</sup> | —    | 0 <sup>(2)</sup>   | —    | 0 <sup>(2)</sup>   | —    | 0          | —    | ns   |
| tWHZ <sup>(1)</sup> | Write Enable to Output in High-Z   | —                | 15   | —                | 20   | —                  | 25   | —                  | 30   | —          | 30   | ns   |
| tOW <sup>(1)</sup>  | Output Active from End-of-Write    | 5                | —    | 5                | —    | 0                  | —    | 0                  | —    | 0          | —    | ns   |

NOTES:

1. This parameter is guaranteed by design, but not tested.
2. tAS=0ns for CS controlled write cycles tDH, tWR= 5ns for CS controlled write cycles.
3. Preliminary specifications only.

2675 tbl 11

AC ELECTRICAL CHARACTERISTICS

INTEGRATED DEVICE

(V<sub>CC</sub> = 5V ± 10%, T<sub>A</sub> = 0°C to +70°C)

| Symbol                          | Parameter                          | 7M4048LxxN |      |      |      |      |      | Unit |
|---------------------------------|------------------------------------|------------|------|------|------|------|------|------|
|                                 |                                    | -85        |      | -100 |      | -120 |      |      |
|                                 |                                    | Min.       | Max. | Min. | Max. | Min. | Max. |      |
| <b>Read Cycle</b>               |                                    |            |      |      |      |      |      |      |
| t <sub>RC</sub>                 | Read Cycle Time                    | 85         | —    | 100  | —    | 120  | —    | ns   |
| t <sub>AA</sub>                 | Address Access Time                | —          | 85   | —    | 100  | —    | 120  | ns   |
| t <sub>ACS</sub>                | Chip Select Access Time            | —          | 85   | —    | 100  | —    | 120  | ns   |
| t <sub>OE</sub>                 | Output Enable to Output Valid      | —          | 48   | —    | 50   | —    | 60   | ns   |
| t <sub>OHZ</sub> <sup>(1)</sup> | Output Disable to Output in High-Z | —          | 33   | —    | 35   | —    | 40   | ns   |
| t <sub>OLZ</sub> <sup>(1)</sup> | Output Enable to Output in Low-Z   | 0          | —    | 0    | —    | 0    | —    | ns   |
| t <sub>CLZ</sub> <sup>(1)</sup> | Chip Select to Output in Low-Z     | 5          | —    | 5    | —    | 5    | —    | ns   |
| t <sub>CHZ</sub> <sup>(1)</sup> | Chip Deselect to Output in High-Z  | —          | 43   | —    | 45   | —    | 50   | ns   |
| t <sub>OH</sub>                 | Output Hold from Address Change    | 10         | —    | 10   | —    | 10   | —    | ns   |
| t <sub>PU</sub> <sup>(1)</sup>  | Chip Select to Power-Up Time       | 0          | —    | 0    | —    | 0    | —    | ns   |
| t <sub>PD</sub> <sup>(1)</sup>  | Chip Deselect to Power-Down Time   | —          | 85   | —    | 100  | —    | 120  | ns   |
| <b>Write Cycle</b>              |                                    |            |      |      |      |      |      |      |
| t <sub>WC</sub>                 | Write Cycle Time                   | 85         | —    | 100  | —    | 120  | —    | ns   |
| t <sub>WP</sub>                 | Write Pulse Width                  | 65         | —    | 75   | —    | 90   | —    | ns   |
| t <sub>AS</sub>                 | Address Set-up Time                | 2          | —    | 5    | —    | 5    | —    | ns   |
| t <sub>AW</sub>                 | Address Valid to End-of-Write      | 82         | —    | 90   | —    | 100  | —    | ns   |
| t <sub>CW</sub>                 | Chip Select to End-of-Write        | 80         | —    | 85   | —    | 100  | —    | ns   |
| t <sub>DW</sub>                 | Data to Write Time Overlap         | 38         | —    | 40   | —    | 45   | —    | ns   |
| t <sub>DH</sub>                 | Data Hold Time                     | 0          | —    | 0    | —    | 0    | —    | ns   |
| t <sub>WR</sub>                 | Write Recovery Time                | 0          | —    | 0    | —    | 0    | —    | ns   |
| t <sub>WHZ</sub> <sup>(1)</sup> | Write Enable to Output in High-Z   | —          | 33   | —    | 35   | —    | 40   | ns   |
| t <sub>OW</sub> <sup>(1)</sup>  | Output Active from End-of-Write    | 0          | —    | 0    | —    | 0    | —    | ns   |

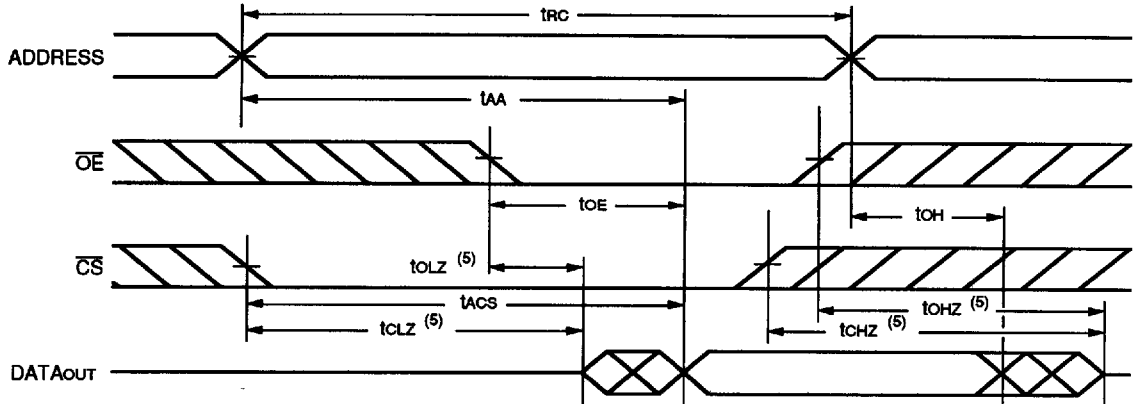
NOTE:

1. This parameter is guaranteed by design, but not tested

2675 tbl 12

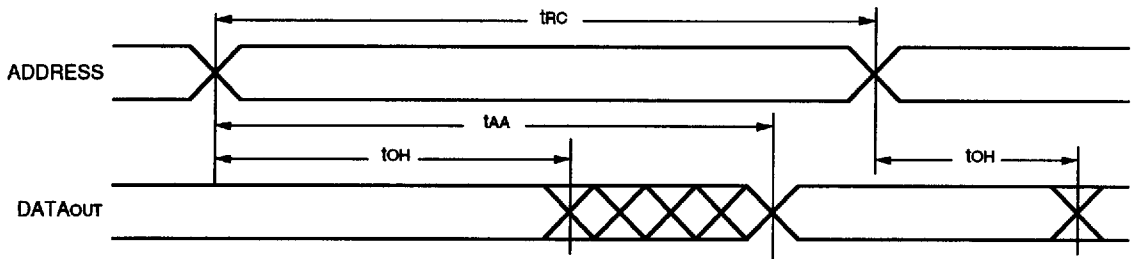
**TIMING WAVEFORM OF READ CYCLE NO. 1<sup>(1)</sup>**

**INTEGRATED DEVICE**



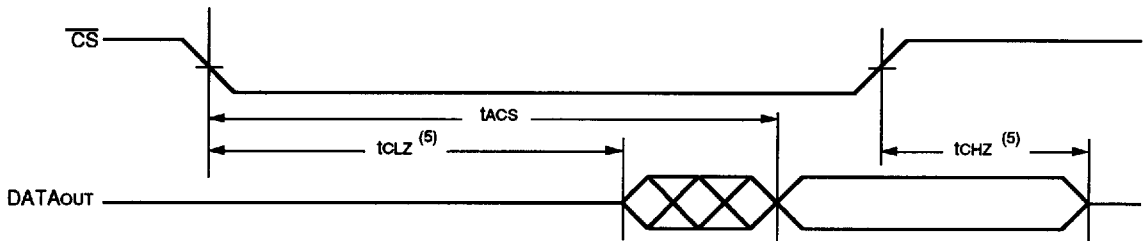
2675 drw 06

**TIMING WAVEFORM OF READ CYCLE NO. 2<sup>(1, 2, 4)</sup>**



2675 drw 07

**TIMING WAVEFORM OF READ CYCLE NO. 3<sup>(1, 3, 4)</sup>**

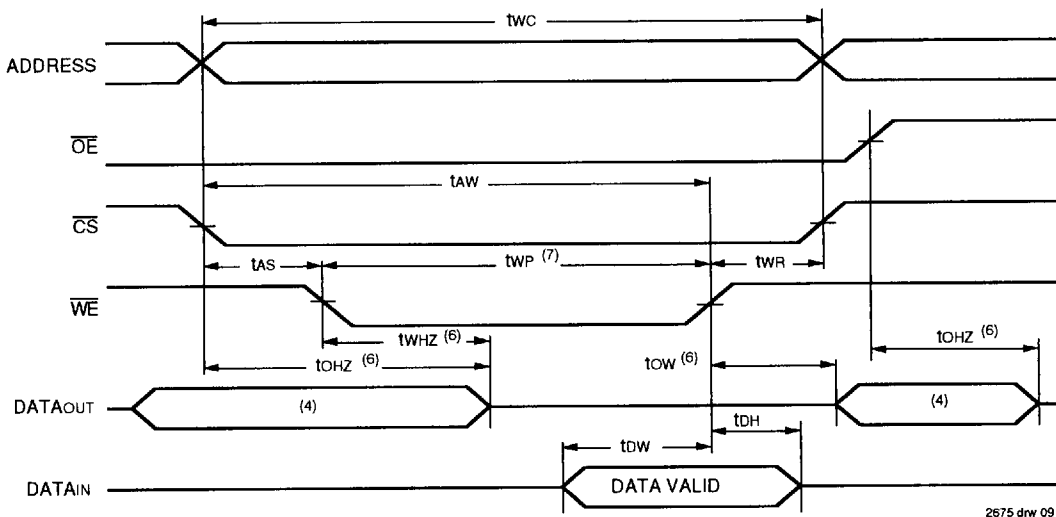


2675 drw 08

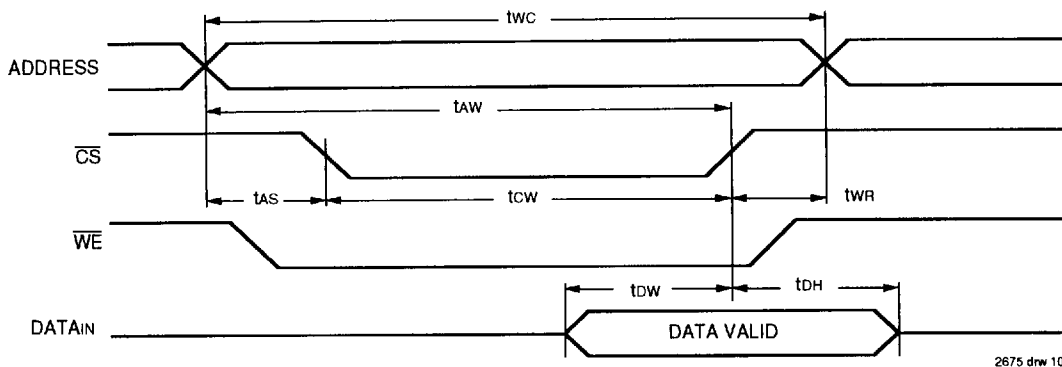
**NOTES:**

1. WE is HIGH for Read Cycle.
2. Device is continuously selected, CS = V<sub>IL</sub>.
3. Address valid prior to or coincident with CS transition LOW.
4. OE = V<sub>IL</sub>.
5. Transition is measured ±200mV from steady state. This parameter is guaranteed by design, but not tested.

**TIMING WAVEFORM OF WRITE CYCLE NO. 1 ( $\overline{WE}$  CONTROLLED TIMING)<sup>(1, 2, 3, 7)</sup>**



**TIMING WAVEFORM OF WRITE CYCLE NO. 2 ( $\overline{CS}$  CONTROLLED TIMING)<sup>(1, 2, 3, 5)</sup>**



**NOTES:**

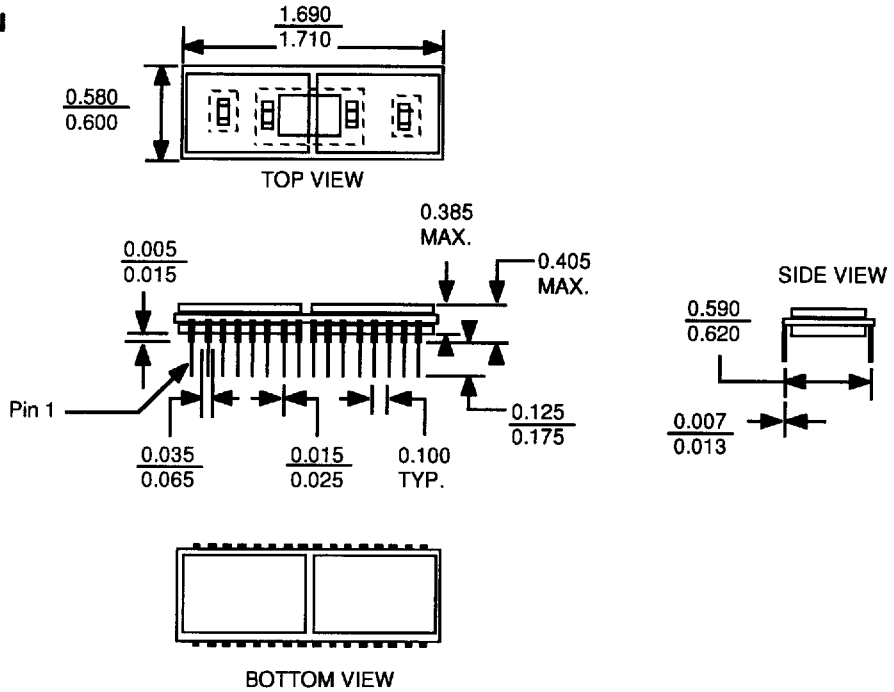
- 1  $\overline{WE}$  or  $\overline{CS}$  must be HIGH during all address transitions
- 2 A write occurs during the overlap ( $t_{WP}$ ) of a LOW  $\overline{CS}$  and a LOW  $\overline{WE}$
- 3  $t_{WR}$  is measured from the earlier of  $\overline{CS}$  or  $\overline{WE}$  going HIGH to the end of write cycle
- 4 During this period, I/O pins are in the output state, and input signals must not be applied.
- 5 If the  $\overline{CS}$  LOW transition occurs simultaneously with or after the  $\overline{WE}$  LOW transition, the outputs remain in a high-impedance state.
- 6 Transition is measured  $\pm 200mV$  from steady state with a 5pF load (including scope and jig) This parameter is guaranteed by design, but not tested.
- 7 If  $\overline{OE}$  is LOW during a  $\overline{WE}$  controlled write cycle, the write pulse width must be the larger of  $t_{WP}$  or  $(t_{WHZ} + t_{dW})$  to allow the I/O drivers to turn off and data to be placed on the bus for the required  $t_{dW}$ . If  $\overline{OE}$  is HIGH during a  $\overline{WE}$  controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified  $t_{WP}$ .



INTEGRATED DEVICE

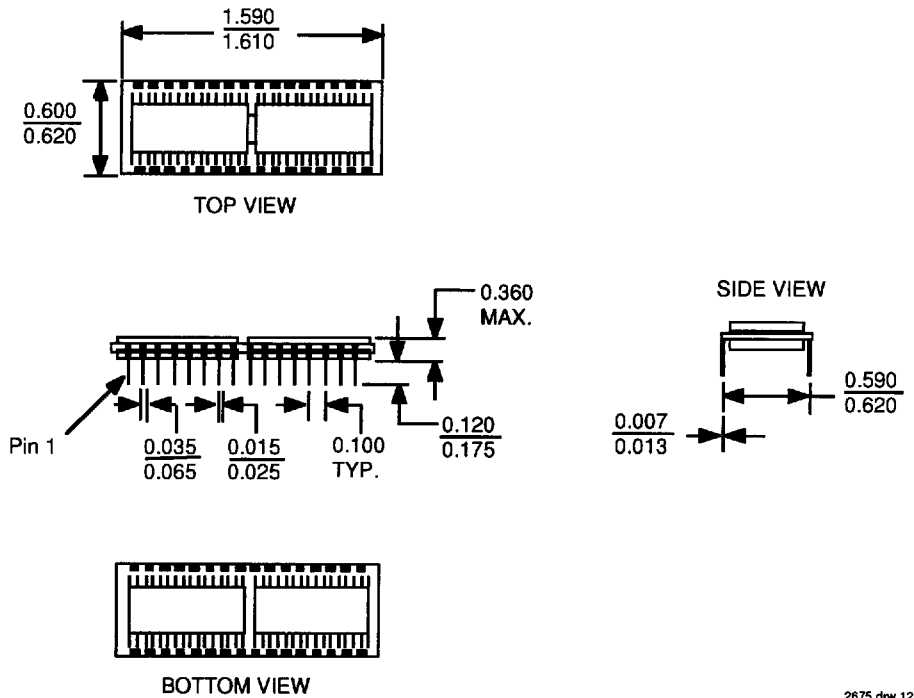
PACKAGE DIMENSIONS

7M4048LxxN



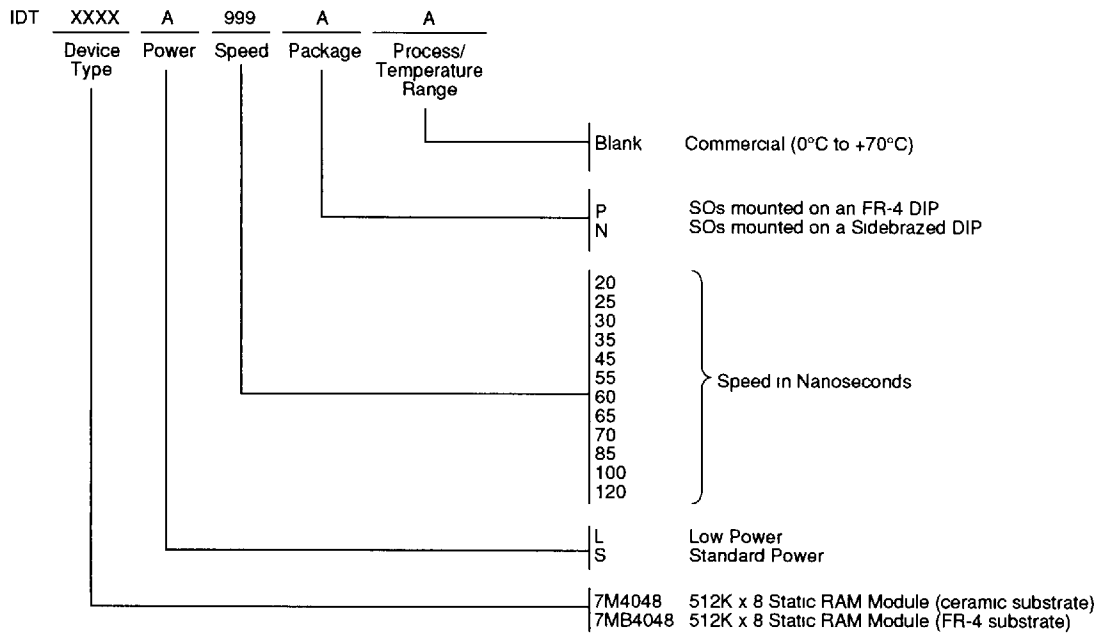
2675 drw 11

7MB4048SxxP



2675 drw 12

ORDERING INFORMATION<sup>(1)</sup>



2675 drw 13

NOTE:

1. Please refer to the "AC ELECTRICAL CHARACTERISTICS" tables for all available power/speed/package combinations for the 7M4048/7MB4048 modules