DMP2540UCB9

P-CHANNEL ENHANCEMENT MODE MOSFET

Product Summary (Typ. @ V_{GS} = -4.5V, T_A = +25°C)

V_{DSS}	$R_{DS(on)}$	Q_g	Q_{gd}	I_D
-25V	33mΩ	4.8nC	1.0nC	-5.2A

Features and Benefits

- LD-MOS Technology with the Lowest Figure of Merit:
  $R_{DS(on)}$ = 33mΩ to Minimize On-State Losses
  Q_g = 4.8nC for Ultra-Fast Switching
- $V_{gs(th)}$ = -0.6V typ. for a Low Turn-On Potential
- CSP with Footprint 1.5mm × 1.5mm
- Height = 0.62mm for Low Profile
- ESD = 6kV HBM Protection of Gate
- **Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- **Halogen and Antimony Free. "Green" Device (Note 3)**
- **Qualified to AEC-Q101 Standards for High Reliability**

Description and Applications

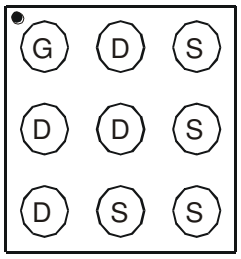
This new generation MOSFET is designed to minimize the on-state resistance ($R_{DS(on)}$) and yet maintain superior switching performance, making it ideal for high efficiency power management applications.

- Battery Management
- Load Switch
- Battery Protection

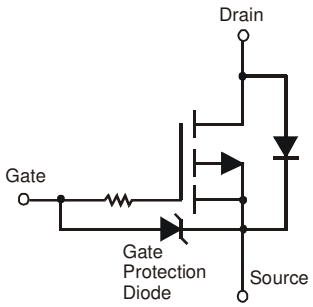
Mechanical Data

- Case: U-WLB1515-9
- Terminal Connections: See Diagram Below
- Weight: 0.0018 grams (Approximate)

ESD PROTECTED TO 6kV



Top-View
Pin Configuration



Equivalent Circuit

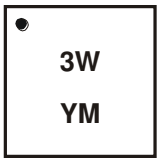
Ordering Information (Note 4)

Part Number	Case	Packaging
DMP2540UCB9-7	U-WLB1515-9	3,000/Tape & Reel

Notes:
1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS) & 2011/65/EU (RoHS 2) compliant.
2. See http://www.diodes.com/quality/lead_free.html for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
4. For packaging details, go to our website at http://www.diodes.com/products/packages.html.

Marking Information

U-WLB1515-9



3W = Product Type Marking Code
YM = Date Code Marking
Y = Year (ex: Y = 2011)
M = Month (ex: 9 = September)

Date Code Key

Year	2011	2012	2013	2014	2015	2016	2017
Code	Y	Z	A	B	C	D	E

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Maximum Ratings (@T_A = +25°C unless otherwise specified.)

Characteristic			Symbol	Value	Units
Drain-Source Voltage			V_{DSS}	-25	V
Gate-Source Voltage			V_{GSS}	-6	V
Continuous Drain Current (Note 5) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	-4.0 -3.0	A
Continuous Drain Current (Note 6) V_{GS} = -4.5V	Steady State	T_A = +25°C T_A = +70°C	I_D	-5.2 -4.0	A
Pulsed Drain Current (Pulse duration 10µs, duty cycle ≤1%)			I_{DM}	-30	A
Continuous Source Pin Current (Note 6)			I_S	-2.0	A
Pulsed Source Pin Current (Pulse duration 10µs, duty cycle ≤1%)			I_{SM}	-15	A
Continuous Gate Clamp Current (Note 5)			I_G	-0.6	A
Pulsed Gate Clamp Current (Pulse duration 10µs, duty cycle ≤1%)			I_{GM}	-8	A

Thermal Characteristics (@T_A = +25°C unless otherwise specified.)

Characteristic	Symbol	Value	Units
Total Power Dissipation (Note 5)	P_D	1.0	W
Total Power Dissipation (Note 6)	P_D	1.8	W
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	126.8	°C/W
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	69	°C/W
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	°C

Electrical Characteristics (@T_A = +25°C unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV_{DSS}	-25	-	-	V	V_{GS} = 0V, I_D = -250µA
Zero Gate Voltage Drain Current @T_C = +25°C	I_{DSS}	-	-	-1	µA	V_{DS} = -20V, V_{GS} = 0V
Gate-Source Leakage	I_{GSS}	-	-	-100	nA	V_{GS} = -6V, V_{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	$V_{GS(th)}$	-0.4	-0.6	-1.1	V	V_{DS} = V_{GS}, I_D = -250µA
Static Drain-Source On-Resistance	$R_{DS\ (ON)}$	-	33	40	mΩ	V_{GS} = -4.5V, I_D = - 2A
			42	50		V_{GS} = -2.5V, I_D = -2A
			52	60		V_{GS} = -1.8V, I_D = -2A
Forward Transfer Admittance	$\|Y_{fs}\|$	-	12	-	S	V_{DS} = -10V, I_D = -2A
Diode Forward Voltage (Note 5)	V_{SD}	-	-0.7	-1	V	V_{GS} = 0V, I_S = -2A
Reverse Recovery Charge	Q_{rr}	-	100	-	nC	V_{dd} = –9.5V, I_F = –2A, di/dt = 200A/µs
Reverse Recovery Time	t_{rr}	-	130	-	ns	
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C_{iss}	-	342	450	pF	V_{DS} = -10V, V_{GS} = 0V, f = 1.0MHz
Output Capacitance	C_{oss}	-	174	225	pF	
Reverse Transfer Capacitance	C_{rss}	-	70	90	pF	
Series Gate Resistance	R_G		28	35	Ω	V_{DS} = 0V, V_{GS} = 0V, f = 1.0MHz
Total Gate Charge (4.5V)	Q_g	-	4.8	6.0	nC	V_{GS} = -4.5V, V_{DS} = -10V, I_D = -2A
Gate-Source Charge	Q_{gs}	-	0.5	-	nC	
Gate-Drain Charge	Q_{gd}	-	1.0	-	nC	
Turn-On Delay Time	$t_{D(on)}$	-	11	-	ns	V_{DD} = -10V, V_{GS} = -4.5V, I_{DS} = -2A, R_G = 2Ω,
Turn-On Rise Time	t_r	-	12	-	ns	
Turn-Off Delay Time	$t_{D(off)}$	-	56	-	ns	
Turn-Off Fall Time	t_f	-	42	-	ns	

Notes:
5. Device mounted on FR-4 PCB with minimum recommended pad layout.
6. Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu
7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to production testing.

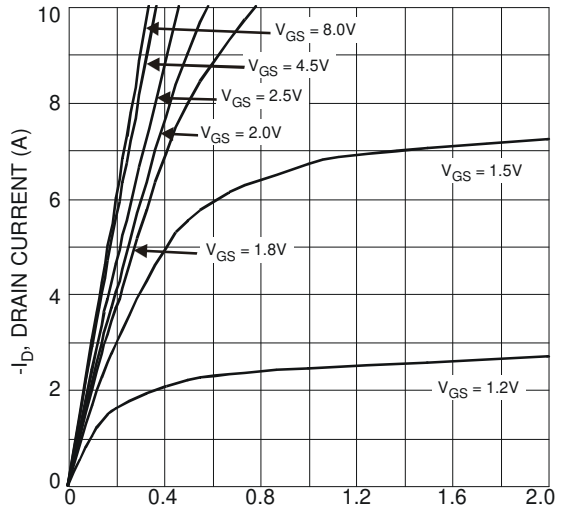


Fig. 1 Typical Output Characteristics

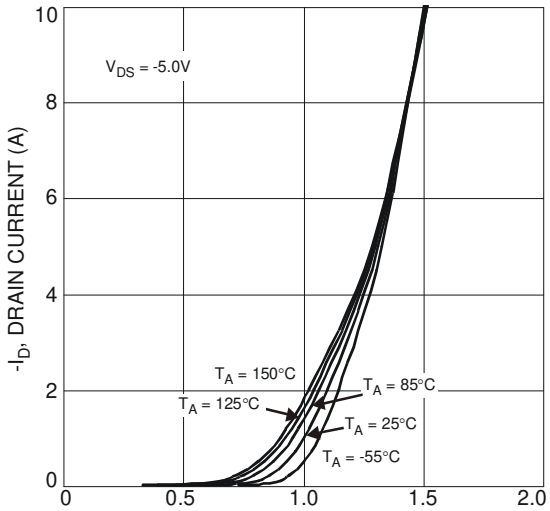


Fig. 2 Typical Transfer Characteristics

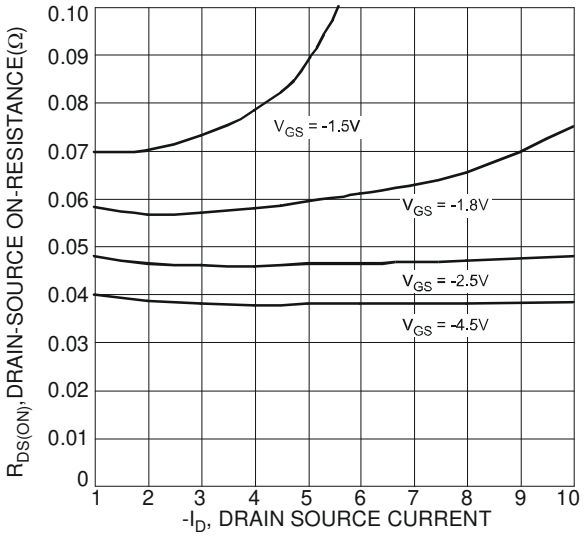


Fig. 3 Typical On-Resistance vs. Drain Current and Gate Voltage

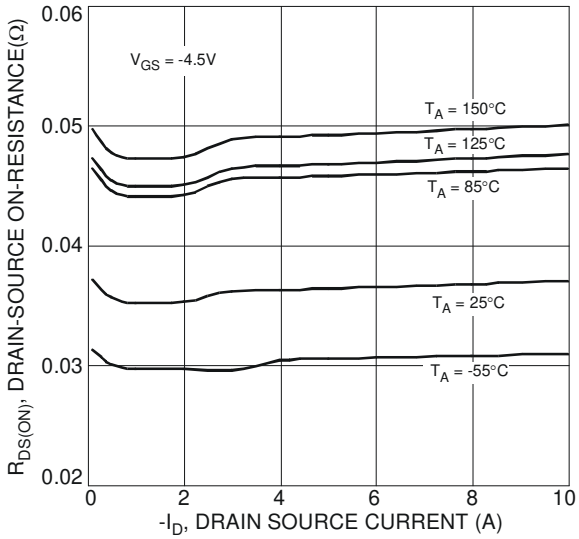


Fig. 4 Typical On-Resistance vs. Drain Current and Temperature

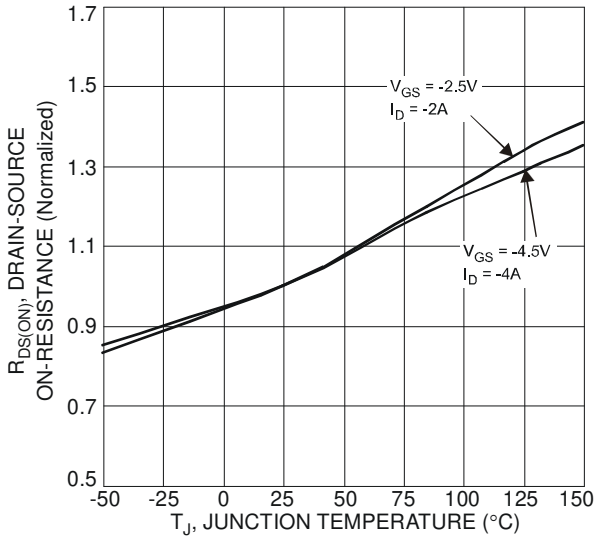


Fig. 5 On-Resistance Variation with Temperature

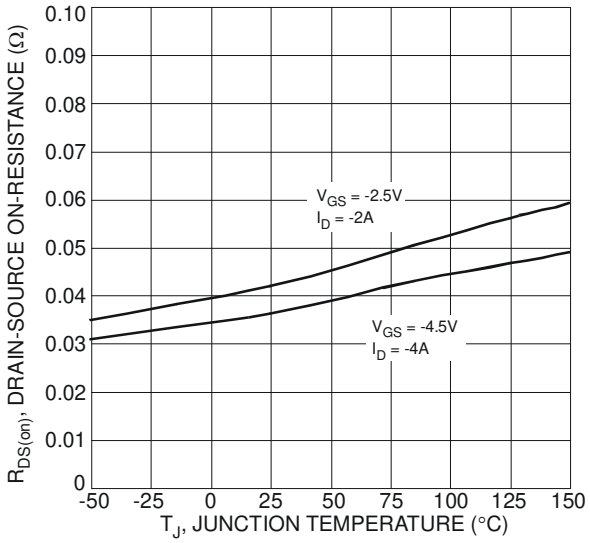


Fig. 6 On-Resistance Variation with Temperature

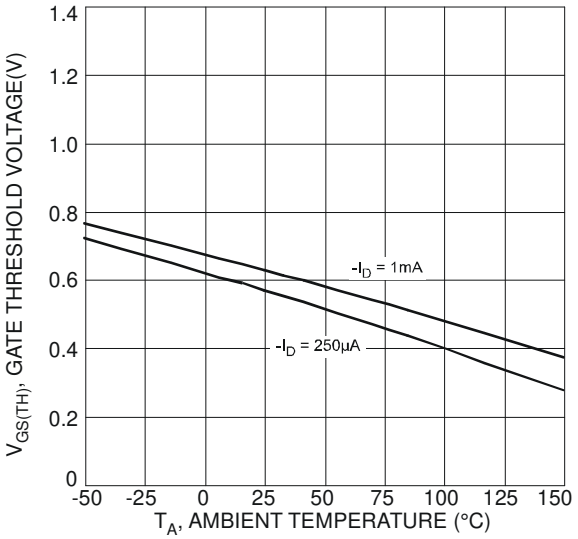


Fig. 7 Gate Threshold Variation vs. Ambient Temperature

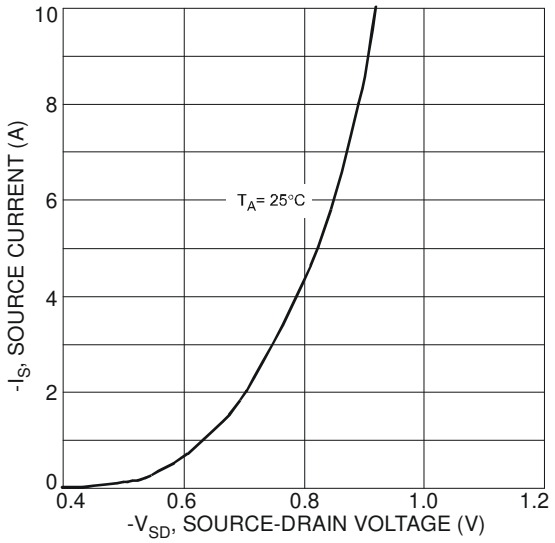


Fig. 8 Diode Forward Voltage vs. Current

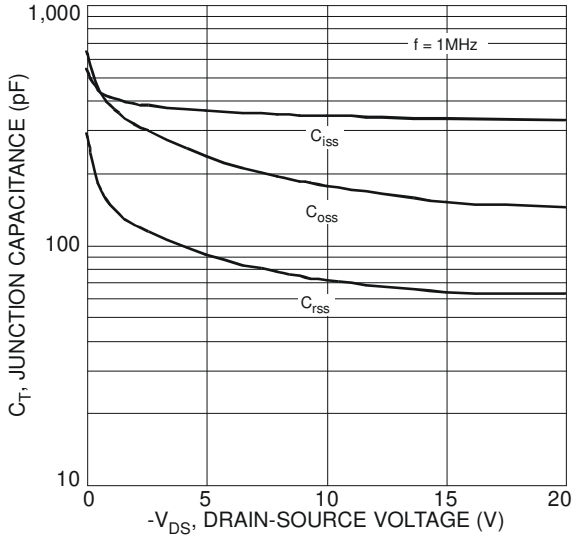


Fig. 9 Typical Junction Capacitance

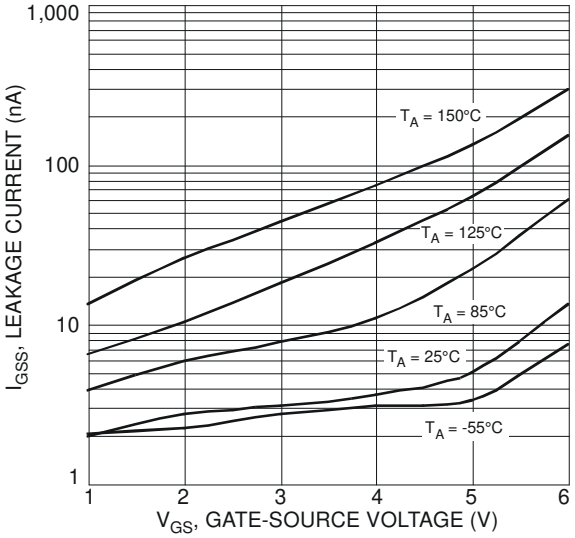


Fig. 10 Gate-Source Leakage Current vs. Voltage

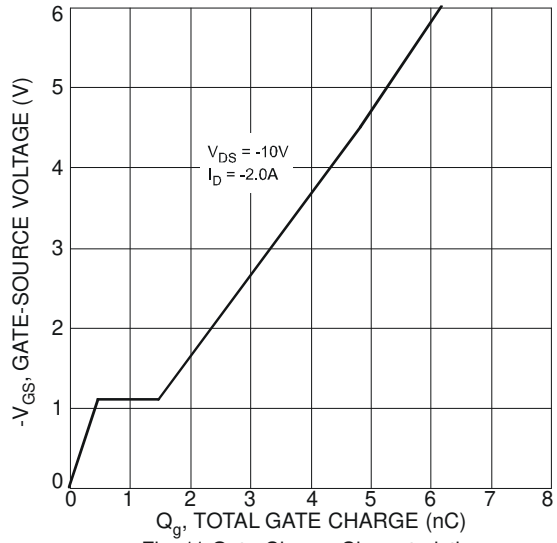


Fig. 11 Gate-Charge Characteristics

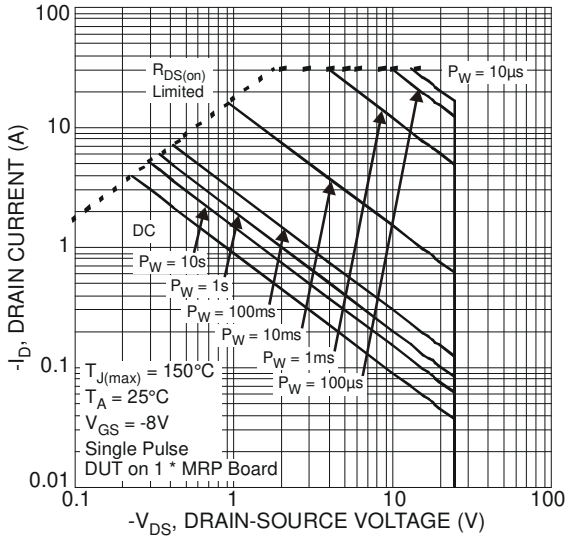


Fig. 12 SOA, Safe Operation Area

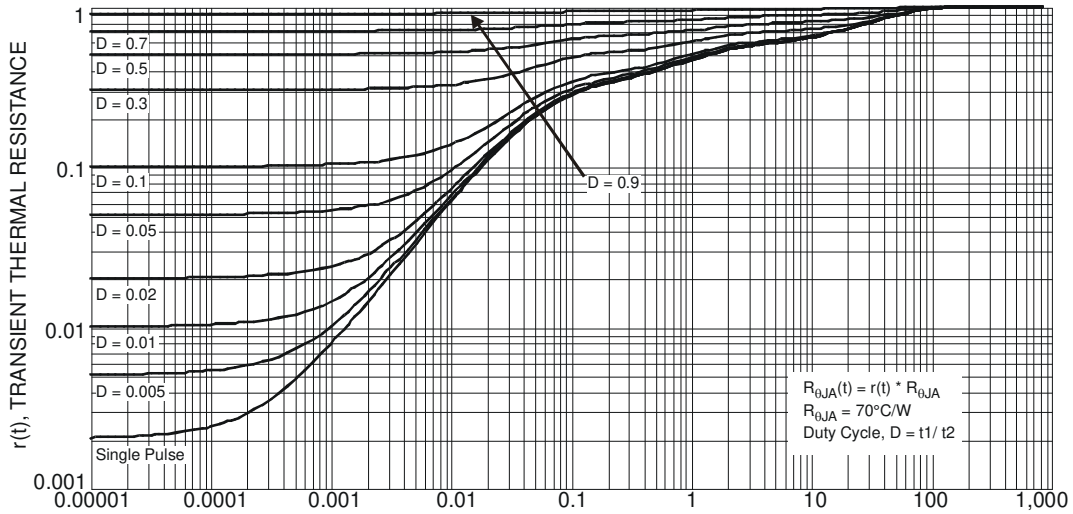
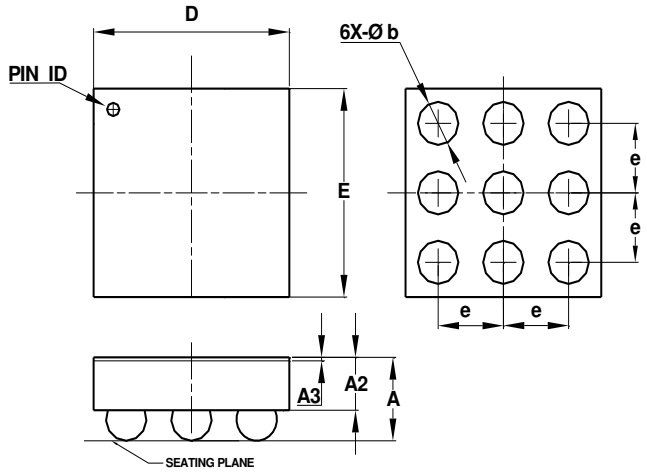


Fig. 13 Transient Thermal Resistance

Package Outline Dimensions

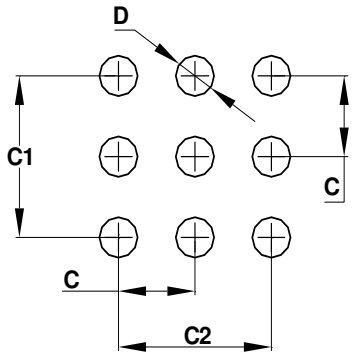
Please see AP02002 at http://www.diodes.com/datasheets/ap02002.pdf for the latest version.



U-WLB1515-9			
Dim	**Min**	**Max**	**Typ**
A	-	0.62	-
A2	-	0.36	0.36
A3	0.020	0.030	0.025
b	0.27	0.37	0.32
D	1.47	1.51	1.49
E	1.47	1.51	1.49
e	-	-	0.50
All Dimensions in mm			

Suggested Pad Layout

Please see AP02001 at http://www.diodes.com/datasheets/ap02001.pdf for the latest version.



Dimensions	Value (in mm)
C	0.50
C1	1.00
C2	1.00
D	0.25

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel. Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

www.diodes.com