45 MHz to 1218 MHz, CATV Power Doubler Hybrid

Data Sheet

ADCA3992

FEATURES

- High RF output: 76.8 dBmV total composite power
- DPD optimized
- High gain of 26.7 dB at 1218 MHz
- Very low distortion
- Low noise figure: 3 dB at 45 MHz, 4.5 dB at 1218 MHz
- Unconditionally stable
- Transient and surge protection
- V_{CC} range from 24 V to 34 V
- Configurable dc current from 300 mA to 550 mA maximum
- Industry-standard, 8-pin SOT115J module package

APPLICATIONS

- 45 MHz to 1218 MHz cable television (CATV) infrastructure amplifier systems
- Remote physical layer (PHY) and fiber deep nodes
- DOCSIS® 3.1 compliant

FUNCTIONAL BLOCK DIAGRAM

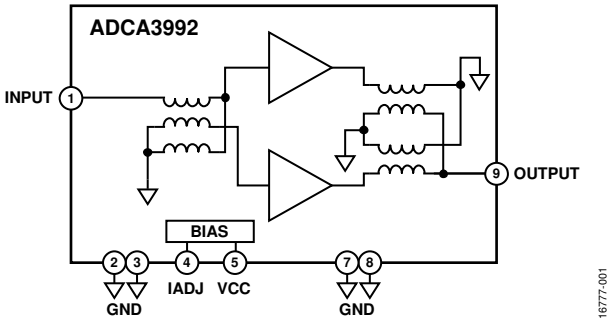

Figure 1.

GENERAL DESCRIPTION

The ADCA3992 is a high gain, power doubler hybrid amplifier optimized for a wide range of bias conditions for power efficiency and customer flexibility. The ADCA3992 is ideally suited for use in digital predistortion (DPD) node designs for maximum power savings. The device achieves extremely high RF output, up to 76.8 dBmV composite power, or 67 dBmV virtual level, using a gallium arsenide (GaAs) pseudomorphic high electron mobility transistor (pHEMT) die in combination with a gallium nitride (GaN) HEMT die. The dc current and supply voltage can be adjusted externally for optimum distortion performance vs. power consumption over a range of output levels. The ADCA3992 is packaged in the industry-standard SOT115J package.

Rev. 0 Document Feedback

Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700
©2020 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

TABLE OF CONTENTS

REVISION HISTORY

1/2020—Revision 0: Initial Version

SPECIFICATIONS

GENERAL PERFORMANCE

Supply voltage (V_{CC}) = 34 V, flange temperature (T_{FLANGE}) = 35°C, source impedance (Z_S) = load impedance (Z_L) = 75 Ω, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
POWER GAIN	S_{21}		24.2		dB	f = 45 MHz
			26.7		dB	f = 1218 MHz
SLOPE OF STRAIGHT LINE[1]	SL		2.5		dB	f = 45 MHz to 1218 MHz
FLATNESS OF FREQUENCY RESPONSE[2]			0.8		dB	f = 45 MHz to 1218 MHz
REVERSE ISOLATION	S_{12}		−30		dB	f = 45 MHz to 1218 MHz
RETURN LOSS						
Input	S_{11}		−26		dB	f = 45 MHz to 320 MHz
			−25		dB	f = 320 MHz to 640 MHz
			−24		dB	f = 640 MHz to 870 MHz
			−28		dB	f = 870 MHz to 1000 MHz
			−24		dB	f = 1000 MHz to 1218 MHz
Output	S_{22}		−25		dB	f = 45 MHz to 320 MHz
			−21		dB	f = 320 MHz to 640 MHz
			−20		dB	f = 640 MHz to 870 MHz
			−23		dB	f = 870 MHz to 1000 MHz
			−24		dB	f = 1000 MHz to 1218 MHz
NOISE FIGURE	NF		3		dB	f = 45 MHz
			4.5		dB	f = 1218 MHz
SUPPLY						
Maximum Operating Voltage	V_{CC}		34		V	Can be biased down to 24 V
DC Current (Total)	$I_{CC\ (TOTAL)}$		535	550	mA	Can be biased between 300 mA and 550 mA

[1] The slope is defined as the delta of the gain at the start frequency and the gain at the stop frequency.
[2] Flatness of frequency response is defined as the deviation of the slope of a straight line.

DISTORTION DATA, 40 MHz TO 550 MHz

V_{CC} = 34 V, T_{FLANGE} = 35°C, Z_S = Z_L = 75 Ω, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DISTORTION						Channel power (V_0) = 63 dBmV at 1218 MHz, 22 dB extrapolated tilt, 79 channels plus 111 digital channels (−6 dB offset)[1]
Composite Triple Beat	CTB		−80		dBc	CTB is defined by the National Cable and Telecommunications Association (NCTA)
Crossmodulation	XMOD		−74		dBc	XMOD is measured at baseband (selective voltmeter method) referenced to 100% modulation of the carrier being tested.
Composite Second Order	CSO		−80		dBc	CSO parameter (sum and difference products) is defined by the NCTA
Carrier to Intermodulation Noise	CIN		62		dB	CIN is defined by ANSI/SCTE 17 (test procedure for carrier to noise)
TOTAL COMPOSITE POWER	TCP		76.8		dBmV	See Figure 7 and Figure 8

[1] 79 analog channels plus 111 digital channels, National Television System Committee (NTSC) frequency raster = 55.25 MHz to 547.25 MHz, −6 dB offset to the equivalent analog carrier, and 22 dB extrapolated tilt.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
VCC, IADJ	
DC Supply over Voltage (5 minute)	38 V
RF Input Power	75 dBmV
Operating Temperature Ranges	
Ambient (T_A)	−30°C to +85°C
Flange (T_{FLANGE})	−30°C to +100°C
Storage Temperature (T_S) Range	−40°C to +100°C

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

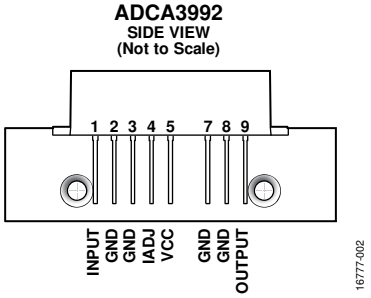

Figure 2. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	INPUT	RF Input.
2, 3, 7, 8	GND	Ground.
4	IADJ	Bias Control Pin. Keep this pin floating for full bias operation. Do not pull negative voltages at this pin.
5	VCC	Positive Supply Voltage. 34 V typical. This pin can be biased down to 24 V.
9	OUTPUT	RF Output.

TYPICAL PERFORMANCE CHARACTERISTICS

V_{CC} = 34 V, T_{FLANGE} = 35°C, Z_S = Z_L = 75 Ω, unless otherwise noted.

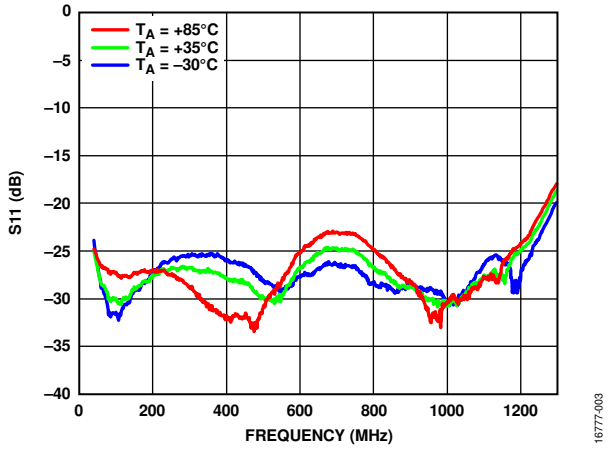

Figure 3. Input Return Loss (S11) vs. Frequency at Various Temperatures

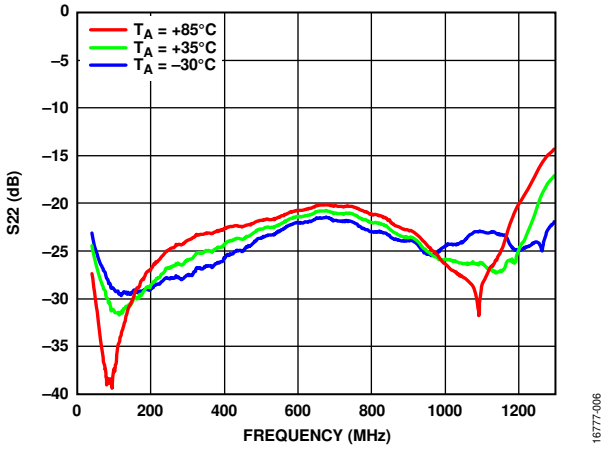

Figure 6. Output Return Loss (S22) vs. Frequency at Various Temperatures

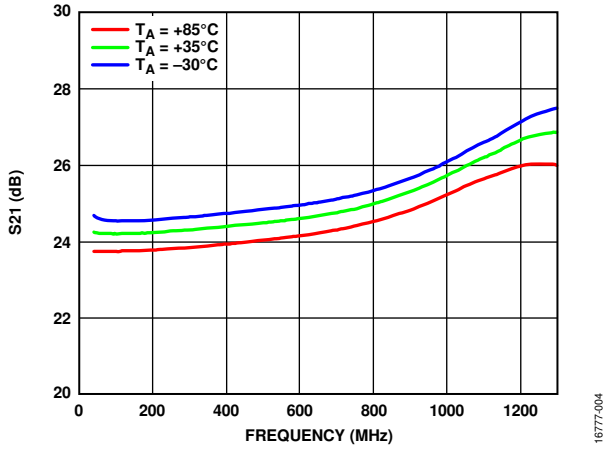

Figure 4. Gain (S21) vs. Frequency at Various Temperatures

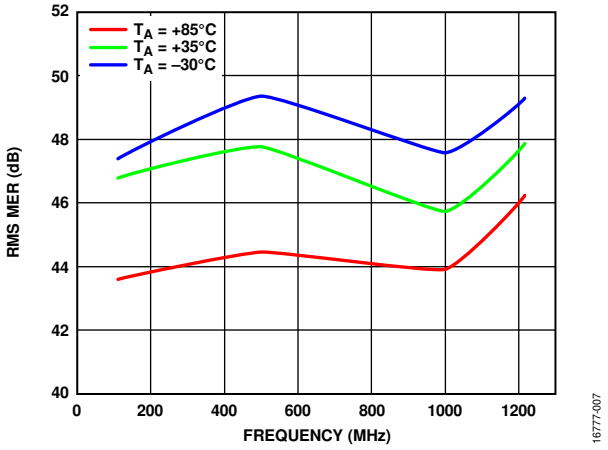

Figure 7. RMS Modulation Error Rate (MER) vs. Frequency at Various Temperatures, V_0 = 61 dBmV at 1218 MHz, 23 dB Extrapolated Tilt, 190 Digital Channels, Total Composite Power = 76.8 dBmV

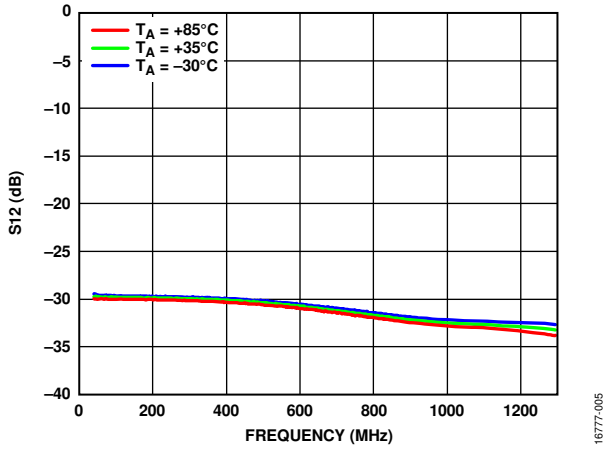

Figure 5. Reverse Isolation (S12) vs. Frequency at Various Temperatures

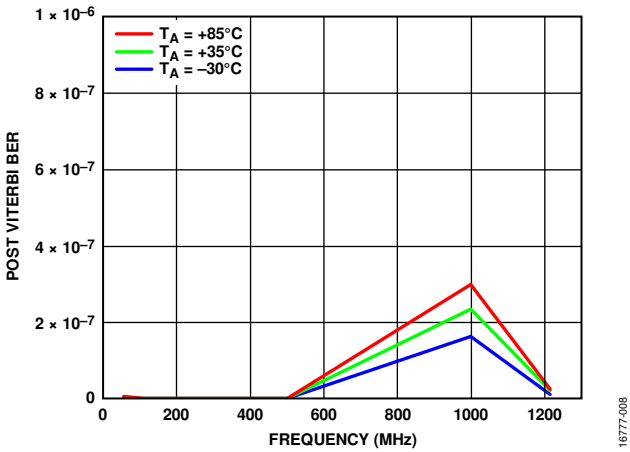

Figure 8. Post Viterbi Bit Error Rate (BER) vs. Frequency at Various Temperatures, V_0 = 61 dBmV at 1218 MHz, 23 dB Extrapolated Tilt, 190 Digital Channels, Total Composite Power = 76.8 dBmV, 10 sec Integration Time

THEORY OF OPERATION

The ADCA3992 is a 75 Ω input and output matched module designed for CATV applications. The ADCA3992 uses cascode field effect transistor (FET) feedback amplifiers in a Class A push pull configuration. The bottom half of the cascode stages are implemented in a single-die linear FET process that minimizes parasitics, thereby enabling higher gain. The top devices in the cascodes are implemented using a linear GaN process that is able to swing very high RF voltages. The frequency of operation is from 45 MHz to 1218 MHz.

Internally, the ADCA3992 module uses a balun to convert the input signal to a balanced signal that feeds the active stages. An output impedance transformer and balun combination converts the balanced GaN signals into an unbalanced 75 Ω output. The output transformer also feeds the dc to the active stages and cancels second-order distortion products coming from the active devices.

The module has a control pin (IADJ) to set the dc current consumption from low bias to the full bias of the device by connecting a resistor from this pin to ground or by using a positive voltage.

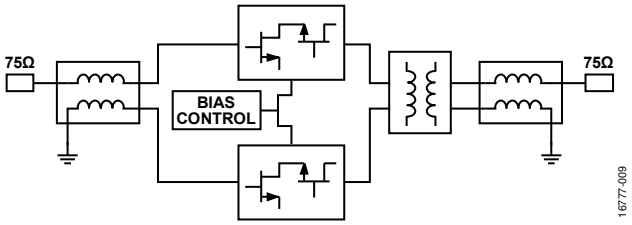

Figure 9. Simplified Schematic

APPLICATIONS INFORMATION

Basic connections for operating the ADCA3992 are shown in Figure 11. Both the input pin (Pin 1) and the output pin (Pin 9) of the ADCA3992 are matched to 75 Ω. Pin 5 is the VCC pin, which requires 34 V for typical operation, and can support as low as 24 V for lower power operation. It is recommended to leave the IADJ pin (Pin 4) open for full bias operation. For bias control on the ADCA3992 supply current, apply an external control voltage between 0 V and 1 V at the IADJ pin. Figure 10 illustrates the ADCA3992 supply current over control voltages at the IADJ pin.

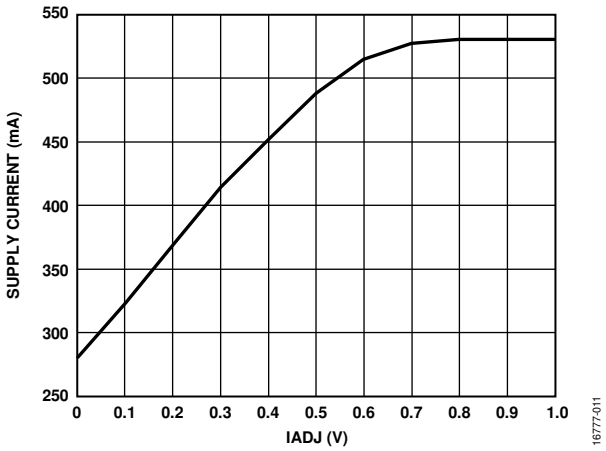

Figure 10. Supply Current vs. IADJ

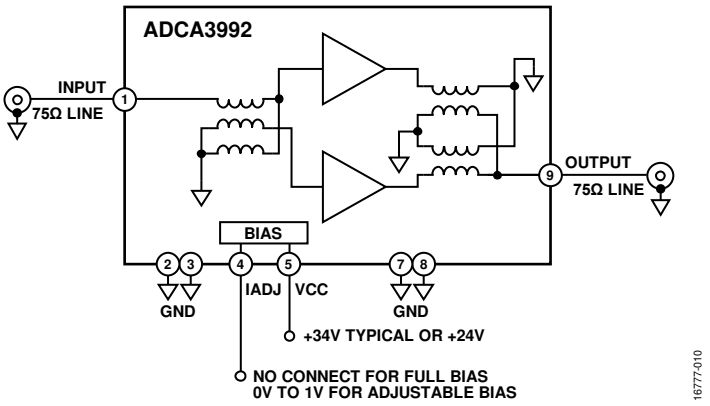

Figure 11. Basic Connections

OUTLINE DIMENSIONS

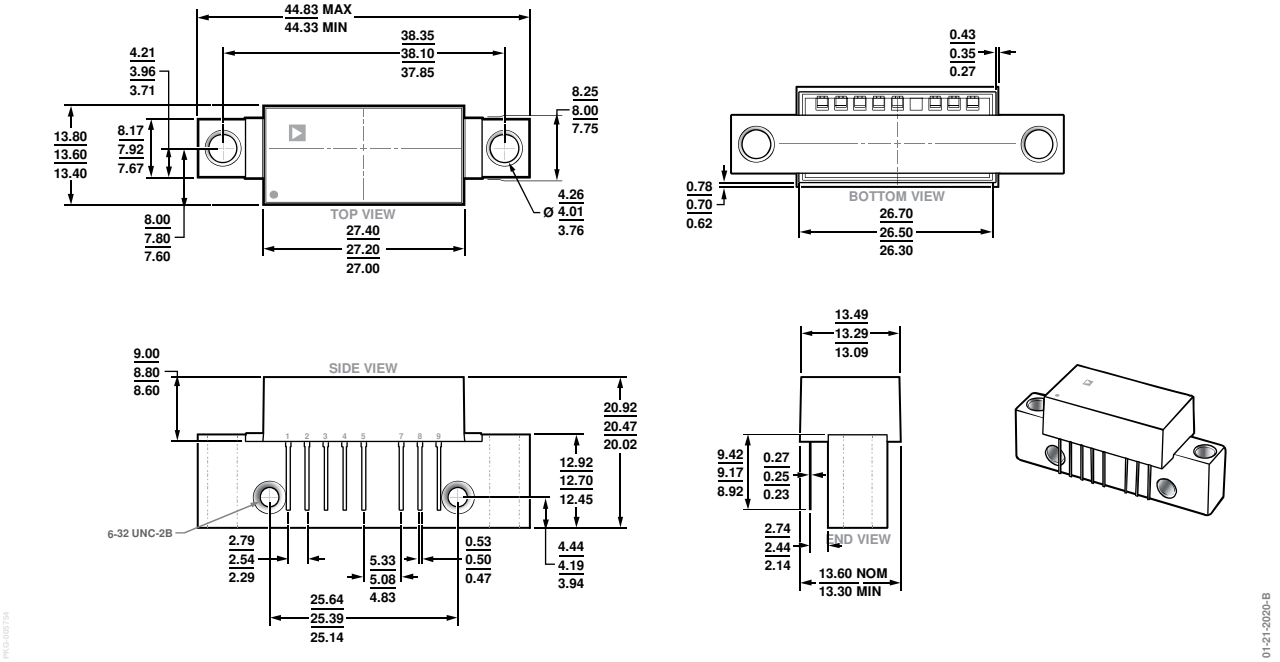

Figure 12. 8-Pin SOT115J Module Package [MODULE]
(ML-8-1)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADCA3992AMLZ	−30°C to +100°C	8-Pin SOT115J Module Package [MODULE], Box with 25 Pieces	ML-8-1

[1] Z = RoHS Compliant Part.

©2020 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D16777-1/20(0)