

## 74LVX574

### Low Voltage Octal D-Type Flip-Flop with 3-STATE Outputs

#### General Description

The LVX574 is a high-speed octal D-type flip-flop which is controlled by an edge-triggered clock input (CP) and a buffered common Output Enable ( $\overline{OE}$ ) input. When the  $\overline{OE}$  input is HIGH, the eight outputs are in a high impedance state. The LVX574 is functionally identical to the LVX374 but with inputs and outputs on opposite sides of the package. The inputs tolerate up to 7V allowing interface of 5V systems to 3V systems.

#### Features

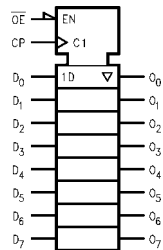
- Input voltage translation from 5V to 3V
- Ideal for low power/low noise 3.3V applications
- Guaranteed simultaneous switching noise level and dynamic threshold performance

#### Ordering Code:

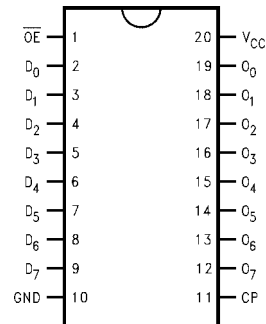
Order Number	Package Number	Package Description
74LVX574M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LVX574SJ	M20D	Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LVX574MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.  
Pb-Free package per JEDEC J-STD-020B.

#### Logic Symbol



#### Connection Diagram



#### Pin Descriptions

Pin Names	Description
D <sub>0</sub> -D <sub>7</sub>	Data Inputs
CP	Clock Pulse Input
$\overline{OE}$	3-STATE Output Enable Input
O <sub>0</sub> -O <sub>7</sub>	3-STATE Outputs

74LVX574 Low Voltage Octal D-Type Flip-Flop with 3-STATE Outputs

## Functional Description

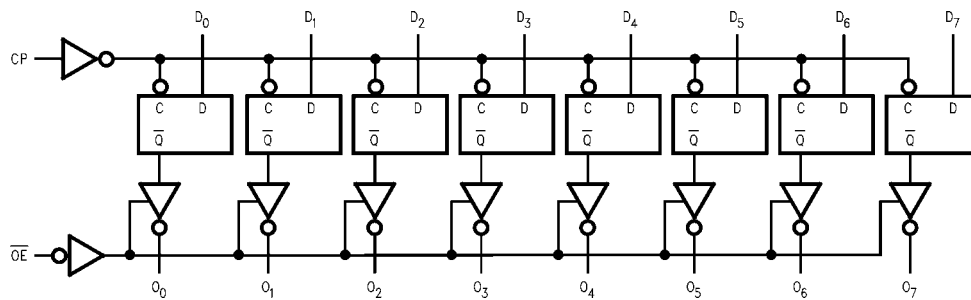
The LVX574 consists of eight edge-triggered flip-flops with individual D-type inputs and 3-STATE true outputs. The buffered clock and buffered Output Enable are common to all flip-flops. The eight flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH Clock (CP) transition. With the Output Enable ( $\overline{OE}$ ) LOW, the contents of the eight flip-flops are available at the outputs. When the  $\overline{OE}$  is HIGH, the outputs go to the high impedance state. Operation of the  $\overline{OE}$  input does not affect the state of the flip-flops.

## Truth Table

Inputs			Outputs
$D_n$	CP	$\overline{OE}$	$O_n$
H	↗	L	H
L	↗	L	L
X	X	H	Z

H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Immaterial  
 Z = High Impedance  
 ↗ = LOW-to-HIGH Transition

## Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
$V_I = -0.5V$	-20 mA
DC Input Voltage ( $V_I$ )	-0.5V to 7V
DC Output Diode Current ( $I_{OK}$ )	
$V_O = -0.5V$	-20 mA
$V_O = V_{CC} + 0.5V$	+20 mA
DC Output Voltage ( $V_O$ )	-0.5V to $V_{CC} + 0.5V$
DC Output Source or Sink Current ( $I_O$ )	$\pm 25$ mA
DC $V_{CC}$ or Ground Current ( $I_{CC}$ or $I_{GND}$ )	$\pm 75$ mA
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C
Power Dissipation	180 mW

**Recommended Operating Conditions** (Note 2)

Supply Voltage ( $V_{CC}$ )	2.0V to 3.6V
Input Voltage ( $V_I$ )	0V to 5.5V
Output Voltage ( $V_O$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $\Delta t/\Delta V$ )	0 ns/V to 100 ns/V

**Note 1:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

**Note 2:** Unused inputs must be held HIGH or LOW. They may not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level Input Voltage	2.0	1.5			1.5		V	
		3.0	2.0			2.0			
		3.6	2.4			2.4			
$V_{IL}$	LOW Level Input Voltage	2.0			0.5		0.5	V	
		3.0			0.8		0.8		
		3.6			0.8		0.8		
$V_{OH}$	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -50 \mu\text{A}$ $I_{OH} = -4 \text{mA}$
		3.0	2.9	3.0		2.9			
		3.0	2.58			2.48			
$V_{OL}$	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 50 \mu\text{A}$ $I_{OL} = 4 \text{mA}$
		3.0		0.0	0.1		0.1		
		3.0			0.36		0.44		
$I_{OZ}$	3-STATE Output Off-State Current	3.6			$\pm 0.25$		$\pm 2.5$	$\mu\text{A}$	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND
$I_{IN}$	Input Leakage Current	3.6			$\pm 0.1$		$\pm 1.0$	$\mu\text{A}$	$V_{IN} = 5.5V$ or GND
$I_{CC}$	Quiescent Supply Current	3.6			4.0		40.0	$\mu\text{A}$	$V_{IN} = V_{CC}$ or GND

**Noise Characteristics** (Note 3)

Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ\text{C}$		Units	$C_L$ (pF)
			Typ	Limit		
$V_{OLP}$	Quiet Output Maximum Dynamic $V_{OL}$	3.3	0.5	0.8	V	50
$V_{OLV}$	Quiet Output Minimum Dynamic $V_{OL}$	3.3	-0.5	-0.8	V	50
$V_{IHD}$	Minimum HIGH Level Dynamic Input Voltage	3.3		2.0	V	50
$V_{ILD}$	Maximum LOW Level Dynamic Input Voltage	3.3		0.8	V	50

**Note 3:** (Input  $t_r = t_f = 3$  ns)

AC Electrical Characteristics (Note 4)									
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
f <sub>MAX</sub>	Maximum Clock Frequency	2.7	60	115		50		MHZ	C <sub>L</sub> = 15 pF
			45	60		40			C <sub>L</sub> = 50 pF
		3.3 ± 0.3	80	125		65			C <sub>L</sub> = 15 pF
			50	75		45			C <sub>L</sub> = 50 pF
t <sub>PLH</sub>	Propagation Delay Time CP to O <sub>n</sub>	2.7		9.2	14.5	1.0	17.5	ns	C <sub>L</sub> = 15 pF
t <sub>PHL</sub>				11.5	18.0	1.0	21.0		C <sub>L</sub> = 50 pF
3.3 ± 0.3			8.5	13.2	1.0	15.5	C <sub>L</sub> = 15 pF		
			11.0	16.7	1.0	19.0	C <sub>L</sub> = 50 pF		
t <sub>PZL</sub>	3-STATE Output Enable Time	2.7		9.8	15.0	1.0	18.5	ns	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ
t <sub>PZH</sub>				11.4	18.5	1.0	22.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
3.3 ± 0.3			8.2	12.8	1.0	15.0	C <sub>L</sub> = 15 pF, R <sub>L</sub> = 1 kΩ		
			10.7	16.3	1.0	18.5	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ		
t <sub>PLZ</sub>	3-STATE Output Disable Time	2.7		12.1	19.1	1.0	22.0	ns	C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>PHZ</sub>		3.3 ± 0.3		11.0	15.0	1.0	17.0		C <sub>L</sub> = 50 pF, R <sub>L</sub> = 1 kΩ
t <sub>w</sub>	CP Pulse	2.7	6.5			7.5		ns	
	Width	3.3 ± 0.3	5.0			5.0			
t <sub>S</sub>	Setup Time	2.7	5.0			5.0		ns	
	D <sub>n</sub> to CP	3.3 ± 0.3	3.5			3.5			
t <sub>H</sub>	Hold Time	2.7	1.5			1.5		ns	
	D <sub>n</sub> to CP	3.3 ± 0.3	1.5			1.5			
t <sub>OSHL</sub>	Output to Output	2.7			1.5		1.5	ns	C <sub>L</sub> = 50 pF
t <sub>OSLH</sub>	Skew (Note 4)	3.3			1.5		1.5		

**Note 4:** Parameter guaranteed by design. t<sub>OSLH</sub> = |t<sub>PLHm</sub> - t<sub>PLHn</sub>|, t<sub>OSHL</sub> = |t<sub>PHLm</sub> - t<sub>PHLn</sub>|.

### Capacitance

Symbol	Parameter	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units
		Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance		4	10		10	pF
C <sub>OUT</sub>	Output Capacitance		6				pF
C <sub>PD</sub>	Power Dissipation Capacitance (Note 5)		27				pF

**Note 5:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

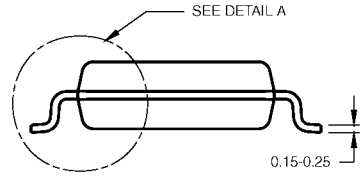
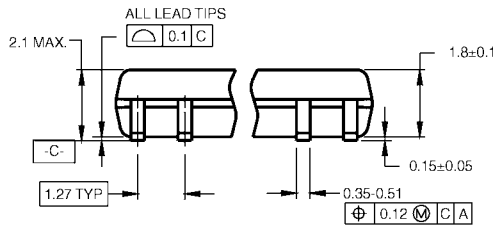
$$\text{Average operating current can be obtained by the equation: } I_{CC(\text{opr})} = \frac{C_{PD} \times V_{CC} \times f_{IN} + I_{CC}}{8 \text{ (per latch)}}$$

**Physical Dimensions** inches (millimeters) unless otherwise noted



**20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide  
Package Number M20B**

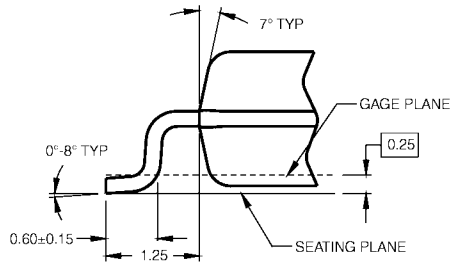
**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

- NOTES:  
 A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.  
 B. DIMENSIONS ARE IN MILLIMETERS.  
 C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

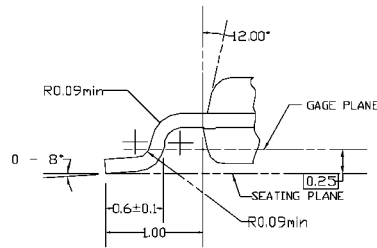
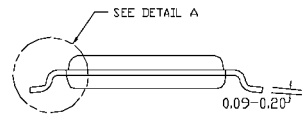
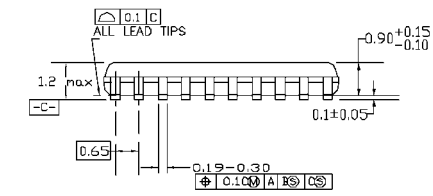
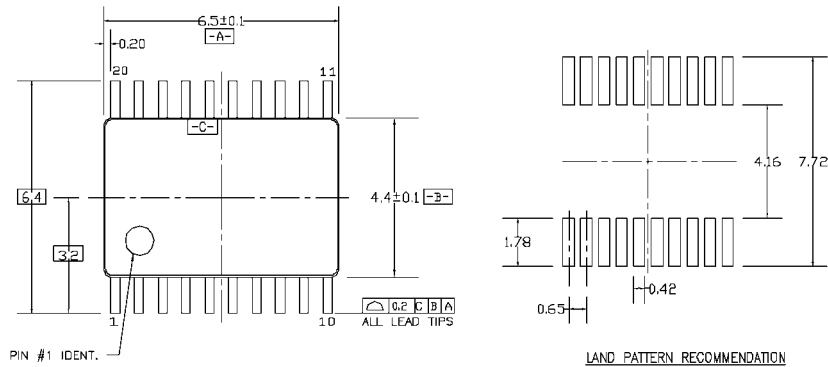
M20DRevB1



DETAIL A

**Pb-Free 20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20REVD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20**

Fairchild does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied and Fairchild reserves the right at any time without notice to change said circuitry and specifications.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

[www.fairchildsemi.com](http://www.fairchildsemi.com)