Order number: MC100ES6226
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2.5/3.3 V Differential LVPECL 1:9 Clock Distribution Buffer and Clock Divider

MC100ES6226

2.5V/3.3V DIFFERENTIAL LVPECL 1:9 CLOCK DISTRIBUTION BUFFER AND CLOCK DIVIDER

FA SUFFIX
32-LEAD LQFP PACKAGE
CASE 873A-03

The MC100ES6226 is a bipolar monolithic differential clock distribution buffer and clock divider. Designed for most demanding clock distribution systems, the MC100ES6226 supports various applications requiring a large number of outputs to drive precisely aligned clock signals. Using SiGe technology and a fully differential architecture, the device offers superior digital signal characteristics and very low clock skew error. Target applications for this clock driver are high performance clock distribution systems for computing, networking and telecommunication systems.

Features

- Fully differential architecture from input to all outputs
- SiGe technology supports near-zero output skew
- Selectable 1:1 or 1:2 frequency outputs
- LVPECL compatible differential clock inputs and outputs
- LVCMOS compatible control inputs
- Single 3.3V or 2.5V supply
- Max. 35 ps maximum output skew (within output bank)
- Max. 50 ps maximum device skew
- Supports DC operation and up to 3 GHz (typ.) clock signals
- Synchronous output enable eliminating output runt pulse generation and metastability
- Standard 32-lead LQFP package
- Industrial temperature range
- 32-lead Pb-free Package Available

Functional Description

MC100ES6226 is designed for very skew critical differential clock distribution systems and supports clock frequencies from DC up to 3.0 GHz. Typical applications for the MC100ES6226 are primary clock distribution systems on backplanes of high-performance computer, networking and telecommunication systems, as well as on-board clocking of OC-3, OC-12 and OC-48 speed communication systems.

The MC100ES6226 can be operated from a 3.3 V or 2.5 V positive supply without the requirement of a negative supply line. Each of the output banks of three differential clock output pairs may be independently configured to distribute the input frequency or half of the input frequency. The FSEL0 and FSEL1 clock frequency selects are asychronous control inputs. Any changes of the control inputs require a MR pulse for resynchronization of the ÷2 outputs.

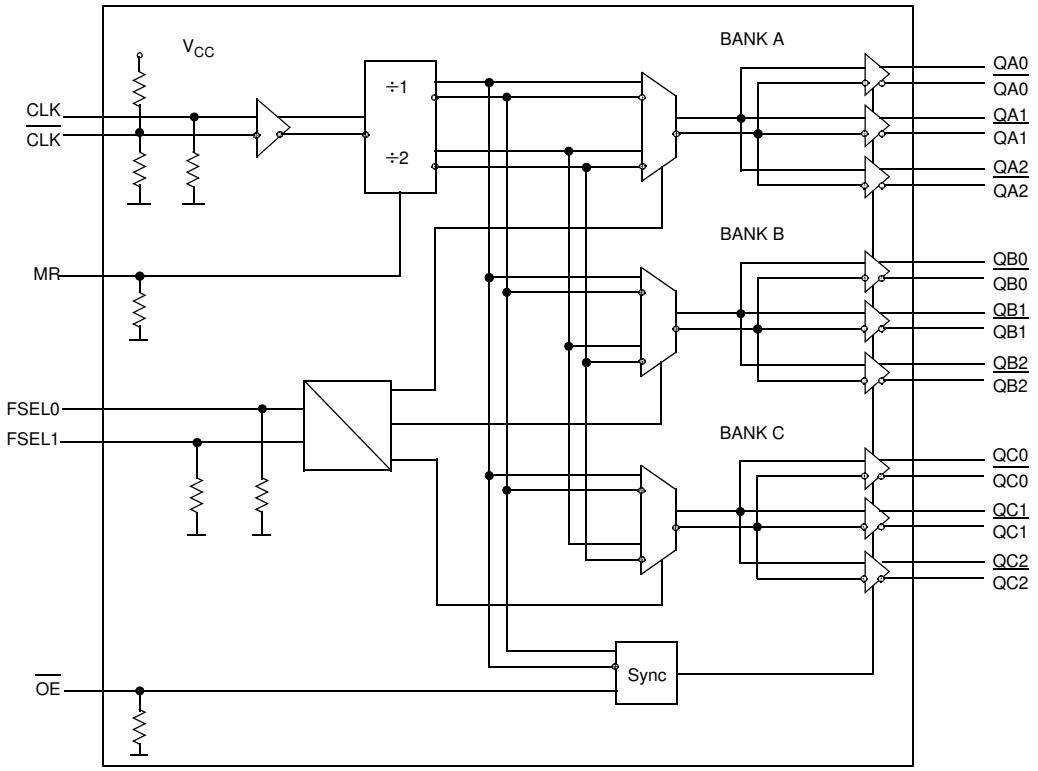

Figure 1. MC100ES6226 Logic Diagram

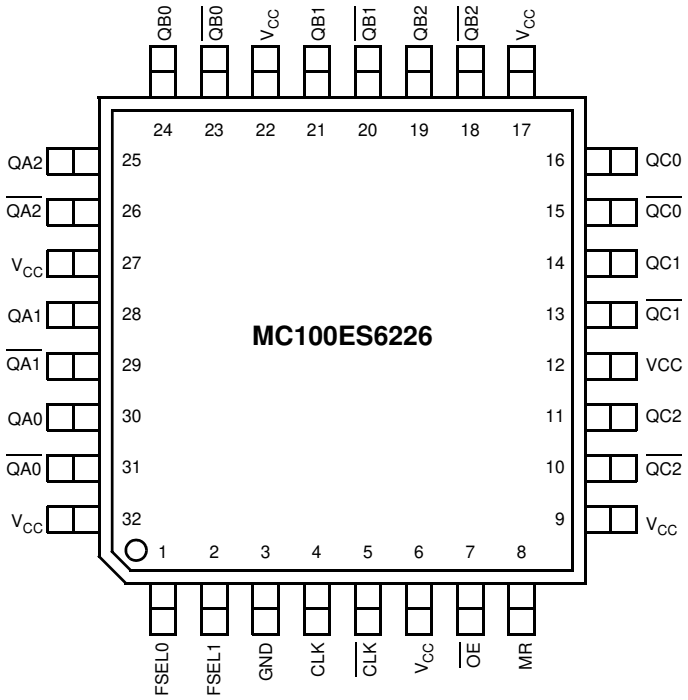

Figure 2. 32-Lead Package Pinout (Top View)

Table 1. Pin Configuration

Pin	I/O	Type	Function
CLK, $\overline{CLK}$	Input	LVPECL	Differential reference clock signal input
$\overline{OE}$	Input	LVCMOS	Output enable
MR	Input	LVCMOS	Device reset
FSEL0, FSEL1	Input	LVCMOS	Output frequency divider select
QA[0-2], $\overline{QA[0–2]}$ QB[0-2], $\overline{QB[0–2]}$ QC[0-2], $\overline{QC[0–2]}$	Output	LVPECL	Differential clock outputs (banks A, B and C)
GND	Supply	GND	Negative power supply
V_{CC}	Supply	V_{CC}	Positive power supply. All V_{CC} pins must be connected to the positive power supply for correct DC and AC operation

Table 2. Function Table

Control	Default	0	1
$\overline{OE}$	0	Qx[0–2], $\overline{Qx[0–2]}$ are active. Deassertion of $\overline{OE}$ can be asynchronous to the reference clock without generation of output runt pulses	Qx[0–2] = L, $\overline{Qx[0–2]}$ =H (outputs disabled). Assertion of $\overline{OE}$ can be asynchronous to the reference clock without generation of output runt pulses
MR	0	Normal operation	Device reset (asynchronous)
FSEL0, FSEL1	00	See Table 3	

Table 3. Output Frequency Select Control

FSEL0	FSEL1	QA0 to QA2	QB0 to QB2	QC0 to QC2
0	0	$f_{QA0:2} = f_{CLK}$	$f_{QB0:2} = f_{CLK}$	$f_{QC0:2} = f_{CLK}$
0	1	$f_{QA0:2} = f_{CLK}$	$f_{QB0:2} = f_{CLK}$	$f_{QC0:2} = f_{CLK} \div 2$
1	0	$f_{QA0:2} = f_{CLK}$	$f_{QB0:2} = f_{CLK} \div 2$	$f_{QC0:2} = f_{CLK} \div 2$
1	1	$f_{QA0:2} = f_{CLK} \div 2$	$f_{QB0:2} = f_{CLK} \div 2$	$f_{QC0:2} = f_{CLK} \div 2$

Table 4. Absolute Maximum Ratings[1]

Symbol	Characteristics	Min	Max	Unit	Condition
V_{CC}	Supply Voltage	-0.3	3.6	V	
V_{IN}	DC Input Voltage	-0.3	V_{CC}+0.3	V	
V_{OUT}	DC Output Voltage	-0.3	V_{CC}+0.3	V	
I_{IN}	DC Input Current		±20	mA	
I_{OUT}	DC Output Current		±50	mA	
T_S	Storage Temperature	-65	125	°C	

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

Table 5. General Specifications

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{TT}	Output Termination Voltage		$V_{CC} - 2$[1]		V	
MM	ESD Protection (Machine model)	200			V	
HBM	ESD Protection (Human body model)	2000			V	
CDM	ESD Protection (Charged device model)	1000			V	
LU	Latch-up Immunity	200			mA	
C_{IN}			4.0		pF	Inputs
θ_{JA}	Thermal Resistance Junction to Ambient					
	JESD 51-3, single layer test board		83.1	86.0	°C/W	Natural convection
			73.3	75.4	°C/W	100 ft/min
			68.9	70.9	°C/W	200 ft/min
			63.8	65.3	°C/W	400 ft/min
			57.4	59.6	°C/W	800 ft/min
	JESD 51-6, 2S2P multilayer test board		59.0	60.6	°C/W	Natural convection
			54.4	55.7	°C/W	100 ft/min
			52.5	53.8	°C/W	200 ft/min
			50.4	51.5	°C/W	400 ft/min
			47.8	48.8	°C/W	800 ft/min
θ_{JC}	Thermal Resistance Junction to Case		23.0	26.3	°C/W	MIL-SPEC 883E Method 1012.1
	Operating Junction Temperature[2] (continuous operation) MTBF = 9.1 years	0		110	°C	

1. Output termination voltage V_{TT} = 0 V for V_{CC} = 2.5 V operation is supported but the power consumption of the device will increase.
2. Operating junction temperature impacts device life time. Maximum continuous operating junction temperature should be selected according to the application life time requirements (See application note AN1545 for more information). The device AC and DC parameters are specified up to 110°C junction temperature allowing the MC100ES6226 to be used in applications requiring industrial temperature range. It is recommended that users of the MC100ES6226 employ thermal modeling analysis to assist in applying the junction temperature specifications to their particular application.

Table 6. DC Characteristics (V_{CC} = 3.3 V ± 5% and 2.5 V ± 5%, T_J = 0°C to +110°C)[1]

Symbol	Characteristics		Min	Typ	Max	Unit	Condition
LVCMOS Control Inputs ($\overline{OE}$, FSEL0, FSEL1, MR)							
V_{IL}	Input voltage low	V_{CC} = 3.3 V V_{CC} = 2.5 V			0.8 0.7	V	
V_{IH}	Input voltage high	V_{CC} = 3.3 V V_{CC} = 2.5 V	2.2 1.7			V	
I_{IN}	Input Current[2]				±150	μA	V_{IN} = V_{CC} or V_{IN} = GND
LVPECL Clock Inputs (CLK, $\overline{CLK}$)[3]							
V_{PP}	DC Differential Input Voltage[4]		0.1		1.3	V	Differential operation
V_{CMR}	Differential Cross Point Voltage[5]		1.0		V_{CC} – 0.3	V	Differential operation
V_{IH}	Input High Voltage		TBD		TBD		
V_{IL}	Input Low Voltage		TBD		TBD		
I_{IN}	Input Current				±150	μA	V_{IN} = TBD or V_{IN} = TBD
LVPECL Clock Outputs (QA[2:0], QB[2:0], QC[2:0])							
V_{OH}	Output High Voltage		V_{CC} – 1.1		V_{CC} – 0.8	V	Termination 50Ω to V_{TT}
V_{OL}	Output Low Voltage		V_{CC} – 1.8		V_{CC} – 1.4	V	Termination 50Ω to V_{TT}
Supply Current							
I_{GND}	Maximum Quiescent Supply Current without Output Termination Current			65	110	mA	GND pin
I_{CC}	Maximum Quiescent Supply Current with Output Termination Current			325	400	mA	All V_{CC} pins

1. AC characteristics are design targets and pending characterization.
2. Input have internal pullup/pulldown resistors which affect the input current.
3. Clock inputs driven by LVPECL compatible signals.
4. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristic.
5. V_{CMR} (DC) is the crosspoint of the differential input signal. Functional operation is obtained when the crosspoint is within the V_{CMR} (DC) range and the input swing lies within the V_{PP} (DC) specification.

Table 7. AC Characteristics (V_{CC} = 3.3 V ± 5% and 2.5 V ± 5%, T_J = 0°C to +110°C)[1, 2]

Symbol	Characteristics	Min	Typ	Max	Unit	Condition
V_{PP}	Differential Input Voltage[3] (peak-to-peak)	0.2	0.3	1.3	V	
V_{CMR}	Differential Input Crosspoint Voltage[4]	1.0		V_{CC} – 0.3	V	
$V_{X,OUT}$	Differential Output Crosspoint Voltage	V_{CC} – 1.45		V_{CC} – 1.1	V	
$V_{O(P-P)}$	Differential Output Voltage (peak-to-peak) f_O < 300 MHz f_O < 1.5 GHz f_O < 2.7 GHz	 0.45 0.3 TBD	 0.72 0.55 0.37	 0.95 0.95 0.95	 V V V	
f_{CLK}	Input Frequency	0		3000[5]	MHz	
t_{PD}	Propagation Delay CLK to Qx[]	475	500	800	ps	Differential
$t_{sk(O)}$	Output-to-Output Skew (within QA[2:0]) (within QB[2:0]) (within QC[2:0]) (within device)		 11 12 4	 25 25 20 60	 ps ps ps ps	Differential
$t_{sk(PP)}$	Output-to-Output Skew (part-to-part)			325	ps	Differential
$t_{JIT(CC)}$	Output Cycle-to-Cycle Jitter single frequency configuration ÷1/÷2 frequency configuration			 1 1		 FSEL0 = FSEL1 FSEL0 ≠ FSEL1
DC_O	Output Duty Cycle Qx = ÷1, f_O < 300 MHz Qx = ÷1, f_O > 300 MHz Qx = ÷2, f_O < 300 MHz Qx = ÷2, f_O > 300 MHz	48 45 49 47.5	50 50 50 50	52 55 51 52.5	% % % %	DC_{fref}= 50%[7]
t_r, t_f	Output Rise/Fall Time	0.05		200	ns	20% to 80%
t_{PDL}[6]	Output Disable Time	2.5·T + t_{PD}		4.5·T + t_{PD}	ns	T=CLK period
t_{PLD}[7]	Output Enable Time	3·T + t_{PD}		5·T + t_{PD}	ns	T=CLK period

1. AC characteristics are design targets and pending characterization.
2. AC characteristics apply for parallel output termination of 50Ω to V_{TT}.
3. V_{PP} is the minimum differential input voltage swing required to maintain AC characteristics including tpd and device-to-device skew.
4. V_{CMR} (AC) is the crosspoint of the differential input signal. Normal AC operation is obtained when the crosspoint is within the V_{CMR} (AC) range and the input swing lies within the V_{PP} (AC) specification. Violation of V_{CMR} (AC) or V_{PP} (AC) impacts the device propagation delay, device and part-to-part skew.
5. The MC100ES6226 is fully operational up to 3.0 GHz and is characterized up to 2.7 GHz.
6. Propagation delay $\overline{OE}$ deassertion to differential output disabled (differential low: true output low, complementary output high).
7. Propagation delay $\overline{OE}$ assertion to output enabled (active).

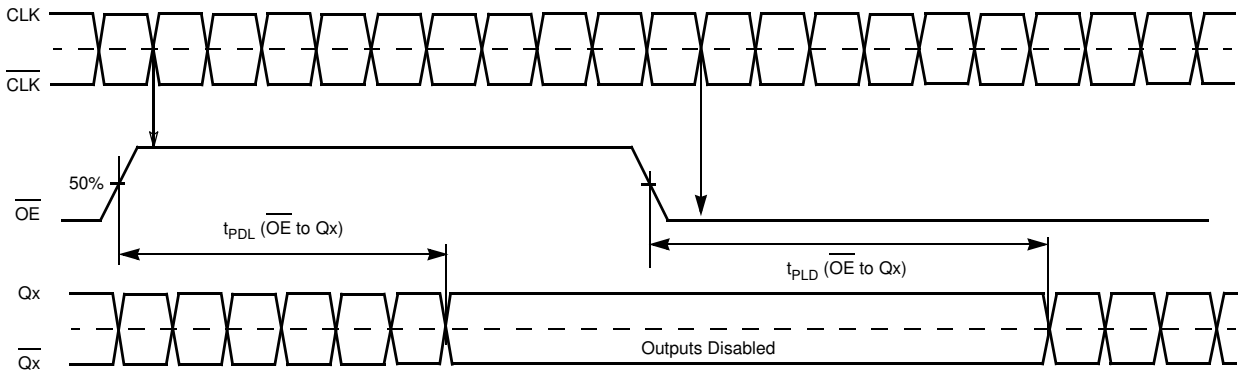

Figure 3. MC100ES6226 Output Disable/Enable Timing

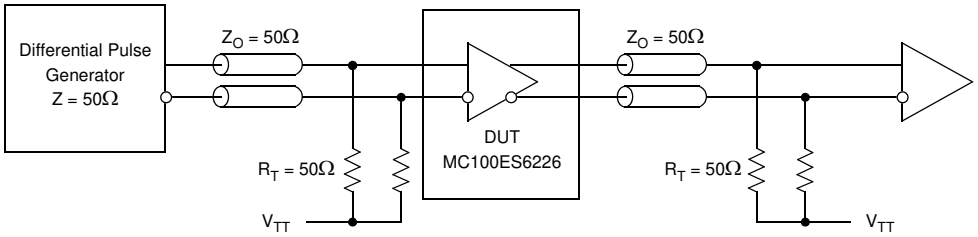

Figure 4. MC100ES6226 AC Test Reference

APPLICATIONS INFORMATION

Maintaining Lowest Device Skew

The MC100ES6226 guarantees low output-to-output bank skew of 35 ps and a part-to-part skew of max. TBD ps. To ensure low skew clock signals in the application, both outputs of any differential output pair need to be terminated identically, even if only one output is used. When fewer than all nine output pairs are used, identical termination of all output pairs within the output bank is recommended. If an entire output bank is not used, it is recommended to leave all of these outputs open and unterminated. This will reduce the device power consumption while maintaining minimum output skew.

Power Supply Bypassing

The MC100ES6226 is a mixed analog/digital product. The differential architecture of the MC100ES6226 supports low noise signal operation at high frequencies. In order to maintain its superior signal quality, all V_{CC} pins should be bypassed by high-frequency ceramic capacitors connected to GND. If the spectral frequencies of the internally generated switching noise on the supply pins cross the series resonant point of an individual bypass capacitor, its overall impedance begins to look inductive and thus increases with increasing frequency. The parallel capacitor combination shown ensures that a low impedance path to ground exists for frequencies well above the noise bandwidth.

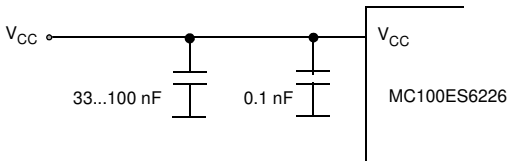

Figure 5. V_{CC} Power Supply Bypass