TPS7A3401 –20-V, –200-mA, Low-Noise Negative Voltage Regulator

1 Features

- Input Voltage Range: –3 V to –20 V
- Noise:
  - 80 μV_{RMS} (10 Hz to 100 kHz)
- Power-Supply Ripple Rejection:
  - 50 dB (1 kHz)
  - ≥ 27 dB (10 Hz to 1 MHz)
- Adjustable Output:
  Approximately –1.18 V to –18 V
- Maximum Output Current: 200 mA
- Dropout Voltage: 500 mV at 100 mA
- Stable With Ceramic Capacitors ≥ 2.2 µF
- CMOS Logic-Level-Compatible Enable Pin
- Built-In, Fixed, Current Limit, and Thermal Shutdown Protection
- Available in High Thermal Performance MSOP-8 PowerPAD™ Package
- Operating Temperature Range: –40°C to 125°C

2 Applications

- Cost-Effective Supply Rails for Op Amps, DACs, ADCs, and Other High-Precision Analog Circuitry
- Cost-Effective Post DC-DC Converter Regulation and Ripple Filtering

3 Description

The TPS7A3401 device is a negative, high-voltage (–20-V), low-noise linear regulator capable of sourcing a maximum load of 200 mA.

These linear regulators include a CMOS logic-level-compatible enable pin. Other features available include built-in current limit and thermal shutdown protection to safeguard the device and system during fault conditions.

The TPS7A3401 is designed using bipolar technology, and is ideal for instrumentation applications where clean voltage rails are critical for improving system performance. This design makes it a cost-effective choice to power operational amplifiers, analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and other analog circuitry.

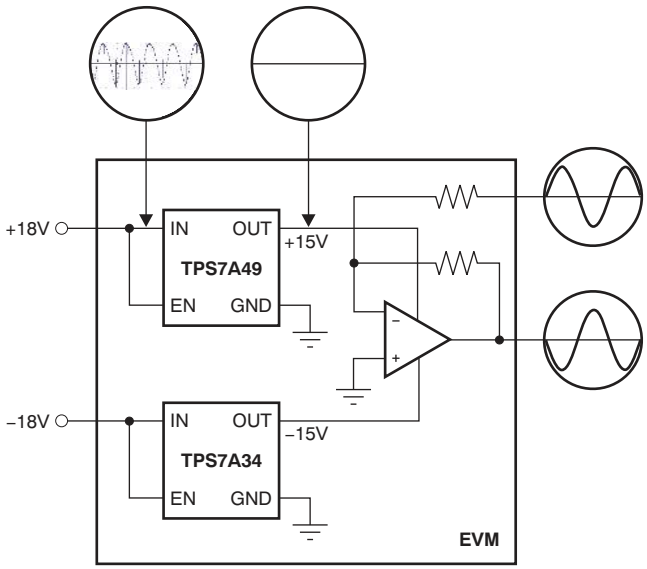
In addition, the TPS7A3401 linear regulator is suitable for cost-effective, post DC-DC converter regulation. By filtering out the output voltage ripple inherent to DC-DC switching conversion, increased system performance is provided in instrumentation applications.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS7A3401	HVSSOP (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Post DC-DC Converter Regulation



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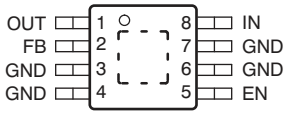
4 Revision History

Changes from Original (June 2011) to Revision A **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1
- Changed Pin Configuration and Functions section; updated table format ... 3
- Changed *Thermal Information* table; updated values ... 5
- Changed parametric symbol for current limit from I_{LIM} to I_{CL} ... 5

5 Pin Configuration and Functions

DGN Package
8-Pin HVSSOP
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
OUT	1	O	Regulator output. A capacitor ≥ 2.2 µF must be tied from this pin to ground to ensure stability.
FB	2	I	This pin is the feedback pin that sets the output voltage of the device.
GND	3, 4, 6, 7	—	Ground
EN	5	I	This pin turns the regulator ON or OFF. If $V_{EN} \geq V_{EN(+HI)}$ or $V_{EN} \leq V_{EN(–HI)}$, the regulator is enabled. If $V_{EN(+LO)} \geq V_{EN} \geq V_{EN(–LO)}$, the regulator is disabled. The EN pin can be connected to IN, if not used. $\lvert V_{EN} \rvert \leq \lvert V_{IN} \rvert$.
IN	8	I	Input supply. A capacitor ≥ 2.2 µF must be tied from this pin to ground to ensure stability.
PowerPAD	—	—	Must either be left floating or tied to GND. Solder to printed-circuit-board (PCB) plane to enhance thermal performance.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted).(1)

		MIN	MAX	UNIT
Voltage	IN pin to GND pin	–22	0.3	V
	OUT pin to GND pin	–22	0.3	
	OUT pin to IN pin	–0.3	22	
	FB pin to GND pin	–2	0.3	
	FB pin to IN pin	–0.3	22	
	EN pin to IN pin	–0.3	22	
	EN pin to GND pin	–22	22	
	NR/SS pin to IN pin	–0.3	22	
	NR/SS pin to GND pin	–2	0.3	
Current	Peak output	Internally limited		
Temperature	Operating virtual junction, T_J	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated is not implied. Exposure to absolute-maximum rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted).

		MIN	NOM	MAX	UNIT
V_{IN}	Input supply voltage	–20		–3	V
V_{EN}	Enable supply voltage	0		V_{IN}	V
V_{OUT}	Output voltage	V_{REF}		–18	V
I_{OUT}	Output current	0		200	mA
T_J	Operating junction temperature	–40		125	°C
C_{IN}	Input capacitor	2.2	10		µF
C_{OUT}	Output capacitor	2.2	10		µF
C_{FF}	Feed-forward capacitor	0	10		nF
R_2	Lower feedback resistor			237	kΩ

6.4 Thermal Information

THERMAL METRIC[1]		TPS7A3401 DGN (HVSSOP) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	63.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	53	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	37.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	37.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	13.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

At T_J = –40°C to 125°C, $|V_{IN}| = |V_{OUT(nom)}| + 1$ V or $|V_{IN}|$ = 3 V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and the FB pin tied to OUT, unless otherwise noted.[1]

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage		–20		–3	V
V_{REF}	Internal reference	T_J = 25°C, $V_{FB} = V_{REF}$	–1.202	–1.184	–1.166	V
V_{OUT}	Output voltage[2]	$\|V_{IN}\| \geq \|V_{OUT(nom)}\| + 1$ V	–18		V_{REF}	V
	Nominal accuracy	T_J = 25°C, $\|V_{IN}\| = \|V_{OUT(nom)}\| + 0.5$ V	–1.5		1.5	$\%V_{OUT}$
	Overall accuracy	$\|V_{OUT(nom)}\| + 1$ V ≤ $\|V_{IN}\|$ ≤ 20 V 1 mA ≤ I_{OUT} ≤ 200 mA	–2.5		2.5	$\%V_{OUT}$
$\left\|\frac{\Delta V_{OUT}(\Delta V_{IN})}{V_{OUT(NOM)}}\right\|$	Line regulation	T_J = 25°C, $\|V_{OUT(nom)}\| + 1$ V ≤ $\|V_{IN}\|$ ≤ 20 V		0.14		$\%V_{OUT}$
$\left\|\frac{\Delta V_{OUT}(\Delta I_{OUT})}{V_{OUT(NOM)}}\right\|$	Load regulation	T_J = 25°C, 1 mA ≤ I_{OUT} ≤ 200 mA		0.04		$\%V_{OUT}$
$\|V_{DO}\|$	Dropout voltage	V_{IN} = 95% $V_{OUT(nom)}$, I_{OUT} = 100 mA		216		mV
		V_{IN} = 95% $V_{OUT(nom)}$, I_{OUT} = 200 mA		500	800	mV
I_{CL}	Current limit	V_{OUT} = 90% $V_{OUT(nom)}$	200	330	500	mA
I_{GND}	Ground current	I_{OUT} = 0 mA		55	100	µA
		I_{OUT} = 100 mA		950		µA
$\|I_{SHDN}\|$	Shutdown supply current	V_{EN} = 0.4 V		1	5	µA
		V_{EN} = –0.4 V		1	5	µA
I_{FB}	Feedback current[3]			14	100	nA
$\|I_{EN}\|$	Enable current	$V_{EN} = \|V_{IN}\| = \|V_{OUT(nom)}\| + 1$ V		0.48	1	µA
		$V_{IN} = V_{EN}$ = –20 V		0.51	1	µA
		V_{IN} = –20 V, V_{EN} = 15 V		0.50	1	µA
$V_{EN(+HI)}$	Positive enable high-level voltage	T_J = –40°C to 125°C	2		15	V
		T_J = –40°C to 85°C	1.8		15	
$V_{EN(+LO)}$	Positive enable low-level voltage		0		0.4	V
$V_{EN(–HI)}$	Negative enable high-level voltage		V_{IN}		–2	V
$V_{EN(–LO)}$	Negative enable low-level voltage		–0.4		0	V
V_n	Output noise voltage	V_{IN} = –3 V, $V_{OUT(nom)} = V_{REF}$, C_{OUT} = 10 µF, BW = 10 Hz to 100 kHz		80		μV_{RMS}
PSRR	Power-supply rejection ratio	V_{IN} = –6.2 V, $V_{OUT(nom)}$ = –5 V, C_{OUT} = 10 µF, f = 1 kHz		50		dB
T_{SD}	Thermal shutdown temperature	Shutdown, temperature increasing		170		°C
		Reset, temperature decreasing		150		

(1) At operating conditions, $V_{IN} \leq 0$ V, $V_{OUT(nom)} \leq V_{REF} \leq 0$ V. At regulation, $V_{IN} \leq V_{OUT(nom)} - |V_{DO}|$. $I_{OUT} > 0$ flows from OUT to IN.
(2) To ensure stability at no load conditions, a current from the feedback resistive network equal to or greater than 5 µA is required.
(3) $I_{FB} > 0$ flows into the device.

Electrical Characteristics (continued)

At T_J = –40°C to 125°C, $|V_{IN}| = |V_{OUT(nom)}| + 1$ V or $|V_{IN}|$ = 3 V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and the FB pin tied to OUT, unless otherwise noted.(1)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_J	Operating junction temperature		–40		125	°C

6.6 Typical Characteristics

At T_J = –40°C to 125°C, $|V_{IN}| = |V_{OUT(nom)}| + 1$ V or $|V_{IN}| = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and the FB pin tied to OUT, unless otherwise noted.

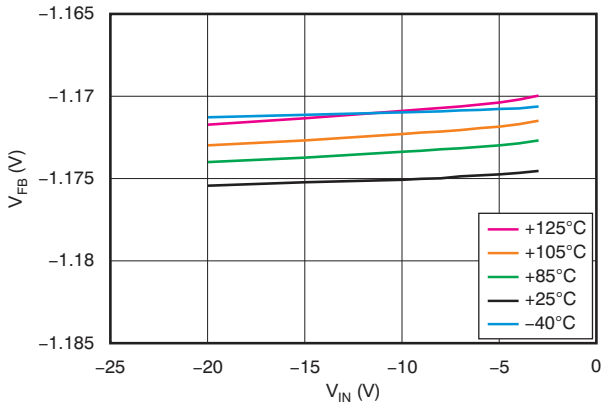


Figure 1. Feedback Voltage vs Input Voltage

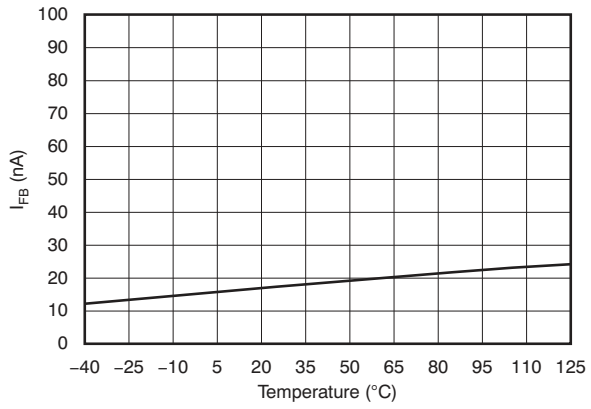


Figure 2. Feedback Current vs Temperature

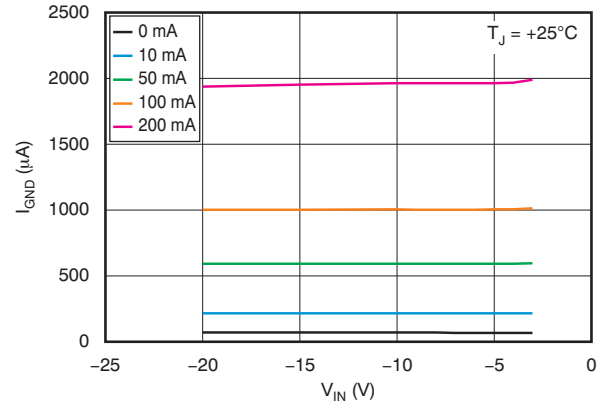


Figure 3. Ground Current vs Input Voltage

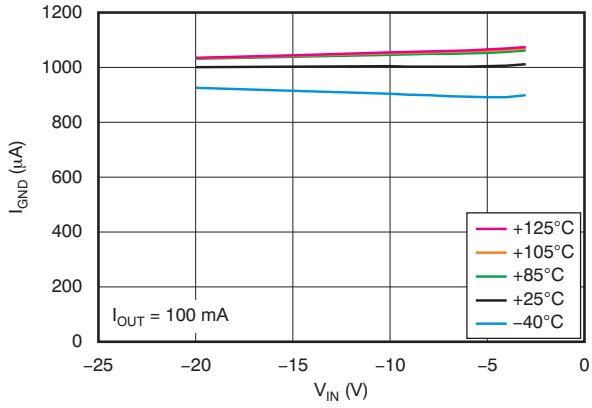


Figure 4. Ground Current vs Input Voltage

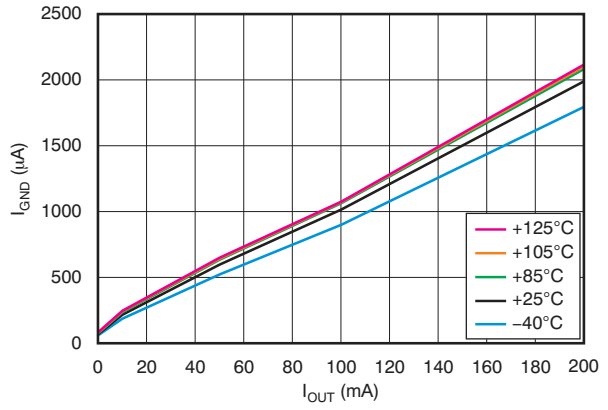


Figure 5. Ground Current vs Output Current

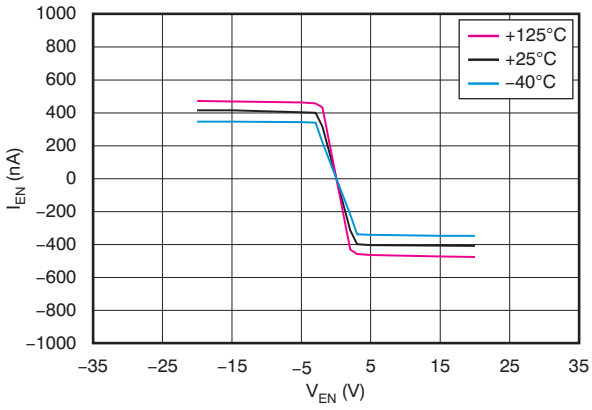


Figure 6. Enable Current vs Enable Voltage

Typical Characteristics (continued)

At T_J = –40°C to 125°C, $|V_{IN}| = |V_{OUT(nom)}| + 1$ V or $|V_{IN}| = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and the FB pin tied to OUT, unless otherwise noted.

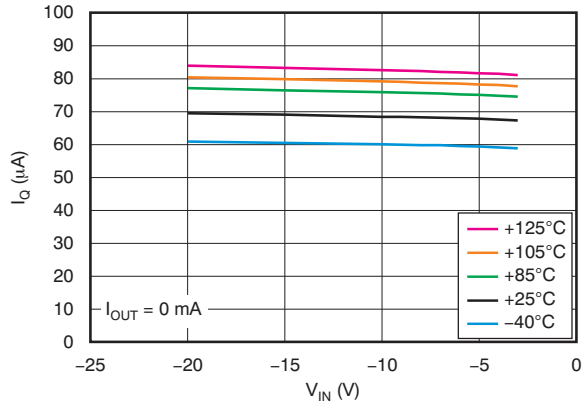


Figure 7. Quiescent Current vs Input Voltage

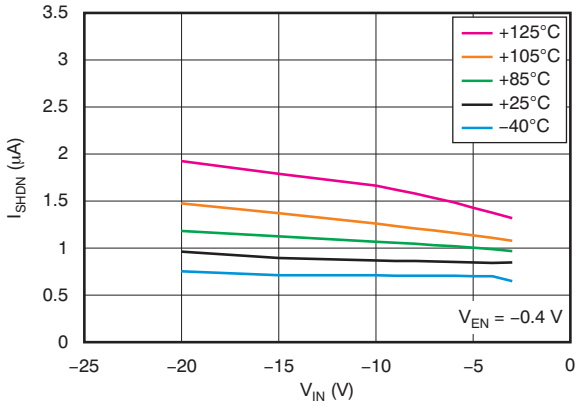


Figure 8. Shutdown Current vs Input Voltage

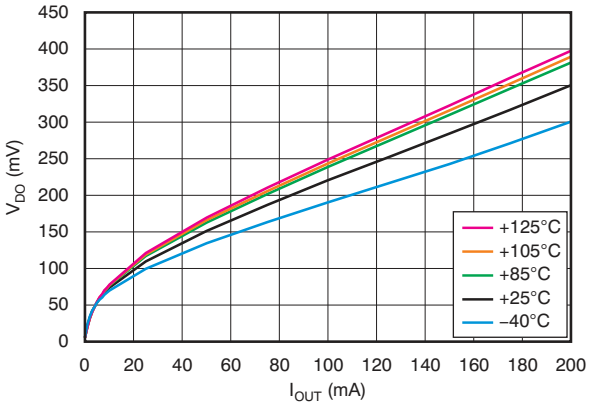


Figure 9. Dropout Voltage vs Output Current

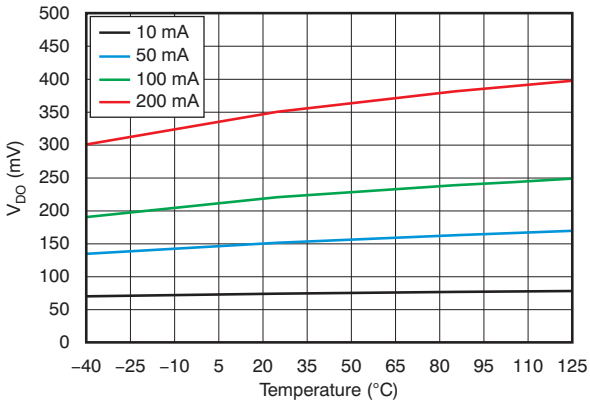


Figure 10. Dropout Voltage vs Temperature

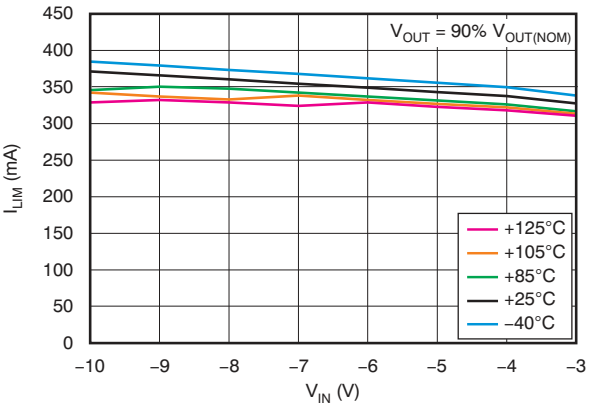


Figure 11. Current Limit vs Input Voltage

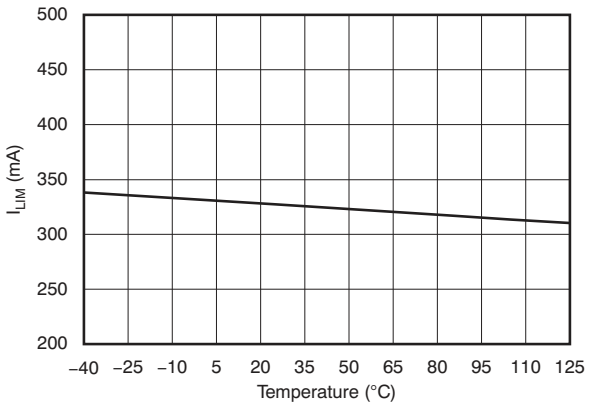


Figure 12. Current Limit vs Temperature

Typical Characteristics (continued)

At T_J = –40°C to 125°C, $|V_{IN}| = |V_{OUT(nom)}| + 1$ V or $|V_{IN}| = 3$ V (whichever is greater), $V_{EN} = V_{IN}$, I_{OUT} = 1 mA, C_{IN} = 2.2 µF, C_{OUT} = 2.2 µF, and the FB pin tied to OUT, unless otherwise noted.

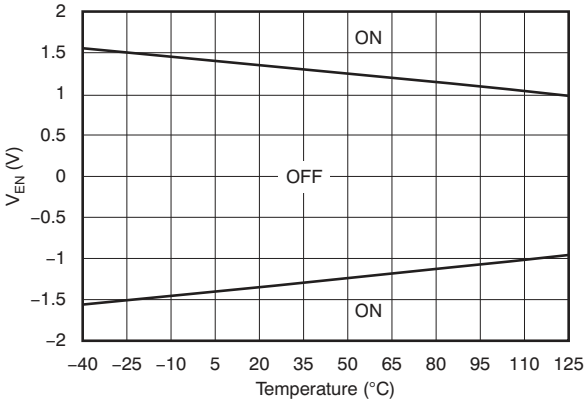


Figure 13. Enable Threshold Voltage vs Temperature

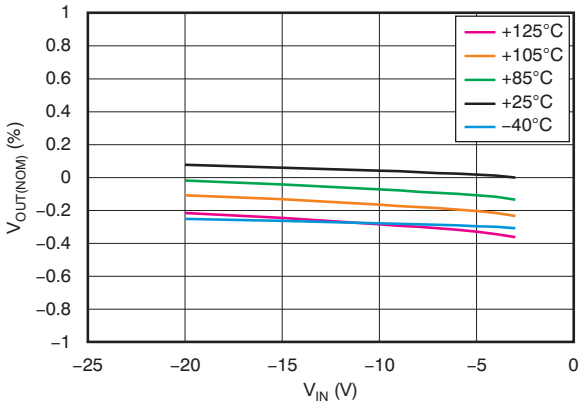


Figure 14. Line Regulation

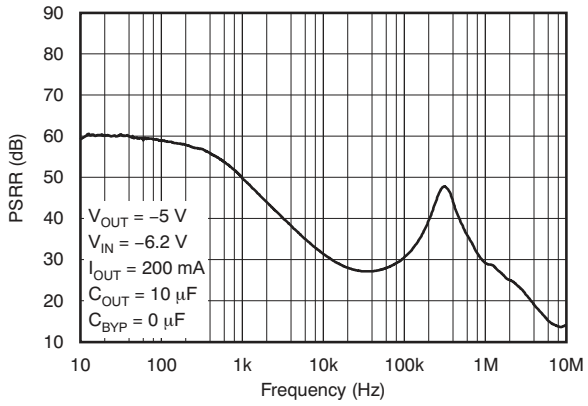


Figure 15. Power-Supply Rejection Ratio

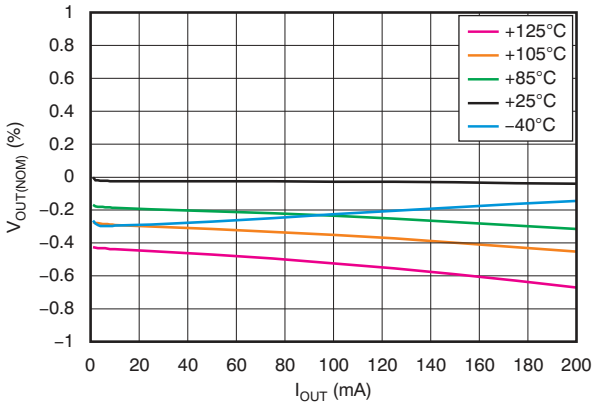


Figure 16. Load Regulation

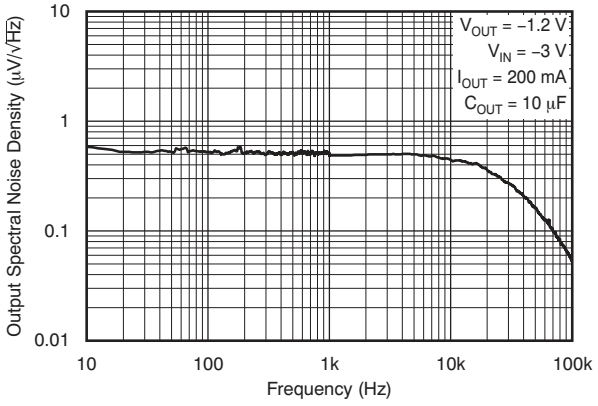


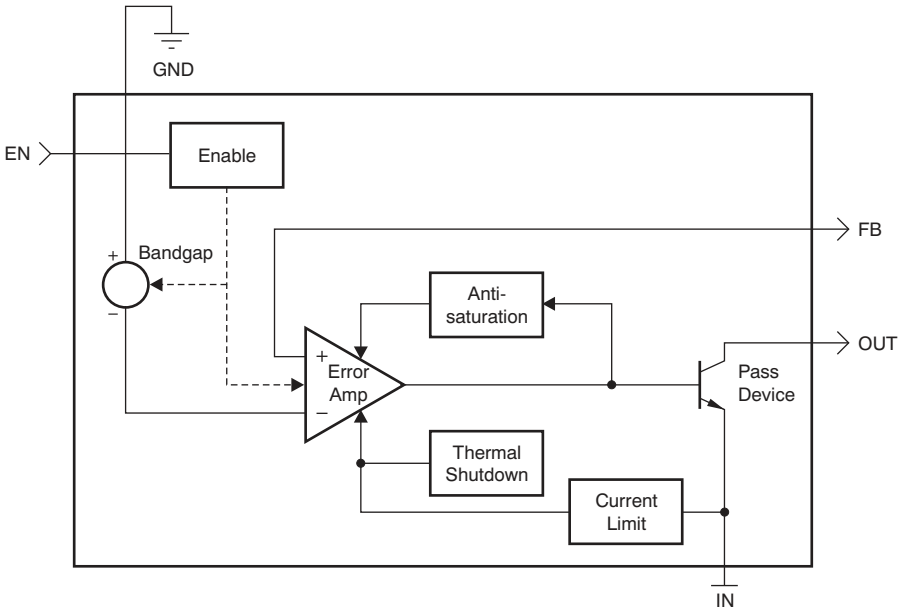
Figure 17. Output Spectral Noise Density

7 Detailed Description

7.1 Overview

The TPS7A3401 device is a wide V_{IN}, low-noise, 150-mA linear regulator (LDO). This device features an enable pin, programmable soft-start, current limiting, and thermal protection circuitry that allow the device to be used in a wide variety of applications. As a bipolar-based device, the TPS7A3401 device is ideal for high-accuracy, high-precision applications at higher voltages.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Internal Current Limit

The fixed internal current limit of the TPS7A3401 device helps protect the regulator during fault conditions. The maximum amount of current the device can source is the current limit (330 mA, typical), and it is largely independent of output voltage. For reliable operation, do not operate the device in current limit for extended periods of time.

7.3.2 Enable Pin Operation

The TPS7A3401 device provides a dual polarity enable pin (EN) that turns on the regulator when $|V_{EN}| > 2$ V, whether the voltage is positive or negative, as shown in Figure 18.

This functionality allows for different system power management topologies:

- Connecting the EN pin directly to a negative voltage, such as V_{IN}, or
- Connecting the EN pin directly to a positive voltage, such as the output of digital logic circuitry.

Feature Description (continued)

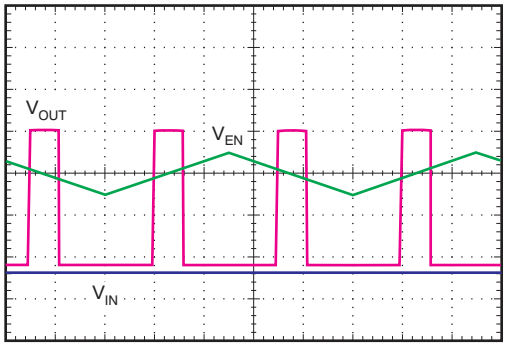


Figure 18. Enable Pin Positive and Negative Threshold

7.4 Device Functional Modes

7.4.1 Normal Operation

The device regulates to the nominal output voltage under the following conditions:

- The input voltage is at least as high as the $|V_{IN(min)}|$.
- The input voltage magnitude is greater than the nominal output voltage magnitude added to the dropout voltage.
- $|V_{EN}| > |V_{EN(HI)}|$
- The output current is less than the current limit.
- The device junction temperature is less than the maximum specified junction temperature.

7.4.2 Dropout Operation

If the input voltage magnitude is lower than the nominal output voltage magnitude plus the specified dropout voltage magnitude, but all other conditions are met for normal operation, the device operates in dropout mode. In this mode of operation, the output voltage magnitude is the same as the input voltage magnitude minus the dropout voltage magnitude. The transient performance of the device is significantly degraded because the pass device (as a bipolar junction transistor, or BJT) is in saturation and no longer controls the current through the LDO. Line or load transients in dropout can result in large output voltage deviations.

7.4.3 Disabled

The device is disabled under the following conditions:

- $|V_{EN}| < |V_{EN(HI)}|$
- The device junction temperature is greater than the thermal shutdown temperature.

Table 1 shows the conditions that lead to the different modes of operation.

Table 1. Device Functional Mode Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	V_{EN}	I_{OUT}	T_J
Normal mode	$\|V_{IN}\| > \{ \|V_{OUT(nom)}\| + \|V_{DO}\|, \|V_{IN(min)}\| \}$	$\|V_{EN}\| > \|V_{(HI)}\|$	$I_{OUT} < I_{CL}$	$T_J < 125°C$
Dropout mode	$\|V_{IN(min)}\| < \|V_{IN}\| < \|V_{OUT(nom)}\| + \|V_{DO}\|$	$\|V_{EN}\| > \|V_{(HI)}\|$	—	$T_J < 125°C$
Disabled mode (any true condition disables the device)	—	$\|V_{EN}\| < \|V_{(HI)}\|$	—	$T_J > 170°C$

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS7A3401 device belongs to a family of new generation linear regulators that use an innovative bipolar process to achieve ultralow-noise. As a bipolar-based device, the TPS7A3401 device is ideal for high-accuracy, high-performance analog applications at higher voltages.

8.1.1 Adjustable Operation

The TPS7A3401 device has an output voltage range from –1.174 V to –18 V. The nominal output voltage of the device is set by two external resistors, as shown in Figure 19.

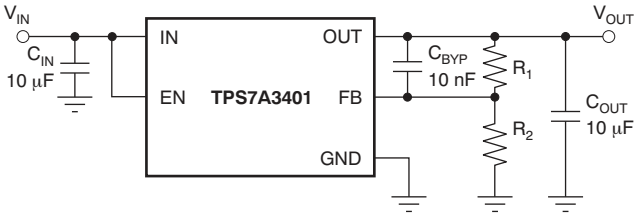


Figure 19. Adjustable Operation for Maximum AC Performance

R_1 and R_2 can be calculated for any output voltage range using the formula shown in Equation 1. To ensure stability under no load conditions, this resistive network must provide a current equal to or greater than 5 µA.

$$R_1 = R_2\left(\frac{V_{OUT}}{V_{FB(nom)}} - 1\right), \text{ where } \frac{|V_{FB(nom)}|}{R_2} > 5\mu A \quad (1)$$

If greater voltage accuracy is required, consider the output voltage offset contributions because of the feedback pin current and use 0.1% tolerance resistors.

8.1.2 Transient Response

As with any regulator, increasing the size of the output capacitor reduces overshoot and undershoot magnitude but increases duration of the transient response.

8.1.3 Post DC-DC Converter Filtering

Most of the time, the voltage rails available in a system do not match the voltage specifications demanded by one or more of its circuits; these rails must be stepped up or down, depending on specific voltage requirements.

DC-DC converters are the preferred solution to step up or down a voltage rail when current consumption is not negligible. They offer high-efficiency with minimum heat generation, but they have one primary disadvantage: they introduce a high-frequency component, and the associated harmonics, on top of the DC output signal.

This high-frequency component, if not filtered properly, degrades analog circuitry performance, reducing overall system accuracy and precision.

The TPS7A3401 device offers a wide-bandwidth, very high power-supply rejection ratio. This specification makes it ideal for post DC-DC converter filtering, as shown in Figure 20. TI highly recommends using the maximum performance schematic shown in Figure 19. Also, verify that the fundamental frequency (and its first harmonic, if possible) is within the bandwidth of the regulator PSRR, shown in Figure 15.

Application Information (continued)

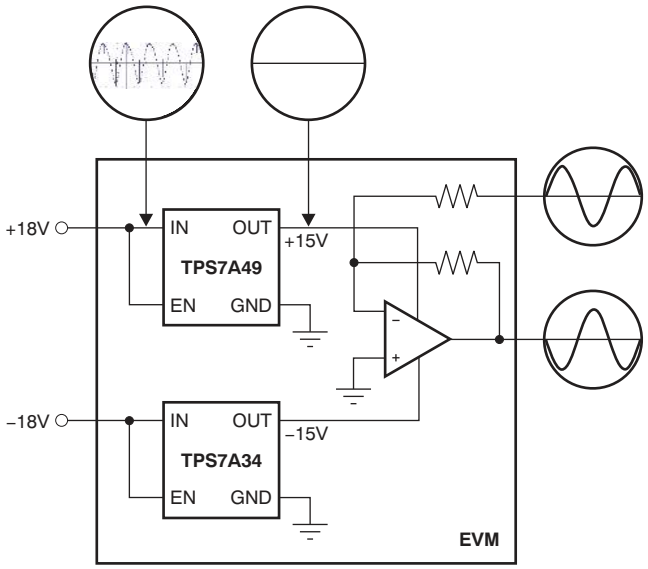


Figure 20. Post DC-DC Converter Regulation to High-Performance Analog Circuitry

8.1.4 Power for Precision Analog

One of the primary applications of the TPS7A3401 device is to provide ultralow-noise voltage rails to high-performance analog circuitry to maximize system accuracy and precision.

The TPS7A3401 negative high-voltage linear regulator provides ultralow noise positive and negative voltage rails to high-performance analog circuitry, such as operational amplifiers, ADCs, DACs, and audio amplifiers.

Because of the ultralow noise levels at high voltages, analog circuitry with high-voltage input supplies can be used. This characteristic allows for high-performance analog solutions to optimize the voltage range, maximizing system accuracy.

8.2 Typical Application

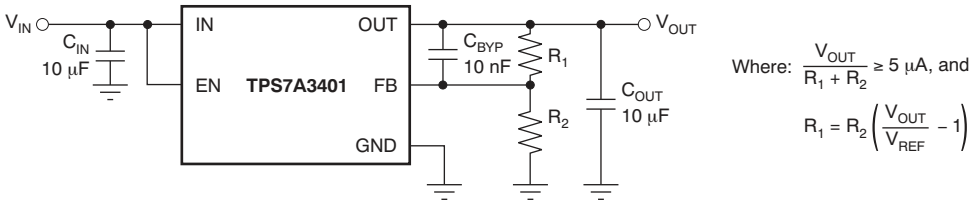


Figure 21. Maximize PSRR Performance and Minimize RMS Noise

8.2.1 Design Requirements

The design goals are V_{IN} = –3 V, V_{OUT} = –1.2 V, and I_{OUT} = 150 mA, maximum. The input supply comes from a supply on the same printed-circuit-board (PCB). The design circuit is shown in Figure 19.

The design space consists of C_{IN}, C_{OUT}, C_{FF}, R_1, and R_2, at $T_{A(max)}$ = 75°C.

Typical Application (continued)

8.2.2 Detailed Design Procedure

The first step when designing with a linear regulator is to examine the maximum load current along with the input and output voltage requirements to determine if the device thermal and dropout voltage requirements can be met. At 150 mA, the input dropout voltage of the TPS7A3401 family is a maximum of 800 mV over temperature; therefore, the dropout headroom of 1.8 V is sufficient for operation over both input and output voltage accuracy. Dropout headroom is calculated as $V_{IN} – V_{OUT} – V_{DO(max)}$, and should be greater than 0 for reliable operation. $V_{DO(max)}$ is the maximum dropout allowed, given worst-case load conditions.

The maximum power dissipated in the linear regulator is the maximum voltage dropped across the pass element from the input to the output, multiplied by the maximum load current. In this example, the maximum voltage drop across in the pass element is |3 V – 1.2 V|, giving us a V_{DO} = 1.8 V. The power dissipated in the pass element is calculated by taking this voltage drop multiplied by the maximum load current. For this example, the maximum power dissipated in the linear regulator is 0.273 W, and is calculated using Equation 2.

$$P_D = (V_{DO})\ (I_{MAX}) + (V_{IN})\ (I_Q) \tag{2}$$

Once the power dissipated in the linear regulator is known, the corresponding junction temperature rise can be calculated. To calculate the junction temperature rise above ambient, the power dissipated must be multiplied by the junction-to-ambient thermal resistance. This calculation gives the worst-case junction temperature; good thermal design can significantly reduce this number. For thermal resistance information, refer to *Thermal Information*. For this example, using the DGN package, the maximum junction temperature rise is calculated to be 17.3°C. The maximum junction temperature rise is calculated by adding junction temperature rise to the maximum ambient temperature, which is 75°C for this example. For this example, the designer calculates the maximum junction temperature is 92.3°C. Keep in mind the maximum junction temperate must be less than 125°C for reliable device operation. Additional ground planes, added thermal vias, and air flow all help to lower the maximum junction temperature.

Use the following equations to pick the rest of the components:

To ensure stability under no-load conditions, the current through the resistor network must be greater than 5 µA, as shown in Equation 3.

$$\frac{V_{FB}}{R_2} > 5\mu A \rightarrow R_2 < 242.4\ k\Omega \tag{3}$$

To set R_2 = 100 kΩ for a standard 1% value resistor, we calculate R_1 as shown in Equation 4.

$$R_1 = R_2 \left(\frac{V_{OUT}}{V_{REF(nom)}} - 1 \right) = 100\ k\Omega \left(\frac{1.2\ V}{1.176\ V} - 1 \right) = 2.04\ k\Omega \tag{4}$$

Use a standard, 1%, 2.05-kΩ resistor for R_1.

For C_{IN}, assume that the –3-V supply has some inductance, and is placed several inches away from the PCB. For this case, we select a 2.2-µF ceramic input capacitor to ensure that the input impedance is negligible to the LDO control loop while keep the physical size and cost of the capacitor low; this component is a common-value capacitor.

For better PSRR for this design, use a 10-µF input and output capacitor. To reduce the peaks from transients but slow down the recovery time, increase the output capacitor size or add additional output capacitors.

8.2.2.1 Capacitor Recommendations

Low-ESR capacitors should be used for the input, output, noise reduction, and feed-forward capacitors. Ceramic capacitors with X7R and X5R dielectrics are preferred. These dielectrics offer more stable characteristics. Ceramic X7R capacitors offer improved overtemperature performance, while ceramic X5R capacitors are the most cost-effective and are available in higher values.

High-ESR capacitors may degrade PSRR.

8.2.2.1.1 Input and Output Capacitor Requirements

The TPS7A3401 negative, high-voltage linear regulator achieves stability with a minimum input and output capacitance of 2.2 µF; however, TI highly recommends using a 10-µF capacitor to maximize AC performance.

Typical Application (continued)

8.2.2.1.2 Feed-Forward Capacitor Requirements

Although feed-forward capacitors (C_{FF}) are not needed to achieve stability, TI highly recommends using 10-nF capacitors to minimize noise and maximize AC performance.

For more information on C_{FF}, refer to Application Report, *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator* (SBVA042). This application report explains the advantages of using C_{FF} (also known as C_{BYP}), and the problems that can occur while using this capacitor.

8.2.3 Application Curves

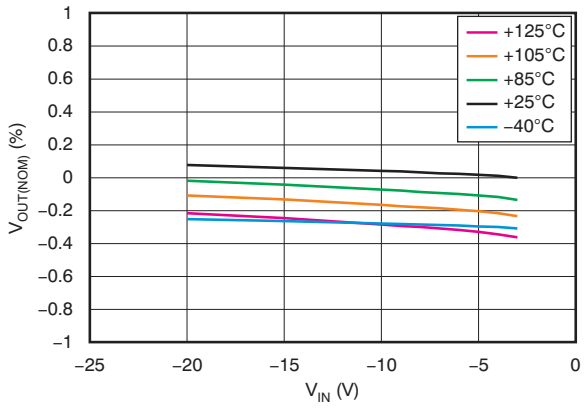


Figure 22. Line Regulation

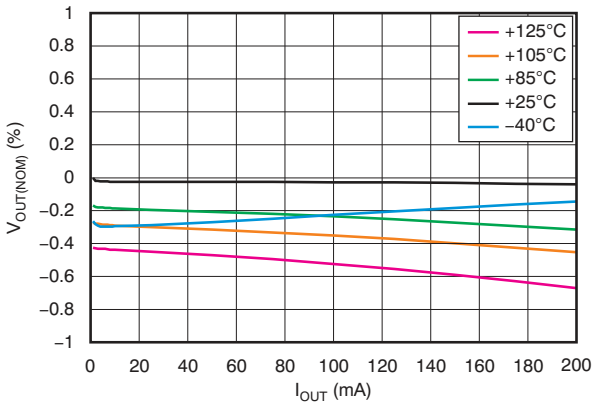


Figure 23. Load Regulation

8.3 Do's and Don'ts

Place at least one, low-ESR, 2.2-µF capacitor as close as possible to both the IN and OUT terminals of the regulator to the GND pin.

Provide adequate thermal paths away from the device.

Do not place the input or output capacitor more than 10 mm away from the regulator.

Do not exceed the absolute maximum ratings.

Do not float the Enable (EN) pin.

9 Power Supply Recommendations

The input supply for the LDO should be within its recommended operating conditions, that is, from –3 V to –20 V. The input voltage should provide adequate headroom in order for the device to have a regulated output. If the input supply is noisy, additional input capacitors with low-ESR can help improve the output noise performance.

The input and output supplies should also be bypassed with at least a 2.2-µF capacitor located near the input and output pins. There should be no other components located between these capacitors and the pins.

10 Layout

10.1 Layout Guidelines

Layout is a critical part of good power-supply design. There are several signal paths that conduct fast-changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power-supply performance. To help eliminate these problems, the IN pin should be bypassed to ground with a low ESR ceramic bypass capacitor with an X5R or X7R dielectric.

The GND pin should be tied directly to the PowerPAD under the IC. The PowerPAD should be connected to any internal PCB ground planes using multiple vias directly under the IC.

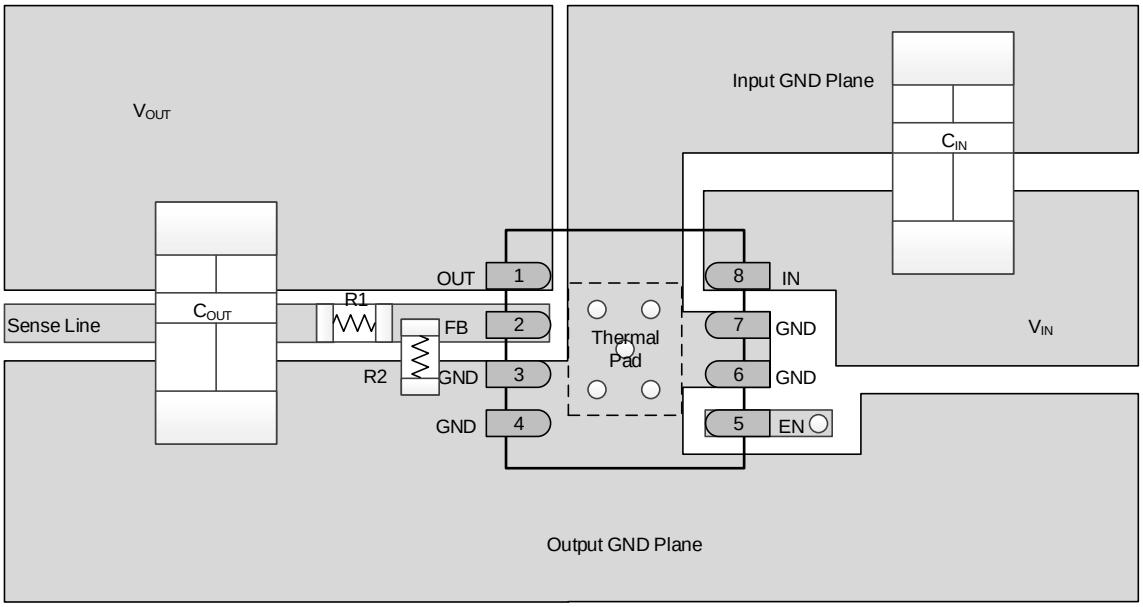
Equivalent series inductance (ESL) and equivalent series resistance (ESR) must be minimized to maximize performance and ensure stability. Every capacitor (C_{IN}, C_{OUT}, C_{FF}) must be placed as close as possible to the device and on the same side of the PCB as the regulator itself.

Do not place any of the capacitors on the opposite side of the PCB from where the regulator is installed. The use of vias and long traces is strongly discouraged because these circuits may impact system performance negatively, and even cause instability.

10.1.1 Board Layout Recommendations to Improve PSRR and Noise Performance

To improve AC performance (such as PSRR, output noise, and transient response), TI recommends designing the board with separate ground planes for V_{IN} and V_{OUT}, with each ground plane star connected only at the GND pin of the device.

10.2 Layout Example



NOTE: C_{IN} and C_{OUT} are size 1208 capacitors, while R_1 and R_2 are size 0402.

Figure 24. PCB Layout Example (DGN Package)

10.3 Thermal Considerations

Thermal protection disables the output when the junction temperature rises to approximately 170°C, allowing the device to cool. When the junction temperature cools to approximately 150°C, the output circuitry is enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle ON and OFF. This cycling limits the dissipation of the regulator, protecting it from damage as a result of overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to a maximum of 125°C. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your particular application. This configuration produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS7A3401 device has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS7A3401 device into thermal shutdown degrades device reliability.

10.4 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Performance data or JEDEC low- and high-K boards are given in *Thermal Information*. Using heavier copper increases the effectiveness in removing heat from the device. The addition of plated through-holes to heat dissipating layers also improves the heatsink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation (P_D) can be approximated by the product of the output current times the voltage drop across the output pass element, as shown in Equation 5.

$$P_D = (V_{IN} - V_{OUT})\ I_{OUT} \quad (5)$$

Power dissipation that results from quiescent current is negligible. Excessive power dissipation triggers the thermal protection circuit.

Figure 25 shows the maximum ambient temperature versus the power dissipation of the TPS7A3401 device. Figure 25 presumes the device is soldered on a JEDEC standard, high-K layout with no airflow over the board. Actual board thermal impedances vary widely. If the application requires high power dissipation, having a thorough understanding of the board temperature and thermal impedances is helpful to ensure the TPS7A3401 device does not operate above a junction temperature of 125°C.

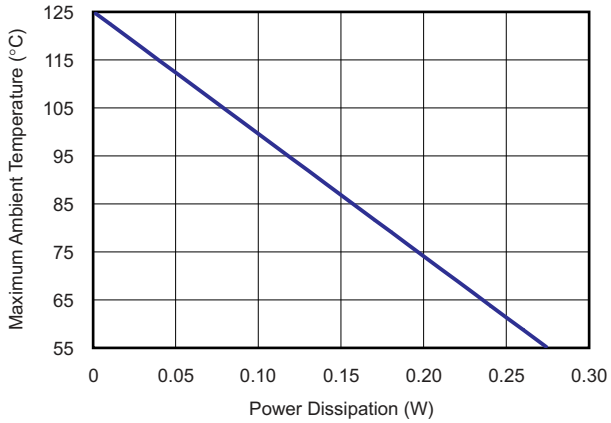


Figure 25. Maximum Ambient Temperature (°C) vs Power Dissipation

Power Dissipation (continued)

Estimating the junction temperature can be done by using the thermal metrics Ψ_{JT} and Ψ_{JB}, shown in *Thermal Information*. These metrics are a more accurate representation of the heat transfer characteristics of the die and the package than $R_{\theta JA}$. The junction temperature can be estimated with Equation 6.

$$\Psi_{JT}: \quad T_J = T_T + \Psi_{JT} \bullet P_D$$

$$\Psi_{JB}: \quad T_J = T_B + \Psi_{JB} \bullet P_D \tag{6}$$

where

- P_D is the power dissipation shown by Equation 5,
- T_T is the temperature at the center-top of the IC package,
- T_B is the PCB temperature measured 1 mm away from the IC package *on the PCB surface*.

NOTE

Both T_T and T_B can be measured on actual application boards using a thermo-gun (an infrared thermometer).

For more information about measuring T_T and T_B, see the application note *Using New Thermal Metrics* (SBVA025), available for download at www.ti.com.

11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Evaluation Modules

An evaluation module (EVM) is available to assist in the initial circuit performance evaluation using the TPS7A3401. The TPS7A3401EVM-042 evaluation module (and related user's guide) can be requested at the Texas Instruments website through the product folders or purchased directly from the TI eStore.

11.1.1.2 Spice Models

Computer simulation of circuit performance using SPICE is often useful when analyzing the performance of analog circuits and systems. A SPICE model for the TPS7A3401 is available through the product folder under the *Tools & Software* tab.

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation see the following:

- *Pros and Cons of Using a Feedforward Capacitor with a Low-Dropout Regulator*, SBVA042.
- *Using New Thermal Metrics*, SBVA025.
- *TPS7A3401EVM-042 Evaluation Module User's Guide*, SLVU428.

11.3 Community Resource

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

PowerPAD, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7A3401DGNR	ACTIVE	HVSSOP	DGN	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPKQ	Samples
TPS7A3401DGNT	ACTIVE	HVSSOP	DGN	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	PPKQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

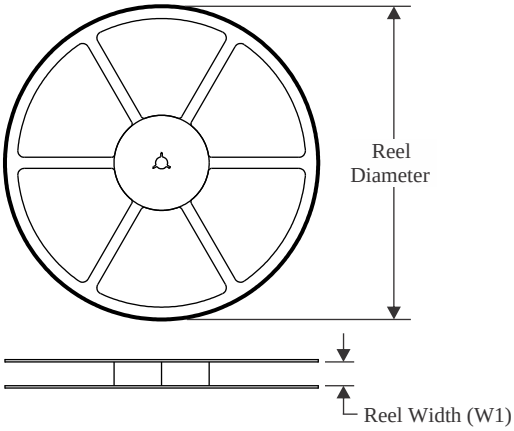
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

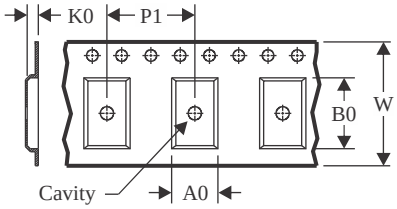
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

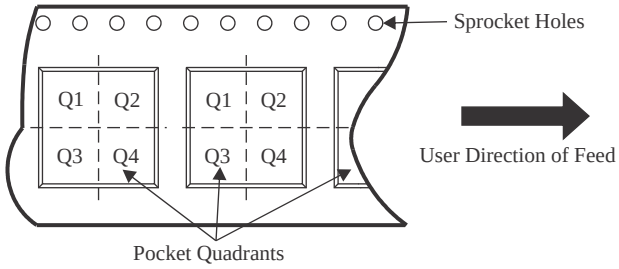


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

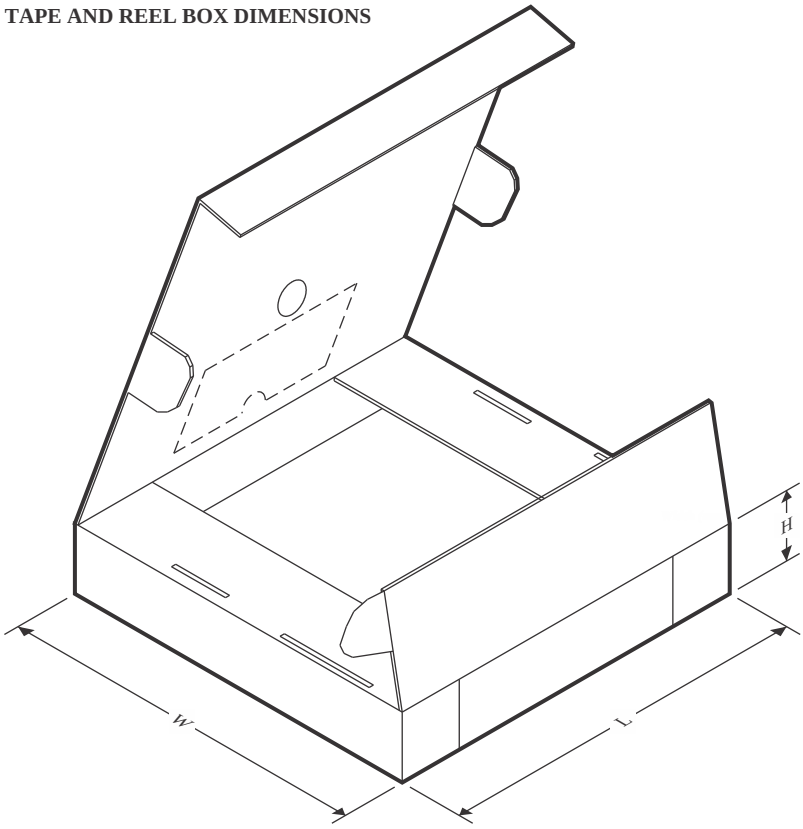
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7A3401DGNR	HVSSOP	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPS7A3401DGNT	HVSSOP	DGN	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7A3401DGNR	HVSSOP	DGN	8	2500	356.0	356.0	35.0
TPS7A3401DGNT	HVSSOP	DGN	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

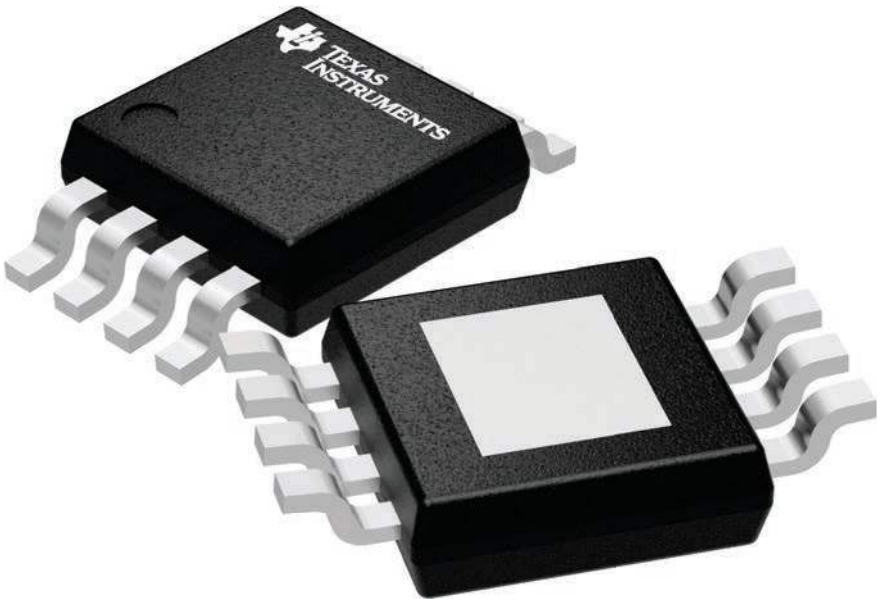
DGN 8

PowerPAD VSSOP - 1.1 mm max height

3 x 3, 0.65 mm pitch

SMALL OUTLINE PACKAGE

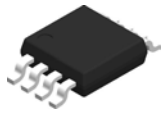
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4225482/A

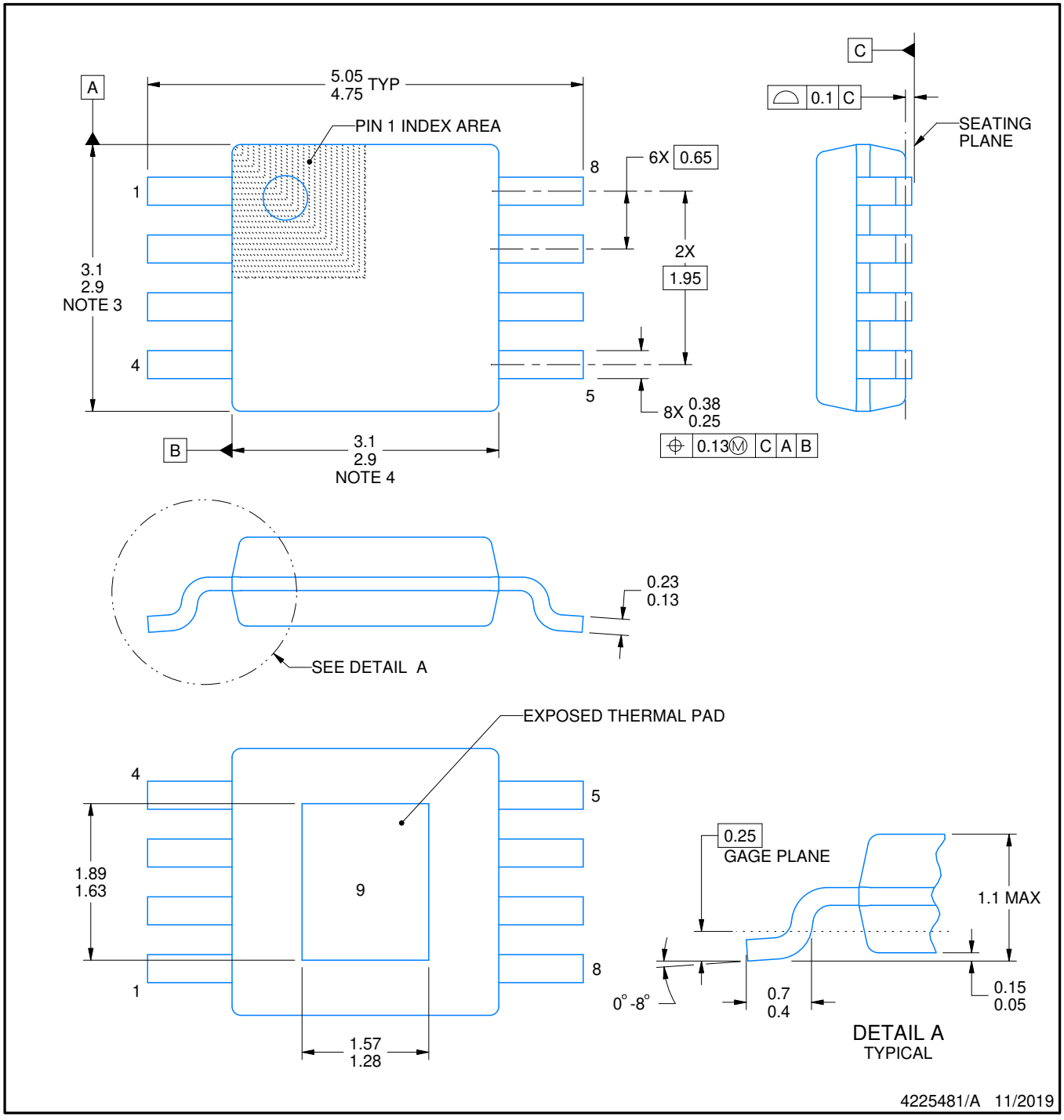
PACKAGE OUTLINE

DGN0008D



PowerPAD™ VSSOP - 1.1 mm max height

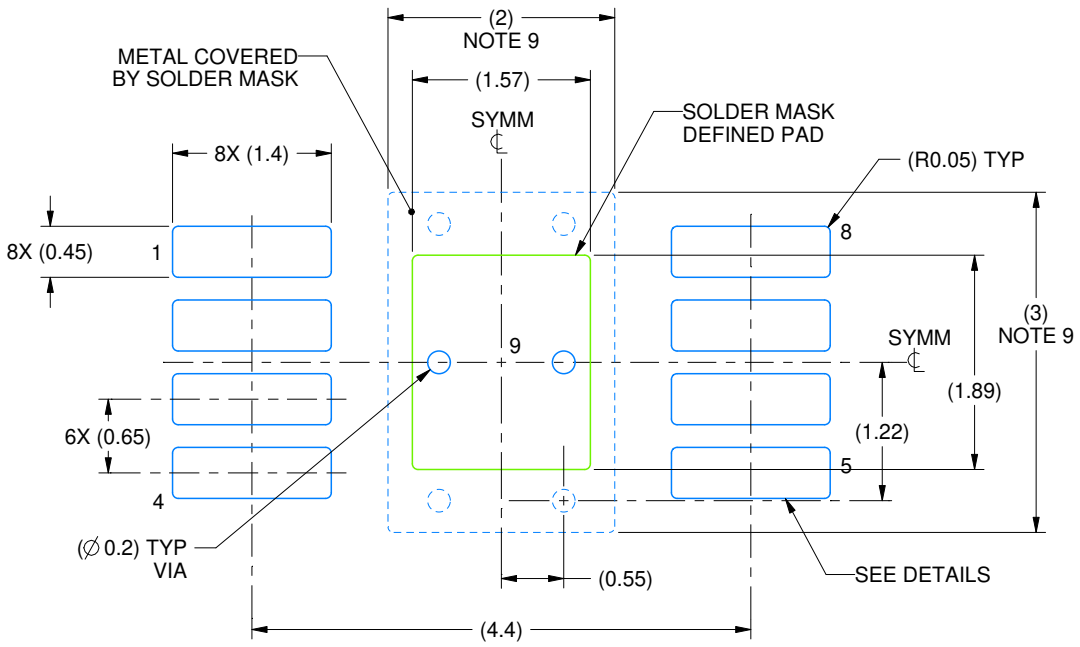
SMALL OUTLINE PACKAGE



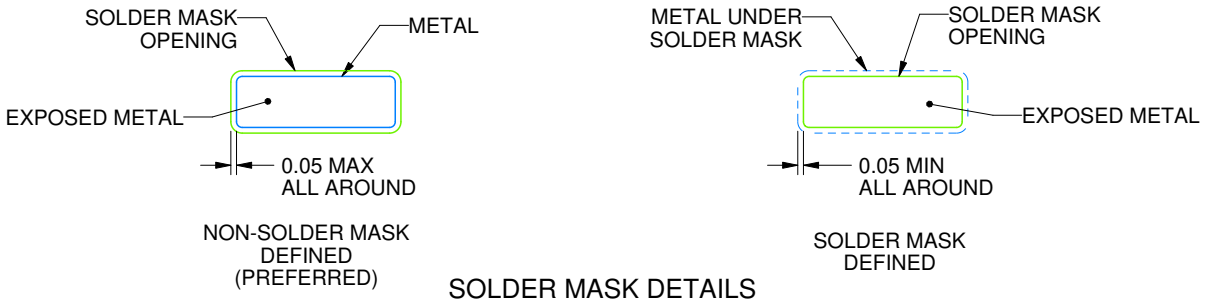
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

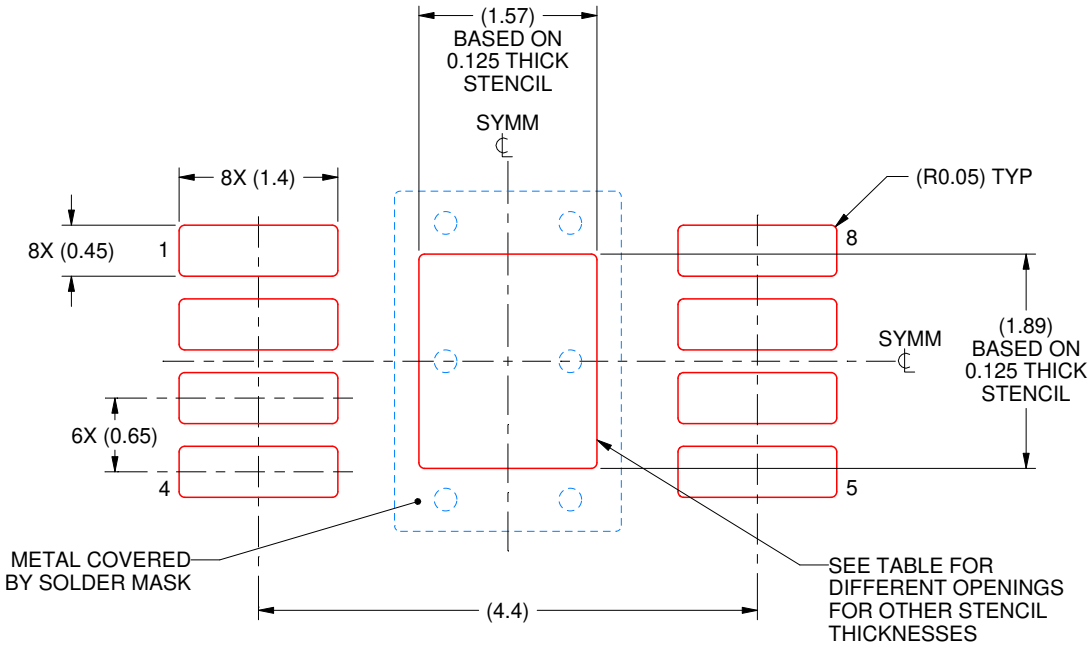


SOLDER MASK DETAILS

4225481/A 11/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.



SOLDER PASTE EXAMPLE
EXPOSED PAD 9:
100% PRINTED SOLDER COVERAGE BY AREA
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.76 X 2.11
0.125	1.57 X 1.89 (SHOWN)
0.15	1.43 X 1.73
0.175	1.33 X 1.60

4225481/A 11/2019

NOTES: (continued)

10. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
11. Board assembly site may have different recommendations for stencil design.

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