KAE-01093

1024 (H) x 1024 (V) Interline Transfer EMCCD Image Sensor

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Interline CCD; with EMCCD
Resolution	1.0 Megapixels
Total Number of Pixels	1064 (H) × 1064 (V)
Number of Effective Pixels	1040 (H) × 1040 (V)
Number of Active Pixels	1024 (H) × 1024 (V)
Pixel Size	9.0 μm (H) × 9.0 μm (V)
Active Image Size	9.21 mm (H) × 9.21 mm (V) 13.0 mm (Diagonal) 1″ Optical Format
Aspect Ratio	1:1
Number of Outputs	2, or 4
Charge Capacity – VOUT2 / VOUT3	60,000 e^- / 30,000 e^-
Output Sensitivity – VOUT2 / VOUT3	16.5 μV/e^- / 44 μV/e^-
Quantum Efficiency Mono (500, 850, 920 nm) / R,G,B	 (54%, 16%, 8%) / 44%, 48%, 43%
Read Noise (40 MHz) Normal Mode (1× Gain) Intra-scene Mode (20× Gain)	 < 20 electrons rms < 1 electron rms
Dark Current (0°C) Photodiode, VCCD	 < 0.1, 8 electrons/s
Dynamic Range Normal Mode (1× Gain) Intra-scene Mode (20× Gain)	 69 dB 95 dB
Charge Transfer Efficiency	0.999999
Blooming Suppression	> 500 X
Smear	−115 dB
Image Lag	< 1 electron
Maximum Data Rate	40 MHz
Maximum Frame Rate Normal Mode (40 MHz) Intra-scene mode (40 MHz) 2x2 binning (40 MHz)	 91 fps (quad), 52 fps (dual) 91 fps (quad), 52 fps (dual) 144 fps (quad), 91 fps (dual)
Package	148 pin PGA with TEC
Cover Glass	MAR, Sealed

NOTE: All Parameters are specified at T = 0°C unless otherwise noted.

Description

The KAE−01093 Image Sensor is a 1 megapixel 1024 × 1024 CCD in a 1″ optical format that provides enhanced Quantum Efficiency (particularly for NIR wavelengths) without a decrease in Modulation Transfer Function (MTF). In quad mode, the KAE−01093 runs at 91 fps. Each of the sensor's four outputs incorporate both a conventional horizontal CCD register and a high gain EMCCD register. An intra-scene switchable gain feature samples each charge packet on a pixel-by-pixel basis. This enables the camera system to determine whether the charge will be routed through the normal gain output or the EMCCD output based on a user selectable threshold. Cameras can thus image in extreme low light even when bright objects are within a dark scene, allowing a single camera to capture quality images from sunlight to starlight.

ON Semiconductor®

www.onsemi.com

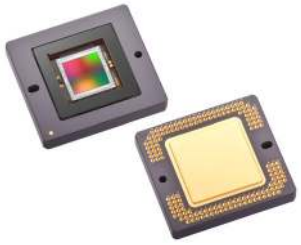


Figure 1. KAE−01093 Interline Transfer EMCCD Image Sensor

Features

- Increased QE, with 2× Improvement at 820 nm
- 91 fps (4 Outputs); 144 fps (Binned)
- Intra-scene Switchable Gain
- Wide Dynamic Range
- Low Noise Architecture
- Exceptional Low Light Imaging
- Global Shutter
- Excellent Image Uniformity and MTF

Applications

- Surveillance
- Scientific Imaging
- Medical Imaging
- Situational Awareness (Ground Vehicles)

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

US export controls apply to all shipments of this product designated for destinations outside of the US and Canada, requiring ON Semiconductor to obtain an export license from the US Department of Commerce before image sensors or evaluation kits can be exported.

Table 2. ORDERING INFORMATION − KAE−01093 IMAGE SENSOR

Part Number	Description	Marking Code
KAE−01093−ABB−SD−FA	Monochrome, Microlens, PGA Package, TEC, Sealed MAR Cover Glass, Standard Grade	KAE−01093−ABB Serial Number
KAE−01093−ABB−SD−EE	Monochrome, Microlens, PGA Package, TEC, Sealed MAR Cover Glass, Engineering Grade	
KAE−01093−FBB−SD−FA	Gen2 Color (Bayer RGB), Microlens, PGA Package, TEC, Sealed MAR Cover Glass, Standard Grade	KAE−01093−FBB Serial Number
KAE−01093−FBB−SD−EE	Gen2 Color (Bayer RGB), Microlens, PGA Package, TEC, Sealed MAR Cover Glass, Engineering Grade	
KAE−01093−QBB−SD−FA	Gen2 Color (Sparse CFA), Microlens, PGA Package, TEC, Sealed MAR Cover Glass, Standard Grade	KAE−01093−QBB Serial Number
KAE−01093−QBB−SD−EE	Gen2 Color (Sparse CFA), Microlens, PGA Package, TEC, Sealed MAR Cover Glass, Engineering Grade	

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

Warning

The KAE−01093−ABB−SD and KAE−01093−FBB−SD, and KAE−01093−QBB−SD packages have an integrated thermoelectric cooler (TEC) and have epoxy sealed cover glass. The seal formed is non-hermetic, and may allow moisture ingress over time, depending on the storage environment.

As a result, care must be taken to avoid cooling the device below the dew point inside the package cavity, since this may result in condensation on the sensor.

For all KAE−01093 configurations, no warranty, expressed or implied, covers condensation.

Please address all inquiries and purchase orders to:

ON Semiconductor
1964 Lake Avenue
Rochester, New York 14615
Phone: (585) 784−5500

DEVICE DESCRIPTION

Architecture

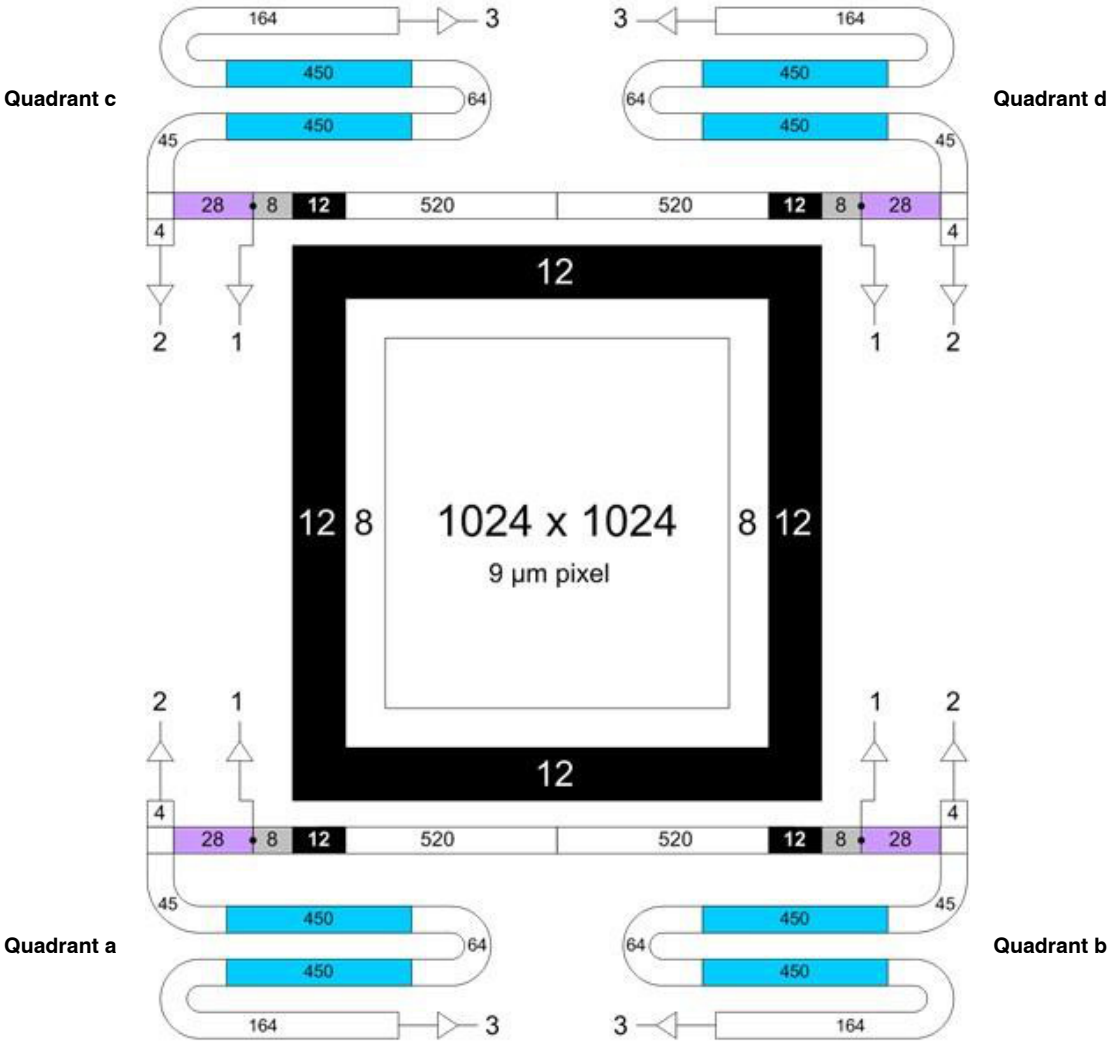


Figure 2. Block Diagram

Dark Reference Pixels

There are 12 dark reference rows at the top and bottom of the image sensor, as well as 12 dark reference columns on the left and right sides. However, the rows and columns at the perimeter edges should not be included in acquiring a dark reference signal, since they may be subject to some light leakage.

Active Buffer Pixels

8 unshielded pixels adjacent to any leading or trailing dark reference regions are classified as active buffer pixels. These pixels are light sensitive but are not tested for defects and non-uniformities.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the individual silicon photodiodes. These photoelectrons are collected locally by the formation of potential wells at each photo-site. Below photodiode saturation, the number of photoelectrons collected at each pixel is linearly dependent upon light level and exposure time and non-linearly dependent on wavelength. When the photodiodes charge capacity is reached, excess electrons are discharged into the substrate to prevent blooming.

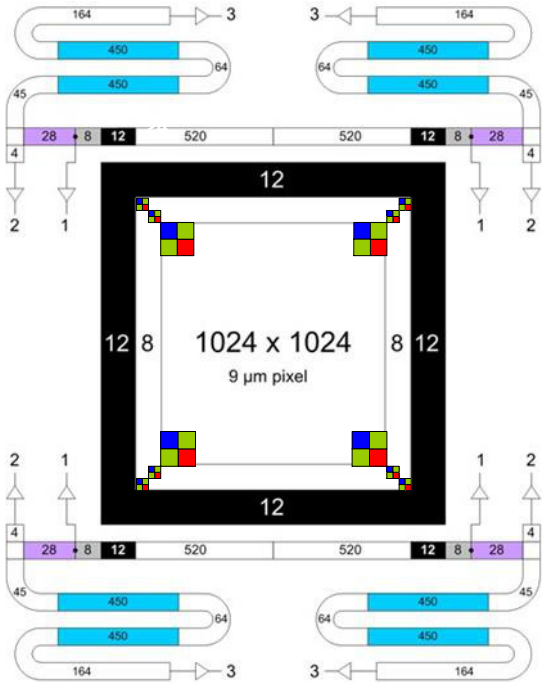


Figure 3. Bayer Color Filter Pattern

Sparse Color Filter Pattern

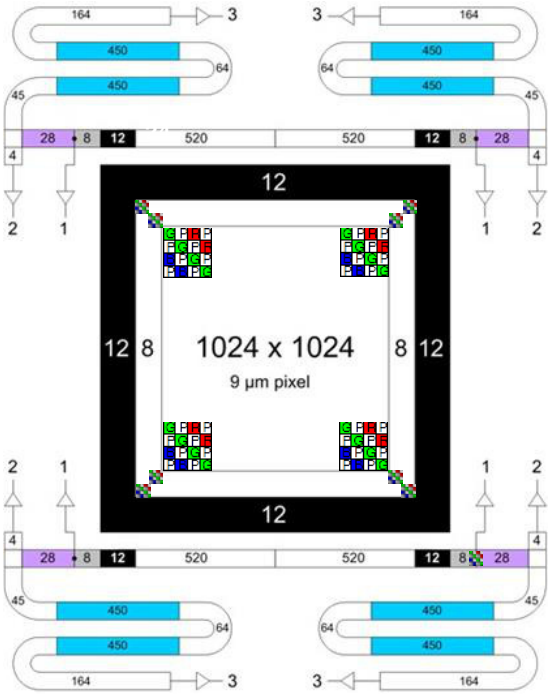


Figure 4. Sparse Color Filter Pattern

Physical Description

Pin Grid Array Configuration

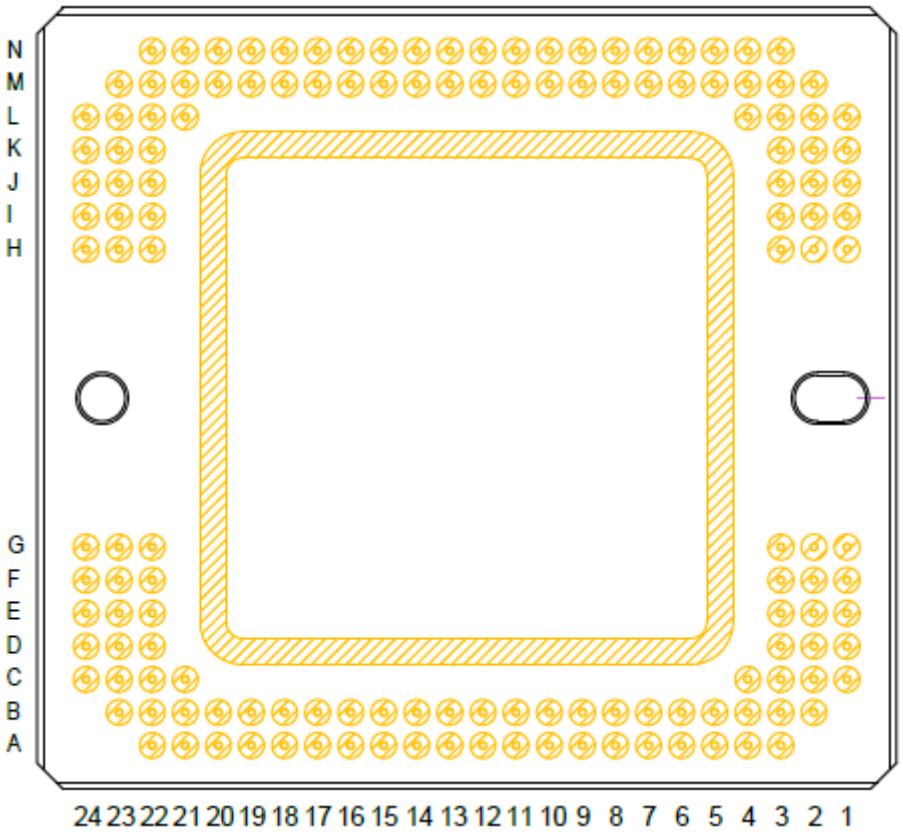


Figure 5. PGA Package Pin Designations (Bottom View)

Table 3. PIN DESCRIPTION

Pin No.	Label	Description
A3	VDD2a	Amplifier 2 Supply, Quadrant a
A4	H2SW3a	HCCD Output 3 Selector, Quadrant a
A5	RG23a	Amplifier 2 and 3 Reset, Quadrant a
A6	VDD3a	Amplifier 3 Supply, Quadrant a
A7	H1BEMa	EMCCD Barrier Phase 1, Quadrant a
A8	H2SEMa	EMCCD Storage Phase 2, Quadrant a
A9	H2a	HCCD Phase 2, Quadrant a
A10	H1Sa	HCCD Storage Phase 1, Quadrant a
A11	H2Ba	HCCD Barrier Phase 2, Quadrant a
A12	H3Ba	HCCD Barrier Phase 3, Quadrant a
A13	H3Bb	HCCD Barrier Phase 3, Quadrant b
A14	H2Bb	HCCD Barrier Phase 2, Quadrant b
A15	H1Sb	HCCD Storage Phase 1, Quadrant b
A16	H2b	HCCD Phase 2, Quadrant b

Table 3. PIN DESCRIPTION (continued)

Pin No.	Label	Description
A17	H2SEMb	EMCCD Storage Multiplier Phase 2, Quadrant b
A18	H1BEMb	EMCCD Barrier Phase 1, Quadrant b
A19	VDD3b	Amplifier 3 Supply, Quadrant b
A20	RG23b	Amplifier 2 and 3 Reset, Quadrant b
A21	H2SW3b	HCCD Output 3 Selector, Quadrant b
A22	VDD2b	Amplifier 2 Supply, Quadrant b
B2	VOUT1a	Video Output 1, Quadrant a
B3	H2Xa	Floating Gate Exit HCCD Gate, Quadrant a
B4	H2SW2a	HCCD Output 2 Selector, Quadrant a
B5	H2La	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant a
B6	VOUT3a	Video Output 3, Quadrant a
B7	H1SEMa	EMCCD Storage Multiplier Phase 1, Quadrant a
B8	H2BEMa	EMCCD Barrier Phase 1, Quadrant a
B9	H1a	HCCD Phase 1, Quadrant a
B10	H2Sa	HCCD Storage Phase 2, Quadrant a
B11	H3Sa	HCCD Storage Phase 3, Quadrant a
B12	H1Ba	HCCD Barrier Phase 1, Quadrant a
B13	H1Bb	HCCD Barrier Phase 1, Quadrant b
B14	H3Sb	HCCD Storage Phase 3, Quadrant b
B15	H2Sb	HCCD Storage Phase 2, Quadrant b
B16	H1b	HCCD Phase 1, Quadrant b
B17	H2BEMb	EMCCD Barrier Phase 2, Quadrant b
B18	H1SEMb	EMCCD Storage Multiplier Phase 1, Quadrant b
B19	VOUT3b	Video Output 3, Quadrant b
B20	H2Lb	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant b
B21	H2SW2b	HCCD Output 2 Selector, Quadrant b
B22	H2Xb	Floating Gate Exit HCCD Gate, Quadrant b
B23	VOUT1b	Video Output 1, Quadrant b
C1	V3B	VCCD Bottom Phase 3
C2	VDD1a	Amplifier 1 Supply, Quadrant a
C3	RG1a	Amplifier 1 Reset, Quadrant a
C4	VOUT2a	Video Output 2, Quadrant a
C21	VOUT2b	Video Output 2, Quadrant b
C22	RG1b	Amplifier 1 Reset, Quadrant b
C23	VDD1b	Amplifier 1 Supply, Quadrant b
C24	V3B	VCCD Bottom Phase 3
D1	V2B	VCCD Bottom Phase 2
D2	OG1a	Output 1 Gate, Quadrant a
D3	VSS1a	Amplifier 1 Return, Quadrant a

Table 3. PIN DESCRIPTION (continued)

Pin No.	Label	Description
D22	VSS1b	Amplifier 1 Return, Quadrant b
D23	OG1b	Output 1 Gate, Quadrant b
D24	V2B	VCCD Bottom Phase 2
E1	V1B	VCCD Bottom Phase 1
E2	V4B	VCCD Bottom Phase 4
E3	ESD	ESD Protection Disable
E22	ESD	ESD Protection Disable
E23	V4B	VCCD Bottom Phase 4
E24	V1B	VCCD Bottom Phase 1
F1	GND	Ground
F2	GND	Ground
F3	GND	Ground
F22	GND	Ground
F23	GND	Ground
F24	GND	Ground
G1	VDD15	+15 V Supply
G2	SUBREF	Substrate Voltage Reference
G3	THERM2	Thermistor Terminal 2
G22	TEC−	Thermal Electric Cooler Negative Terminal
G23	TEC−	Thermal Electric Cooler Negative Terminal
G24	TEC−	Thermal Electric Cooler Negative Terminal
H1	SUB	Substrate
H2	SUB	Substrate
H3	THERM1	Thermistor Terminal 1
H22	TEC+	Thermal Electric Cooler Positive Terminal
H23	TEC+	Thermal Electric Cooler Positive Terminal
H24	TEC+	Thermal Electric Cooler Positive Terminal
I1	GND	Ground
I2	GND	Ground
I22	GND	Ground
I23	GND	Ground
I24	GND	Ground
J1	V1T	VCCD Top Phase 1
J2	V4T	VCCD Top Phase 4
J3	ID	Device ID
J22	VDD15	+15 V Supply
J23	V4T	VCCD Top Phase 4
J24	V1T	VCCD Top Phase 1
K1	V2T	VCCD Top Phase 2

Table 3. PIN DESCRIPTION (continued)

Pin No.	Label	Description
K2	OG1c	Output 1 Gate, Quadrant c
K3	VSS1c	Amplifier 1 Return, Quadrant c
K22	VSS1d	Amplifier 1 Return, Quadrant d
K23	OG1d	Output 1 Gate, Quadrant d
K24	V2T	VCCD Top Phase 2
L1	V3T	VCCD Top Phase 3
L2	VDD1c	Amplifier 1 Supply, Quadrant c
L3	RG1c	Amplifier 1 Reset, Quadrant c
L4	VOUT2c	Video Output 2, Quadrant c
L21	VOUT2d	Video Output 2, Quadrant d
L22	RG1d	Amplifier 1 Reset, Quadrant d
L23	VDD1d	Amplifier 1 Supply, Quadrant d
L24	V3T	VCCD Top Phase 3
M2	VOUT1c	Video Output 1, Quadrant c
M3	H2Xc	Floating Gate Exit HCCD Gate, Quadrant c
M4	H2SW2c	HCCD Output 2 Selector, Quadrant c
M5	H2Lc	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant c
M6	VOUT3c	Video Output 3, Quadrant c
M7	H1SEMc	EMCCD Storage Multiplier Phase 1, Quadrant c
M8	H2BEMc	EMCCD Barrier Phase 2, Quadrant c
M9	H1c	HCCD Phase 1, Quadrant c
M10	H2Sc	HCCD Storage Phase 2, Quadrant c
M11	H3Sc	HCCD Storage Phase 3, Quadrant c
M12	H1Bc	HCCD Barrier Phase 1, Quadrant c
M13	H1Bd	HCCD Barrier Phase 1, Quadrant d
M14	H3Sd	HCCD Storage Phase 3, Quadrant d
M15	H2Sd	HCCD Storage Phase 2, Quadrant d
M16	H1d	HCCD Phase 1, Quadrant d
M17	H2BEMd	EMCCD Barrier Phase 2, Quadrant d
M18	H1SEMd	EMCCD Storage Multiplier Phase 1, Quadrant d
M19	VOUT3d	Video Output 3, Quadrant d
M20	H2Ld	HCCD Last Gate, Outputs 1, 2 and 3, Quadrant d
M21	H2SW2d	HCCD Output 2 Selector, Quadrant d
M22	H2Xd	Floating Gate Exit HCCD Gate, Quadrant d
M23	VOUT1d	Video Output 1, Quadrant d
N3	VDD2c	Amplifier 2 Supply, Quadrant c
N4	H2SW3c	HCCD Output 3 Selector, Quadrant c
N5	RG23c	Amplifier 2 and 3 Reset, Quadrant c
N6	VDD3c	Amplifier 3 Supply, Quadrant c

Table 3. PIN DESCRIPTION (continued)

Pin No.	Label	Description
N7	H1BEMc	EMCCD Barrier Phase 1, Quadrant c
N8	H2SEMc	EMCCD Storage Multiplier Phase 2, Quadrant c
N9	H2c	HCCD Phase 2, Quadrant c
N10	H1Sc	HCCD Storage Phase 1, Quadrant c
N11	H2Bc	HCCD Barrier Phase 2, Quadrant c
N12	H3Bc	HCCD Barrier Phase 3, Quadrant c
N13	H3Bd	HCCD Barrier Phase 3, Quadrant d
N14	H2Bd	HCCD Barrier Phase 2, Quadrant d
N15	H1Sd	HCCD Storage Phase 1, Quadrant d
N16	H2d	HCCD Phase 2, Quadrant d
N17	H2SEMd	EMCCD Storage Multiplier Phase 2, Quadrant d
N18	H1BEMd	EMCCD Barrier Phase 1, Quadrant d
N19	VDD3d	Amplifier 3 Supply, Quadrant d
N20	RG23d	Amplifier 2 and 3 Reset, Quadrant d
N21	H2SW3d	HCCD Output 3 Selector, Quadrant d
N22	VDD2d	Amplifier 2 Supply, Quadrant d

NOTE: Pin No. I3 is connected to the heat sink.

Imaging Performance

Table 4. TYPICAL OPERATION CONDITIONS

(Unless otherwise noted, the Imaging Performance Specifications are measured using the following conditions)

Description	Condition
Light Source (Note 1)	Continuous Red, Green, Blue, and IR LED Illumination
Operation	Nominal Operating Voltages and Timing
Temperature	0°C

1. For monochrome sensor, only green and IR LED illumination is used.

Table 5. PERFORMANCE PARAMETERS

(Performance parameters are evaluated at initial design validation.) (Note 5)

Description	Symbol	Nom	Unit
Maximum Photoresponse Non-linearity (EMCCD gain = 1) (Note 1)	NL	2	%
Maximum Gain Difference Between Outputs (EMCCD gain = 1) (Note 4)	ΔG	10	%
Maximum Signal Error due to Non-linearity Differences (EMCCD gain = 1) (Note 1)	ΔNL	1	%
Photodiode Dark Current (Average)	I_{PD}	0.1	e/p/s
Vertical CCD Dark Current		8	e/p/s
Image Lag	Lag	<1	e^-
Anti-blooming Factor	X_{AB}	500	
Vertical Smear (Blue Light)	Smear	−115	dB
Read Noise (VOUT2) (Note 2)	n_{e-T}	21	e^- rms
Read Noise (EMCCD Gain = 1, VOUT3) (Note 2)	n_{e-T}	11	e^- rms
Read Noise (EMCCD Gain = 20)	n_{e-T}	<1	e^- rms
EMCCD Excess Noise Factor (Gain = 20x)		1.4	

Table 5. PERFORMANCE PARAMETERS (continued)
(Performance parameters are evaluated at initial design validation.) (Note 5)

Description	Symbol	Nom	Unit
Dynamic Range (Gain = 1) (Notes 2, 3)	DR	69	dB
Dynamic Range (60 ke^-/1 e^- Noise)		95	dB
Output Amplifier Bandwidth (Note 6)	f_3db	250	MHz
Output Amplifier Impedance	R_{OUT}	140	Ω
Output Amplifier Sensitivity (VOUT3)	ΔV/ΔN	44	μV/e^-
Output Amplifier Sensitivity (VOUT2)	ΔV/ΔN	16.5	μV/e^-
Output Amplifier Sensitivity (VOUT1)	ΔV/ΔN (FG)	5.8	μV/e^-
Quantum Efficiency (Monochrome, Peak) Green (500 nm) NIR (850 nm) NIR (920nm)	QE_{max}	 54 16 8	%
Quantum Efficiency (Color, Peak) Red (620 nm) Green (540 nm) Blue (470nm)	QE_{max}	 44 48 43	%
Power (Note 2) 4-output Mode Gain = 1x Gain = 100x 2-output Mode Gain = 1x Gain = 100x		 0.9 1.2 0.5 0.65	W

1. Value is over the range of 10% to 90% of photodiode saturation.
2. At 40 MHz.
3. Uses 20 LOG (P_{Ne}/n_{e-T})
4. The output-to-output gain differences may be adjusted by independently adjusting the EMCCD amplitude for each output.
5. Nominal performance as measured at 0°C
6. Calculated from $f_{-3db} = 1 / 2\pi \times R_{OUT} \times C_{LOAD}$ where C_{LOAD} = 5 pF.

Table 6. PERFORMANCE SPECIFICATION

Description	Symbol	Min	Nom	Max	Unit	Temperature Tested at (°C)
Dark Field Global Non-uniformity	DSNU	–	–	2.0	mV pp	0
Bright Field Global Non-uniformity (Note 1)		–	2.0	5.0	% rms	0
Bright Field Global Peak to Peak Non-uniformity (Note 1)	PRNU	–	5.0	15.0	%pp	0
Bright Field Center Non-uniformity (Note 1)		–	1.0	2.0	% rms	0
Photodiode Charge Capacity (Note 2)	P_{Ne}		60		ke^-	0
Horizontal CCD Charge Transfer Efficiency	HCTE	0.999995	0.999999	–		0
Vertical CCD Charge Transfer Efficiency	VCTE	0.999995	0.999999	–		0
Output Amplifier DC Offset (VOUT2, VOUT3)	V_{ODC}	8	10	12	V	0
Output Amplifier DC Offset (VOUT1)	V_{ODC}	−0.5	1	2.5	V	0

1. Per color.
2. The operating value of the substrate reference voltage, V_{AB}, can be read from V_{SUBREF}.

TYPICAL PERFORMANCE CURVES

Quantum Efficiency

Monochrome and Color with Microlens and MAR Glass

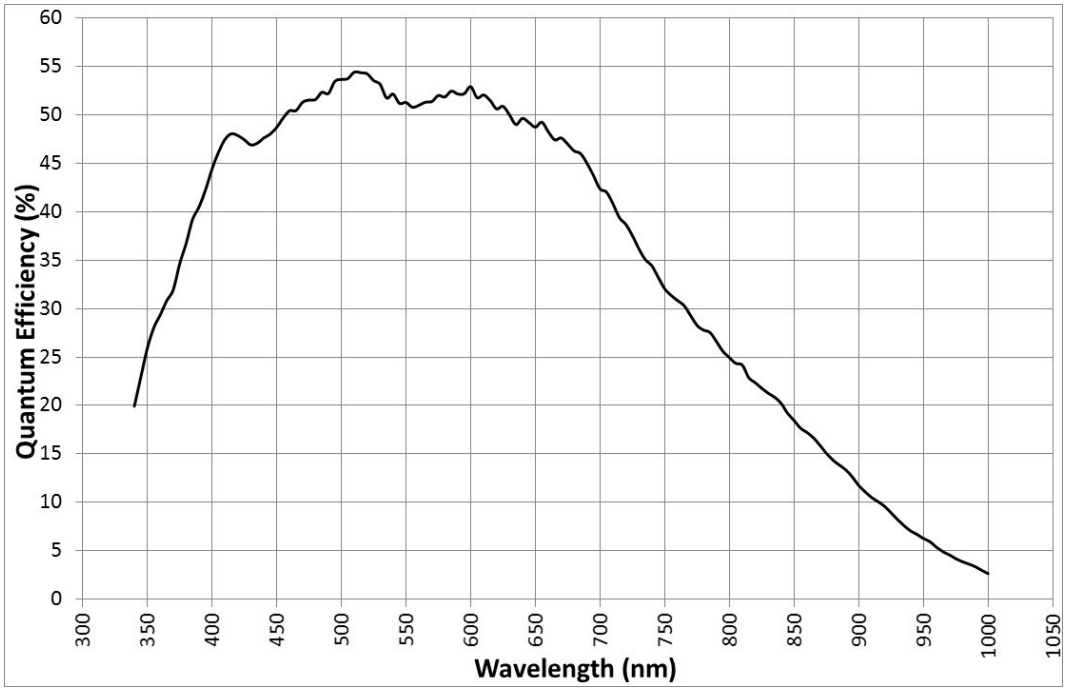


Figure 6. Monochrome Quantum Efficiency

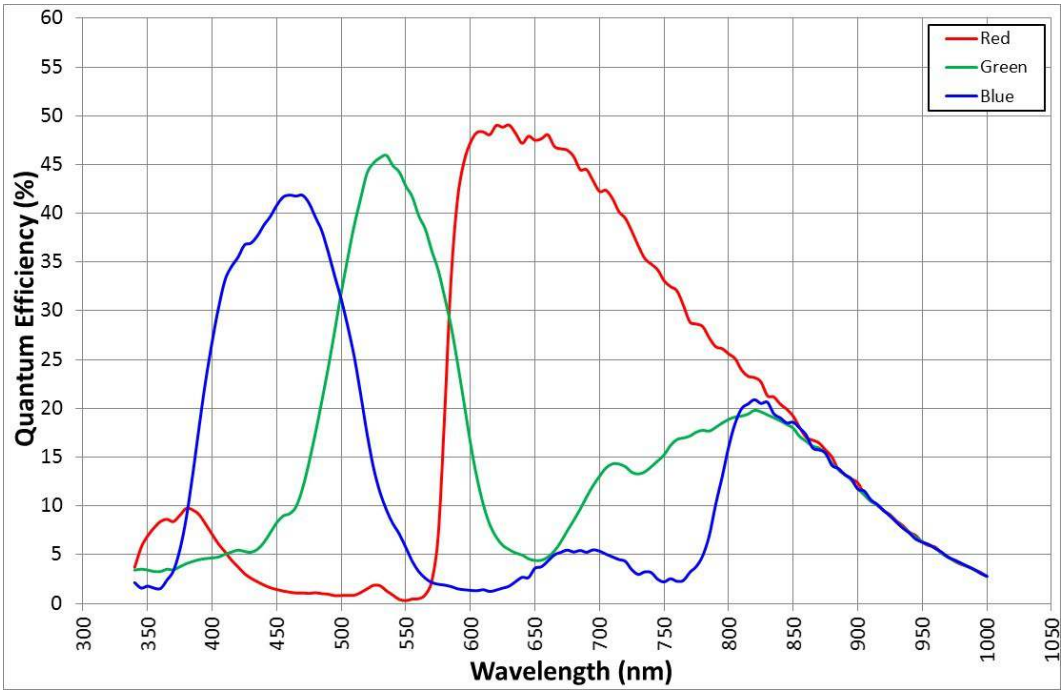


Figure 7. Color Quantum Efficiency

Angled Response

Monochrome and Color with Microlens and MAR Glass

Horizontal − the incident light angle is varied in a plane parallel to the HCCD.
Vertical − the incident light angle is varied in a plane perpendicular to the HCCD.

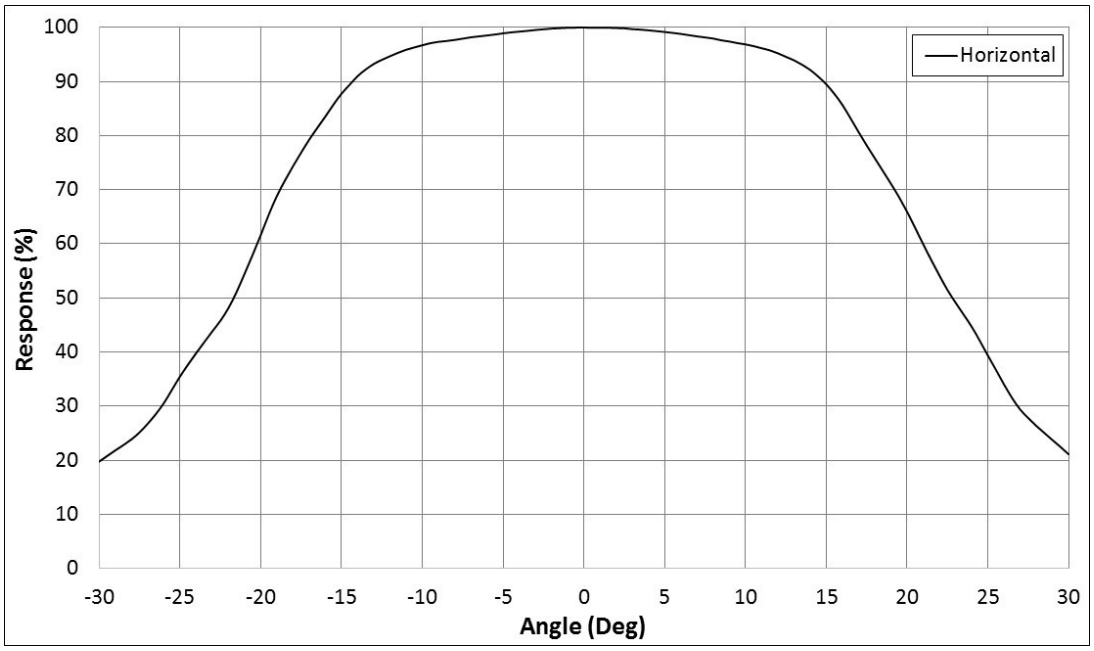


Figure 8. Angled Response for Monochrome Device

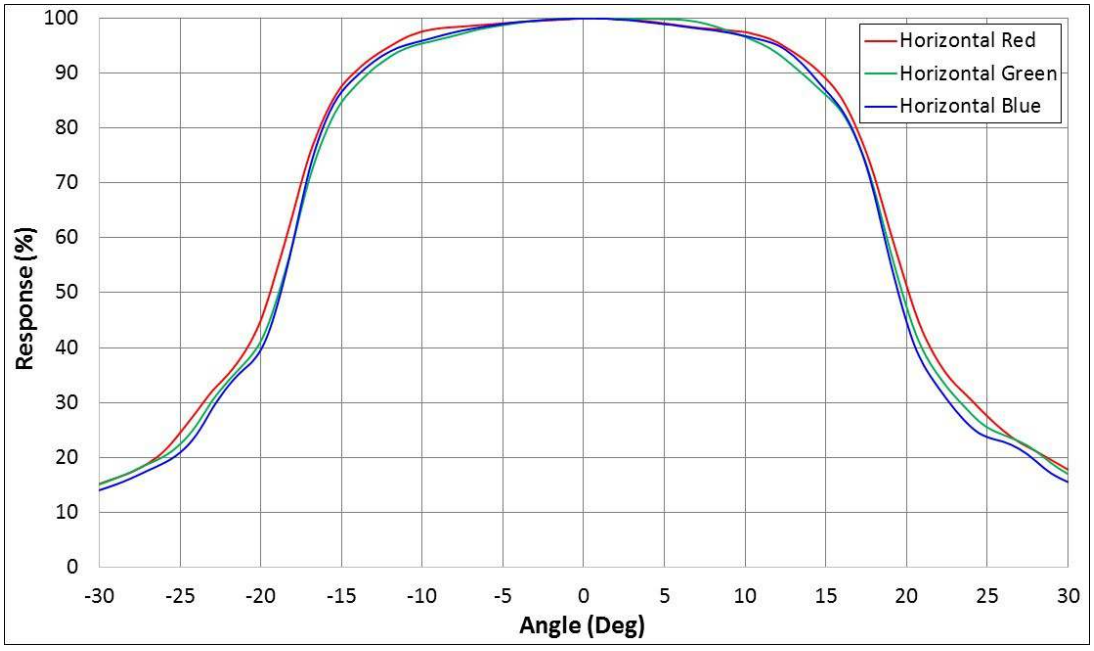


Figure 9. Angled Response for Color Sensor

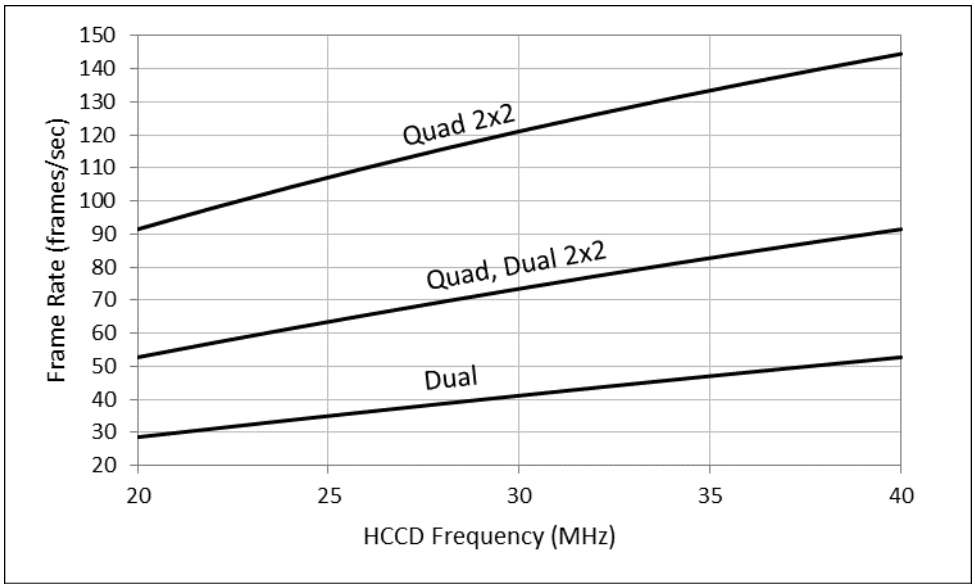


Figure 10. Frame Rates vs. Clock Frequency

DEFECT DEFINITIONS

Table 7. DEFECT DEFINITIONS

Description	Definition	Maximum Number Allowed
Major Dark Field Defective Bright Pixel	Defect ≥ 30 mV deviation from the mean, for all pixels in the active image area	20
Major Bright Field Defective Dark Pixel	≥ 12%	
Minor Dark Field Defective Bright Pixel	Defect ≥ 15 mV deviation from the mean, for all pixels in the active image area	200
Cluster Defect	A group of 2 to 10 contiguous major defective pixels, with no more than 2 adjacent defects horizontally	8
Column Defect	A group of more than 10 contiguous major dark defective pixels along a single column or 10 contiguous bright defective pixels along a single column	0

1. For the color device, a bright field defective pixel deviates by 12% with respect to pixels of the same color.
2. Column and cluster defects are separated by no less than 2 good pixels in any direction (excluding single pixel defects).
3. Low exposure dark column defects are not counted at temperatures above 0°C.

Absolute Maximum Ratings

Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or the condition is exceeded, the device will be degraded and may be damaged. Operation at these values will reduce MTTF.

The KAE−01093 image sensors are provided with configurations with epoxy sealed cover glass. The seal formed is non-hermetic, and may allow moisture ingress over time, depending on the storage environment. As a result, care must be taken to avoid cooling the device below the dew point inside the package cavity, since this may result in condensation on the sensor. For all KAE−01093 configurations, no warranty, expressed or implied, covers condensation.

Table 8. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Unit
Operating Temperature Range (Note 1)	T_{OP}	−50	+60	°C
Parameter Specification Temperature Range (Note 2)	T_{PSR}	−2	+2	°C
Output Bias Current, Total for Each Output (Note 3)	I_{OUT}	−	−15	mA

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Device degradation is not evaluated outside of these temperature ranges.
2. The device will operate effectively within a specified temperature range. The device is tested at nominally 0°C. Performance may not be guaranteed per the PERFORMANCE SPECIFICATION table for temperatures that are different than those specified within. Noise performance may degrade beyond the specification at die temperatures higher than specified here. Additionally, charge transfer may degrade beyond the specification at temperatures lower than specified here.
3. Avoid shorting output pins to ground or any low impedance source during operation. Irreparable damage will occur and is not covered by warranty. Amplifier bandwidth increases at higher current and lower load capacitance at the expense of reduced gain (sensitivity).

Table 9. ABSOLUTE MAXIMUM VOLTAGE RATINGS BETWEEN PINS AND GROUND

Description	Minimum	Maximum	Unit
VDD2(a,b,c,d), VDD3(a,b,c,d)	−0.4	17.5	V
VDD1(a,b,c,d), VOUT1(a,b,c,d)	−0.4	7.0	V
V1B, V1T	ESD − 0.4	ESD + 22.0	V
V2B, V2T, V3B, V3T, V4B, V4T	ESD − 0.4	ESD + 14.0	V
H1(a,b,c,d), H2(a,b,c,d) H1S(a,b,c,d), H2S(a,b,c,d) H1B(a,b,c,d), H2B(a,b,c,d) H1BEM(a,b,c,d), H2BEM(a,b,c,d) H2SW2(a,b,c,d), H2SW3(a,b,c,d) H2L(a,b,c,d) H2X(a,b,c,d) H3S(a,b,c,d), H3B(a,b,c,d) RG1(a,b,c,d), RG23(a,b,c,d)	−0.4	+10	V
H1SEM(a,b,c,d), H2SEM(a,b,c,d)	−0.4	+20	V
ESD	−9.0	0.0	V
SUB (Notes 1 and 2)	5.0	25	V

1. Refer to Application Note *Using Interline CCD Image Sensors in High Intensity Visible Lighting Conditions.*
2. The measured value for VSUBREF is a diode drop (0.5 V) higher than the recommended minimum VSUB bias.

GUIDELINES FOR OPERATION

Power Up and Power Down Sequence

SUB and ESD power up first, then power up all other biases in any order. No pin may have a voltage less than ESD at any time. All HCCD pins must be greater than or equal to GND at all times. The SUBREF pin will not become valid until VDD15 has been powered. The SUB pin should be at least 4 V before powering up VDD2(a,b,c,d) and VDD3(a,b,c,d).

Table 10. DC BIAS OPERATING CONDITIONS

Description	Pins	Symbol	Min	Nom	Max	Unit	Maximum DC Current
Output Amplifier Return	VSS1(a,b,c,d)	VSS1 (ISS1)	−8.3	−8.0	−7.7	V	4 mA (Per Output)
Output Amplifier Supply	VDD1(a,b,c,d)	VDD1 (IDD1)	4.5	5.0	6.0	V	3 mA + IOUT (Per Output)
Output Amplifier Supply	VDD2(a,b,c,d)	VDD2 (IDD2)	+14.7	+15.0	+15.3	V	2 mA + IOUT (Per Output)
Output Amplifier Supply	VDD3(a,b,c,d)	VDD3 (IDD3)	+14.7	+15.0	+15.3	V	2 mA + IOUT (Per Output)
Supply Voltage (Note 1)	VDD15 VDD3(a,b,c,d)	VDD15 (IDD15)	+14.7	+15.0	+15.3	V	9 mA (Full Sensor)
Ground	GND	GND	0.0	0.0	0.0	V	
Substrate (Notes 2 and 3)	SUB	VSUB	5.0	VAB	9.0	V	Up to 1 mA (Determined by Photocurrent)
ESD Protection Disable	ESD	ESD (IESD)	−8.3	−8.0	−7.7	V	2 mA (Full Sensor)
Output Bias Current	VOUT1(a,b,c,d), VOUT2(a,b,c,d), VOUT3(a,b,c,d)	IOUT	4.5	5.0	7.0	mA	Per Output

1. VDD15 bias pins must be maintained at 15 V during operation.
2. The value of VAB (nominal VSUB) printed on the label for each sensor corresponds to the voltage output on the VSUBREF pin minus 0.5 V. VSUBREF is programmed to be one diode drop, 0.5 V, above the nominal VAB voltage at 0°C during production testing (for other temperatures, there is a temperature dependence of approximately 0.01 V/degree). Therefore the proper VSUB value can be determined from the sensor itself by measuring VSUBREF when VDD2(a,b,c,d) and VDD3(a,b,c,d) are at their specified voltages and then subtracting 0.5 V. It is noted that VSUBREF is unique to each image sensor and may vary from 5.5 to 9.5 V. In addition, the output impedance of VSUBREF is approximately 25 kΩ.
3. **Caution:** The EMCCD register must NOT be clocked while the electronic shutter pulse is high.

AC Operating Conditions

Clock Levels

Table 11. CLOCK LEVELS

Pin	Function	HCCD and RG					
		Low Level			Amplitude		
		Min	Nom	Max	Min	Nom	Max
H3B(a,b,c,d)	Reversible HCCD Barrier 3	−0.2	0.0	+0.2	3.1	3.3	3.6
H2B(a,b,c,d)	Reversible HCCD Barrier 2	−0.2	0.0	+0.2	3.1	3.3	3.6
H1B(a,b,c,d)	Reversible HCCD Barrier 1	−0.2	0.0	+0.2	3.1	3.3	3.6
H3S(a,b,c,d)	Reversible HCCD Storage 3	−0.2	0.0	+0.2	3.1	3.3	3.6
H2S(a,b,c,d)	Reversible HCCD Storage 2	−0.2	0.0	+0.2	3.1	3.3	3.6
H1S(a,b,c,d)	Reversible HCCD Storage 1	−0.2	0.0	+0.2	3.1	3.3	3.6
H2SW2(a,b,c,d), H2SW3(a,b,c,d)	HCCD Switch 2 and 3	−0.2	0.0	+0.2	3.1	3.3	3.6
H2L(a,b,c,d)	HCCD Last Gate	−0.2	0.0	+0.2	3.1	3.3	3.6
H2X(a,b,c,d)	Floating Gate Exit	−0.2	0.0	+0.2	5.7	6.0	6.3
OG1(a,b,c,d)	Output Gate 1	−3.0	−2.7	−2.4	5.7	6.0	6.3
RG1(a,b,c,d)	Floating Gate Reset	Cap			3.1	3.3	3.6
RG23(a,b,c,d)	Floating Diffusion Reset	Cap			3.1	3.3	3.6
H1BEM(a,b,c,d)	Multiplier Barrier 1	−0.2	0.0	+0.2	4.6	5.0	5.4
H2BEM(a,b,c,d)	Multiplier Barrier 2	−0.2	0.0	+0.2	4.6	5.0	5.4
H1SEM(a,b,c,d)	Multiplier Storage 1	−0.3	0.0	+0.3	8.0	–	18.0
H2SEM(a,b,c,d)	Multiplier Storage 2	−0.3	0.0	+0.3	8.0	–	18.0

1. HCCD Operating Voltages. There can be no overshoot on any horizontal clock below −0.4 V: the specified absolute minimum. The H1SEM and H2SEM clock amplitudes need to be software programmable independently for each quadrant to adjust the charge multiplier gain.
2. Reset Clock Operation: The RG1, RG23 signals must be capacitive coupled into the image sensor with a 0.01 μF to 0.1 μF capacitor. The reset clock overshoot can be no greater than 0.3 V, see Figure 13.

Clock Capacitances

Pin	pF
H1SEMa	54
H2SEMa	54
H1BEMa	54
H2BEMa	54
H1a	42
H2a	42
H1Sa	52
H2Sa	52
H3Sa	52
H1Ba	39
H2Ba	39
H3Ba	39

Pin	pF
H1SEMb	54
H2SEMb	54
H1BEMb	54
H2BEMb	54
H1b	42
H2b	42
H1Sb	52
H2Sb	52
H3Sb	52
H1Bb	39
H2Bb	39
H3Bb	39

Pin	pF
H1SEMc	54
H2SEMc	54
H1BEMc	54
H2BEMc	54
H1c	42
H2c	42
H1Sc	52
H2Sc	52
H3Sc	52
H1Bc	39
H2Bc	39
H3Bc	39

Pin	pF
H1SEMd	54
H2SEMd	54
H1BEMd	54
H2BEMd	54
H1d	42
H2d	42
H1Sd	52
H2Sd	52
H3Sd	52
H1Bd	39
H2Bd	39
H3Bd	39

Pin	nF
V1B	11
V2B	8
V3B	9
V4B	9
V1T	11
V2T	8
V3T	9
V4T	9

NOTE: The capacitances of H2X, RG1, RG23, H2SW, H2L, and OG1 are each 20 pF or less.

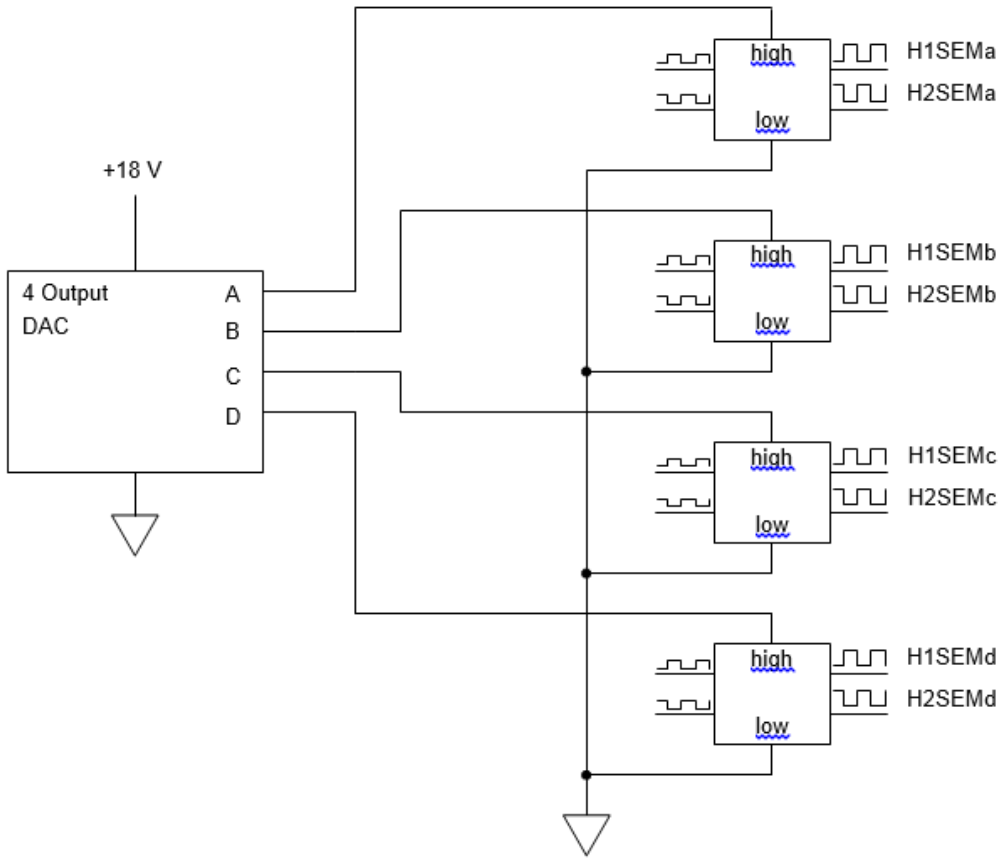


Figure 11. EMCCD Clock Adjustable Levels

For the EMCCD clocks, each quadrant must have independently adjustable high levels. All quadrants have a common low level of GND. The high level adjustments must be software controlled to balance the gain of the four outputs.

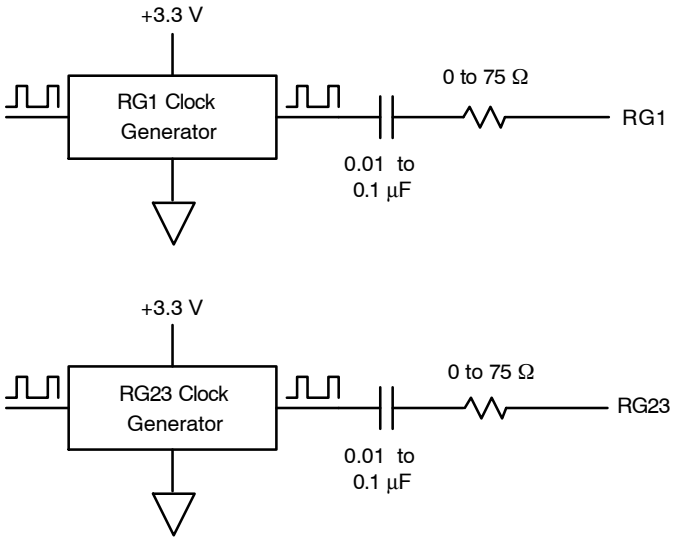


Figure 12. Reset Clock Drivers

The RG1, RG23 signals must be capacitive coupled into the image sensor with a 0.01 μF to 0.1 μF capacitor. The reset clock overshoot can be no greater than 0.3 V, see Figure 13. The damping resistor values would vary between 0 and 75 Ω depending on the layout of the circuit board.

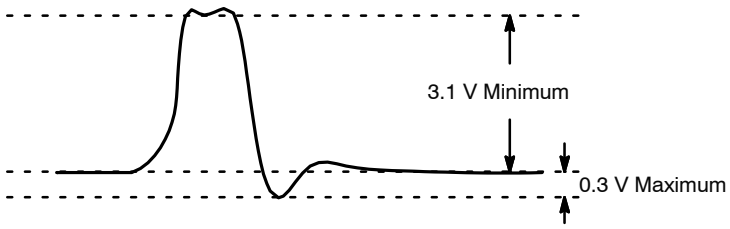


Figure 13. RG Clock Overshoot

Table 12. VCCD

Pin	Function	Min	Nom	Max
V1T, V1B, V2T, V2B, V3T, V3B, V4T, V4B	Vertical CCD Clock, Low Level	−8.0	−6.5	−6.0
V1T, V1B, V2T, V2B, V3T, V3B, V4T, V4B	Vertical CCD Clock, Mid Level	−0.2	0.0	+0.2
V1T, V1B	Vertical CCD Clock, High (3rd) Level	10.5	11.0	12.0

Table 13. ELECTRONIC SHUTTER PULSE (VES)

Pin	Function	Low Level (DC)	High Level (Pulse) Minimum	High Level (Pulse) Maximum
SUB	Electronic Shutter	VAB (VSUBREF − 0.5)	18	25

Device Identification

The device identification pin (DevID) may be used to determine which ON Semiconductor interline EMCCD sensor is being used.

Table 14. DEVICE IDENTIFICATION VALUES

Description	Pin	Symbol	Min	Nom	Max	Unit	Maximum DC Current
Device Identification (Notes 1, 2 and 3)	ID	DevID	700	920	1100	Ω	0.3 mA

1. Nominal value subject to verification and/or change during release of preliminary specifications.
2. If the Device Identification is not used, it may be left disconnected.
3. After Device Identification resistance has been read during camera initialization, it is recommended that the circuit be disabled to prevent localized heating of the sensor due to current flow through the R_DeviceID resistor.

Recommended Circuit

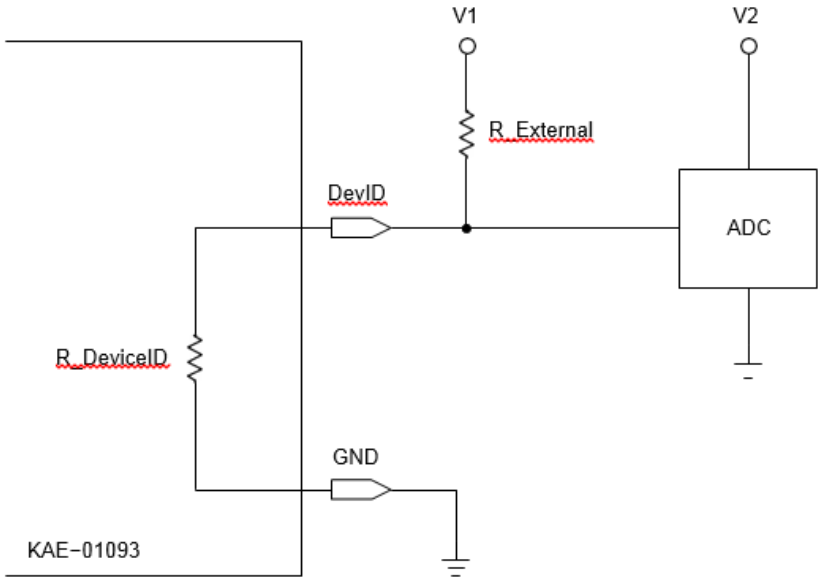


Figure 14. Device Identification Recommended Circuit

THEORY OF OPERATION

Image Acquisition

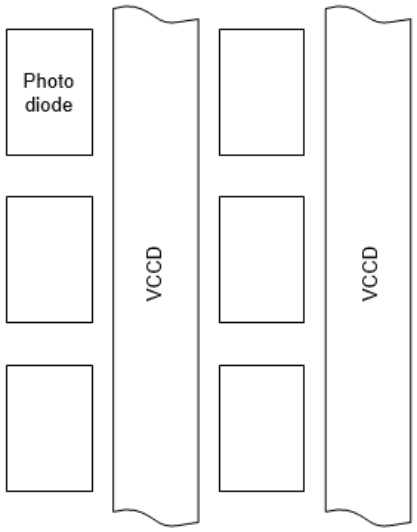


Figure 15. An Illustration of Two Columns and Three Rows of Pixels

This image sensor is capable of detecting up to 60,000 electrons with a small signal noise floor of less than 1 electron all within one image. Each 9.0 μm square pixel, as shown in Figure 15 above, consists of a light sensitive photodiode and a portion of the vertical CCD (VCCD). Not shown is a microlens positioned above each photodiode to focus light away from the VCCD and into the photodiode. Each photon incident upon a pixel will generate an electron in the photodiode with a probability equal to the quantum efficiency.

The photodiode may be cleared of electrons (electronic shutter) by pulsing the SUB pin of the image sensor up to the minimum VES voltage (VES_{min}) of 18 V for a time of at least 2 μs. When the SUB pin is at VES_{min}, the photodiode can hold no electrons, and the electrons flow downward into the substrate. When the SUB pin is returned to its DC level (VAB), the integration of electrons in the photodiode begins. The HCCD and EMCCD clocks should be stopped when the electronic shutter is pulsed, to avoid having the large voltage pulse on SUB coupling into the video outputs and altering the EMCCD gain.

It should be noted that there are certain conditions under which the device will have no anti-blooming protection: when the V1T and V1B pins are high, very intense illumination generating electrons in the photodiode will flood directly into the VCCD.

The VCCD is shielded from light by metal to prevent detection of more photons. For very bright spots of light, some photons may leak through or around the metal light shield and result in electrons being transferred into the VCCD. This is called image smear.

Image Readout

At the start of image readout, the voltage on the V1T and V1B pins is pulsed from 0 V up to the high level for at least 10 μs and back to 0 V, which transfers the electrons from the photodiodes into the VCCD. If the VCCD is not empty, then the electrons will be added to what is already in the VCCD.

The VCCD is read out one row at a time. During a VCCD row transfer, the HCCD clocks are stopped. All gates of type H1 stop at the high level and all gates of type H2 stop at the low level. After a VCCD row transfer, charge packets of electrons are advanced one pixel at a time towards the output amplifiers by each complimentary clock cycle of the H1, H2, and H3 gates.

To prevent overfilling the charge multiplier, a non-destructive floating gate output amplifier (VOUT1) is provided on each quadrant of the image sensor as shown in Figure 16 below.

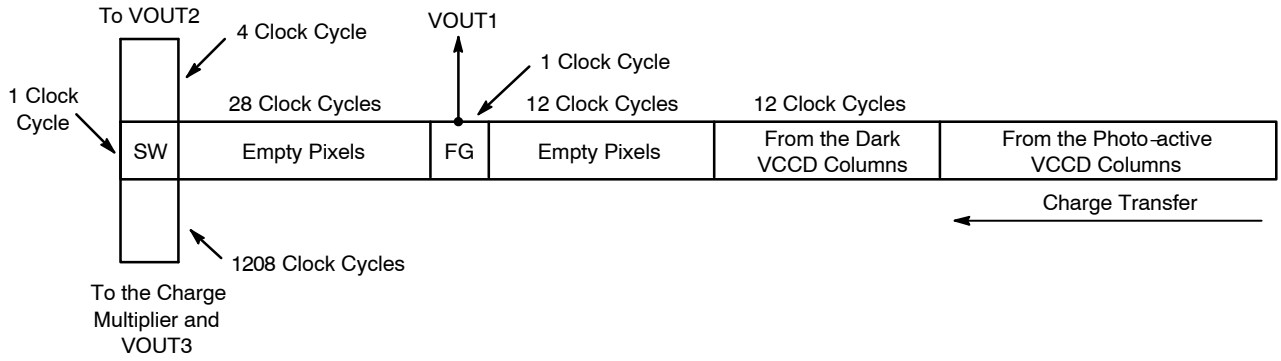


Figure 16. The Charge Transfer Path of One Quadrant

After one row has been transferred from the VCCD into the HCCD, the HCCD clock cycles should begin. After 12 HCCD clock cycles the first dark VCCD column pixel will arrive at (VOUT1). After another 12 (24 total) HCCD clock cycles the first photo-active pixel charge packet will arrive (see Figure 16).

Before reaching the output amplifiers, each pixel charge packet passes through VOUT1. The floating gate output amplifier is able to sense how much charge is present in a pixel charge packet without altering the number of electrons in that charge packet. An output load sink must be applied to each VOUT1 pin to activate each floating gate output amplifier. The voltage at the output of the floating gate output amplifier is measured using the traditional correlated double sampling technique and digitized to allow for analysis by the camera.

The floating gate output amplifier functions as a charge threshold detector. For each pixel, the camera evaluates the number of electrons contained in the pixel, compares the measured number of electrons to the camera's Charge Threshold (see Setting the Charge Threshold) and routes the pixel charge packet to either the normal floating diffusion output amplifier (VOUT2) or to the EMCCD output amplifier (VOUT3) by controlling the timing of the H2SW2 and H2SW3 signals.

The pixel packet routing action takes place 28 HCCD clock cycles after the pixel charge packet passes through the floating gate amplifier (VOUT1). The 28 HCCD clock cycle delay is to allow for pipeline delays of the A/D converter inside the Analog Front End (AFE). The camera's timing generator must dynamically alter the timing of the H2SW2 and H2SW3 signals on a pixel by pixel basis based on the results of the pixel packet measurement performed on the VOUT1 signal (see Figure 17 FPGA Pipeline).

To route a charge packet to the EMCCD charge multiplier (VOUT3) H2SW2 is held at GND and H2SW3 is clocked with the same timing as H2 for that one clock cycle.

To route a charge packet to the normal output (VOUT2) H2SW3 is held at GND and H2SW2 is clocked with the same timing as H2 for that one clock cycle.

For optimum performance, alignment of the critical timing signals is very important (see CCD clock signal optimization).

Setting the Charge Threshold

The charge multiplier has a maximum charge handling capacity (above 20x gain) of 30,000 electrons. Therefore, the average signal level should be 20,000 electrons or less to accommodate a normal distribution of signal levels (see Figure 18). At the maximum gain of 130x no more than 150 electrons should be allowed into the EMCCD.

The criteria that determines which output the pixel charge packet will be routed to is the Charge Threshold. For most applications, it is recommended that the Charge Threshold be set to 150 electrons. Pixels with charge packets measured to be greater than 150 electrons should be routed to the normal floating diffusion output amplifier VOUT2. Pixels with charge packets measured to be less than 150 electrons should be routed to the EMCCD and VOUT3.

Considerations when setting the camera's Charge Threshold:

1. EMCCD large signal performance. Sending signals larger than 150 electrons into the EMCCD will produce images with lower signal to noise ratio than if they were read out of the normal floating diffusion output amplifier.
2. EMCCD capacity. The EMCCD charge multiplier has a maximum charge handling capacity of 30,000 electrons. Overfilling the charge multiplier beyond 30,000 electrons will shorten its useful operating lifetime and risks inducing a latchup condition within the imager. To recover from an EMCCD latchup condition the HSEM clock voltages have to be lowered to +8.0 volts and clocked with this lower voltage for a time period that will allow the EMCCD to be emptied of charge.
   The non-destructive floating gate output amplifier is able to sense how much charge is present in a charge packet without altering the number of electrons in that charge packet. This type of amplifier has a low charge-to-voltage conversion gain (about 5.8 $\mu V/e^-$) and high noise (about 65 electrons), but it is being used only as a threshold detector, and not an imaging detector. Even with 65 electrons of noise, it is adequate to determine whether a charge packet is greater than or less than the recommended threshold of 150 electrons.

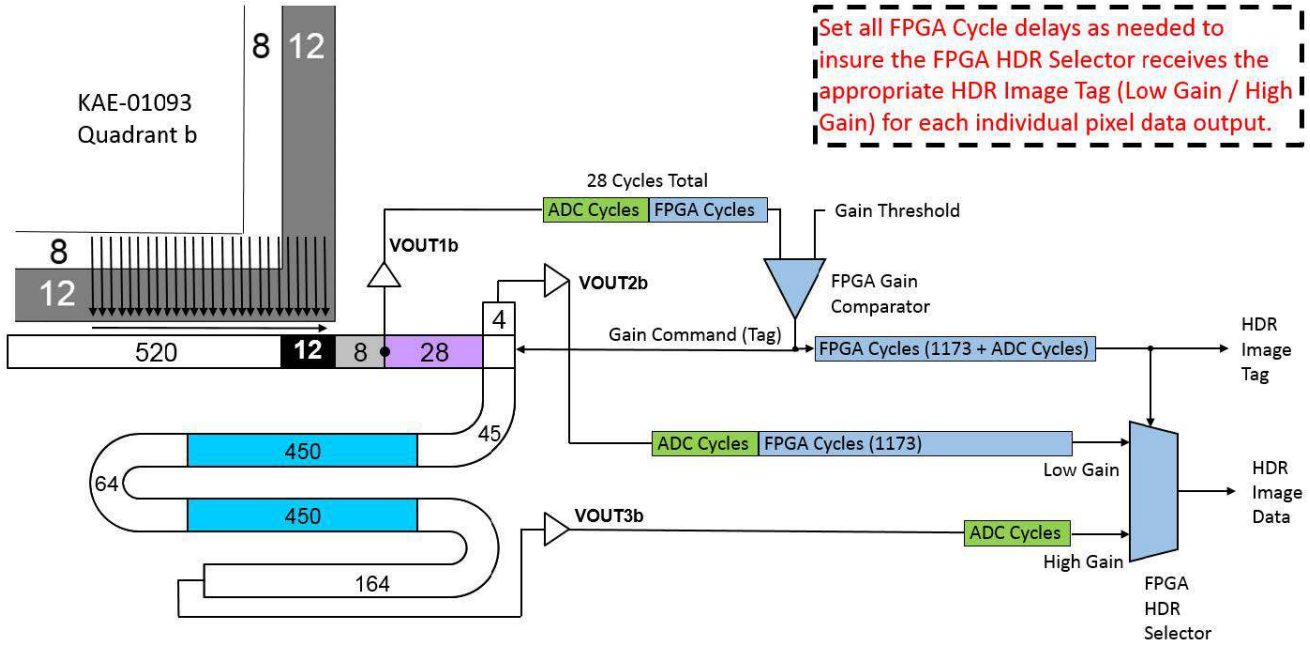


Figure 17. KAE−01093 FPGA Pipeline

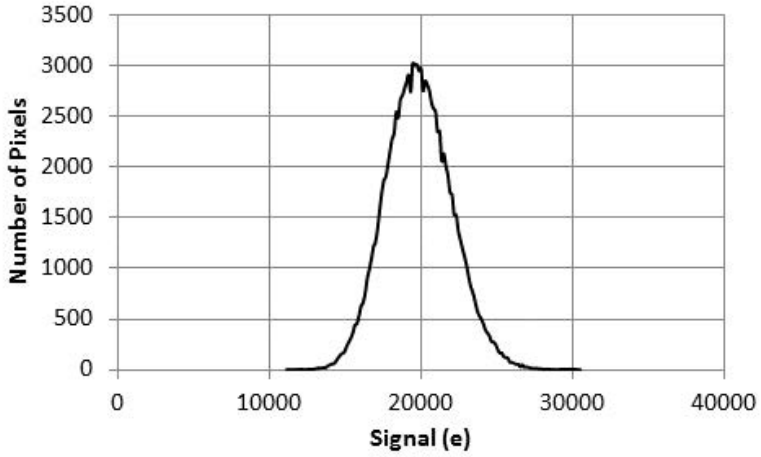


Figure 18. EMCCD Charge Multiplier (VOUT3) Histogram at the Maximum Gain of 130x and Charge Threshold Set to 150 Electrons

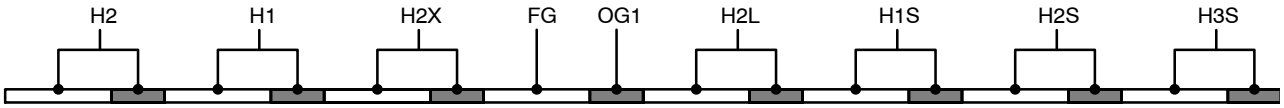


Figure 19. The Structure of the HCCD and Floating Gate Amplifier. The Direction of Charge is from Right to Left

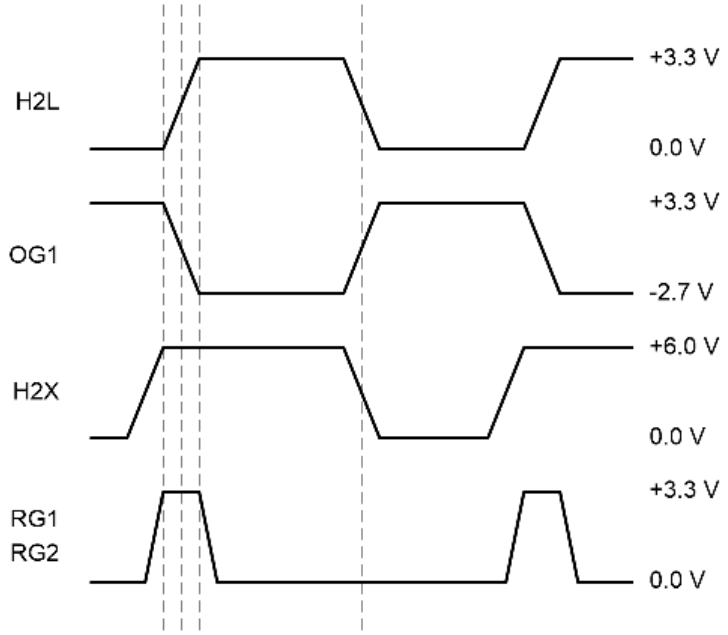


Figure 20. The Timing of the Clock Inputs Associated with the Floating Gate Amplifier, VOUT1

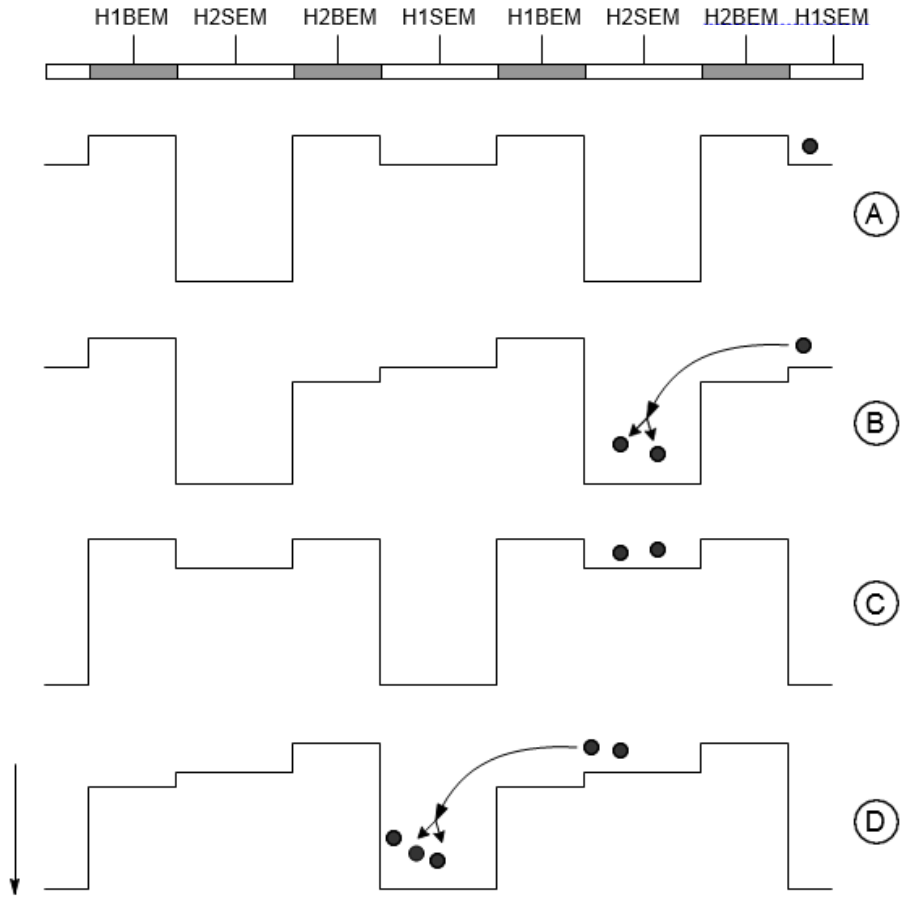
CCD Clock Signal Optimization

The RG1 input signal is pulsed during the rising edge of the H2L signal to reset the floating gate to a known starting voltage. The OG1 signal is clocked opposite of the H2X and H2L signals. The OG1 clocking counteracts any capacitive coupling effects that clocking the H2X and H2L signals would otherwise have on the floating gate. For maximum charge handling capability, the rising edge of the H2X signal should lead the rising edge of the H2L signal and the falling edge of the OG1 signal.

Aligning the rising edge of H2X with the rising edge of H2L limits the maximum signal level to less than 60 ke$^-$. The falling edges of the H2X and H2L signals should be coincident with the rising edge of the OG1 signal.

The RG1, RG2, H2X, H2L, and OG1 signals are all continuously running clocks. These signals should not be stopped during a VCCD line transfer.

EMCCD OPERATION



NOTE: Charge flows from right to left.

Figure 21. The Charge Multiplication Process

The charge multiplication process, shown in Figure 21 above, begins at time step A, when an electron is held under the H1SEM gate. The H2BEM and H1BEM gates block the electron from transferring to the next phase until the H2SEM has reached its maximum voltage. When the H2BEM is clocked from 0 to +5 V, the channel potential under H2BEM increases until the electron can transfer from H1SEM to H2SEM. When the H2SEM gate is above 10 V, the electric field between the H2BEM and H2SEM gates gives the electron enough energy to free a second electron which is collected under H2SEM. Then the voltages on H2BEM and H2SEM are both returned to 0 V at the same time that H1SEM is ramped up to its maximum voltage. Now the process can repeat again with charge transferring into the H1SEM gate.

The alignment of clock edges is shown in Figure 22. The rising edge of the H1BEM and H2BEM gates must be delayed until the H1SEM or H2SEM gates have reached their maximum voltage. The falling edge of H1BEM and H2BEM must reach 0 V before the H1SEM or H2SEM reach 0 V. There are a total of 1,800 charge multiplying transfers through the EMCCD on each quadrant.

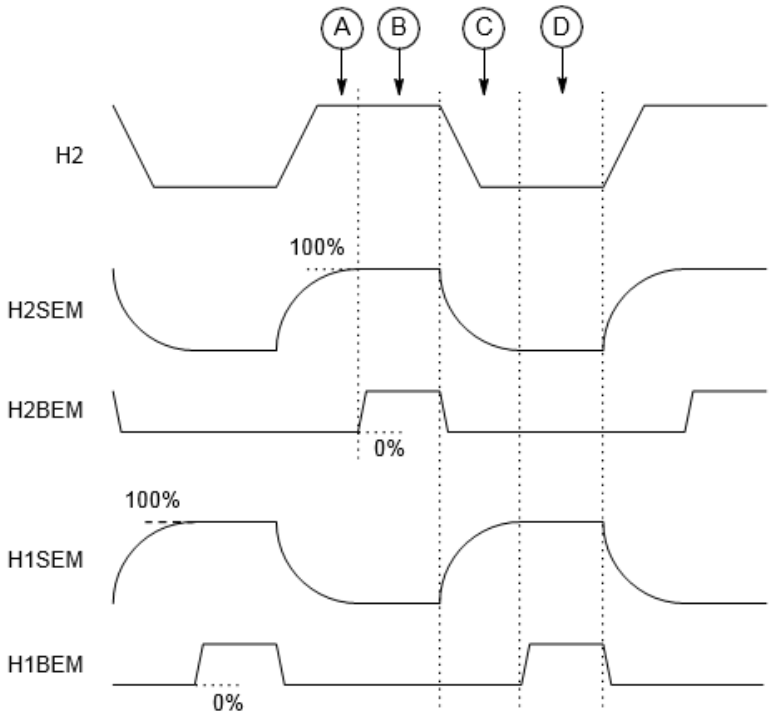
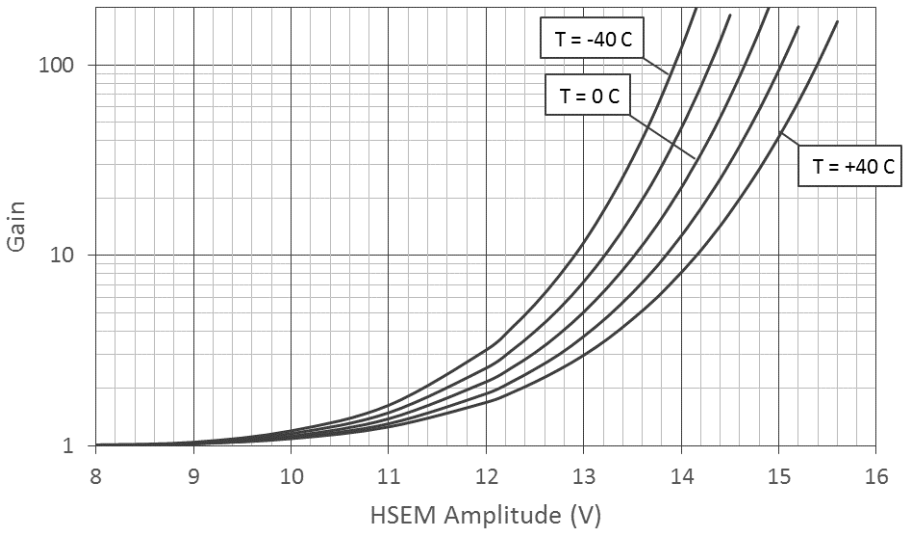


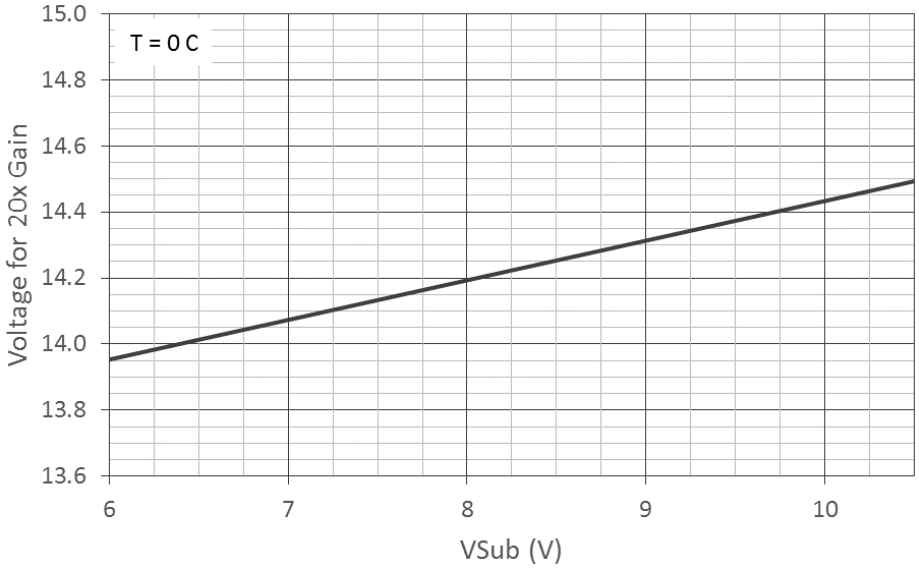
Figure 22. The Timing Diagram for Charge Multiplication

The amount of gain through the EMCCD will depend on temperature and H1SEM and H2SEM voltage as shown in Figure23. Gain also depends on substrate voltage, as shown in Figure 24, and on the input signal, as shown in Figure 25.



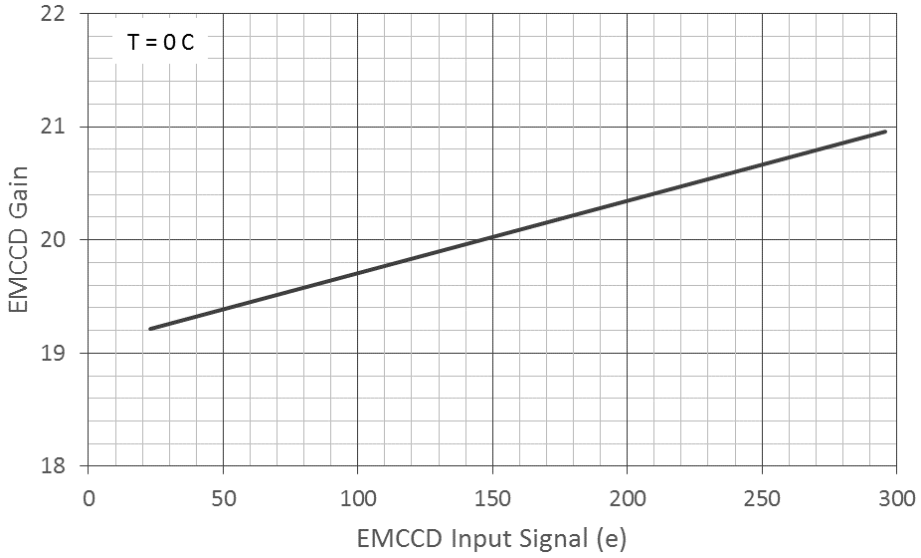
NOTE: This figure represents data from only one example image sensor, other image sensors will vary.

Figure 23. The Variation of Gain vs. EMCCD High Voltage and Temperature



NOTE: EMCCD gain is not constant with substrate voltage.

Figure 24. The Requirement EMCCD Voltage for Gain of 20x vs. Substrate Voltage



NOTE: The EMCCD voltage was set to provide 20x gain with an input of 150 electrons.

Figure 25. EMCCD Gain vs. Input Signal

If more than one output is used, then the EMCCD high level voltage must be independently adjusted for each quadrant. This is because each quadrant will require a slightly different voltage to obtain the same gain. In addition, the voltage required for a given gain differs unpredictably from one image sensor to the next, as in Figure 26. Because of this, the gain vs. voltage relationship must be calibrated for each image sensor, although within each quadrant, the H1SEM and H2SEM high level voltage should be equal.

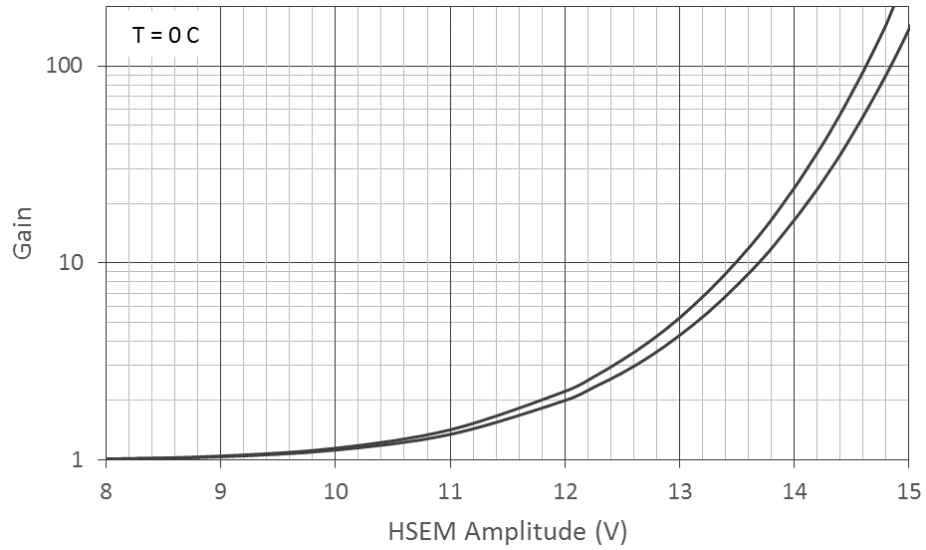
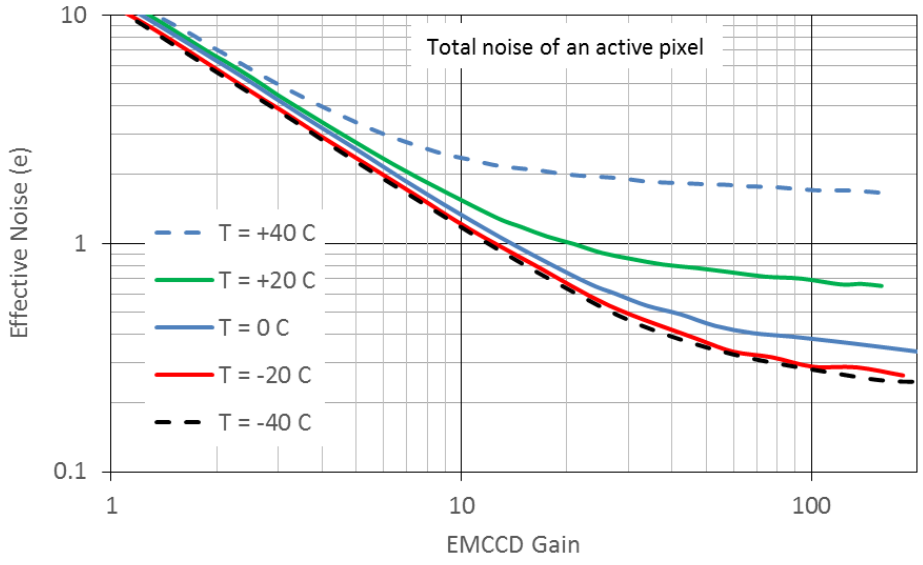


Figure 26. An Example Showing How Two Image Sensors Can have Different Gain vs. Voltage Curves

The effective output noise of the image sensor is defined as the noise of the output signal divided by the gain. This is measured with zero input signal to the EMCCD. Figure 27 shows the EMCCD by itself has a very low noise that goes as the noise at gain = 1 divided by the gain. The EMCCD has very little clock-induced charge and does not require elaborate sinusoidal waveform clock drivers. Simple square wave clock drivers with a resistor between the driver and sensor for a small RC time constant are all that is needed. The minimum possible noise is limited by a combination of vertical CCD spurious charge, EMCCD spurious charge, and output amplifier glow.



NOTE: The data represented by this chart includes noise from dark current and spurious charge generation.

Figure 27. EMCCD Output Noise vs. EMCCD Gain in Quad Output Mode from −40°C to +40°C

Because of these pixel array noise sources, it is recommended that the maximum gain used be 130x, which typically gives a noise floor between 0.3e and 0.6e at 0°C. Using higher gains will provide limited benefit and will degrade the signal to noise ratio due to the EMCCD excess noise factor. Furthermore, the image sensor noise is not limited by dark current noise sources when the temperature is below −20°C. Therefore, cooling below −20°C will not provide a significant improvement to the noise floor, with the negative consequence that lower temperatures increase the probability of poor charge transfer.

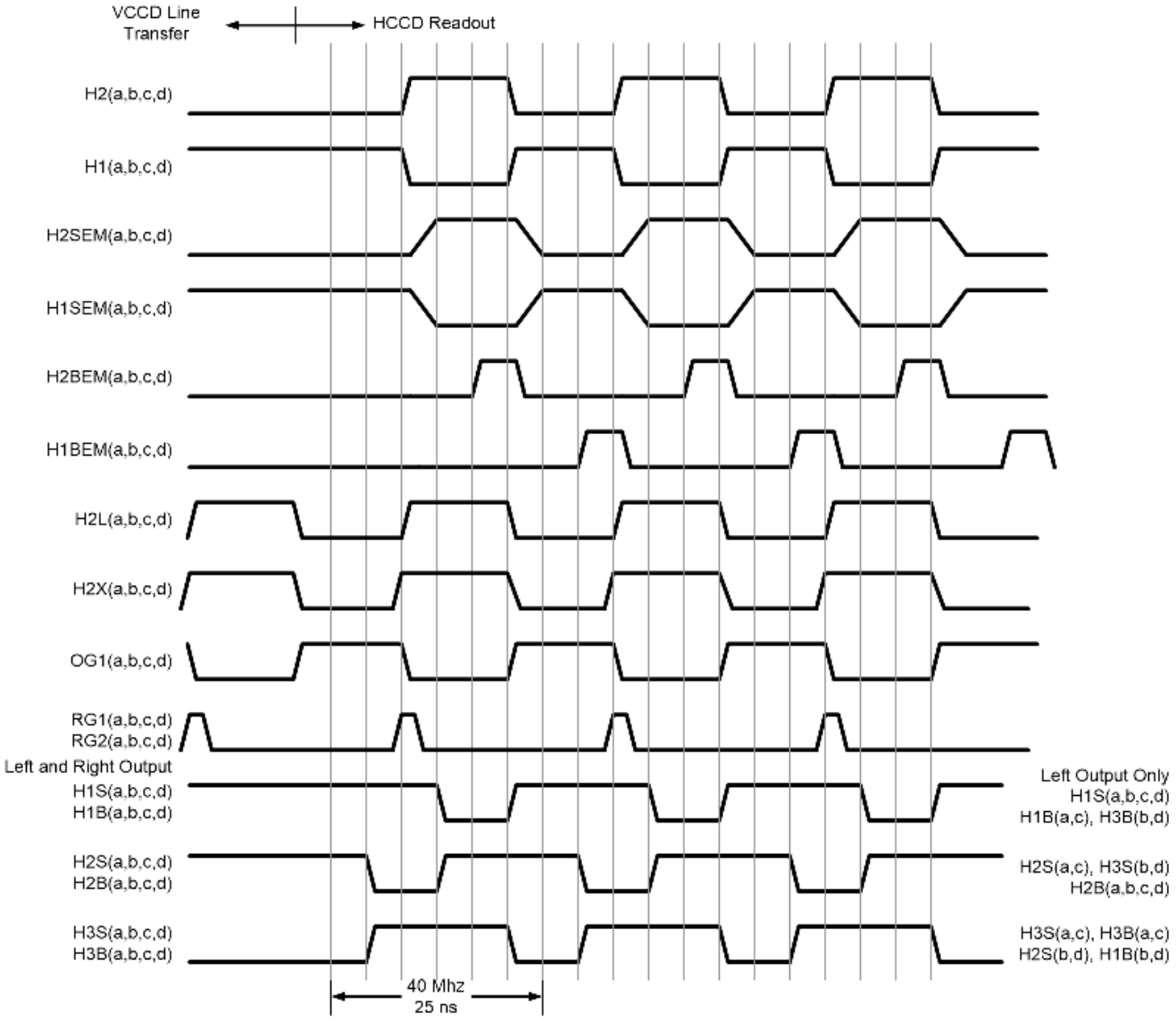
CAUTION: The EMCCD should not be operated near saturation for an extended period, as this may result in gain aging and permanently reduce the gain. It should be noted that device degradation associated with gain aging is not covered under the device warranty.

Operating Temperature

The reasons for lowering the operating temperature are to reduce dark current noise and to reduce image defects. The average dark signal from the VCCD and photodiodes must be less than 1 e^- in order to have a total system noise less than 1 e^- when using the EMCCD. The recommended operating temperature is 0°C. This represents the best compromise of low noise performance vs. complexity of cooling the image sensor. Operation below −20°C is not recommended, and temperatures below −20°C may result in poor charge transfer in the HCCD. Operation above +20°C may result in excessive dark current noise.

TIMING DIAGRAMS

Pixel Timing



NOTE: The minimum time for one pixel is 25 ns.

Figure 28. Pixel Timing Pattern P1

2x Horizontal Charge Binning

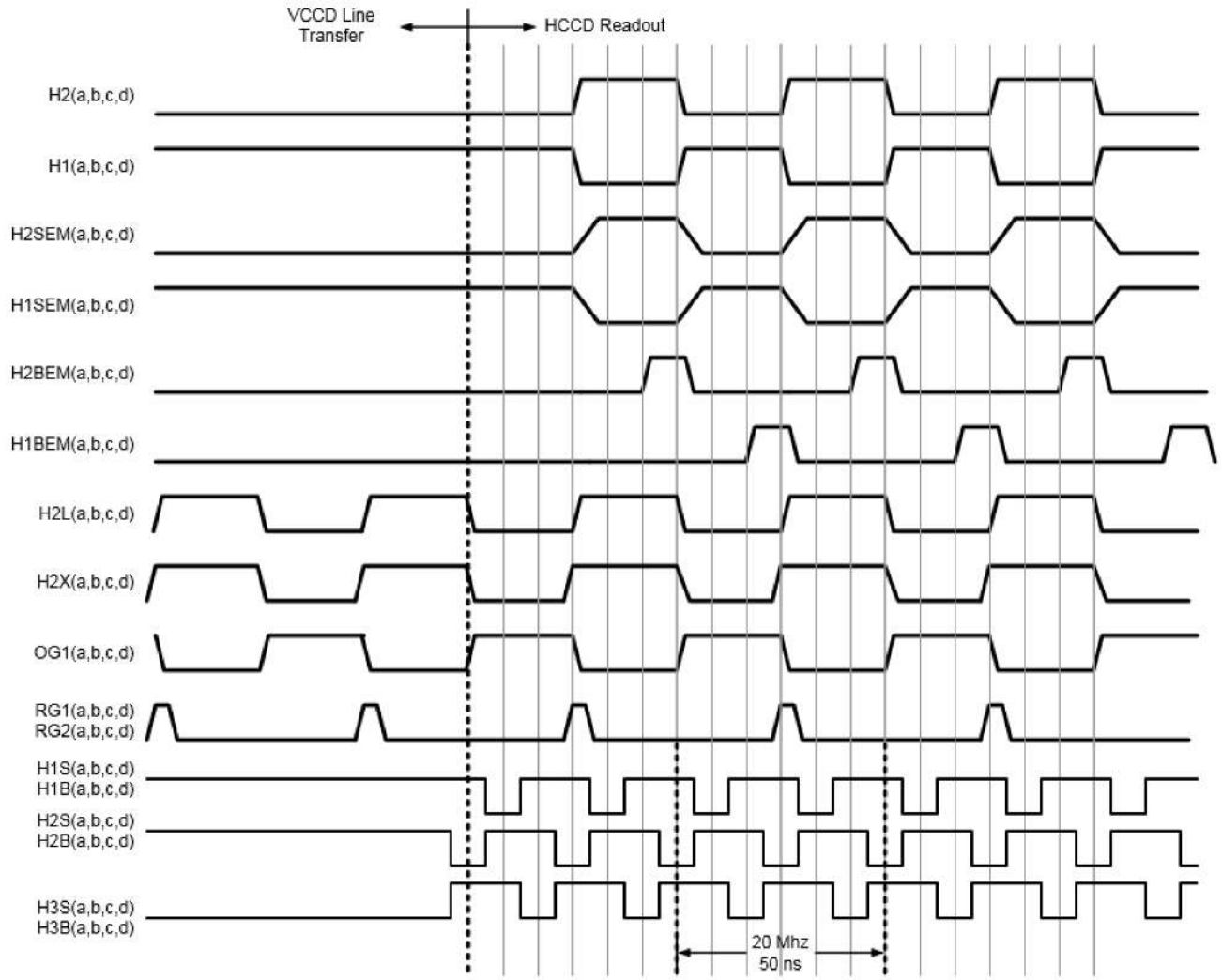


Figure 29. 2x Horizontal Charge Binning Timing Pattern

Black, Clamp, VOUT1, VOUT2, and VOUT3

Alignment at Line Start

The black level clamping operation of the analog front end (AFE) should take place within the first 28 clock cycles of every row. This applies to all modes of operation.

VCCD Timing

Vertical Transfer Times and Pulse Widths

Table 15. TIMING DEFINITIONS

Symbol	Definition	Min	Nom	Max	Unit
T_V	VCCD Transfer Time A	0.3	0.4	2.0	μs
T_{SUB}	Electronic Shutter Pulse	2.0	4.0	10.0	μs
T_{3D}	Photodiode Transfer Delay Time	280	300	320	μs
T_3	Photodiode to VCCD Transfer Time	5.0	8.0	10.0	μs

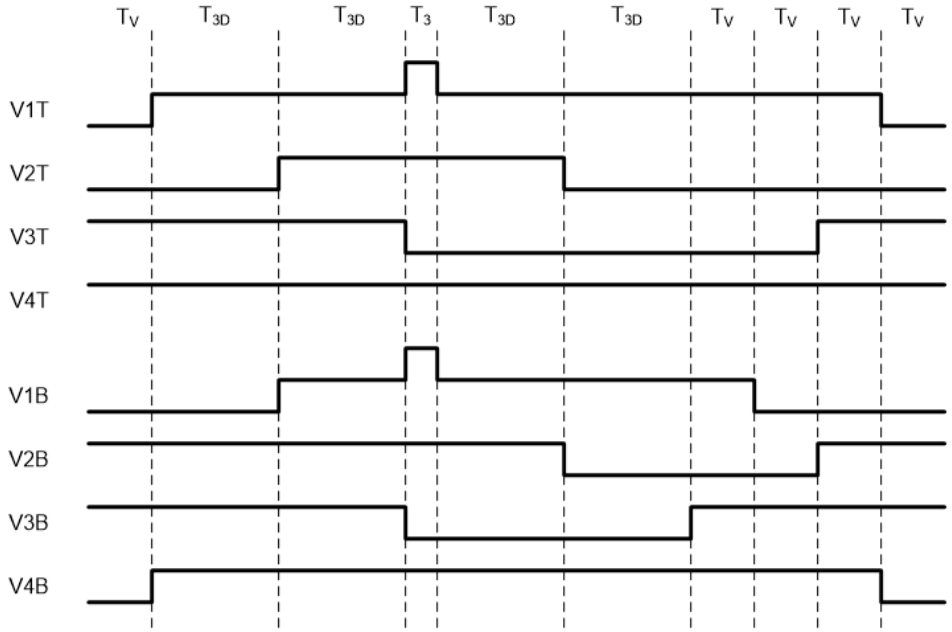


Figure 30. Timing Pattern F1. VCCD Frame Timing to Transfer Charge from Photodiodes to the VCCD

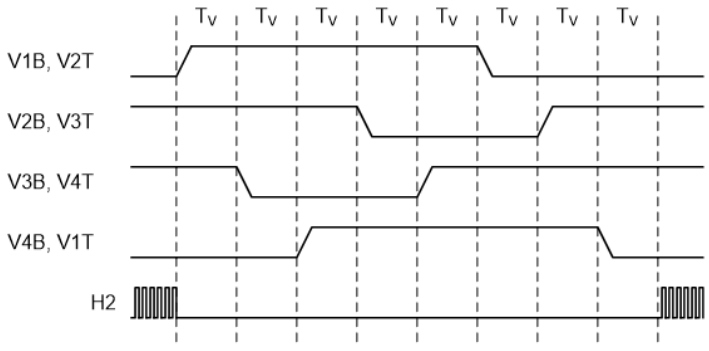


Figure 31. Line Timing L2. VCCD Line Timing to Transfer One Line of Charge from the VCCD to the HCCD

Electronic Shutter

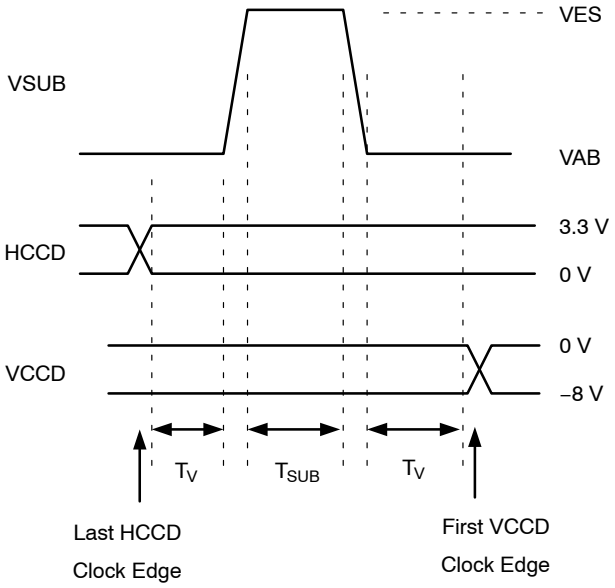


Figure 32. Electronic Shutter Timing Pattern S1

CAUTION: Caution: The EMCCD register must not be clocked while the electronic shutter pulse is high.

HCCD and EMCCD Clocks for Electronic Shutter

The HCCD and EMCCD clocks must be static during the frame, line, and electronic shutter timing sequences.

Table 16. HCCD AND EMCCD CLOCKS FOR ELECTRONICS SHUTTER

Clocks	State
H1S, H2S, H1, H1SEM, H1BEM	High
H3S, H2, H2SEM, H2BEM	Low

Table 17. FRAME RATES

Dual (Top/Bottom)	Quad	Unit
52	91	fps

Image Exposure and Readout

The flowchart for image exposure and readout is shown in the figure below. The electronic shutter timing may be omitted to obtain an exposure time equal to the image read out time. NEXP is the number of lines exposure time and NV is the number of VCCD clock cycles (row transfers).

Table 18. IMAGE READOUT TIMING

Mode	NH	NV
Dual	1208	532
Quad	1208	1064

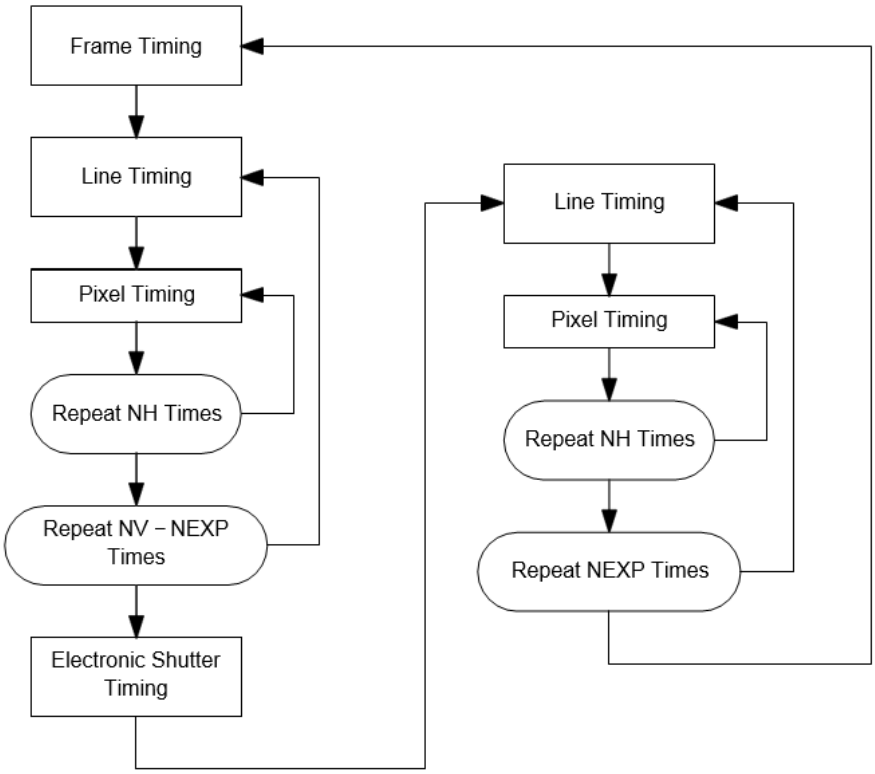


Figure 33. The Image Readout Timing Flow Chart

Long Integrations and Readout

For extended integrations the output amplifiers need to be powered down. When powered up, the output amplifiers emit near infrared light that is sensed by the photodiodes. It will begin to be visible in images of 30 second integrations or longer.

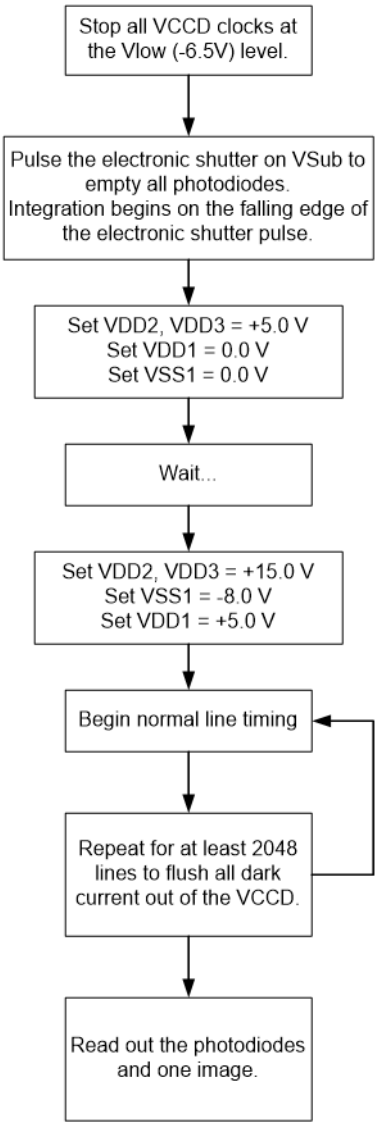


Figure 34. Timing Flow Chart for Long Integration Time

To power down the output amplifiers set VDD1 and VSS1 to 0 V, and VDD2(a,b,c,d) and VDD3(a,b,c,d) to +5 V. VDD2 or VDD3 must not be set to 0 V during the integration of an image. During the time the VDD2 and VDD3 supplies are reduced to +5 V the VDD15 pin is to be kept at +15 V. The substrate voltage reference output SUBV will be valid as long as VDD15 is powered. The HCCD and EMCCD may be continue to clock during integration. If they are stopped during integration then the EMCCD should be re-started at +7 V amplitude to flush out any undesired signal before increasing the voltage to charge multiplying levels.

THERMOELECTRIC COOLER

Representative performance plots for the TEC are shown in the following graphs.

Performance Plots of PGA Integrated TEC

For the performance plots below, the TEC was operated at maximum pulse width (DC mode) to maintain the cold EMCCD register of each or the four outputs was 20 mV, the EMCCD gain was 20x, and the horizontal clock rate was 40 MHz. The recommended maximum input current (Imax) is 2.0 A, requiring an input voltage (Vmax) of 11.1 V, but the optimum current and voltage needed for a given temperature gradient may be lower.

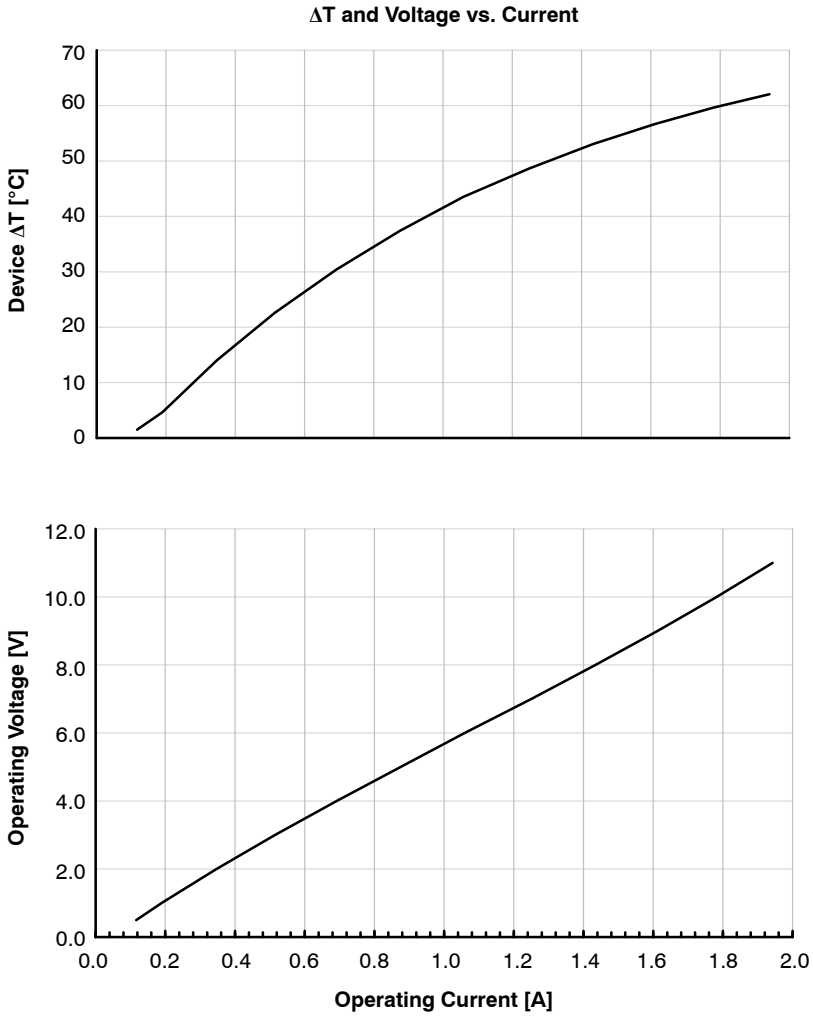


Figure 35. PGA with Integrated TEC, Temperature Gradient and Required Voltage vs. Applied Current

Performance Plot of Thermistor in PGA with Integrated TEC

The thermoelectric cooler (TEC) has an on-board thermistor with ±3% tolerance, and 10 kΩ (Ro) at 25°C (298°K, T_o). Its performance follows the equation shown below, where T = temperature in °K, over the range of 233 to 398°K, R_T = thermistor resistance in ohms. A plot of resistance vs. temperature is shown in Equation 1.

$$T = \frac{1}{\left\{(7.96E-4) + (2.67E-4)\cdot \ln(R_T) + (1.21E-7)\cdot \left(\ln(R_T)\right)^3\right\}} \quad \text{(eq. 1)}$$

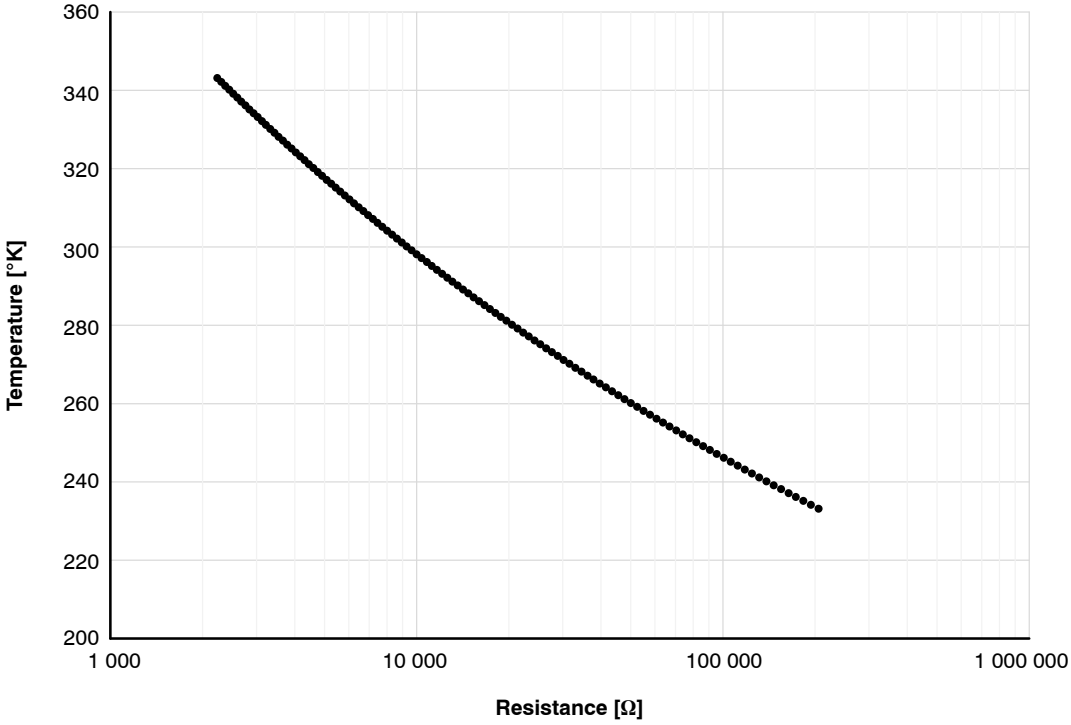


Figure 36. Thermistor Resistance vs. Temperature

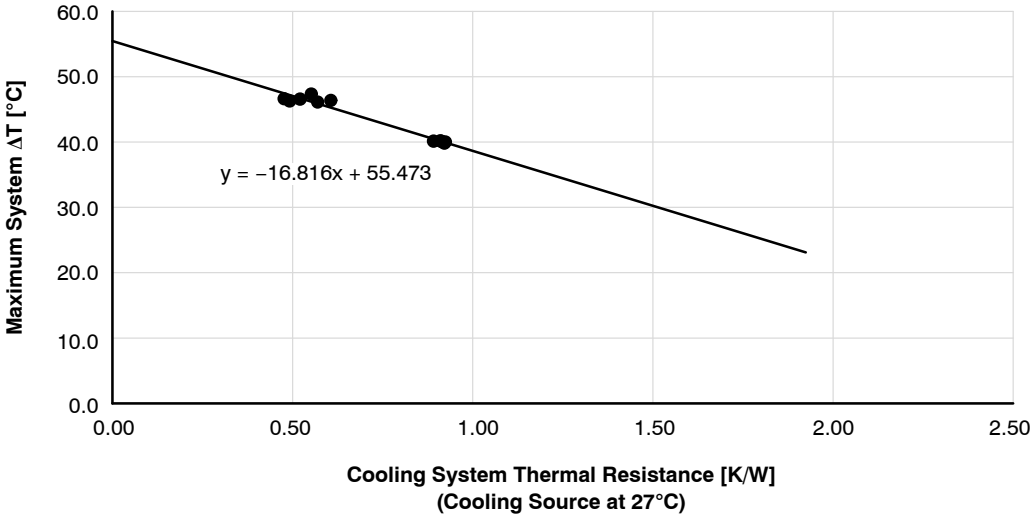


Figure 37. Maximum DT vs. Cooling System Thermal Resistance

STORAGE AND HANDLING DETAILS

For information on Storage, ESD prevention, cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com. Please note that CCD products are not shipped or stored in Moisture Barrier Bags (MBB) and Moisture Sensitivity Level (MSL) ratings are not specified.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

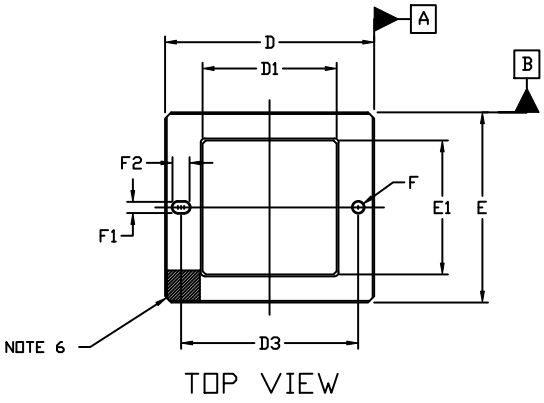
For quality and reliability information, please download the Quality & Reliability Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the Device Nomenclature technical note (TND310/D) from www.onsemi.com.

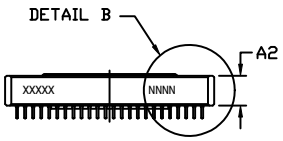
For information on Standard terms and Conditions of Sale, please download *Terms and Conditions* from www.onsemi.com.

PACKAGE DIMENSIONS

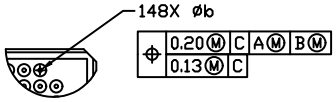
CPGA148, 33x30
CASE 107FK
ISSUE O



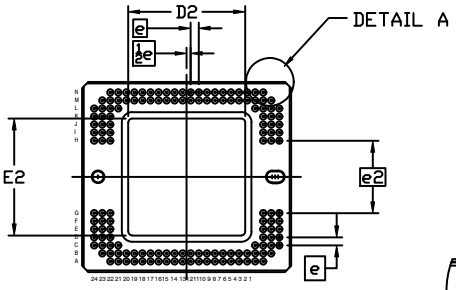
TOP VIEW



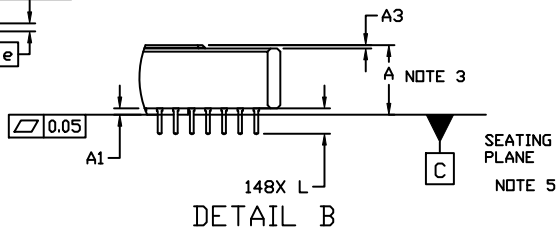
SIDE VIEW



DETAIL A



BOTTOM VIEW



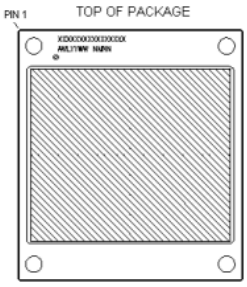
DETAIL B

NOTES:

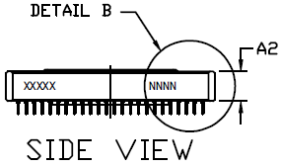
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION A INCLUDES THE PACKAGE BODY, GLASS, AND HEATSINK.
4. DIMENSIONS D AND E DO NOT INCLUDE PROTRUSIONS. SUCH PROTRUSIONS SHALL NOT EXTEND MORE THAN 0.08 ON ANY SIDE. CORNERS AND EDGES OF THE PACKAGE MAY HAVE CHAMFERS.
5. THE SEATING PLANE IS DEFINED BY THE OUTER HEATSINK SURFACE.
6. PIN A1 IDENTIFICATION WILL BE IN THIS AREA. ID TYPE MAY CONSIST OF NOTCHES, METALLIZED MARKINGS, OR OTHER FEATURES.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A		5.49 REF	
A1	0.45	0.50	0.55
A2	4.24	4.72	5.20
A3		0.27 REF	
b	0.25	0.30	0.35
D	32.67	33.00	33.33
D1	21.05	21.13	21.21
D2	18.34	18.44	18.54
D3	27.66	27.94	28.22
E	29.70	30.00	30.30
E1	21.05	21.13	21.21
E2	18.34	18.44	18.54
e		1.27 BSC	
e2	11.30	11.43	11.56
F	1.65	1.75	1.85
F1	1.65	1.75	1.85
F2	2.57	2.72	2.87
L	1.80	2.00	2.20

GENERIC MARKING DIAGRAM



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
NNNN = Serial Number



SIDE VIEW

XXXX = Specific Device Code
NNNN = Serial Number

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303−675−2175 or 800−344−3860 Toll Free USA/Canada
Fax: 303−675−2176 or 800−344−3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800−282−9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

ON Semiconductor Website: **www.onsemi.com**

Order Literature: http://www.onsemi.com/orderlit

For additional information, please contact your local Sales Representative